A New Isolated Phase-Shift Controlled Full Bridge Converter

Eduardo F. R. Romaneli and Ivo Barbi.
Federal University of Santa Catarina
Power Electronics Institute P.O. Box 5119
88040-970 Florianópolis, SC, BRAZIL
E-mails: romaneli@inep.ufsc.br, ivo@inep.ufsc.br

Abstract - This paper deals with a new converter capable of operating in high frequency, featuring high efficiency and improved circuit EMI characteristics. The main characteristic of the circuit is to work with non-pulsating input and output currents. Besides, it presents zero-voltage switching (ZVS) and constant clamping voltage. Theory and experimental results taken from a 600W, 25 kHz laboratory prototype are presented.

I. INTRODUCTION

A new DC-DC converter presenting low current ripple characteristics either in the input and output is the main purpose of this paper. The reasons for researching these topologies are the improved EMI characteristics in the input and the reduced size of the output filter. The proposed converter was developed based on previously presented converters [5] and [6]. Commercial components were used to assure industrial application.

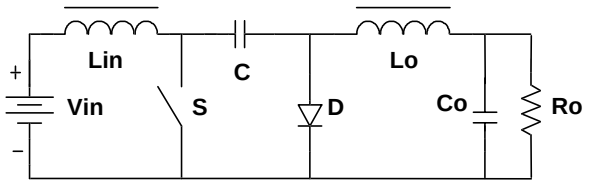


Fig. 1. Cuk converter.

Of the large variety of topologies with these characteristics [1], [2], [4] and [7], Cuk, Figure 1, is the most used and better understood topology. The converter presented in [5], Figure 2, was basically developed to improve some characteristic of Cuk converter. A full bridge version of this topology was presented in [6], Figure 3.

The proposed converter was developed using the converters on Figure 2 as a basement.

The converter [5] was developed in order to improve some characteristics of Cuk converter as:

- Isolation;
- Soft switching;
- Active voltage clamping.

Despite of its good efficiency [5] presents variable reverse voltage across switches. The converter presented in [6] was developed to deal with higher power levels and it presents lower voltage levels when compared to [5]. But, this converter presents asymmetrical operation and each switch is submitted to a different current stress. The proposed converter is the second generation of [6] and presents the following characteristics:

- Better symmetry between the switches;
- Constant reverse voltage under any load.

Even newer solutions, as [7], don't present all these features.

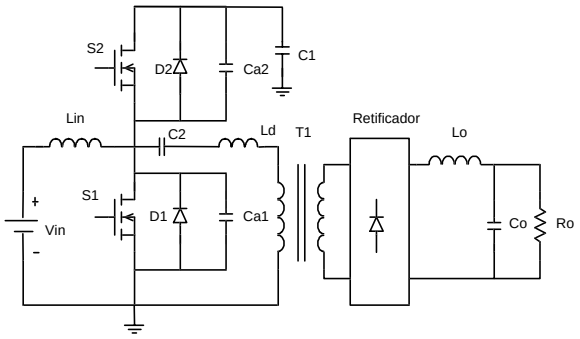


Fig. 2. Converter already presented in [5].

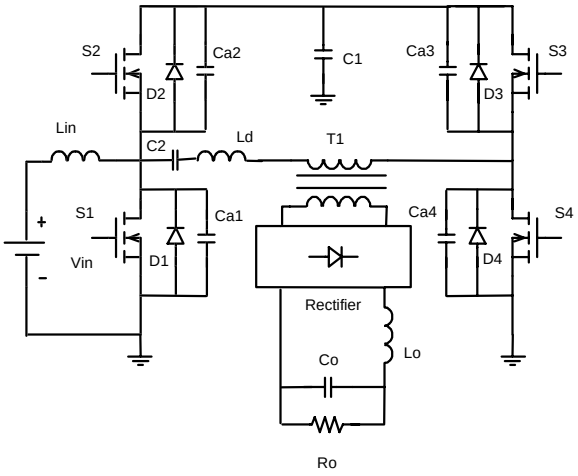


Fig. 3. Converter presented in [6].

II. THE CIRCUIT AND PRINCIPLE OF OPERATION

The converter is presented in Fig. 4 It is basically a full bridge version of the converter presented in [5] . L_{in1}, L_{in2} and L_o operate in continuous current mode. The inductance L_d along with snubber capacitors C_{a1} to C_{a4} provide a resonant transition permitting zero-voltage turn-on that eliminates turn-on switching power losses. Capacitors C_{a1} to C_{a4} also provide capacitive turn-off snubbing reducing the commutation losses. The switches are arranged in bridge structure, they are driven in phase-shift way. The

voltage across C_1 imposes the voltage across the blocking switch of the pair. Fig. 5 shows the key waveforms.

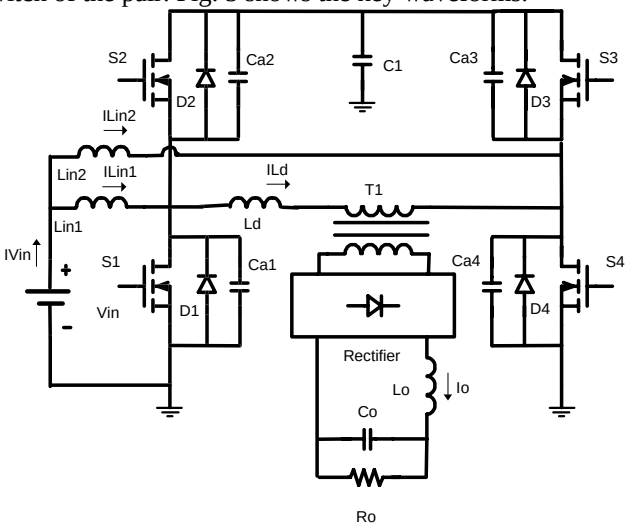


Fig. 4. Proposed Structure.

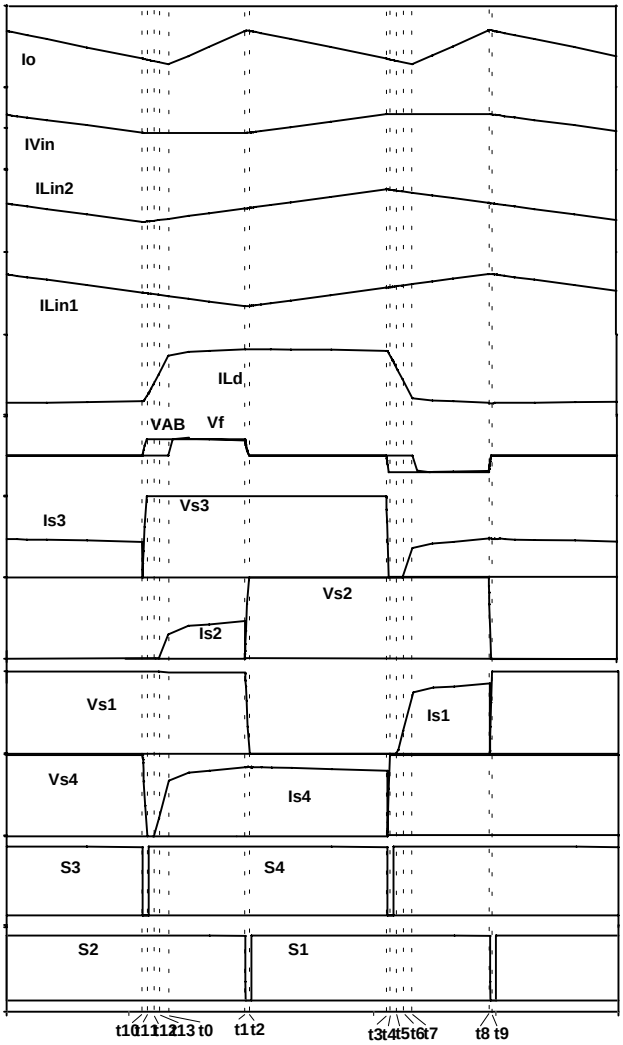


Fig. 5. Basic waveforms.

Complete operation can be described in 14 stages. They are shown in Fig. 6 until Fig. 19.

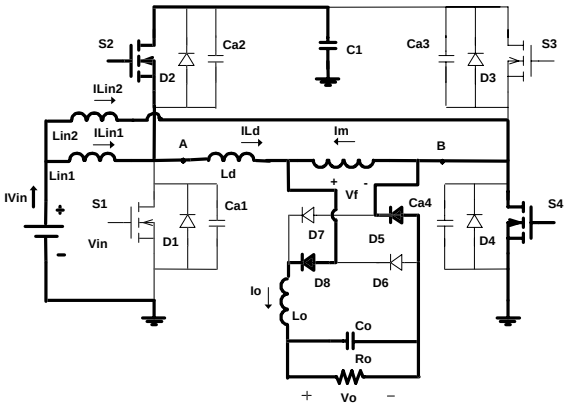


Fig. 6. First stage.

First Stage(t_0 ,t_1): Switches S_2 and S_4 conduct. During this stage energy stored in C_1 is transferred to load. Voltage V_{AB} is equal $V_{in}/(1-D)$ and it is completely absorbed by output filter. It finishes when S_2 is opened.

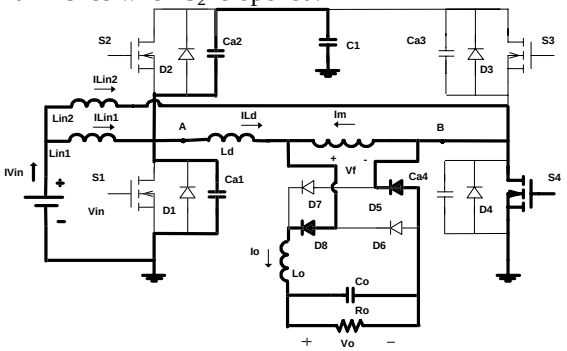


Fig. 7. Second stage.

Second stage(t_1 ,t_2): When S_2 is closed, voltage across C_{a2} grows linearly from zero until $V_{in}/(1-D)$, while voltage across C_{a1} decreases from $V_{in}/(1-D)$ until zero. V_{AB} is positive , D_8 and D_5 are biased. It ends at t_2, when V_{AB} is equal to zero.

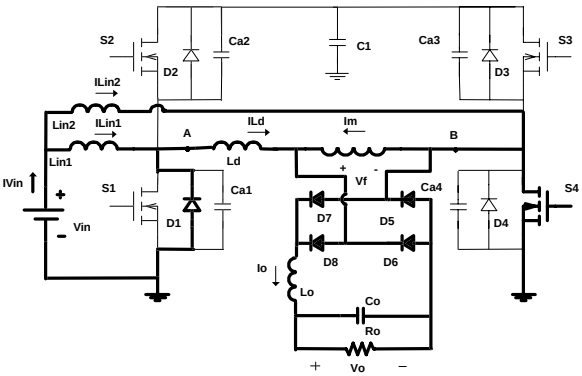


Figure. 8. Third stage.

Third stage(t_2 ,t_3): Voltage V_{AB} should become negative. D_1 conducts and allows S_1 turn on under zero voltage. D_6 e D_7 are biased and the rectifier bridge stay in short circuit. V_{AB} is equal to zero. From the converter's point of view, branch A-B is reduced to an inductor (L_d) charged with (I_o-I_m). This state lasts until S_4 is turned off.

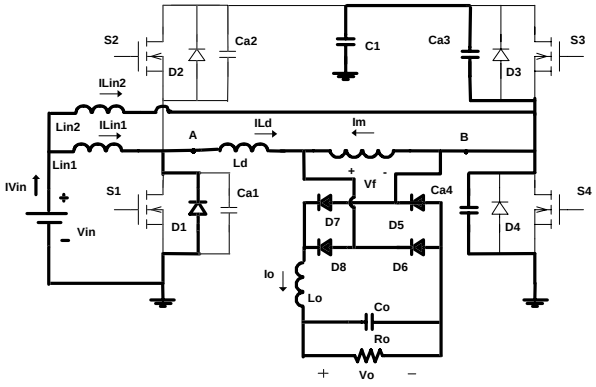


Fig. 9. Forth stage.

Forth stage (t_3 ,t_4): This stage begins when S_4 is turned off, voltage across C_{a4} increases from zero until $V_{in}/(1-D)$, while voltage across C_{a3} decreases from $V_{in}/(1-D)$ until zero. It ends when D_3 conducts.

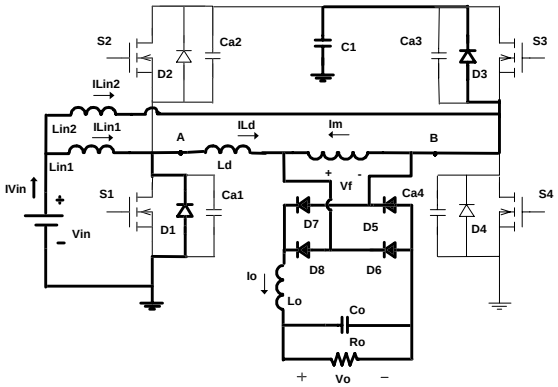


Fig. 10. Fifth stage.

Fifth stage (t_4 ,t_5): S_3 must be commanded to turn on. Voltage V_{AB} become negative, equal to $-V_{in}/(1-D)$. Current I_{Ld} decreases from I_o-I_m until reach I_{Lin1}. In this point, the stage is over.

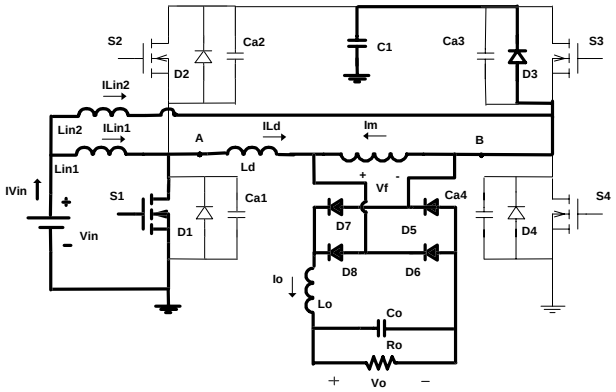


Fig. 11. Sixth stage.

Sixth stage (t_5 ,t_6): Current I_{Ld} decreases, becomes negative and continues to decrease until reaches -I_{Lin2}. In this point the stage is over.

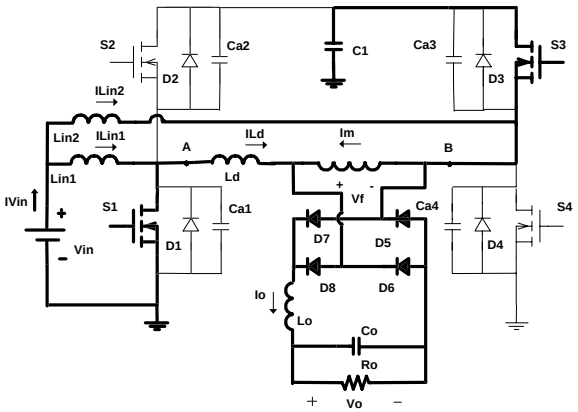


Fig. 12. Ninth stage.

Seventh stage (t_6 ,t_7): S_3 turns on. I_{Ld} still decreases until reach -(I_o+I_m).

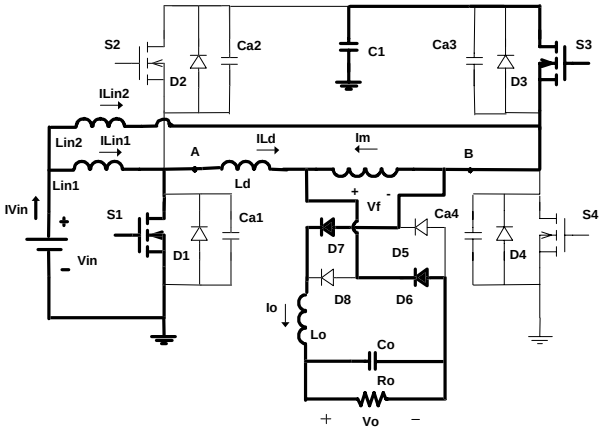


Fig. 13. Eighth stage.

Eighth stage (t_7 ,t_8): When I_{Ld} reaches -(I_o + I_m), D_8 and D_5 are turned off. V_{C1} is equal to $-V_{in}/(1-D)$ and it is applied to the output filter. Energy is stored in L_{in1}. During this stage C_1 transfers energy to output. It ends when S1 is opened.

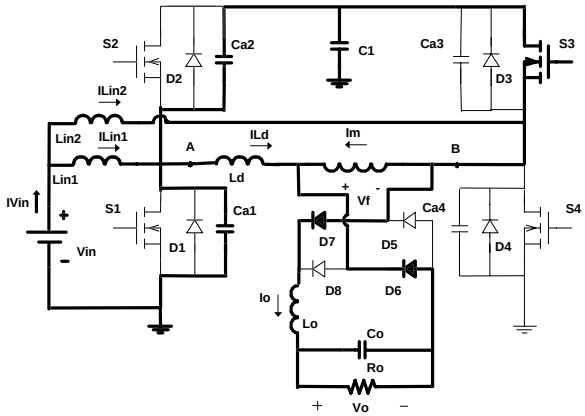


Fig. 14. Ninth stage.

Ninth stage (t_8 ,t_9): When S_1 is turned off under zero voltage, voltage across C_{a1} increases linearly from zero until $V_{in}/(1-D)$, while voltage across C_{a2} decreases from $V_{in}/(1-D)$ until zero. V_{AB} is negative, D_7 and D_6 are directly biased. It ends when V_{AB} is equal to zero.

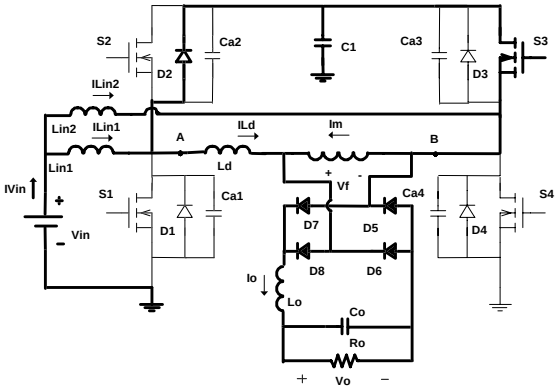


Fig. 15. Tenth stage.

Tenth stage (t_9 ,t_{10}): Voltage V_{AB} should become positive. D_5 e D_8 are biased but the sense of current I_{Ld} put the rectifier bridge in short circuit condition. V_{AB} is still equal to zero. From the converter's point of view , the branch A-B is reduced to inductor (L_d) conducting current $-(I_o+I_m)$. It ends when S3 is turned off.

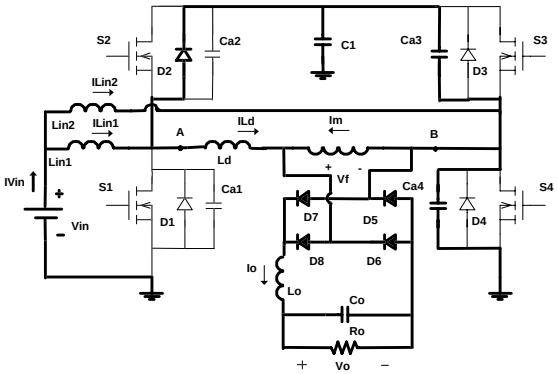


Fig. 16. Eleventh stage.

Eleventh stage (t_{10} ,t_{11}): It begins when S_3 is turned off. Voltage across C_{a3} grows from zero until $V_{in}/(1-D)$, while voltage across C_{a4} decreases from $V_{in}/(1-D)$ until zero. It ends when D_4 is turned on. It is a resonant stage.

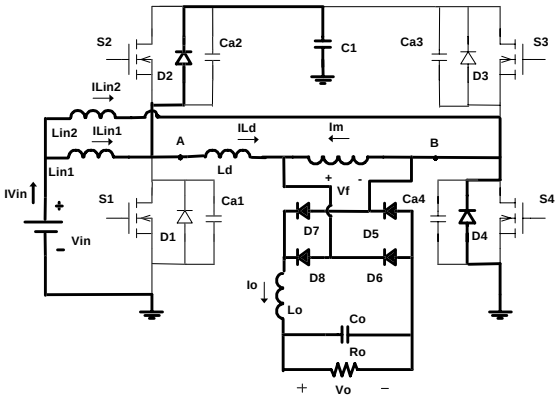


Fig. 17. Twelfth stage.

Twelfth stage (t_{11} ,t_{12}): In this point S_4 must be ordered to turn on. Voltage between points A e B become positive and equal to $V_{in}/(1-D)$. I_{Ld} decreases from $-(I_o+I_m)$ until reach I_{Lin2}. When it happens the stage is over.

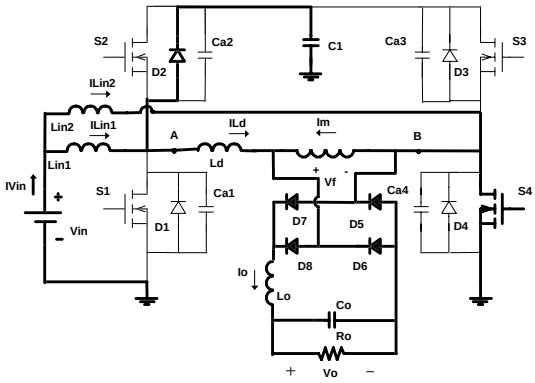


Fig. 18. Thirteenth stage.

Thirteenth stage (t_{12} ,t_{13}): Current I_{Ld} still decreases until inverting its sense and become positive and reach I_{Lin1} . The stage is over

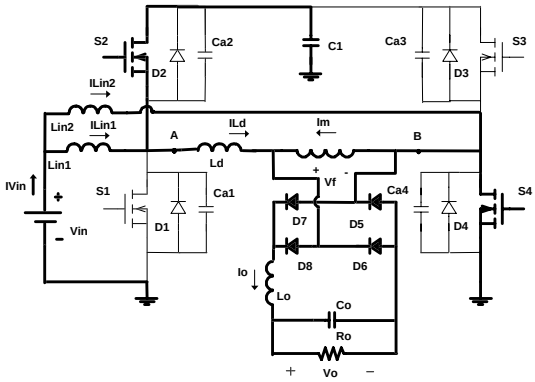


Fig. 19. Fourteenth stage.

Fourteenth stage (t_{13} ,t_{14}): S_2 is turned on. I_{Ld} still increases until it reaches I_o-I_m.

III. ANALISYS OF THE CONVERTER

The voltage drop is proportional to the current demanded by the load.

$$V_o = \frac{1}{T} \cdot \left[\int_{T2}^{DT-T4} 2 \cdot V_{in} \cdot dt \right] \quad (1)$$

Where:

$$T_2 = \frac{L_D \cdot I_o}{V_{in}} \quad (2)$$

$$T_4 = \frac{L_D \cdot I_o}{V_{in}} \quad (3)$$

Thus:

$$q = \frac{V_o}{V_{in}} = 2 \cdot D - \frac{4 \cdot L_D \cdot f_s \cdot I_o'}{V_{in}} \quad (4)$$

From (4) that represents the dc voltage conversion ratio

of the converter, it can be noticed that the larger L_{rs} is, the larger also is the reduction of the output voltage caused by the reactive voltage drop. Clamping voltage behaves as a Boost converter when operating at 0.5 duty-cycle.

$$\frac{V_{C1}}{V_{in}} = \frac{1}{1 - D_{boost}} \quad (5)$$

Where:

$$D_{Boost} = 0.5 \quad (6)$$

Thus:

$$\frac{V_{C1}}{V_{in}} = 2 \quad (7)$$

The descending lines that constitute the output characteristic curve are shown in Fig. 20. Fig. 21 shows V_{C1} that is the voltage across C_1 and represents the maximum voltage applied to the switches. V_{C1} is constant to any load as expected.

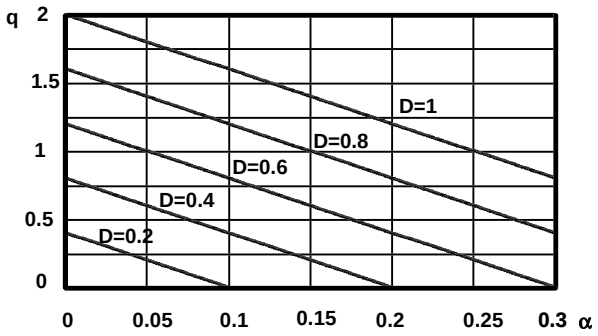


Fig. 20. Output characteristic curve.

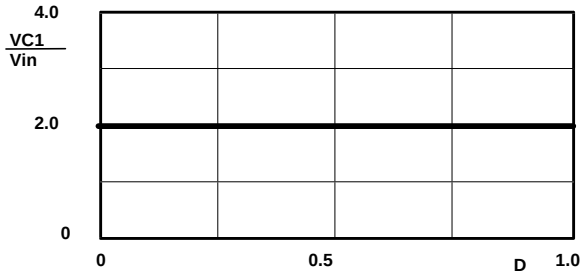


Fig. 21. Clamping voltage $V_{C1.}$

IV. Experimental Results

- Output power P_o = 600W
- Input voltage: Vin = 400 V
- Output voltage: V_o = 60 V
- Switching frequency: f_S = 25 kHz
- Maximum duty-cycle: D_{max} = 0.5
- Voltage ripple across C_1,C_o ΔV = 2%
- Current ripple through L_{in},L_o ΔI = 20%

The experimental efficiency is shown on Fig. 22. Steady state operation is achieved when D = 0.4. A Fig. 23 shows currents I_{in1}, I_{in2}, e I_{Vin}. Fig. 24 until Fig. 27 present S1, S2, S3 and S4 commutations. ZVS commutation can be observed. Voltage V_{AB} and V_f can be observed in Fig. 28. Fig. 29 presents current through the resonant inductor I_{Ld}. Voltage ripple across C_o is on Fig. 30. Clamping voltage V_{C1} and output voltage are shown in Fig. 31.

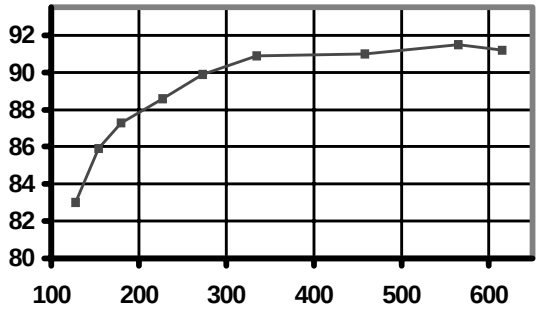
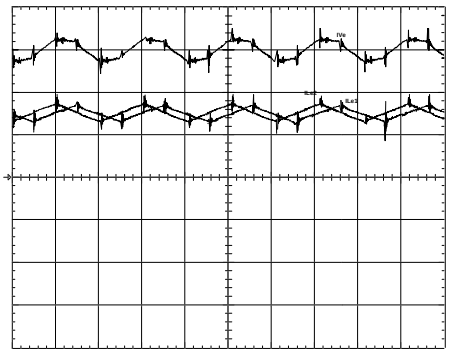
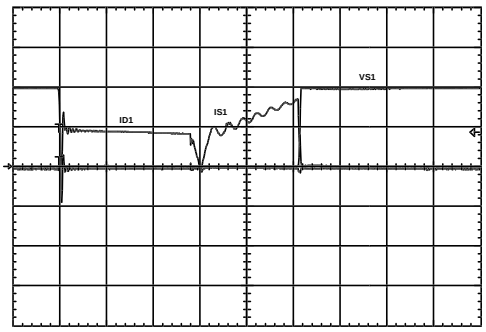


Fig. 22. Experimental efficiency x output current.



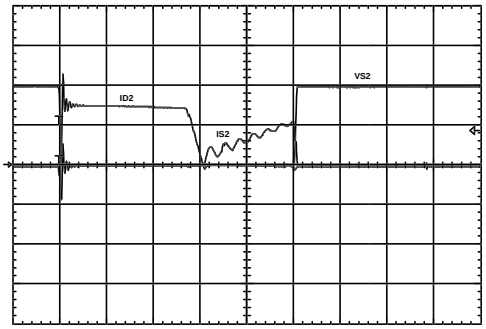
I_{Lin1}, I_{Lin2}, I_{Vin} – 400 mA/div 20μs/div

Fig. 23. Current ILin1, ILin2 e Ivin



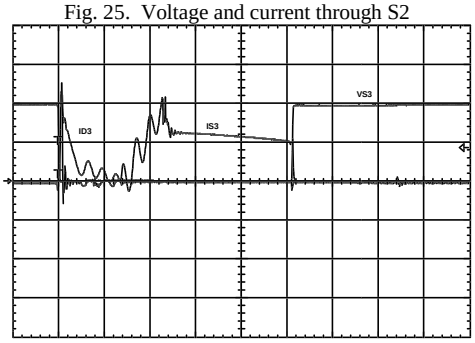
Vs1 – 400 V/div 4μs/div IS1-ID1 – 2 A/div

Fig. 24. Voltage and current through S1.



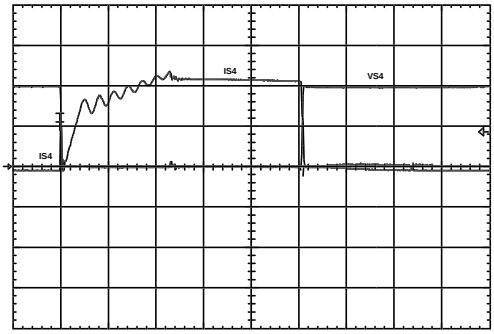
Vs2 – 400 V/div 4μs/div IS2-ID2 – 2 A/div

Fig. 25. Voltage and current through S2



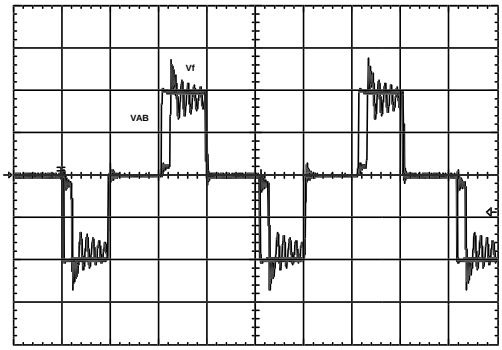
Vs3 – 400 V/div 4µs/div IS3- 2 A/div ID3- 400 mA/div

Fig. 26. Voltage and current through S3.



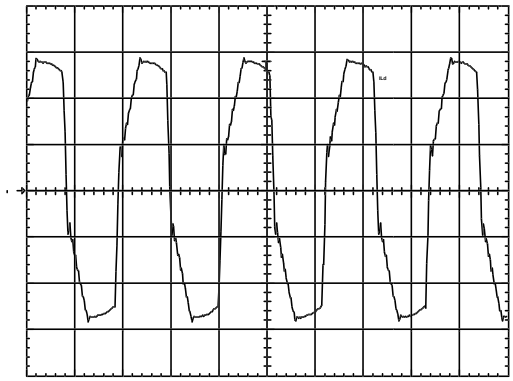
Vs4 – 400 V/div 4µs/div IS4- 2 A/div ID4- 200 mA/div

Fig. 27. Voltage and current through S4.



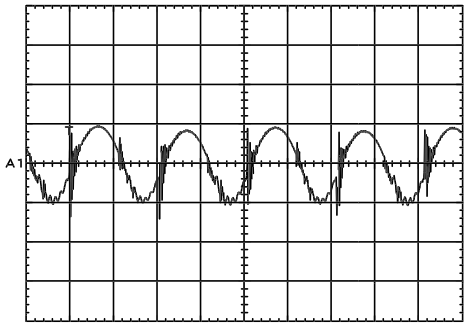
V_{AB}, V_f – 400 V/div 10µs/div

Fig. 28. Voltages V_{AB} e V_f.



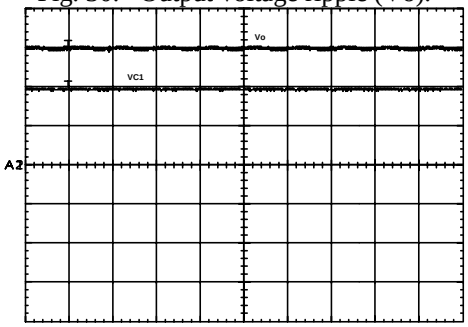
I_{Ld} – 1 A/div 20µs/div

Fig. 29. Current through L_d.



Vo – 400 mV/div 10µs/div

Fig. 30. Output voltage ripple (Vo).



Vo – 20 V/div V_{C1} – 400 V/div 20µs/div

Fig. 31. Voltages V_{C1} and Vo.

V. CONCLUSIONS

This paper presents the analysis, design procedure and experimental results of a new isolated ZVS-PWM active clamping non pulsating input and output current and output DC converter. Non pulsating currents characteristic is interesting when lower EMI level in the input and lower output capacitor volume are required.

The proposed converter is suited to applications where high efficiency is required due to its ZVS characteristics.

Its clamping voltage is always constant and equal to twice input voltage. It is an unusual characteristics in an active clamping converter that represents an improvement in this kind of converter.

REFERENCES

[1] S. Cuk, "Switching DC-to-DC Converter with Zero input or Zero output Current Ripple" IEEE Industry Applications Society Annual Meeting, 1978 Record, pp. 1131-1146, Toronto, Ont., October 1-5, 1978.

[2] D.A. Ruiz-Caballero and I. Barbi, "A New ZVS-PWM Clamping Mode Isolated Non Pulsating Input and Output Current DC-to-DC Converter" INTELEC 99, pp 20-1, Copenhagen, June 6-9, 1999.

[3] C. Duarte and I. Barbi, "A New Family of ZVS-PWM Active Clamping DC-to-DC Boost Converters: Analisys, Design and Experimentation" IEEE INTELEC'96, pp. 305-312.

[4] R. Severns, "High Frequency Converters with Non Pulsating Input and Output Currents" HPFC Proceedings , pp 223-234, May, 1990.

[5] E. F. R. Romaneli and I. Barbi, "A New ZVS-PWM Clamping Mode Isolated Non Pulsating Input and Output Current DC-to-DC Converter" PESC00, Galway, June 18-23, 2000.

[6] E. F. R. Romaneli and I. Barbi, "A New DC-DC Converter with Low Current Ripple Characteristics" INTELEC00, Phoenix, September 10-15, 2000.

[7] M. Qiu, G. Moschopoulos, H. Pinheiro and P. Jain; "A PWM Full-Bridge Converter with Natural Input Power Factor Correction", PESC98, pp 1605 – 1611.