Fully Digital Voltage and Current Controller for Three-Phase Voltage Source PWM Inverters

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***Abstract* – This paper proposes discrete time voltage and current controllers for three-phase PWM inverters used in UPS applications. An accurate state space discrete model of the PWM inverter-filter-load, which takes into account non-linearities and propagation delays associated with a real time digital implementation, is derived for the controller design. The output voltages and inductors currents are dynamically limited by means of MIMO controllers designed using optimal servo linear quadratic regulators, which ensure stability for the system at all operating conditions. In order to ensure smooth transitions among the different modes of operation, a nonlinear MIMO anti-windup method is proposed to update the servo variables. A 15kVA PWM inverter fully controlled by the DSP controller TMS320F241 has been used to validate the proposed approach. Simulations and experimental results show a good transient and steady state performances from no-load to short circuit operation.**

I. Introduction

The main goal of an UPS is to provide high quality output voltage for critical loads even under disturbances coming from both AC line or from the load. Many controllers have been proposed to obtain an output voltage with low total harmonic distortion for three phase PWM inverters [1–6]. Among them, deadbeat and OSAP controllers [1-3] presents a fast transient response, however, they are sensitive to parametric variations and model uncertainties, which often results in undesirable transient performance, or even instability. On the other hand, nonlinear state feedback controller in the synchronous frame [4-5] have been described, however, the design is usually carried out in the continuous time domain, and the relevant delays associated with a digital implementation are not taking into account, which can degrade its final performance [6]. In addition, in none of the case reported the output voltage controller and the current limiter controller, which is required to clear faulty loads and to protect the inverter against overloads, are simultaneously designed with systematic procedure.

This paper proposes a rotating frame fully digital voltage and current controllers for PWM inverters where good performance from no load to short circuit is assured by the proper selection of the cost functions of the voltage and current linear quadratic regulator. A systematic procedure for the controller design in the state space is derived.

The remainder part of this paper is organized as follows: Section II presents a discrete model in the rotating frame for the space vector modulated inverter and LC filter and load, which is normalized to couple with limited dynamic range of a fixed-point DSP implementation. Section III presents the voltage and current controller design. Section IV proposes an anti-windup strategy; Section V presents a brief description of the DSP algorithm, while Section VI presents experimental results from a 15kVA inverter prototype. Finally, Section VII summarizes the main points of this paper.

II. Discrete Normalized PWM Inverter Model

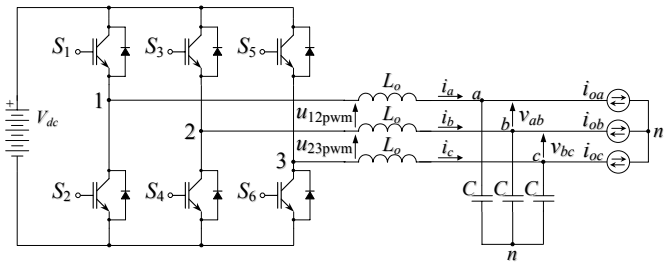

Fig. 1. Three-phase Inverter and LC filter.

A typical three-phase voltage source inverter with LC filter and load found in UPS applications is shown in Fig. 1. The DC link voltage usually has low impedance and can be considered as an ideal voltage source. On the other hand, the output LC filter and load can be modeled by the following state space model where the load are considered as disturbances, that is:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\,\mathbf{x}(t) + \mathbf{B}\,\mathbf{u}(t) + \mathbf{F}\,\mathbf{w}(t) \qquad (1)$$

The matrices **A**, **B**, **F** in (1) can be found by applying Kirchhoff´s law in the circuit and the vectors **x**, **u** and **w** have been selected as:

$$\mathbf{x} = \begin{bmatrix} i_a & i_b & i_c & v_a & v_b & v_c \end{bmatrix}^{\mathrm{T}} \quad \mathbf{u} = \begin{bmatrix} u_{12\,pwm} & u_{23\,pwm} \end{bmatrix}^{\mathrm{T}}$$
$$\mathbf{w} = \begin{bmatrix} i_{oa} & i_{ob} & i_{oc} \end{bmatrix}^{\mathrm{T}}$$

A. Normalization

Aiming to limit the dynamic range of variables for a fix point implementation of the controller, a linear transformation that normalizes the circuit variable is applied to (1). By choosing the base values, the normalized voltage and current variables can be written as: $v_n = \dfrac{v}{V_{base}}$ $\quad i_n = \dfrac{i}{I_{base}}$.

Now, defining a normalizing linear transformation $\mathbf{T_n}$ where $\mathbf{T_n}$ is a diag $(1/I_{base}\ 1/I_{base}\ 1/I_{base}\ 1/V_{base}\ 1/V_{base}\ 1/V_{base})$ matrix the normalized state, input and disturbance vectors become:

$$\mathbf{x_n}(t) = \mathbf{T_n}\mathrm{x}(t) \qquad \mathbf{u}(t) = V_{base}\mathbf{u_n}(t) \qquad \mathbf{w}(t) = I_{base}\mathbf{w_n}(t)$$

As a result the state equation (1) can be written in a compact form as (2)

$$\dot{\mathbf{x}}_\mathbf{n}(t) = \mathbf{T_n}\mathbf{A}\mathbf{T_n}^{-1}\mathbf{x_n}(t) + \mathbf{T_n}\mathbf{B}V_{base}\mathbf{u_n}(t) + \mathbf{T_n}\mathbf{F}I_{base}\mathbf{w_n}(t). \qquad (2)$$

B. State space model in rotating d-q frame

By representing (2) into the αβ frame and then in the rotating *dq* frame, the following state-space normalized continuous model of the LC filter and load is obtained:

$$\begin{bmatrix}\dot{v}_d\\ \dot{v}_q\\ \dot{i}_d\\ \dot{i}_q\end{bmatrix}=\begin{bmatrix}0 & \omega & \frac{1}{C} & 0\\ -\omega & 0 & 0 & \frac{1}{C}\\ -\frac{1}{L_o} & 0 & 0 & \omega\\ 0 & -\frac{1}{L_o} & -\omega & 0\end{bmatrix}\begin{bmatrix}v_d\\ v_q\\ i_d\\ i_q\end{bmatrix}+\begin{bmatrix}0 & 0\\ 0 & 0\\ \frac{1}{L_o} & 0\\ 0 & \frac{1}{L_o}\end{bmatrix}\begin{bmatrix}u_{dpwm}\\ u_{qpwm}\end{bmatrix}+\begin{bmatrix}-\frac{1}{C} & 0\\ 0 & -\frac{1}{C}\\ 0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}I_{od}\\ I_{oq}\end{bmatrix} \quad (3)$$

where "ω" in (3) is the desired output frequency. Equation (3) can be expressed into the following compact form:

$$\dot{\mathbf{x}}_{\mathbf{dq}}(t)=\mathbf{A}_{\mathbf{dq}}\mathbf{x}_{\mathbf{dq}}(t)+\mathbf{B}_{\mathbf{dq}}\mathbf{u}_{\mathbf{dq}}(t)+\mathbf{F}_{\mathbf{dq}}\mathbf{w}_{\mathbf{dq}}(t) \quad (4)$$

where $\mathbf{x}_{\mathbf{dq}}=\begin{bmatrix}v_d & v_q & i_d & i_q\end{bmatrix}^{\mathrm{T}}$ $\mathbf{u}_{\mathbf{dq}}=\begin{bmatrix}u_{dpwm} & u_{qpwm}\end{bmatrix}^{\mathrm{T}}$ $\mathbf{w}_{\mathbf{dq}}=\begin{bmatrix}I_{od} & I_{oq}\end{bmatrix}^{\mathrm{T}}$.

Note that (4) is a normalized continuous model where u_{dpwm} and u_{qpwm} are the voltages produced by the inverter represented in the rotating *dq* frame, as shown in Fig. 2 (a) and (b) respectively.

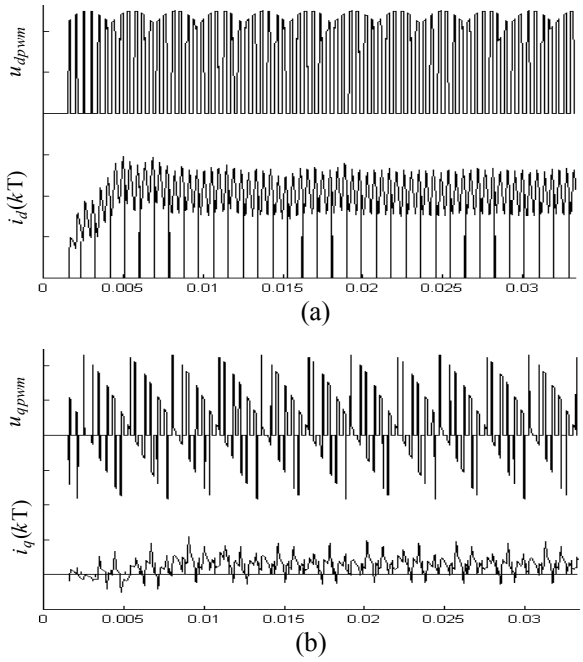

Fig. 2. (a) PWM output voltage u_{dpwm} and inductor current id in the rotating *dq* frame. (b) PWM output voltage u_{qpwm} and inductor current i_q in the rotating *dq* frame.

The block diagram of Fig. 3 describes the operation of the digitally implemented space vector modulation where the discrete control action is generated in the *dq* frame. By making some assumptions the diagram of Fig. 3 can be simplified, that is: (i) By assuming that the variables are sampled at their mean values and that the (2) has a low pass characteristic then the blocks associated with the SVM/inverter and the *abc*-αβ transformation can be simplified to a gain proportional to de DC bus voltage *Vdc*. (ii) If the switching frequency is mush higher then the output frequency then discrete *dq*-αβ transformation and the continuous αβ-*dq* transformation can also be simplified. As a result the block diagram of Fig. 3 (a) is rendered to the one shown in Fig. 3 (b). If these assumptions are violated, a non-linear model should be considered to describe the relationship between the input and output variables of three-phase PWM inverter in the rotating frame.

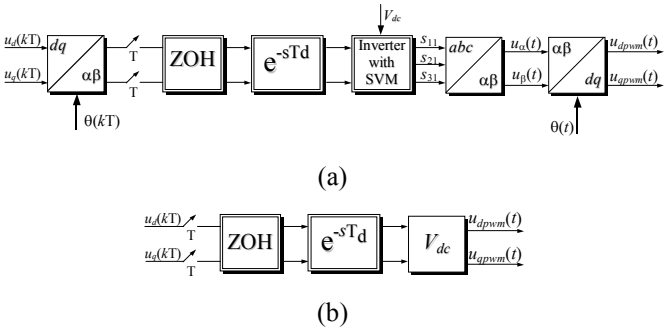

Fig. 3. (a) Block diagram representation of three-phase PWM inverter in the *dq* frame. (b) Simplified representation.
ZOH: zero-order hold, SVM: Space Vector Modulator. "T" is the sampling period.

C. Discrete state-space model in rotating d-q Frame

As mentioned before digital controllers require a finite time for its computation, which can represent a significant portion of the sampling period. In this section, a discrete state-space model, which takes into account this computational delay, defined as $\mathrm{T_d}$ is derived.

Referring to Fig. 4 during the *k*-th sampling interval both actual action control, $\mathbf{u_{dq}}(k\mathrm{T})$ and last $\mathbf{u_{dq}}((k\text{-}1)\mathrm{T})$, are applied to the inverter. As result, an additional state variable $\mathbf{u_{dq\_d}}$ (last control action) can be used to model this delay.

In order to obtain the discrete state space equation, which takes an account mentioned delay the state space equation (4) is solved along one sampling period (in this case also the switching), that is:

$$\mathbf{x_{dq}}((k+1)\mathrm{T})=e^{\mathbf{A_{dq}}\mathrm{T}}\mathbf{x_{dq}}(k\mathrm{T})+\int_0^{\mathrm{T_d}}e^{\mathbf{A_{dq}}(\mathrm{T}-\tau)}d\tau\,\mathbf{B_{dq}}\,\mathbf{u_{dq}}((k-1)\mathrm{T})+ +\int_0^{\mathrm{T}-\mathrm{T_d}}e^{\mathbf{A_{dq}}(\mathrm{T}-\mathrm{T_d}-\tau)}d\tau\,\mathbf{B_{dq}}\,\mathbf{u_{dq}}(k\mathrm{T}) \quad (5)$$

The solution of (5) result in the matrix state space equation (6):

$$\begin{bmatrix}\mathbf{x_{dq}}(k+1)\\ \mathbf{u_{dq\_d}}(k+1)\end{bmatrix}=\begin{bmatrix}\mathbf{G} & \mathbf{H_0}\\ \mathbf{0} & \mathbf{0}\end{bmatrix}\begin{bmatrix}\mathbf{x_{dq}}(k)\\ \mathbf{u_{dq\_d}}(k)\end{bmatrix}+\begin{bmatrix}\mathbf{H_1}\\ \mathbf{I}\end{bmatrix}\mathbf{u_{dq}}(k), \quad (6)$$

where:

$$\mathbf{G}=e^{\mathbf{A_{dq}}\mathrm{T}} \qquad \mathbf{H_0}=e^{\mathbf{A_{dq}}(\mathrm{T}-\mathrm{T_d})}\mathbf{A_{dq}}^{-1}(e^{\mathbf{A_{dq}}\mathrm{T_d}}-\mathbf{I})\mathbf{B_{dq}}$$

$$\mathbf{H_1}=\mathbf{A_{dq}}^{-1}\left[e^{\mathbf{A_{dq}}(\mathrm{T}-\mathrm{T_d})}-\mathbf{I}\right]\mathbf{B_{dq}}.$$

By defining, $\boldsymbol{\psi}(k)=\begin{bmatrix}\mathbf{x_{dq}}(k) & \mathbf{u_{dq\_d}}(k)\end{bmatrix}^{\mathrm{T}}$ the discrete state space equation (6) becomes:

$$\boldsymbol{\psi}(k+1)=\mathbf{G_P}\boldsymbol{\psi}(k)+\mathbf{H_P}\,\mathbf{u_{dq}}(k) \quad (7)$$

where the matrices $\mathbf{G_p}$ and $\mathbf{H_p}$ are defined in agreement with (6).

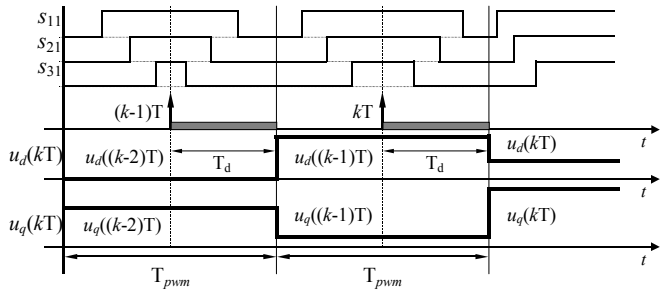

Fig. 4. Control signal (u_{dq}) and sampling instants with reference to a symmetric space vector modulation pattern (s_{11}, s_{21}, s_{31}).

III. VOLTAGE AND CURRENT CONTROLLER DESIGN

For the task of controlling the output voltage and limiting the inductors current it is proposed a servo current and voltage controller. It consists of an inner current loop controller and an outer voltage loop controller, in an arrangement as shows in Fig. 5. For the design of the servo current and voltage controllers the steady-state discrete linear quadratic regulator approach is used. The next two sub-sections derive discrete state-space error current and voltage models that are adequate for the controllers design. The last sub-section investigates the impact of the weighting matrices on the closed-loop performance.

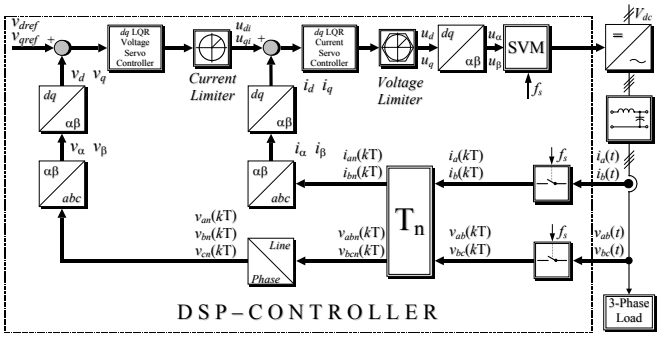

Fig. 5. Block diagram of the proposed linear quadratic current-voltage controller.

A. Inner current loop model.

Fig. 6 shows the block diagram of the proposed inner loop current controller. The linear quadratic current servo controller state equation can be defined as:

$$\mathbf{v_i}(k+1) = \mathbf{v_i}(k) + \mathbf{u_{dqi}}(k) - \mathbf{y_i}(k) \tag{8}$$

where the $\mathbf{v_i}$ is a 2x1 vector. As shown in Fig. 6, the discrete input control equation, which is applied to the plant, is:

$$\mathbf{u_{dq}}(k) = -\mathbf{K_{2i}}\boldsymbol{\psi}(k) + \mathbf{K_{1i}}\mathbf{v_i}(k) \tag{9}$$

In order to transform the current servo design problem into state feedback design problem the following error state variables are defined:

$$\boldsymbol{\psi}_e(k) = \boldsymbol{\psi}(k) - \boldsymbol{\psi}(\infty) \qquad \mathbf{u}_e(k) = \mathbf{u_{dq}}(k) - \mathbf{u_{dq}}(\infty)$$

With these variables the error state-space representation becomes:

$$\begin{bmatrix} \boldsymbol{\psi}_e(k+1) \\ \mathbf{u}_e(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{G_P} & \mathbf{H_P} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{\psi}_e(k) \\ \mathbf{u}_e(k) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{I_i} \end{bmatrix} \mathbf{w}(k) , \tag{10}$$

where, $\mathbf{w}(k) = \left[(\mathbf{K_{2i}} - \mathbf{K_{2i}}\mathbf{G_P} - \mathbf{K_{1i}}\mathbf{C_i}) \vdots (\mathbf{I_i} - \mathbf{K_{2i}}\mathbf{H_P}) \right] \begin{bmatrix} \boldsymbol{\psi}_e(k) \\ \mathbf{u}_e(k) \end{bmatrix}$,

which can also be written as, $\mathbf{w}(k) = \mathbf{K_i} \begin{bmatrix} \boldsymbol{\psi}_e(k) & \mathbf{u}_e(k) \end{bmatrix}^{\mathrm{T}}$.

The feedback gain matrix $\mathbf{K_i}$ can be determined to ensure the desired system performance. Then $\mathbf{K_{1i}}$ and $\mathbf{K_{2i}}$ can be easily obtained from $\mathbf{K_i}$.

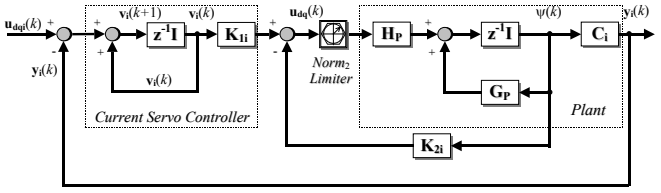

Fig. 6. The inner current loop block diagram

B. Outer voltage loop model.

Let us now focus in the model for design the output voltage controller. In this case the inverter-filter-load and the servo current controller can be considered as a new plant for the purpose of the outer loop voltage servo design. The implemented servo dynamic equation is:

$$\mathbf{v_v}(k) = \mathbf{v_v}(k-1) + \mathbf{r_v}(k) - \mathbf{y_v}(k) . \tag{11}$$

As result, the discrete current reference, which is applied to the inner loop as shown in Fig. 7, is given by:

$$\mathbf{u_{dqi}}(k) = -\mathbf{K_{2v}}\boldsymbol{\psi_i}(k) + \mathbf{K_{1v}}\mathbf{v_v}(k) \tag{12}$$

In a similar manner as a servo current controller, the state feedback representation becomes as shown in equation (13).

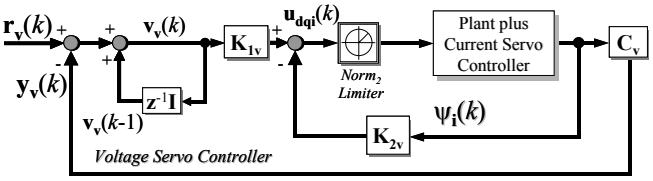

Fig. 7. The plant plus inner current loop and outer voltage loops block diagram

$$\begin{bmatrix} \boldsymbol{\psi}_{ie}(k+1) \\ \mathbf{u_{dqi}}_e(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{G_i} & \mathbf{H_i} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{\psi}_{ie}(k) \\ \mathbf{u_{dqi}}_e(k) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{I_v} \end{bmatrix} \mathbf{u_v}(k) , \tag{13}$$

where $\mathbf{u_v}(k) = [(\mathbf{K_{2v}} - \mathbf{K_{2v}}\mathbf{G_i} - \mathbf{K_{1v}}\mathbf{C_v}\mathbf{G_i}) \vdots (\mathbf{I_v} - \mathbf{K_{2v}}\mathbf{H_i} - \mathbf{K_{1v}}\mathbf{C_v}\mathbf{H_i})] \begin{bmatrix} \boldsymbol{\psi}_{ie}(k) \\ \mathbf{u_{dqi}}_e(k) \end{bmatrix}$

which can also be written as, $\mathbf{u_v}(k) = \mathbf{K_v} \begin{bmatrix} \boldsymbol{\psi}_{ie}(k) & \mathbf{u_{dqi}}_e(k) \end{bmatrix}^{\mathrm{T}}$

The $\mathbf{K_{1v}}$ and $\mathbf{K_{2v}}$ feedback matrices are obtained from to gain matrix $\mathbf{K_v}$, which is selected to ensure the desired closed-loop performance.

Next section discusses the selection of $\mathbf{K_i}$ and $\mathbf{K_v}$ gain matrices using the discrete linear quadratic regulator approach.

C. Steady-state discrete linear quadratic design

For the design of feedback gains, the steady-state discrete linear quadratic optimal control approach has been adopted. In this approach the controller feedback gains are selected to minimize the discrete cost function (14). By selecting

weighting matrices **Q** as positive definite or positive semidefinite Hermitian matrix and **R** as positive definite Hermitian matrix, the resulting system is asymptotically stable. However, the system performance depends on the specific entries of $\mathbf{Q_i}$ and $\mathbf{R_i}$ for the inner current-controller as likewise on the entries $\mathbf{Q_v}$ and $\mathbf{R_v}$ for the outer voltage-controller.

$$J = \frac{1}{2}\sum_{k=0}^{\infty} \boldsymbol{\psi_i}^{\mathrm{T}}(k)\,\mathbf{Q_i}\,\boldsymbol{\psi_i}(k) + \mathbf{u_i}^{\mathrm{T}}(k)\,\mathbf{R_i}\,\mathbf{u_i}(k) \qquad (14)$$

where,

$\mathbf{Q_i} = \mathbf{diag}\,[q_{vd} \quad q_{vq} \quad q_{id} \quad q_{iq} \quad q_{uad} \quad q_{uaq} \quad q_{vid} \quad q_{viq}]$

$\mathbf{R_i} = r_i\,\mathbf{I}_{2\times 2}$ where r_i is a scalar.

$\mathbf{Q_v} = \mathbf{diag}\,[q_{vd} \quad q_{vq} \quad q_{id} \quad q_{iq} \quad q_{uad} \quad q_{uaq} \quad q_{vid} \quad q_{viq} \quad q_{vvd} \quad q_{vvq}]$

$\mathbf{R_v} = r_v\,\mathbf{I}_{2\times 2}$ where r_v is a scalar.

In order to define the weighting matrix **Q** and **R**, it is possible to use the transient response and the root locus as performances criteria.

If more the one set of **{Q,R}** results in a similar performance then, the set with a smaller cost function *J* or the one that result in the smaller feedback gains, should be selected. Once the weight matrices are defined, the feedback gain matrix that minimizes the cost function (14) is uniquely determined.

In the next sub-section analyses supported by experimental results for the PWM inverter operating in both current and voltage control are presented where the feedback gain matrices are obtained with the steady-state LQR design.

D. Design Examples

Fig. 8 and Fig. 9 presents the root locus diagrams of closed-loop poles for the current and voltage operating modes. The entries of the weighting matrices have been adjusted from their nominal values to ensure that: (i) the closed-loop poles are in a well damped region for the entire load variation, that is, from no-load to the rated load when in the voltage control mode and from the rated load to short-circuit when in the current control mode. (ii) the poles sensitivity to the load changes are limited, (iii) the transient response is fast.

By taking into account that the model used in the designs have does not match exactly the real system, is worth to verify the closed loop performance experimentally.

Fig. 10, show the closed-loop transient responses due to step change in the reference for both current and voltage control mode. It is seen that the transient response is well damped as predicted in the design. This is also seen in Fig. 11 and, which show the transient response during the voltage control mode. In all figures the current reference changes from 0.5 pu to 0.75 pu at k = 341 and from 0.75 pu to 0.5 pu at k = 683. Note to that 1 p.u. $\Rightarrow 1/\sqrt{2}$ in *dq* frame and the sampling period is T=100 μs. The parameters LC filter are L_o = 500μH and C = 70μF.

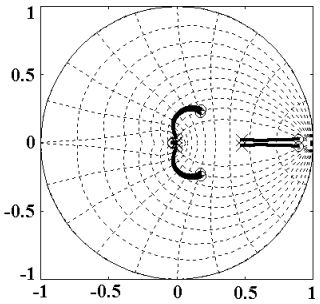

Fig. 8. Root Locus for the current control mode, when the load resistance changes from full load (o) to short circuit (x).
$\mathbf{Q_i} = \mathbf{I}$ and $\mathbf{R_i} = \mathbf{I}$. (3.22 to 0 Ω).

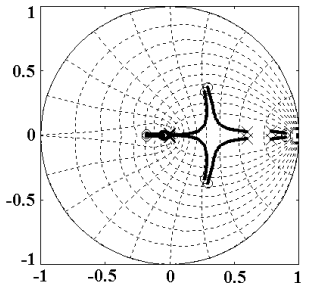

Fig. 9. Root Locus for voltage control mode, when the load resistance changes from no load (o) to full load (x).
$\mathbf{Q_v}$= **diag**[1 1 5.10^3 5.10^3 15.10^3 15.10^3 1 1 1 1]
$\mathbf{R_v} = \mathbf{I}$. (∞ to 3.22 Ω)

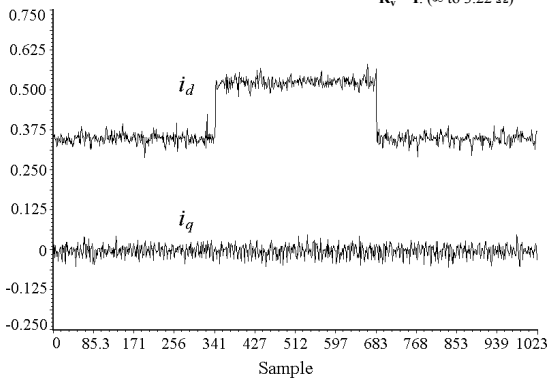

Fig. 10. Experimental Results. i_d and i_q current transient due to step changes on the reference.

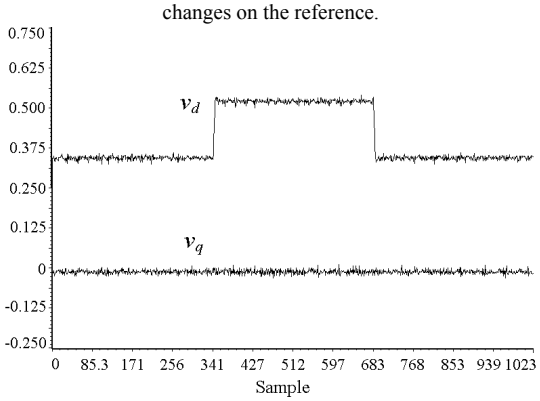

Fig. 11. Experimental Results. v_d and v_q voltage transient due to step changes on the reference.

IV. ANTI-WINDUP COMPENSATION

Windup may occur when the control actions saturate since the servo controllers have eigenvalues on the unity circle. In order to avoid oscillation due to the overload of the voltage servo integral states during the current mode control a tracking mode controller anti-windup compensation algorithm is proposed. The block diagram of this compensator is depicted in Fig. 12. This tracking mode controller ensures that the voltage controller state vector $\mathbf{v_v}(k)$ will correspond to the controller input-to-output vector pairs even when the control action is limited. The current limiter block in Fig. 12 limits current reference vector to be smaller than a maximum desired value, for this case is equal to $\sqrt{3/2}$ in *dq* coordinates, which correspond to 1 p.u. in the

abc coordinates. The implemented current limiter can be expressed as:

$$\mathbf{u_{dqi\lim}}(k)=\begin{cases}\dfrac{\mathbf{u_{dqi}}(k)}{\left\|\mathbf{u_{dqi}}(k)\right\|_2} & \text{if} \quad \left\|\mathbf{u_{dqi}}(k)\right\|_2 > \sqrt{3/2} \\ \mathbf{u_{dqi}}(k) & \text{if} \quad \left\|\mathbf{u_{dqi}}(k)\right\|_2 < \sqrt{3/2}\end{cases} \tag{15}$$

where, $\left\|\mathbf{u_{dqi}}(k)\right\|_2$ is the Euclidean norm of the vector $\mathbf{u_{dqi}}(k)$, that is: $\left\|\mathbf{u_{dqi}}(k)\right\|_2 = \sqrt{u_{di}(k)^2 + u_{qi}(k)^2}$.

The design of the tracking mode controller may be formulated as an observer problem [8]-[10]. The state space representation of the voltage servo controller with the anti-windup compensation of Fig. 12 can be written as:

$$\begin{aligned}\mathbf{v_v}(k) = [\mathbf{I_v} - \mathbf{K_{sv}}\mathbf{K_{1v}}]\mathbf{v_v}(k-1) + \mathbf{e_v}(k) + \mathbf{K_{sv}}\mathbf{u_{dqi\lim}}(k-1) \\ + \mathbf{K_{sv}}\mathbf{K_{2v}}\boldsymbol{\psi}_\mathbf{i}(k-1)\end{aligned} \tag{16}$$

If (16) is observable the matrix $\mathbf{K_{sv}}$ can be chosen so that $[\mathbf{I_v} - \mathbf{K_{sv}}\mathbf{K_{1v}}]$ has prescribed eigenvalues inside of the unit disc. Similar situation may occur with the current servo-controller state. For example, during the startup or shutdown, when the DC bus voltage is smaller than its nominal value, windup may occur.

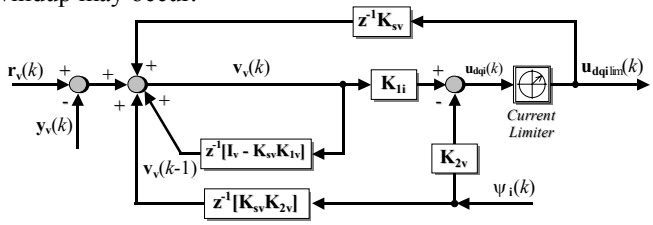

Fig. 12. Block diagram voltage controller with anti-windup compensation.

Fig. 13 shows the current controller with an anti-windup compensation.

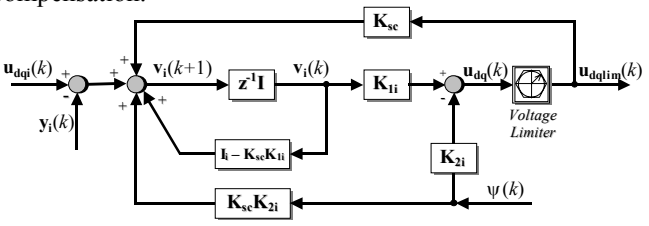

Fig. 13. Block diagram current controller with anti-windup compensation.

The current controller state-space representation can be found as:

$$\begin{aligned}\mathbf{v_i}(k+1) = (\mathbf{I_i} - \mathbf{K_{sc}}\mathbf{K_{1i}})\mathbf{v_i}(k) + [\mathbf{u_{dqi}}(k) - \mathbf{y_i}(k)] \\ + \mathbf{K_{sc}}\mathbf{u_{dq\lim}}(k) + \mathbf{K_{sc}}\mathbf{K_{2i}}\boldsymbol{\psi}(k)\end{aligned} \tag{17}$$

Again, if (17) is observable the matrix $\mathbf{K_{sc}}$ can be chosen so that $[\mathbf{I_i} - \mathbf{K_{sc}}\mathbf{K_{1i}}]$ has prescribed eigenvalues inside of the unit disc.

In order to demonstrate the operation of the proposed anti-windup compensator algorithm some experimental results are presented. Fig. 14 shows the current reference u_{di} before current limiter when inverter operating in short-circuits. Fig. 15, show the current reference u_{dil} after current limiter in similar operating conditions, meanwhile Fig. 16 present the compensated voltage servo controller state. The transient occur due to a change in the reference value. It is seen that the variables are well limited.

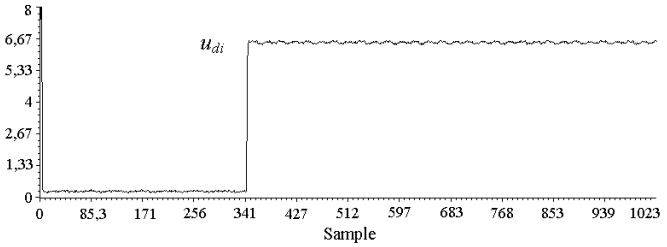

Fig. 14. Experimental results. Current reference u_{di} before current limiter.

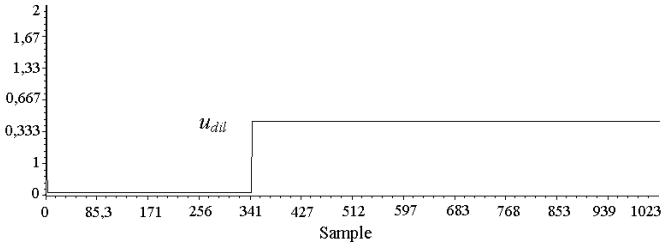

Fig. 15. Experimental results. Current reference u_{dil} after current limiter.

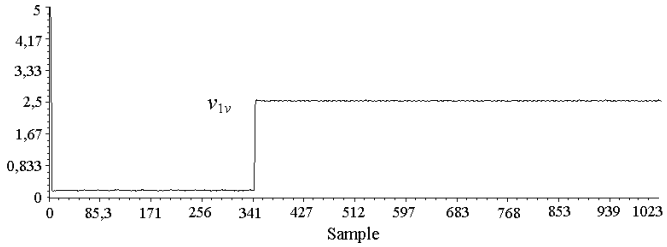

Fig. 16. Experimental results. Compensated voltage servo controller state v_{1v}.

V. Algorithm Implementation

The algorithm implemented in the DSP controller is composed of four routines: An *Initialization Routine*, a *Calibration Routine*, the *Interrupt Routine* and a *Waiting loop Routine*. A brief description of each routine is given below.

A. Initialization Routine

After a reset event, the initialization routine executes the following tasks: CPU configuration, variables initialization, and look-up table transfer from program memory to data memory, which will be addressed on the interrupt routine.

B. Calibration Routine

The goal of this routine is to obtain the offset value of each measured variable; in this case, both v_{ab} and v_{bc} line-to-line voltage and both i_a and i_b line current. This procedure automatically adjusts the offset variables introduced by the measurement circuits, eliminating the requirements of potentiometers.

C. Interrupt Routine

This is the main algorithm. At each sampling period this routine samples the variables, normalizes, and performs coordinate transformations, as well as calculates the outer and inner loop controllers, and finally actualizes the PWM duty cycles.

D. Waiting Loop Routine

Once the interrupt routine was executed, the remaining time until the next interrupt, the current servo controller is

computed and the variables are updated. During this time, $sin(\theta(kT))$ and $cos(\theta(kT))$ are computed, which are necessary for the coordinate transformations.

In order to illustrate the operation of the implemented software Fig. 17 gives the flux and time diagram.

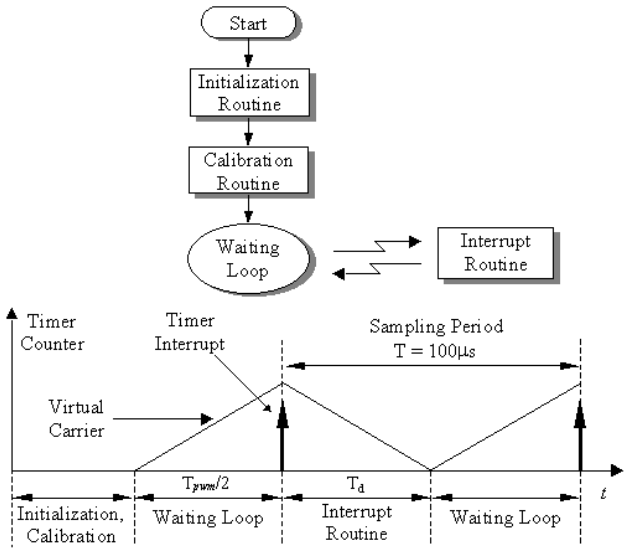

Fig. 17. General flux diagram of DSP algorithm and time diagram

VI. Experimental Results

This section presents experimental results from a 15kVA PWM inverter with the proposed controller. The experimental setup operates with 220V line-to-line rms voltage at 60 Hz.

The inverter switching frequency has been selected to 10 kHz, to limit the switching losses.

The TMS320F241 has been selected for this implementation. This DSP controller is a digital signal processors core with the peripherals of a micro-controller, which integrates an Event-Manager that facilitates the implementation of space vector algorithms. This DSP-controller is capable of executing up to 20 MIPS, which allows the execution of manifold tasks and of complex control in real time reducing the circuitry of the UPS. The analog-to-digital conversions and the implemented space vector algorithm take 45 μs of the CPU time. Therefore, switching frequencies up to 20 kHz can be easily achieved. Fig. 18 shows the three-phase line-to-line voltages v_{ab}, v_{bc} and v_{ca}, for operation at no load. Even in this condition is possible to see that the waveform well damped. Fig. 19, shows the three-phase line current i_a, i_b and i_c, during short circuit operation. The current ripple is small since the output voltage is zero. Finally, Fig. 20 shows the transient from no load to short-circuit. The transient seen in this figure is mainly due to rebound on the mechanic switch used to make short-circuit.

VII. Conclusions

In this paper, a new digital current and voltage controller for three-phase PWM inverters are described and verified experimentally. The developed model takes in to account the execution time required for digital implementation. A systematic design procedure based on an optimal discrete linear quadratic regulator applied to the plant has been developed. With this procedure the controller, parameters that ensure stability from no load to short-circuit can be easily obtained. These results show a good performance with faster responses, reduced settling times and without steady-state error. An anti-windup compensator is proposed to allow a smooth transition between the different modes of operation. Experimental results from a 15kVA PWM inverter using a DSP controller TMS320F241 are presented to demonstrate the performance and validate the analysis carried out.

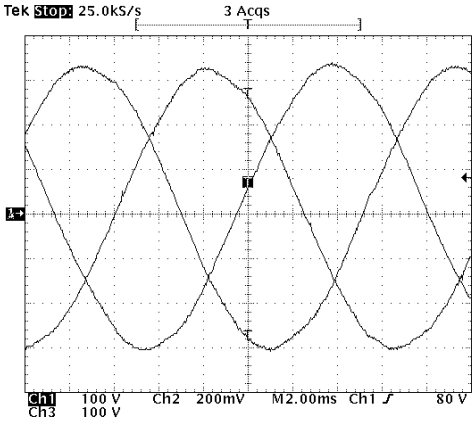

Fig. 18. Experimental results. Three-phase line-to-line voltage under no load operation. Vertical scale: 100V/div, Horizontal scale: 2 ms/div

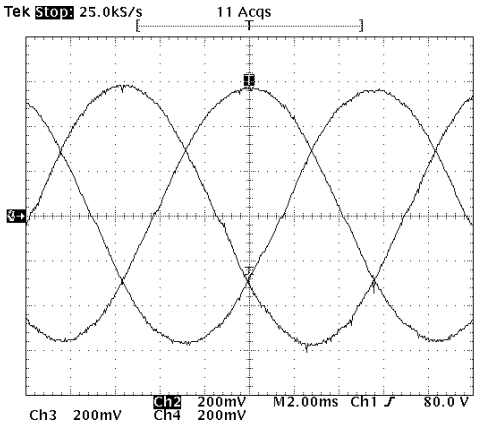

Fig. 19. Experimental results. Three-phase line current in short circuit operation. Vertical scale: 20 A/div, Horizontal scale: 2 ms/div.

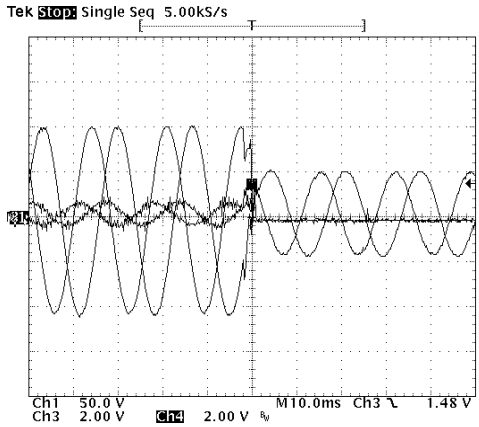

Fig. 20. Experimental results. Output voltage v_{ab} and v_{bc} and the currents i_a and i_b during a transient from no load to short-circuit.

ACKNOWLEDGMENT

The authors wish to thank Mr. Guilherme Bonan and Mr. Marcelo Hey, for assistance in the experimental set-up, and the FOMEC, CNPq and FAPERGS for the financial support.

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