# New Power MOSFET family and SiC-Schottky Diode determine the future Power Electronic Systems

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## I. INTRODUCTION

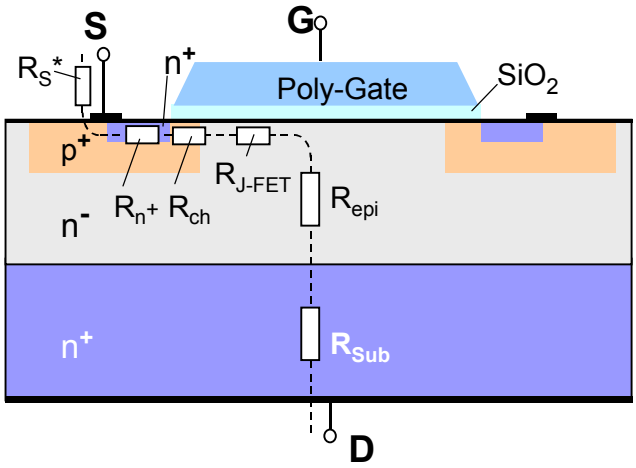
The power MOSFET was developed as early as the second half of the seventies. The superior electrical characteristics of this device ousted bipolar transistors from many applications, and new fields of application were opened up. Further developments focused on reducing the on-resistance $R_{DS\ on}$ and making the devices more rugged, specifically in terms of overvoltage, dv/dt and di/dt capability. With the new generation of OptiMOS transistors from Infineon, as well as the characteristic reduction in on-resistance and self-capacitances, the overvoltage withstand capability both in the input circuit $V_{GS}$ and in the output circuit $V_{DS}$ has been improved. In the input circuit, the familiar planar gate structure has been retained and the gate oxide has been improved in a selective, multi-stage process sequence. In the output circuit, a homogenous cell design and p+ islands more deeply indiffused in a selective process sequence provide these low voltage types with a high degree of avalanche strength. The inherent breakdown strength of the transistors reduces the reverse voltage safety margin, thereby minimizing the static turn-on losses. Consequently, there is no longer any need to match the voltage margin in the MOSFET to the worst-case scenario of non-periodic voltage fluctuations.

Care must be taken to ensure that the maximum junction temperature of the transistor is not exceeded in avalanche mode. The single-pulse avalanche energy is shown in the data book. During avalanche operation, no heat is dissipated by the transistor because of the short time ($t < 1\mu s$); the Si chip is the heat store. The very good commutation capability of the transistor is achieved by the new cell process. This ensures that the parasitic bipolar transistor structure does not come into play even for short commutation processes (high di/dt and dv/dt values).

The second focus of further development is to reduce the on-resistance $R_{DS\ on}$ of the transistor. Whereas in the upper voltage range $200V \leq V_B \leq 1000V$ the on-resistance is basically determined by the epi material (required region for reverse voltage pickup), in the lower voltage range ($V_{BR} \leq 75V$) the on-resistance is made up of a number of component resistances (see Fig. 1). An optimized cell design (horizontal transistor optimization) leading to OptiMOS (new generation transistor technology) has resulted – as Fig. 2 shows – in a drastic reduction in the on-resistance. This further development of the chip made it possible to realize on-resistances of $R_{DS\ on} < 2.5\ m\Omega$ in a TO220 package. This enormously reduces the power dissipation in the transistor, so that power transistors can even be manufactured in SMD packages hitherto only used for ICs.

## OPTIMOS – A NEW CELL CONCEPT

The purpose of developing the OptiMOS concept as an SFET successor technology is to retain the advantages of the SFET (minimum on-resistance, maximum ruggedness) while continuously improving the switching behavior in order to significantly reduce the switching losses particularly in high-frequency applications. From these boundary conditions, a totally new cell concept has emerged (Fig. 3). A significant reduction in the channel resistance has been achieved by once again substantially reducing the channel length. This is made possible by




**$R_{DS(on)}$**

| $V_{DS} \approx 30V$ | | $V_{DS} \approx 600V$ | |
|---|---|---|---|
| $R_S$* | 7% | $R_S$* | 0.5% |
| $R_{n+}$ | 6% | $R_{n+}$ | 0.5% |
| $R_{ch}$ | 28% | $R_{ch}$ | 1.5% |
| $R_{J\text{-}FET}$ | 23% | $R_{J\text{-}FET}$ | 0.5% |
| $R_{epi}$ | 29% | $R_{epi}$ | 96.5% |
| $R_{Sub}$ | 7% | $R_{Sub}$ | 0.5% |

$R_S$* = packaging

Fig. 1: Basic cell structure of a power MOSFET including RDS(on) Distribution for low and high voltage components

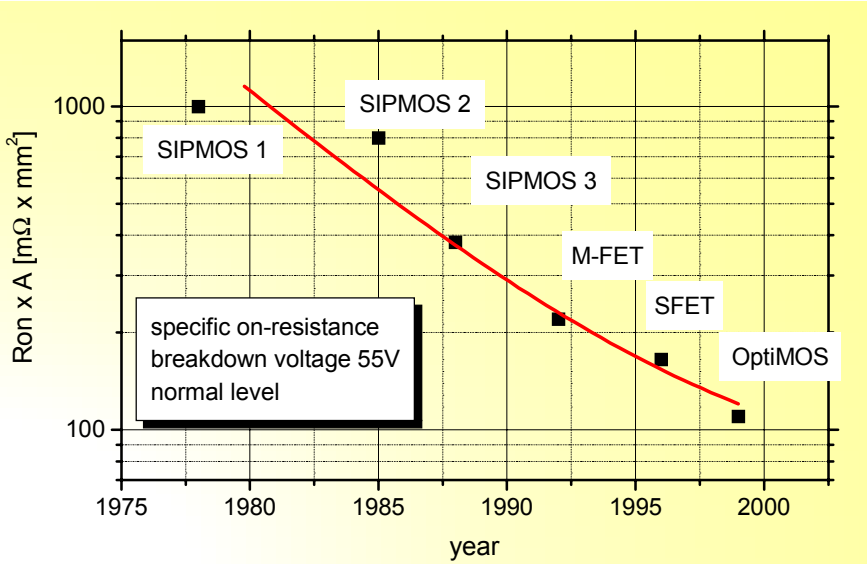



Fig. 2: Development of ON-state resistors

reducing the channel length. This is made possible by selectively introducing the carriers necessary for breakdown voltage or threshold voltage. This technological trick also has a positive effect on fabrication with respect to ruggedness in the case of breakdown (avalanche mode). The smaller the on-resistances of the transistor (Fig. 4), the more important the role of hitherto disregarded contributions even in the low voltage range. This has also been taken into account by further reducing the die thickness and increasing the substrate doping, as well as making the front-side metallization thicker.

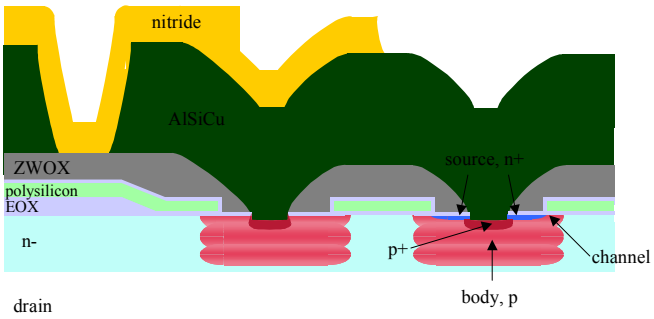



Fig. 3: Cell structure of OptiMOS transistor

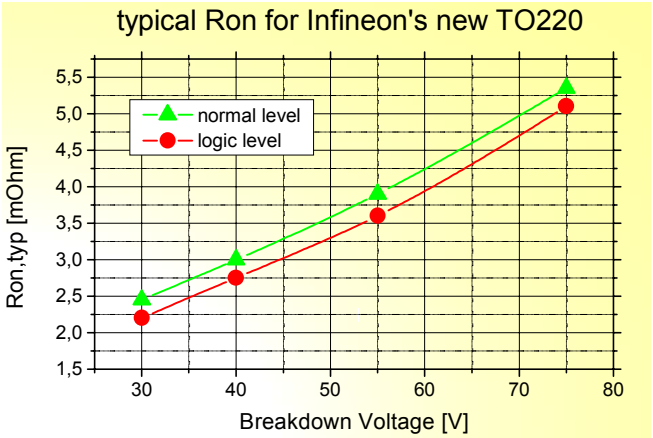



Fig. 4: Outstanding low ON-resistor of new MOSFET generation

## NEW TYPE OF HIGH VOLTAGE POWER MOSFET

At the end of the 80s, high voltage transistors (400 to 1000 V) reached the limits of their development with the well known MOS structure. Improvements to the turn-on resistance could often only be achieved – due to lack of technological improvement potential – by maximizing the silicon area mountable in the traditional housings such as TO-220 or D-Pak.

Now, after two years of intensive development, Infineon is presenting a new high voltage MOSFET family (600 to 1000 V) under the name of CoolMOS. Behind this is a revolutionary MOS technology which enables a reduction of the $R_{DS(on)}$ by factor 5 to 10 with the same chip area in comparison with known technologies.

The increase in performance density with the aim of miniaturization and system integration is one of the basic challenges facing future electronic power systems. In addition they will be subject to stricter requirements with regard to a high system efficiency over the whole load range, with regard to the control dynamic on disturbance variables, reliability etc. The power semiconductor components provide the basic impulse for these further developments.

In the past, attempts to build much smaller electronic power systems such as power packs or converters often failed due to the necessary components. The power semiconductor switches which need to withstand off-state voltages of 600 V, 800 V or 1000 V – depending on their circuit topology – for systems on the 240/400 V mains are a central component here.

Reduction of the turn-on resistance $R_{DS(on),\ an}$ increase in the robustness with respect to critical switching states, avalanche resistance and the reduction of the necessary driver performance by reducing the gate charge are at the forefront of this development. The high voltage MOSFET family CoolMOS sets new standards here as far as turn-on resistance, switching frequency, control power and dynamic losses are concerned.

## COOLMOS DEVICE CONCEPT

The on-resistance of the conventional high voltage power MOSFET is dominated by the resistance of the voltage-sustaining drift zone. The blocking capability of this region is determined by its thickness and the doping. In order to increase the blocking voltage, the doping must be simultaneously reduced and the layer thickness increased. The resistance of the transistor therefore increases disproportionately strongly as a function of its blocking capability. Accordingly, the drift zone causes over 95 % of the total on-resistance in e.g. a 600 V transistor. The main emphasis in improving the transistor's performance must therefore be directed toward reducing this drift region resistance.

The CoolMOS concept (see Figure 5) offers a new approach here to overcome the challenge of the drift-zone resistance. The electrical conductivity is provided by majority carriers only. There is no bipolar current contribution, and hence the switching losses are equal to those of conventional MOSFETs. The doping of the voltage-sustaining layer is raised by roughly one order of magnitude; additional vertical p-stripes are inserted into the structure, which compensate the surplus current-conducting n-charge. When the transistor is reverse-biased, a lateral electric field is built up, which drives the charge toward the contact regions. The space charge layer builds up along the physical pn-junction line and spreads at a voltage of around 50 V across the whole p/n-striped structure. The drift zone is now completely depleted and acts like the voltage-sustaining layer of a pin structure. If the voltage is further increased, the electrical field rises linearly without any further expansion of the space charge layer. The current flows through the space charge layer. Both carrier types are driven toward the contacts by very low electric fields within their columns. This behaviour is characteristic for charge compensated devices and leads to extremely low losses.

This gives an almost linear relationship between the specific resistance and the maximum blocking capability of the transistor shown in Figure 6. The switching behaviour of these transistors corresponds to that of conventional MOSFETs. On the contrary, the gate charge, and with it the necessary activation power of the transistor, is reduced due to the possible reduction in chip area, as compared to a conventional MOSFET with the same on state resistance. With this technology it is now possible in a standard TO220 package 190 mΩ in the 600 V category and 270 mΩ in the 800 V category.

## DYNAMIC BEHAVIOUR

The non-linear spread of the space charge layer as a function of voltage can easily be observed in the characteristic output capacitance. This is reflecting in the resulting drain – source capacitance $C_{DS}$ curve (Figure 7). Due to the drastically increased internal surface of the pn-junction, this capacitance shows large values at small blocking voltages. However, with increase in the blocking voltage, the internal p/n-striped structure starts to deplete. Both, the reduction of this surface and the expansion of the space charge layer width lead to a non-linear behaviour of the output capacitance resulting in a lower value than a conventional MOSFET, at the same $V_{DS}$, and hence lower switching losses. The gate/drain capacitance shows a similar internal meachanism. The gate/source capacitance benefits from the shrink potential of the new concept in comparison with conventional MOSFETs.

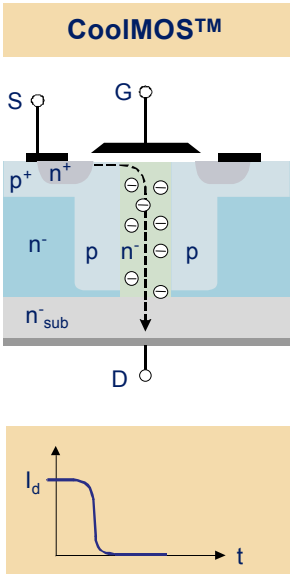



Figure 5: Schematic cross-section through the new CoolMOS high MOSFET from Infineon.

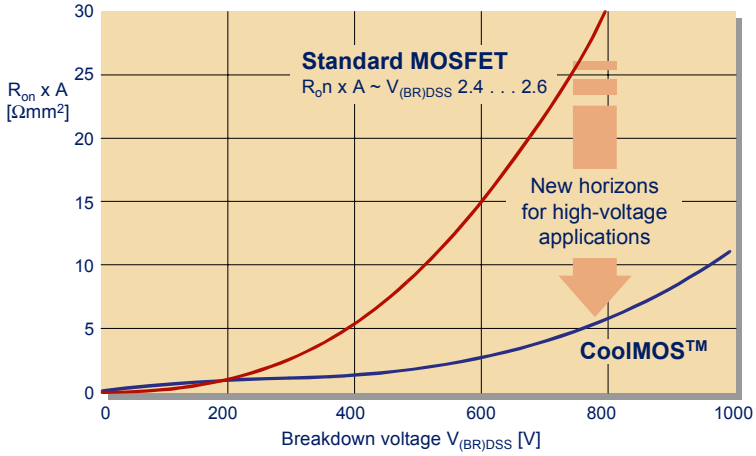



Fig. 6: On state Resistor of CoolMOS company to an conventional MOSFET

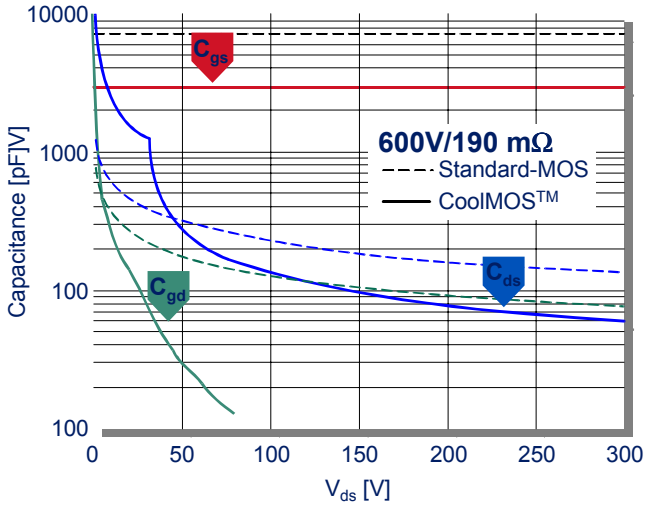



Figure 7: The CoolMOS technology achieves a reduction of all MOSFET capacitances

Due to smaller chip areas CoolMOS transistors exhibit very low gate charge values compared with $R_{DS(on)}$-identical transistors implemented in conventional technology. The gate charge $Q_g$, on the other hand, is a measure of the driver power $P_g$ required at a certain switching frequency $f_{sw}$:

$$P_g = Q_g \cdot V_{gs} \ f_{sw} \qquad (1)$$

The rise and fall times of the drain source voltage during the switching process – and therefore the switching losses – are determined as shown in Figure 8 by the charging process of the gate drain feedback capacitance ("Miller" capacitance $C_{gd}$). The lower the $Q_{gd}$ in particular, the lower the switching losses. The drastic reduction in the gate charge in the new CoolMOS technology is very beneficial for the driving. As a result, CoolMOS transistor can be operated with the lowest control power, the cheapest driver circuit and the highest switching frequencies.

From the application viewpoint, the high value of $C_{ds}$ at low voltages acts like a turn-off-relieve network ("in-built snubber"). However, it is very important for use at high switching frequencies that, in high voltage applications ($V_{DS}$max > 200 V), the energy $E_{DS}$ stored in the output capacitance.

$$E_{DS} = \int_0^{V_{DS\,\max}} C_{DS}(V).V dV \qquad (2)$$

Is lower than in the case of $R_{DS(on)}$-identical transistors in standard MOSFET technology (see Figure 7). This energy, which is converted into heat during every turn-on process, increases with the chip area and therefore limits the minimum attainable power loss in hard switching circuit topologies. Due to the optimized parameters of $R_{DS(on)}$ and $E_{DS}$ and their low input capacitances, CoolMOS transistors are superior to conventional power MOSFETs at both low and high switching frequencies.

This energy which is converted into heat in every turn-on process increases with the chip area and therefore limits the minimum attainable power loss (Figure 9). Due to the optimized product of $R_{DS(on)}$ and $E_{DS}$ and its low input capacitances, the CoolMOS is superior to the conventional power MOS transistor at both low and high switching frequencies.

The output characteristic field of a CoolMOS corresponds to that of a standard MOSFET with the characteristic linear curve at low $U_{DS}$ values without the diode start-up threshold typical for IGBT and bipolar transistors. The gate source insertion voltage has been increased to a typical 4.5 V (range 3.5 V to 5.5 V at 25°C) to improve the signal-to-noise ratio in bridge applications. Due to their great steepness the CoolMOS transistors still reach their nominal $R_{DS(on)}$ already at 10 V gate voltage.

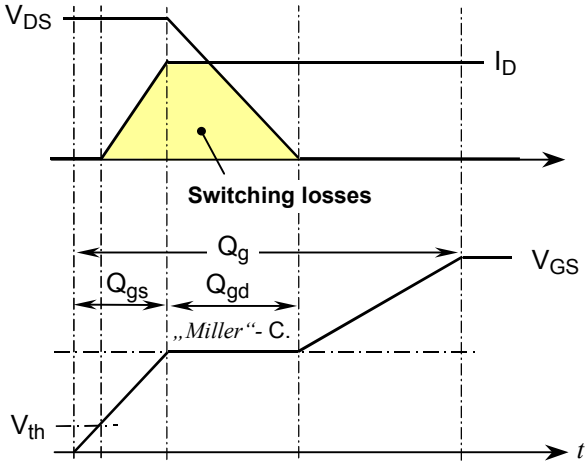



Fig. 8: Time curve of the gate source voltage, drain source voltage and drain current during the turn-on process.

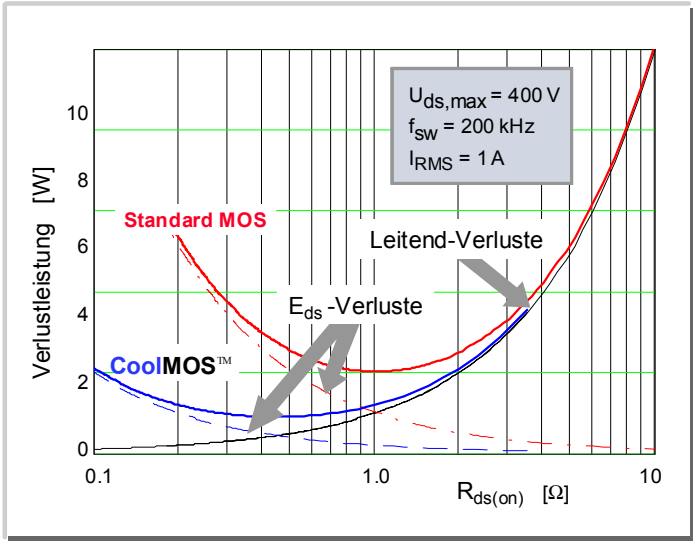



Fig. 9: Lower total losses due to improved product of $R_{DS(on)}$ and $E_{DS}$.

## THE NEW COOLMOS ADJUSTABLE FOR ANY SWITCHING SPEED

The main focus of the new development for the second generation of CoolMOS – which is called the C2 type – was put on the reduction of switching time. Together with the low gate charge well known by the CoolMOS devices and the drastic reduction of internal gate resistor the switching time is almost unlimited but in all parameters

adjustable like in a conventional power MOSFET. This new generation of CoolMOS has a complete different gate structure compared to the first generation (S5 type). In this new gate structured elements the internal gate resistance has a value of less than 1Ω and is almost independent on the chip size. The main question in many applications is, how the switching times, di/dt- and du/dt-values be adjusted. To answer these questions the following investigations have been done.

The controllability of the di/dt- and dv/dt values of CoolMOS is a strong requirement for the application engineer.

The noise emission and oscillation (ringing) is proportional to the di/dt- and dv/dt-slopes during the turn-on and turn-off transients. Further investigations have been done in test set-up by only the external gate resistor values and using the 600 V SiC (a prototype SDP06S60) as a varying commuted diode.

Next two figures demonstrate the drain current and source voltage (Figure 10 and 11) slopes during the turn-off transient for various values of external gate resistor. The turn-on behaviour is controllable in the same manner.

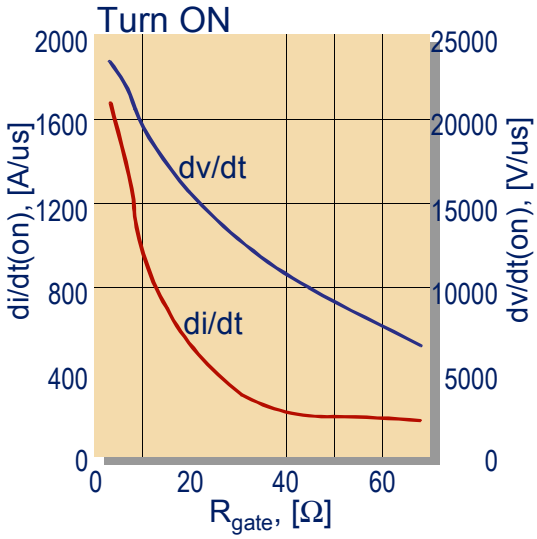



Figure 10: Drain current vs. External gate resistor during turn-off

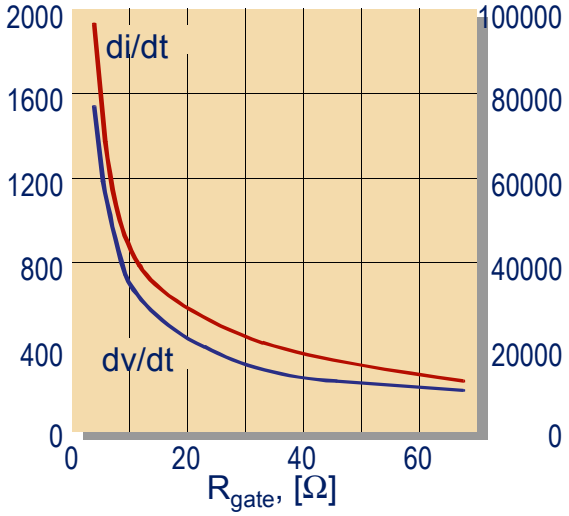



Figure 11: Drain to source voltage vs. external gate resistors during turn-off

Silicon Carbide (SiC) Schottky diodes as unipolar devices offer unique ultra fast switching behaviour making them extremely attractive for applications requiring blocking voltages ranging from 300V to 3000V and switching frequencies higher than 50 kHz. For blocking voltages less than 300V there is a choice of other unipolar diodes like Si or GaAs Schottky diodes. Above 3000V most likely SiC-bipolar diodes will be the option with the best overall performance due to their significantly lower leakage current together with a weaker temperature dependence of this property compared to Schottky diodes.

So far, many groups reported on the manufacturing technology and the rectifying behaviour of Schottky diodes. On the other hand, information about the reliability of such devices regarding peak current capability, and thermal stress tolerance is still rare.

## Switching Behaviour

As already reported by several other groups SiC-Schottky diodes show only capacitive switching losses.

## Overcurrent Stability

In many diode applications short time peak currents may occur occasionally or regularly under certain operating conditions (e. g. capacitor charging). For Si pn diodes the peak current capability is a fixed part of the specification and usually reaches about 2 orders of magnitude higher values than the rated current of the device. On the opposite, there is very little expertise in the literature about this property for SiC diodes.

With a constant forward voltage in the range of 35-75V applied to our diodes for 10µs, a current response as displayed in Fig. 12 can be observed: The current reaches a peak value of up to 140A (1.5mm$^2$ diode area; 120A for 1mm$^2$) immediately after the voltage is switched on. After this the current drops significantly towards the end of the voltage pulse. Such pulses have been repeated up to $10^5$ times (one second delay from pulse to pulse) without destruction of the device. Contrary, forward voltages in excess of 75V cause a destruction of the device, mostly during the first pulse. Failure analysis showed, that the destruction occurred in the edge area. Together with the fact, that the critical forward voltage level closely corresponds to the voltage value where the p-type edge termination area is expected to be completely depleted by the field of the Schottky contact, we conclude, that the destruction is caused by an extremely high current density occurring in the edge area after this complete depletion.

The drastic drop of the current in Fig. 12 is caused by the dissipation of the electrical power in the chip and the strong temperature dependence of the differential on-resistivity of such unipolar devices as described above. From this one can expect a general limitation of the peak current tolerance of SiC-Schottky diodes expecially for longer lasting current pulses due to a thermal runaway.

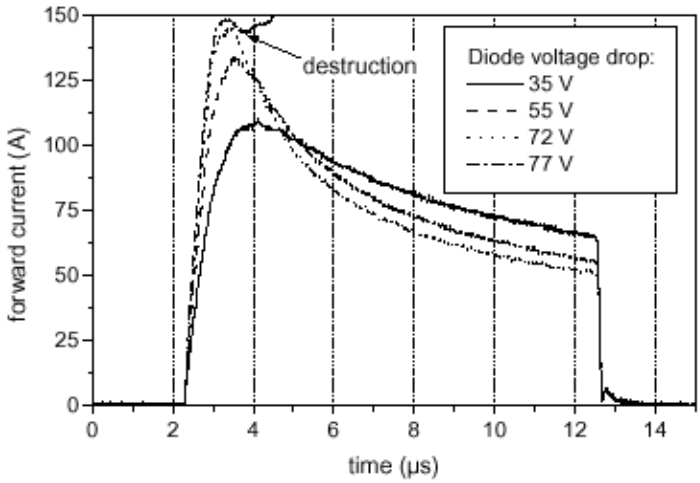



Fig. 12: Current as a function of time for a SiC Schottky diode (10µs constant forward voltage pulse).

## APPLICATION OF COOLMOS C3 WITH SIC DIODE

Boost derived Active Power Factor Correction (APFC) – as shown in Fig. 13- imposes high stress on the main diode and main switch due to the high reverse voltage which may result in a very high reverse current. This study analyses the engineering requirements of the diode and transistor in APFC applications and compares a design with a Silicon Carbide (SiC) diode without snubber. The theoretical considerations where verified by comparing the performance of an ultra fast diode with a lossless snubber to that of a SiC diode without a snubber, in 750W Boost APFC stage. The experiments confirm the conclusions of the theoretical prediction that the SiC is an excellent technological solution to Boost APFC stage operating under continuous current mode (CCM) conditions.

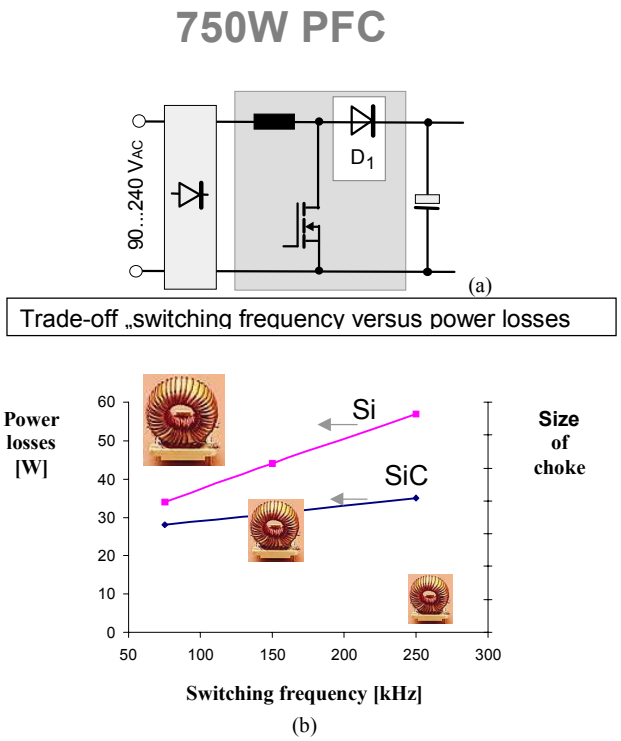



Fig. 13: a) Active power factor correction circuit diagramm b)power loss diagramm

With the SiC-Schottky diode the efficiency shows a virtually independent behaviour regarding frequency due to very low switching power losses, where also ultra fast silicon diodes decrease dramatically in efficiency (Fig.14).

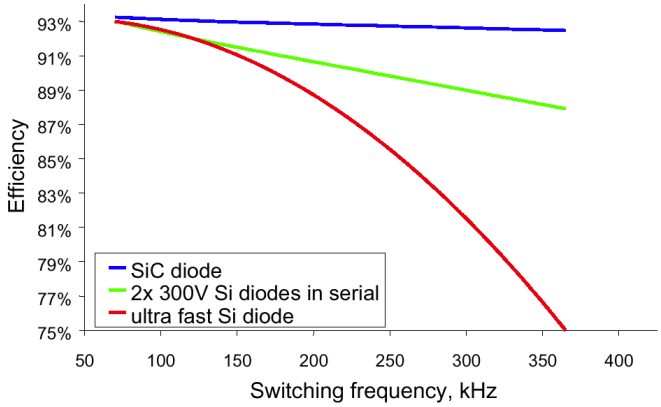



Fig. 14: Efficiency of a PFC boost converter in dependence of the switching frequency at 85 Vac.

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