An Improved of Control Algorithm for Static Synchronous Series Compensator Based on Instantaneous *p-q* Power Theory

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***Abstract* - This paper presents an improved control scheme for the Static Synchronous Series Compensator (SSSC) based on the concepts of instantaneous real and imaginary power theory. The SSSC is a Flexible AC Transmission Current (FACTS) device based on a Voltage Source Inverter (VSI). Several strategies and control techniques are proposed in such a way that the SSSC injects a sinusoidal voltage, with a variable magnitude and phase, in series with transmission line. In the instantaneous *p-q* based control the SSSC is controlled to inject or drain only imaginary power in series with the transmission line, thereby emulating a capacitive or inductive reactance. All control strategies presented was tested using an Alternative Transients Program (ATP/EMTP) simulation package. Digital simulation results are carried out to compare the performance of the improved control algorithm.**

Keywords – Series reactive power compensators, SSSC, FACTS devices.

I. INTRODUCTION

Nowadays, the design of static power compensators for power system applications has an important role in the field of the power electronics. Thyristor Controlled Series Capacitor (TCSC), Static Synchronous Series Compensator (SSSC) among other compensators named as FACTS devices are real options to control ac energy systems. These compensators are based on large capacity naturally commutated switches (*e.g.* thyristors) and self-commutated switches (*e.g.* GTOs, IGBTs and IGCTs). They are expecting to be powerful tools to increase the performance and the controllability of the transmission and distribution ac lines.

Specifically for SSSCs, they are based on self-commutated VSI (Voltage Source Inverter), which are connected in series with the ac lines through series transformers. They can be used to control the active power flow, to increase the transfer power capability through ac lines, to reduce the drop along the transmission paths, etc.

Three basic strategies are used to control the SSSC compensation voltages. The first scheme forces the SSSC to emulate a series reactance. Thus, if the injected VSI voltage is lagging with the respect to the line current, the SSSC will emulate a series capacitive reactance. Other wise, if the injected voltage is leading with respect to the line current the SSSC will synthesize a series inductive reactance. As the magnitudes of the VSI ac voltages can be varying continuously, the ac line compensation level can be continuously controlled.

The second strategy forces the SSSC to inject a compensation voltage, with constant magnitude, lead or lag by $\pi/2$ *rad* with respect to the line current while the last scheme proposes the usage of the SSSC to generated or absorb reactive power in series with the ac line. Thus, the design of the SSSC is easier because all compensation strategies generate voltages in quadrature with respect to the line currents. This characteristic assures that ideally the VSI does not have to supply active power in series with the system.

As explained before the application of power electronics to power transmission and distribution systems should be based on high-voltage withstand capability devices as well as high reliability controls. Presently, a great number of algorithms have been proposed in the literature to control the SSSC [2],[3],[5],[6].

In this paper, after presenting a short review of the compensation strategies based on the instantaneous *p-q* (real and imaginary) powers theory, it will be proposed an improved scheme to control the SSSC. This theory was developed initially to design and control active power filters (APF) [7] and it was modified very successfully to control shunt and series compensators [4],[5],[10]-[12].

The improved control strategy and the fundamentals of the SSSC were tested using the Alternative Transients Program (ATP/EMTP) simulation package. Some simulation results with discussions are also presented.

II. SYSTEM CONFIGURATION

Fig. 1 shows the simplified block diagram of the proposed SSSC connected at the sending-end side of a three-phase power transmission line modeled by three series reactance X_L at fundamental frequency. The source

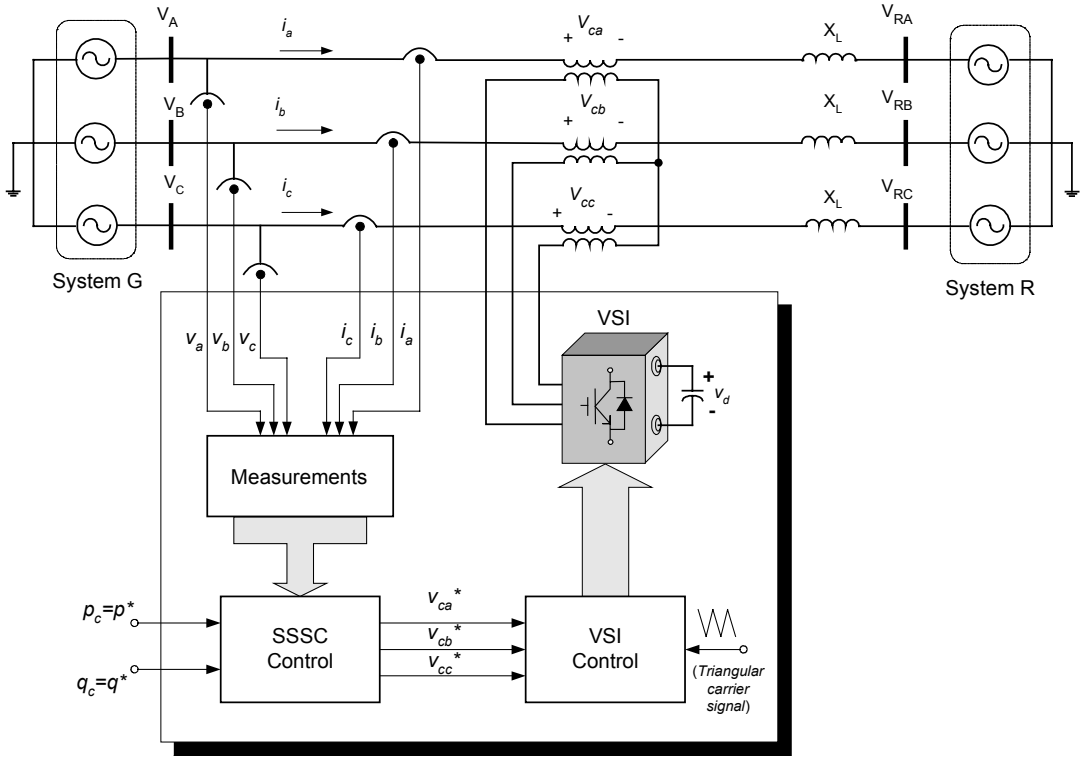

Fig. 1: Schematic diagram of Static Series Synchronous Series Compensator (SSSC) connection.

(system G) and the load (system R) are represented by two ideal three-phase voltage sources, which are phase shifted by an angle δ and their magnitudes are taken equal to *V*.

In this figure, the *SSSC Control* block, which is the main objective of this work, uses the concepts of instantaneous real and imaginary power theory. The signals p^* and q^* are the instantaneous reference powers that the SSSC should inject in series with the ac line. To calculate the reference voltages (v_{ca}^*, v_{cb}^*, v_{cc}^*) the control block needs the measurements of the sending-end three-phase transmission line voltages and the line currents.

The *VSI Control* block uses a sinusoidal PWM (Pulse Width Modulation) technique to control the upper and lower switch of each VSI branch in a complementary manner. The PWM switching pattern is determined through the comparisons of the reference voltages v_{ca}^*, v_{cb}^*, v_{cc}^* with a triangular carrier wave [13].

It will be shown later that four PWM-VSIs connected in series through four Y-Y transformers form the VSI used in this work. However to minimize the harmonics of the output voltages the VSIs should be modulated by 4 triangular carrier waves with same frequency but displaced by π/2 *rad* [2],[6].

III. Brief Review of Control Schemes Based on Instantaneous Powers Theory

The instantaneous real power *p* (*W*) and the instantaneous imaginary power *q* (*vai – imaginary volt-ampère*) in a three-phase system are defined by [7]:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \tag{1}$$

or by,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}, \tag{2}$$

where, v_α, v_β, i_α and i_β are the instantaneous system voltages (*V*) and currents (*A*) after a (α-β-0) transformation, respectively.

A control algorithm to SSSC based on (2) was proposed in [5]. The SSSC emulates three controllable voltages in series with the transmission line in such a way to control the active power flowing in the power system. For the system shown in Fig. 1, for a given p_c and q_c, the series reference compensating voltages can be calculated in α-β coordinates by:

$$\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} = \frac{1}{\left(i_\alpha^2 + i_\beta^2\right)} \begin{bmatrix} i_\alpha & -i_\beta \\ i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} p_c \\ q_c \end{bmatrix} \tag{3}$$

where, $v_{c\alpha}$ and $v_{c\beta}$ are the instantaneous series compensating voltages (*V*) in α-β coordinates.

Ideally, the proposed Static Synchronous Series Compensator is designed to generate or absorb only reactive power. Thus,

$$p_c = p^* = 0 \quad \text{and} \quad q_c = q^* \tag{4}$$

where, p^* is the instantaneous real reference power and q^*

is the instantaneous imaginary reference power that have to be injected or absorbed by the compensator in series with the ac transmission line by the SSSC.

The variables with superscript (*) in previous equations are reference signals, which are supplied by the series compensator control block shown in Fig. 1 to the controller of the VSI. As the instantaneous reference powers are $p_c = p^* = 0$ and $q_c = q^*$, the SSSC generates three series compensating voltage in quadrature with respect to the line currents. This characteristic makes the design of the VSI easier because ideally the compensator does not have to absorb or to supply any real power in series with the line. However as shown in [6] since the compensating voltages are directly dependent on the line currents, the system becomes unstable for low levels of active power flowing through the ac line.

In [10] the series part of a UPFC (*Unified Power Flow Controller*) was controlled using an adapted algorithm developed for a hybrid series Active Power Filter (APF) [9]. This algorithm is summarized below considering the system configuration shown in Fig. 1.

Based on (1), for a given p_c and q_c, the following equation can be written:

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} = \frac{1}{\Delta}\begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix}\begin{bmatrix} p_c \\ q_c \end{bmatrix}, \tag{5}$$

where, $\Delta = v^2_\alpha + v^2_\beta$; v_α and v_β are the instantaneous sending-end ac line voltages (V) obtained through α-β-0 transformation; i^*_α and i^*_β are reference currents (A) that should flow through the compensator terminals.

From (5), the instantaneous series voltages $v^*_{c\alpha}$ and $v^*_{c\beta}$ that the SSSC has to synthesize in series with the transmission line can be calculated as:

$$\begin{bmatrix} v^*_{c\alpha} \\ v^*_{c\beta} \end{bmatrix} = K_R \begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix}, \tag{6}$$

where, K_R is a compensation gain.

As shown in [9] for the APF control and in [10] in the control of the UPFC the compensator emulates three series resistances. Thus an average instantaneous real power arises at the SSSC terminals. This characteristic is easily explained because the reference voltages given in (6) are not in quadrature with respect to the ac line currents but to the sending-ending transmission line voltages. Therefore, the operation of the SSSC without any power source connected at the VSI dc side will be possible if an instantaneous real power feedback control loop is designed to assure that the dc capacitor voltage will stay constant.

IV. The Improved Control

The calculation of the value of the gain K_R in (6) is not easy because the compensation level is highly influenced by the system impedance [9] and it can be determined after exhausting digital simulations. In [10] the author showed that high values of K_R could also make the system unstable.

Neglecting the harmonics generated by the VSIs, the following approximation can be done $v_{c\alpha} = v^*_{c\alpha}$ and $v_{c\beta} = v^*_{c\beta}$. Then, substituting (5) and (6) in (2), for a given $p_c = p^* = 0$ and $q_c = q^*$, the following expression are obtained for the real and imaginary powers at the SSSC terminals:

$$p_{sssc} = K_R\left(\frac{q_S}{\Delta}\right)q^* \tag{7}$$

and,

$$q_{sssc} = -K_R\left(\frac{p_S}{\Delta}\right)q^*, \tag{8}$$

where, $p_S = (v_\alpha i_\alpha + v_\beta i_\beta)$ is instantaneous real power (W) and $q_S = (v_\alpha i_\beta - v_\beta i_\alpha)$ is instantaneous imaginary power (vai) flowing into the source, respectively.

Based on (8), if instantaneous imaginary power (q_{sssc}) at the SSSC terminals is equal to the instantaneous imaginary reference power (q^*), the value of the gain K_R should be taken:

$$K_R = -\frac{\Delta}{p_S}. \tag{9}$$

Fig. 2 shows a block diagram of the SSSC control scheme. From the above discussions, the *on line* calculation of the gain K_R is more efficient than the original algorithm, given by (5) and (6), in spite of the need of knowing the instantaneous real (p_s) power flowing at the sending-end side of the ac line. From (7), the SSSC will never produce an instantaneous imaginary power q^* without an associated instantaneous real power p_{sssc}.

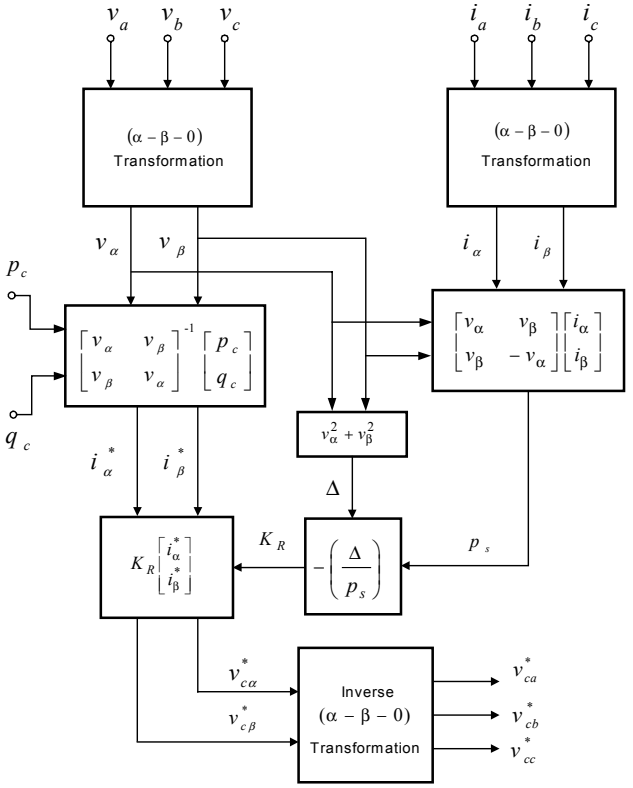

Fig. 2: Block diagram of the SSSC control scheme.

In parallel with this undesired behavior, the SSSC internal losses discharge the dc VSI capacitor and as explained in the previous section the instantaneous reference real power signal (p^*) could be used by a dc voltage regulator forcing the VSI to absorb some amount of instantaneous real power in series with the ac line. Then, the action of the controller will keep the dc capacitor voltage constant on its nominal value.

Thus, considering $p_c = p^* \neq 0$ and $q_c = q^*$, the compensating voltages can be calculated in (α-β) coordinates by (5) and (6). Substituting the obtained result in (2), the following expressions can be written for the instantaneous powers at the SSSC terminals:

$$p_{sssc} = K_R\left(\frac{p_s}{\Delta}\right)p^* + K_R\left(\frac{q_s}{\Delta}\right)q^* \qquad (10)$$

and,

$$q_{sssc} = K_R\left(\frac{q_s}{\Delta}\right)p^* - K_R\left(\frac{p_s}{\Delta}\right)q^* . \qquad (11)$$

From (10) and (11), the SSSC will never produce an instantaneous real power p^* without an associated instantaneous imaginary power q_{sssc} and an instantaneous imaginary power q^* without an associated instantaneous real power p_{sssc}. With the objective to overcome this problem, the authors proposed a modification in the original control algorithm given by (5) and (6). Fig. 3 shows the improved SSSC control where two uncoupling signals, Δp and Δq, are added to the *instantaneous reference real* (p_{Cref}) and *imaginary* (q_{Cref}) *powers* that the SSSC should inject in series with the ac line.

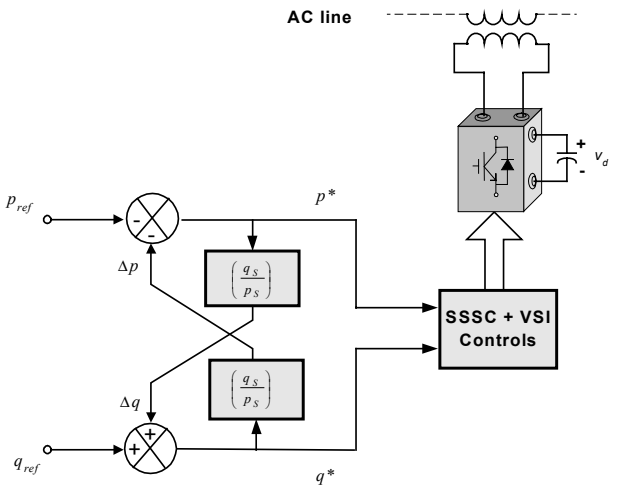

Fig. 3: Block diagram of the improved SSSC control.

From Fig. 3, doing $p^* = (-p_{Cref} - \Delta p)$ and $q^* = (q_{Cref} + \Delta q)$ in (10) and (11), the uncoupling signals can be determined, for $p_{SSSC} = p_{Cref}$ and $q_{SSSC} = q_{Cref}$, as follows:

$$\Delta p = \left(\frac{q_s}{p_s}\right)q^* \qquad (12)$$

and,

$$\Delta q = \left(\frac{q_s}{p_s}\right)p^* . \qquad (13)$$

where, p_S and q_S are the instantaneous real (W) and imaginary (vai) powers at the sending-end side of ac transmission line, respectively.

V. Simulation Results

In order to study the usefulness of the proposed control scheme, the SSSC shown in Fig. 1 was implemented using the ATP/EMTP simulation package. The source and the load were modeled as two ideal three-phase voltages with 230 kV/60 Hz connected by a transmission line with 188 Ω of series reactance. The transmission angle δ, between the source and load, was taken equal π/9 rad. This procedure will permit to investigate the performance of the SSSC when low currents are flowing over the ac line.

The SSSC was synthesized by four PWM-VSI connected in series through four Y-Y transformers, as shown in Fig. 4, with a 500 μF / 10 kV dc capacitor. Each VSI is switched at 1 kHz and the semiconductor devices are modeled as ideal switches with reverse diode connected in anti-parallel. The control algorithm proposed in this work was implemented using the TACS.

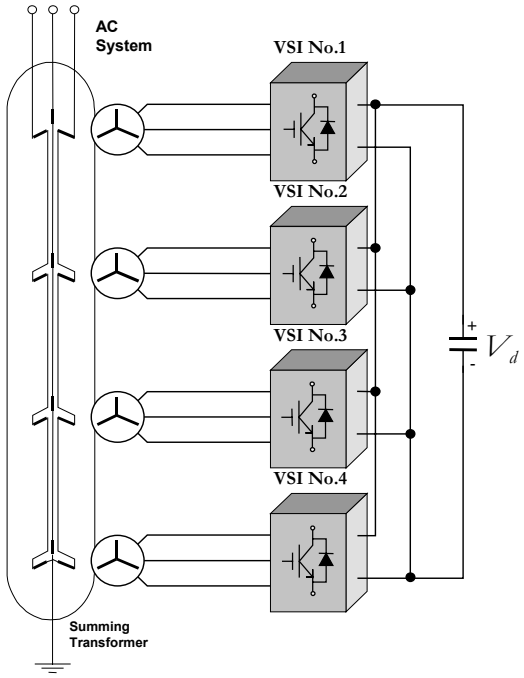

Fig. 4: Multilevel PWM-VSI.

Fig. 5 and Fig. 6 show the instantaneous real and imaginary powers at SSSC terminals, respectively. The SSSC operates initially with a null compensation characteristics when in $t = 0.2\ s$ the instantaneous reactive reference power is step changed from 0 to –10 Mvai. Fig. 7 and Fig. 8 show the instantaneous reference compensating voltage, generated by the SSSC control block, and the instantaneous voltage synthesized by the SSSC in phase "a", respectively.

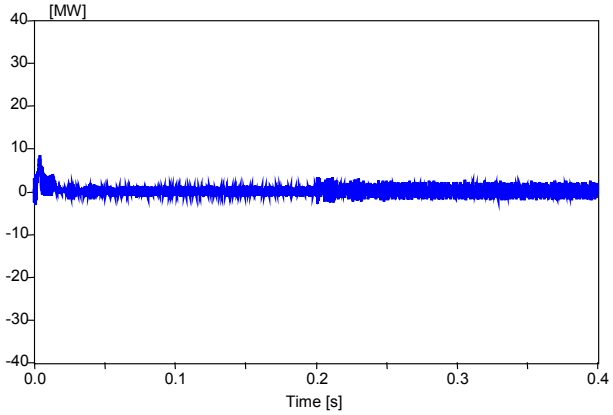

Fig. 5: Instantaneous real power at SSSC terminals.

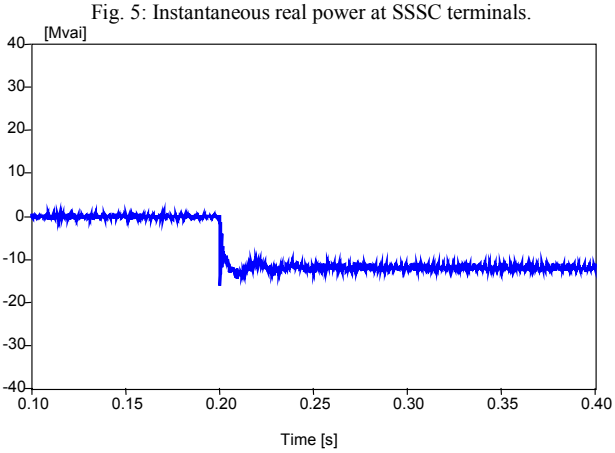

Fig. 6: Instantaneous imaginary power at SSSC terminals.

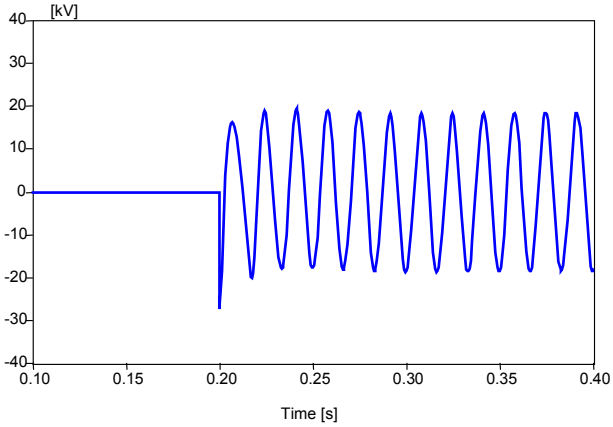

Fig. 7: Instantaneous reference compensating voltage for phase "a".

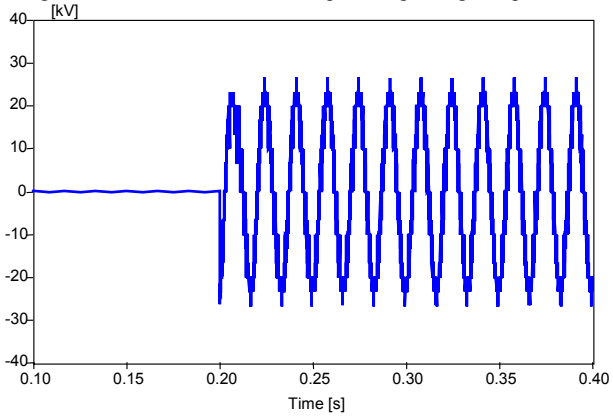

Fig. 8: Instantaneous compensating voltage at phase "a" of the SSSC.

Fig. 9 shows the ac line current of phase "a". Fig. 10 shows instantaneous real and imaginary powers at the source terminal. Note that the line current, and consequently the real power over the ac line, increases when the SSSC starts its operation with a capacitive characteristic (negative imaginary power).

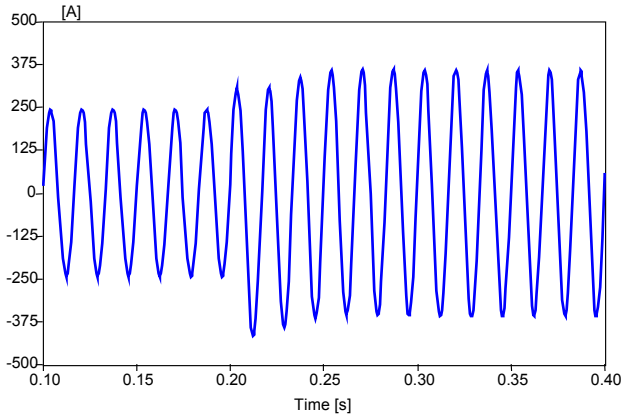

Fig. 9: Instantaneous phase "a" line current.

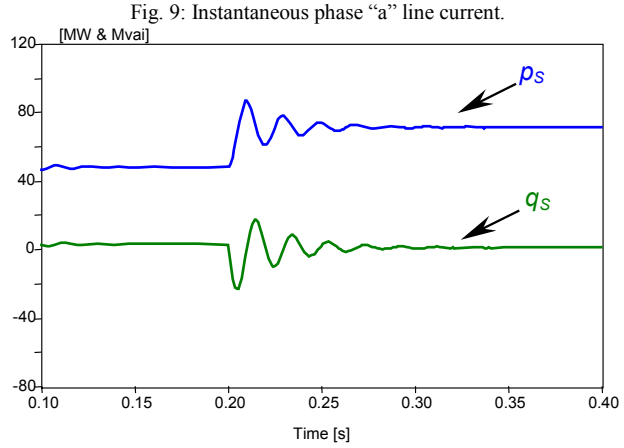

Fig. 10: Instantaneous real power at source terminals.

Fig. 11 shows the dc capacitor voltage. Fig. 12 and Fig. 13 show the signals Δp and Δq used to uncouple the control variables p^* and q^*, respectively. Note that when the dc capacitor varies the SSSC absorbs a small amount of real power in series with the ac line due to the operation of a dc voltage regulator, not shown in Fig. 3. This characteristic explains the oscillatory behavior observed in Fig. 13. However, during the periods in which the dc capacitor voltage is equal to its nominal value ($10\,kV$) the instantaneous real power at the SSSC terminals is practically zero and consequently $\Delta q = 0$.

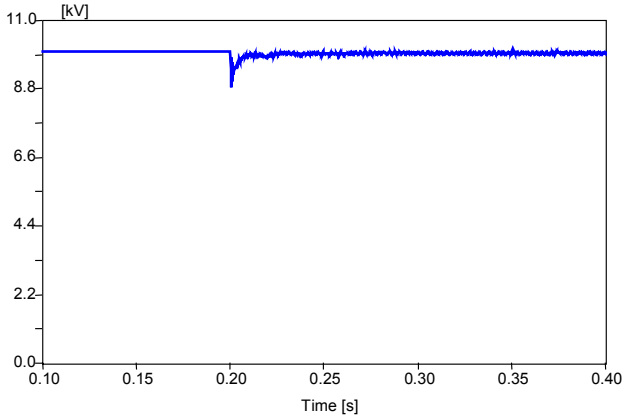

Fig. 11: DC capacitor voltage.

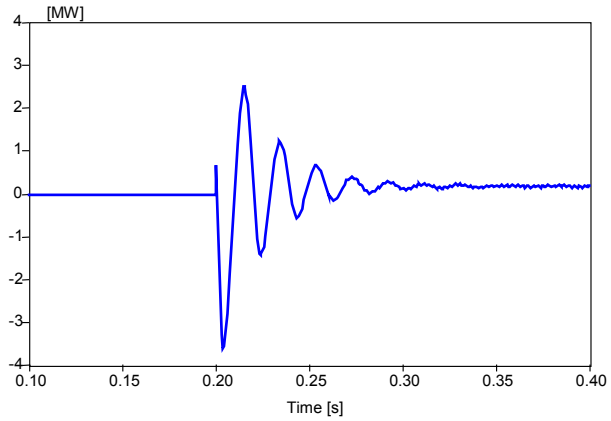

Fig. 12: Additional uncoupling signal Δp.

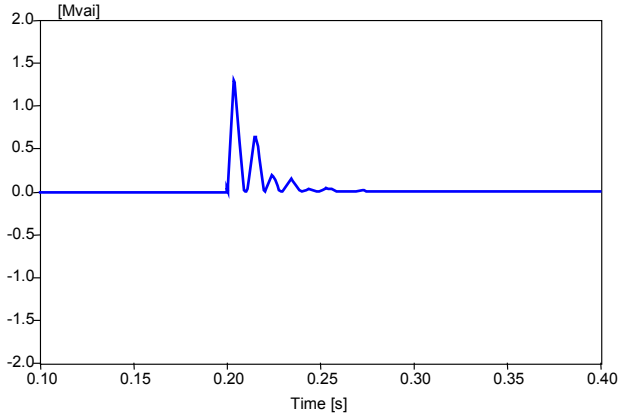

Fig. 13: Additional uncoupling signal Δq.

Finally, Fig. 14 shows a detail of the PWM-VSI multilevel voltage lags by $\pi/2$ *rad* from the ac line current.

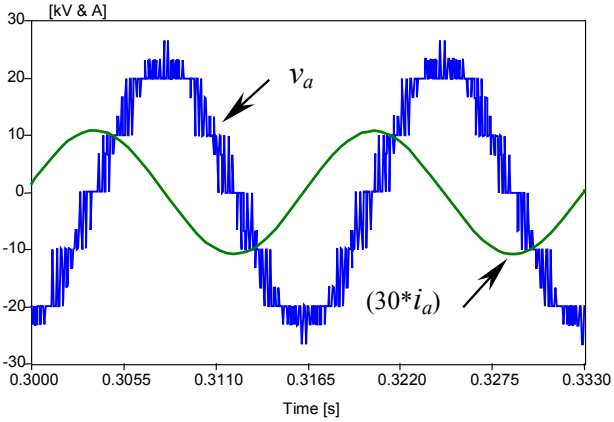

Fig. 14: Detail of the phase "a" PWM-VSI voltage and line current.

VI. Conclusions

In this paper, an improved control algorithm for Static Synchronous Series Compensator was proposed. The control scheme was based on *p-q* powers theory. General equations relating the real and imaginary powers at the compensator terminals were presented. These equations are very useful to design the controllers' gains and to improve the SSSC performance. Digital simulation results shown that new compensation technique operates very well for low level of active power flow. The authors believe that the presented concepts will be very important to design series FACTS devices.

VII. References

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