Using Duality Properties to Develop Hysteresis Based, Voltage Controllers for a Current Source Converter

Lourenço Matakas Junior and Wilson Komatsu

University of Sao Paulo / Department of Electrical Energy and Automation
Av. Prof. Luciano Gualberto, trav. 3, n. 158
05508-900 São Paulo, SP; BRAZIL
Phone: +55-11-3818-5483 FAX: +55-11-3818-5719 e.mail: matakas@pea.usp.br

Abstract - Based on the duality between the equivalent circuits of the Voltage and Current Source converters this paper applies the decoupled hysteresis voltage controller for the CSC (current source converter) case. With this strategy, the converter operates like three independent three-phase units, permitting after the decoupling, the use of independent hysteresis comparators. It presents excellent tracking and transient response. The mapping of the switching functions of the equivalent converter to the real three-phase one is discussed, resulting in a new proposed method. The decoupled case is compared to the simple controller with three comparators. The behavior of their switching frequency and operation range is discussed.

I. INTRODUCTION

Unlike the Voltage Source Converter (VSC), which has widespread applications and a great variety of well-known PWM strategies [9], the Current Source Converter (CSC), have a more restricted use. The existing duality properties of the 'one-phase' VSC and CSC, allows one to easily obtain the CSC PWM strategies from the VSC ones. In the past, the 'three-phase' VSC and CSC were not considered dual circuits by many authors, forcing the researchers to find specific PWM strategies for the CSC case [3,4,5,8].

[1] proposed a high performance, fixed frequency, simple method for the CSC, by substituting the real three-phase, six switches converter (fig.1) by a fictitious unit consisting of three one-phase, delta connected, two level (+Idc/2, -Idc/2) current sources (fig.2). This equivalent circuit is planar and is dual of the equivalent circuit of the VSC (Fig. A2, Appendix A). In [1] the independent fictitious current sources are controlled by individual triangular PWMs and their results are easily mapped to the real six switches converter. This method seems to be adequate for the implementation of the AC voltage control by means of an hysteresis PWM. However this paper shows that this configuration has the same problems caused by the coupling between the converter phases in the VSC, which can lead to the loss of control for short periods and the voltage error will exceed the tolerance band [11].

This paper shows that the use of a decoupling block [6,7], associated to three hysteresis controllers leads to a simple and high performance solution. This strategy is compared to the conventional hysteresis control with independent comparators for each phase, based on their tracking ability, transient response, behavior of the switching frequency and operation range.

A simple method to map the switching actions of the fictitious converter to the switches of the real three-phase converter is proposed.

These results were previously shown in [12], and are presented here including some corrections and additional explanations.

II. CONVERTER CIRCUIT AND ITS EQUIVALENT REPRESENTATION

The purpose of the control circuit is to force the AC side capacitor voltages ($V_{rs}; V_{st}; V_{tr}$), to track the desired reference signals ($V_{rs\,ref}; V_{st\,ref}; V_{tr\,ref}$). The AC load is modeled as a three-phase current source. The original circuit in fig.1 is modified by considering the converter as composed by three independent ideal current sources 'i_{rs}, i_{st}, i_{tr}', with two levels ($-I_{dc}/2, +I_{dc}/2$) as shown in fig.2, which can produce AC side currents (i_r, i_s, i_t) with three levels ($+I_{dc}, 0, -I_{dc}$), like the original converter.

A delta-connected load (fig. 3) will be more convenient to explain the duality between the VSC and CSC cases.

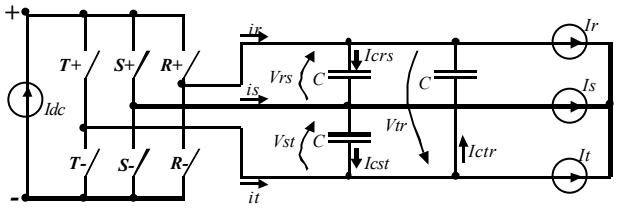

Fig. 1. Original Converter Circuit + filter +load

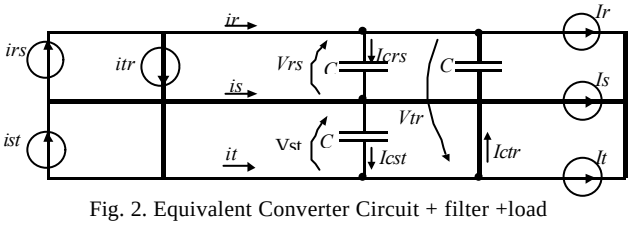

Fig. 2. Equivalent Converter Circuit + filter +load

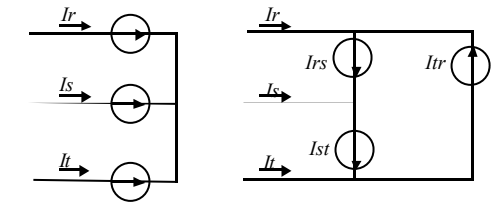

Fig. 3. Equivalence of the Y and Δ load connections

III. LINE AND PHASE CURRENTS RELATIONSHIP

According to [1], the current sources instantaneous

amplitudes (i_{rs}, i_{st}, i_{tr}) are related to the set of AC side reference currents (i_r, i_s, i_t) by (1):

$$\begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} = \mathbf{A} \begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} \quad (1)$$

As det(A)=0, A has no inverse. However a particular solution (2) can be obtained if $i_{rs} + i_{st} + i_{tr} = 0$.

$$\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} = \mathbf{B} \begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} \quad (2)$$

This fact must be better explained. It is easy to verify that, the sum $i_{rs} + i_{st} + i_{tr}$ is instantaneously not null, for the eight possible states of the two level current sources i_{rs}, i_{st}, i_{tr}. So, (2) cannot be used to map the three-level currents i_r, i_s, i_t to the fictitious currents i_{rs}, i_{st}, i_{tr}. By the other side, if the averaged behavior of the system is considered, (2) can be used calculate the reference currents of the fictitious converters ($i_{rsref}, i_{st\,ref}, i_{trref}$), from the values of the desired values of the line currents $i_{rref}, i_{sref}, i_{tref}$. So, (2) must be used with care.

Additionally, rank(A)=0 and any set ($i_{rs} + i_0, i_{st} + i_0, i_{tr} + i_0$) will be a solution of (2). This suggests the use of the injection of a zero sequence signal i_0, to the references of the fictitious converters. This will not affect the averaged behavior of the line currents, but will affect their harmonic contents. So, it can be used for harmonics minimization as will be presented in a coming paper.

IV. CONVERTER MODELING

The state space equation of the system in fig. 2 is given by (3).

$$\frac{d}{dt}\begin{bmatrix} V_{rs} \\ V_{st} \\ V_{tr} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} I_{C\,rs} \\ I_{C\,st} \\ I_{C\,tr} \end{bmatrix} = \frac{1}{C}\left(\mathbf{BA}\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \mathbf{B}\begin{bmatrix} I_r \\ I_s \\ I_t \end{bmatrix} \right) =$$

$$\frac{1}{C}\left(\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \mathbf{B}\begin{bmatrix} I_r \\ I_s \\ I_t \end{bmatrix} \right) = \quad (3)$$

$$\frac{1}{C}\left(\mathbf{BA}\left(\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \begin{bmatrix} I_{rs} \\ I_{st} \\ I_{tr} \end{bmatrix} \right) \right)$$

As a consequence of coupling between the phases imposed by matrix **BA**, changes in any of the variables i_{rs}, i_{st}, i_{tr} affect the three line voltages ($V_{rs}; V_{st}; V_{tr}$). This coupling disturbs the operation of independent hysteresis controllers. A decoupling strategy is shown in section VI.

V. DUALITY PROPERTIES AND PWM

The original three-phase bridge (fig.1) is not a planar circuit (can not be drawn without line crossings), and does not have a dual counterpart. The equivalent circuit in fig.2, with delta connected load, is planar, and its dual corresponds to the equivalent circuit of the VSC shown in Fig. A2 (Appendix A). As equations (3) and (A-1) have the same structure, all PWM strategies used for VSC can also be applied to the equivalent CSC in fig.2.

A two-level PWM strategy applied to the equivalent converter ($i_{rs}, i_{st}, i_{tr} = \pm I_{dc}/2$), results in the three-level AC side line signals ($i_r, i_s, i_t = \pm I_{dc}$), which can be easily mapped to the states of the six switches of the real three-phase converter (fig. 1). (see section VII and [1,12])

VI. DECOUPLING STRATEGY

The signal '$i_0 = (i_{rs} + i_{st} + i_{tr})/3$', defined as the 'instantaneous zero sequence current', can be added to the currents ($i_{rs}; i_{st}; i_{tr}$) of the 'equivalent converter. Since the load currents satisfy ($I_{rs} + I_{st} + I_{tr} = 0$), from (3) results:

$$\frac{d}{dt}\begin{bmatrix} V_{rs} \\ V_{st} \\ V_{tr} \end{bmatrix} = \frac{1}{C}\left(\mathbf{BA}\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} + \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \mathbf{BA}\begin{bmatrix} I_{rs} \\ I_{st} \\ I_{tr} \end{bmatrix} \right) =$$

$$= \frac{1}{C}\left(\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\left(\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \begin{bmatrix} I_{rs} \\ I_{st} \\ I_{tr} \end{bmatrix} \right) \right) = \frac{1}{C}\left(\begin{bmatrix} i_{rs} \\ i_{st} \\ i_{tr} \end{bmatrix} - \begin{bmatrix} I_{rs} \\ I_{st} \\ I_{tr} \end{bmatrix} \right) \quad (4)$$

The system described by (4) is fully decoupled, and behaves like a six wire three-phase system consisting of three independent sets of one-phase converter, capacitor and load as shown in fig.4.

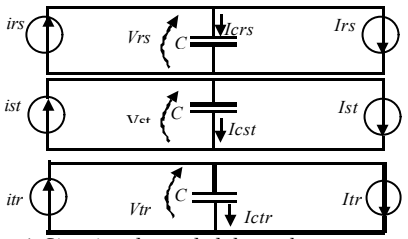

Fig. 4. Six wire, decoupled three phase system

The difference between the circuits shown in fig.4 and fig.2, is that the instantaneous zero sequence currents 'i_0' generated by 'i_{rs}, i_{st}, i_{tr}', cannot flow nor in the AC lines ($i_r; i_s; i_t$), neither in the capacitors of fig.2.

Based on the above statements, the instantaneous value of the fictitious zero sequence current 'i_0' can be on line calculated, and added to the real capacitor currents, resulting in fictitious capacitor voltages equal to that found in a six wire system. A control strategy based on the comparison of the fictitious voltages ($V_{rs} + v_0; V_{st} + v_0; V_{tr} + v_0$) with the reference voltage signals ($V_{rs\,ref}; V_{st\,ref}; V_{tr\,ref}$) is similar to the hysteresis control of the six wire case (fig.4)[6,7]. As a consequence, an independent per-phase control will not present the

problems of error signals [9] exceeding the tolerance band and the occurrence of limit cycles with high switching frequency periods [11]. The duality properties allow applying, all the knowledge related to three-phase, three-wire VSC, to the CSC case. The block diagram of the proposed system is shown in fig.5. This strategy is similar to the ones presented in [6,7].

The zero sequence capacitors' voltage v_0, added to the set of measured voltages '$(V_{rs};V_{st};V_{tr})$', is calculated by (5).

$$\frac{dv_0}{dt}=\frac{1}{3C}(i_{rs}+i_{st}+i_{tr})=\frac{1}{C}i_0 \qquad (5)$$

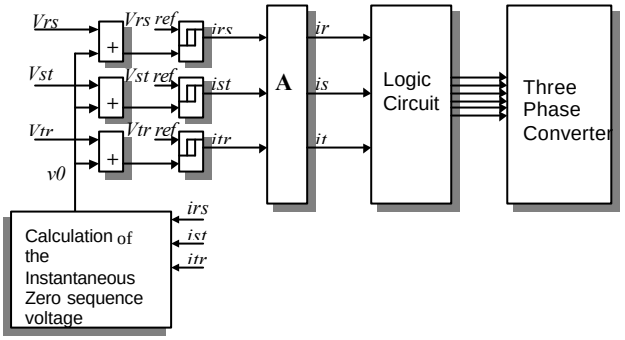

Fig. 5. Block diagram of the proposed decoupled controller

VII. MAPPING $i_r;i_s;i_t$ TO THE SWITCHES' STATES

Table I presents the eight possible status of the sets 'i_{rs},i_{st},i_{tr}' and '$i_r;i_s;i_t$'. The space vectors corresponding to '$i_r;i_s;i_t$' (see table I), are plotted in fig.6. The mapping of the active space vectors to the status of the switches 'R^+,R^-,S^+,S^-,T^+,T^-' (fig.1) is straightforward. The two possible null vectors can be accomplished by freewheeling the phase R (R^+,R^- on), phase S (S^+,S^- on) or the phase T (T^+,T^- on).

TABLE I
MAPPING OF '$i_r;i_s;i_t$' TO THE SWITCHES'ST ATE.S (ACTIVE VECTORS) x= number of the corresponding space vector V_x^*

x	i_{rs}	i_{st}	i_{tr}	i_r	i_s	i_t	R^+	R^-	S^+	S^-	T^+	T^-
0	-1	-1	-1	0	0	0	?	?	?	?	?	?
0	+1	+1	+1	0	0	0	?	?	?	?	?	?
1	+1	+1	-1	+1	0	-1	1	0	0	0	0	1
2	-1	+1	-1	0	+1	-1	0	0	1	0	0	1
3	-1	+1	+1	-1	+1	0	0	1	1	0	0	0
4	-1	-1	+1	-1	0	+1	0	1	0	0	1	0
5	+1	-1	+1	0	-1	+1	0	0	0	1	1	0
6	+1	-1	-1	+1	-1	0	1	0	0	1	0	0

[1] and [12] present some solutions for mapping the null vectors in the case of fixed frequency PWM, which show regular patterns for the sequence of space vectors. This does not occur with the hysteresis controlled converters, because their switches operate asynchronously. The analysis of typical waveforms shows that the majority of the transitions occur between neighbor space vectors, resulting in only two switch transitions per space vector transition. Fig.7 shows all the six active switches status, related to their space vector V_x^*. The converter is represented by a two pole three positions switch as shown in fig.8. Fig.7 also shows the best free wheeling option is a function of the last two active vectors. If, for example, the two last vectors were V_1 and V_2 (or V_2 and V_1), freewheeling the phase T (T^+,T^- on), provides the lowest number of switchings. At this condition, phase T is connected to the negative pole of the DC source, while the positive pole is connected sequentially to the phases R, S and T.

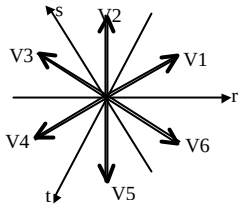

Fig. 6. Space vectors corresponding to the line currents '$i_r;i_s;i_t$'

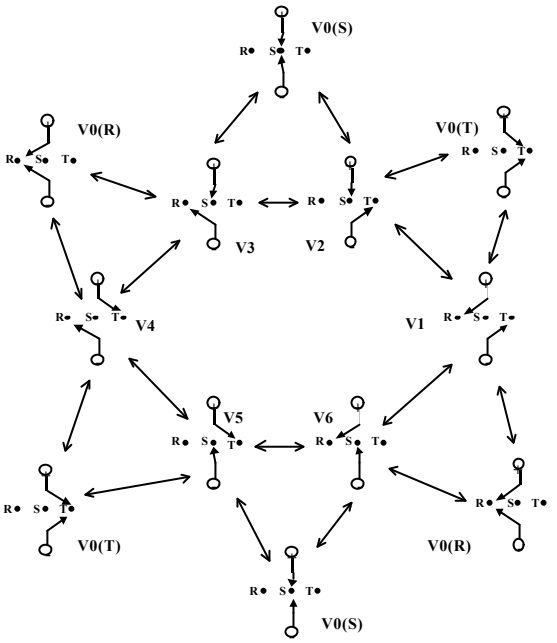

Fig. 7. Choice of the null space vectors

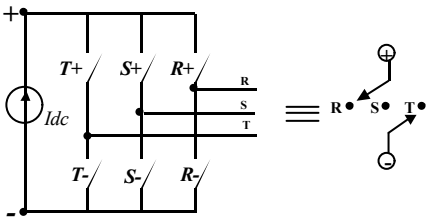

Fig. 8. Simplified converter representation

The freewheeling phase is chosen from a look-up table (table II), using the values of the last the last two active vectors. Neighbor transitions are shown in gray cells. Transitions between non-neighbor vectors occur less frequently, and provide two possible null vectors, which

can be arbitrarily chosen. Table II shows one viable look up table.

TABLE II
FREEWHEELING PHASE AS A FUNCTION OF THE LAST TWO ACTIVE VECTORS *V(K-1)* AND *V(K-2*)

		V(k-2)					
		V1	***V2***	***V3***	***V4***	***V5***	***V6***
V*(k-1)	***V1***	**X**	**T**	R	T	T	**R**
	V2	**T**	**X**	**S**	T	S	S
	V3	R	**S**	**X**	**R**	S	R
	V4	T	T	**R**	**X**	**T**	R
	V5	T	S	S	**T**	**X**	**S**
	V6	**R**	S	R	R	**S**	**X**

VIII. SIMULATION RESULTS AND COMMENTS

Three cases are compared by numerical simulation:

.case a six wire system, independent hysteresis controllers

.case b three-wire system, three independent controllers

.case c three-wire system, decoupled hysteresis controller

A discussion about the choice of the system parameters is presented in Appendix B.

A. Waveforms and Spectra comparisons

This section shows the waveforms of the line voltages '$V_{rs};V_{st};V_{tr}$', the current at the 'equivalent converter' 'i_{rs},i_{st},i_{tr}', the line currents '$i_r;i_s;i_t$' and the spectra of the line voltages for cases a,b and c.

The three cases present a good tracking ability according to figs.9,10,11 and the value of the fundamental of the capacitor voltage V_{frs} in table III.

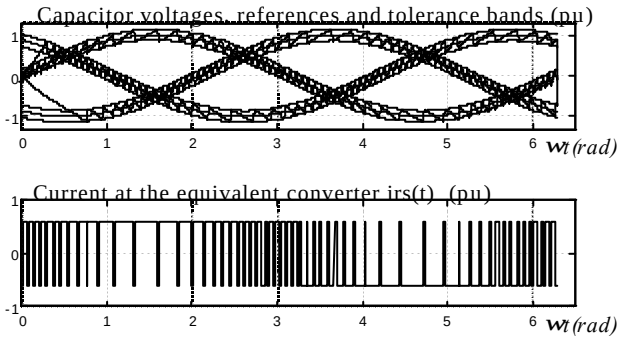

Fig. 9. Case A- Six wire system, independent hysteresis controllers.

The transient response was verified by starting the converters with null initial voltages at the capacitors (fig.9,10,11). Eq.(3) shows that higher load currents cause lower capacitor currents and slower speed for the capacitor voltages. Fig. 9,10,11 present fast response even for full load conditions.

The currents at the equivalent converter '$i_{rs};i_{st};i_{tr}$' are equal for cases a and c. This happens because the signals at the input of the hysteresis comparator, '$V_{rs}+v_0;V_{st}+v_0;V_{tr}+v_0$', are identical, producing the same switching functions.

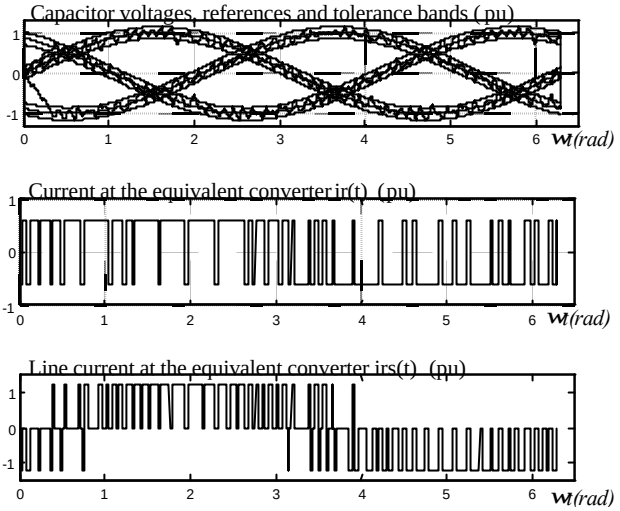

Fig. 10. Case B- Three-wire system, three independent controllers.

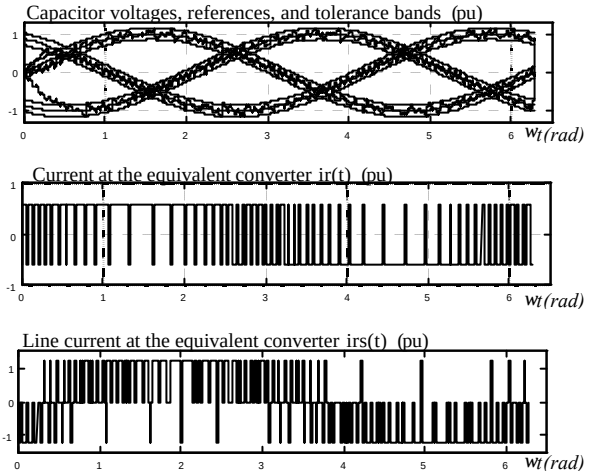

Fig. 11. Case C- Three-wire system, decoupled hysteresis controller

The three cases present a good tracking ability according to figs.9,10,11 and the value of the fundamental of the capacitor voltage V_{frs} in table III.

TABLE III.
NUMERICAL VALUES OBTAINED FROM SIMULATION
p= pulses/cycle/phase for the equivalent converter
pp= pulses/cycle/phase for the switches
V_{frs} = fundamental of the capacitor voltage (peak value)
$\Delta vrms$ = rms of the ripple at the capacitor voltages
Δv_{peak} = peak of the ripple at the capacitor voltages

case	pp	p	V_{frs}	$\Delta vrms$	Δv_{peak}	
A	62.8	---	0.999	0.0882	0.15	RS
				0.0884	0.15	ST
				0.0882	0.15	TR
B	33.6	31	0.991	0.0866	0.23	RS
				0.0894	0.25	ST
				0.0852	0.25	TR
C	62.8	57	0.997	0.0716	0.19	RS
				0.0725	0.19	ST
				0.0693	0.18	TR

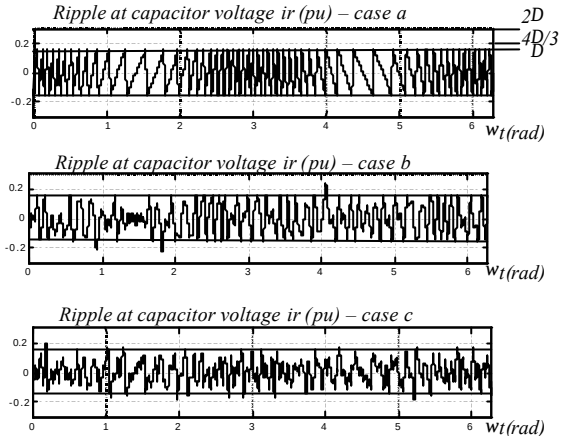

Fig. 12. ripple at the capacitor voltage $i_r\,(pu)$, with band $\Delta = 0.15$ for cases a, b and c.

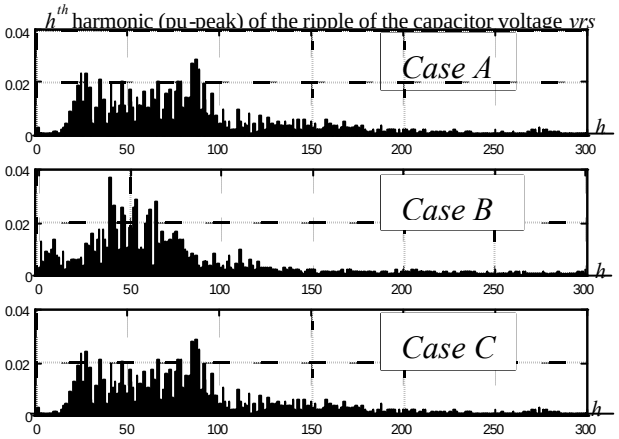

Fig. 13. Spectra of the capacitor voltage v_{rs} .

Fig.12 presents only the voltage ripple at the capacitors. The ripple in 'case a' is strictly bounded by the band $\Delta = \pm 0.15 pu$. In the decoupled controller (case c), the ripple of the controlled signal, $V_{rs} + v_0; V_{st} + v_0; V_{tr} + v_0$ is equal to the one in 'case a'. The instantaneous zero sequence current $i_0 = i_{rs} + i_{st} + i_{tr}$ cannot flow through the capacitors. The capacitor voltage ripple waveform (see fig.12c) corresponds to the one of 'case a' (see fig.12a) subtracted by v_0 given by (5). The resulting ripple cannot respect the original tolerance band Δ, however it is bounded to '$\pm 4\Delta / 3$' [7] as confirmed by fig.12c.

The ripple waveform at the coupled 'case b' is similar to the VSC case, and exceeds the original tolerance band. However it is bounded to $\pm 2\Delta$ [11] as confirmed by fig.12b.

B. Behavior of the switching frequency and 'Mapping Strategy'

Fig. 14, 15 shows the influence of the amplitude and phase of the load currents '$I_r; I_s; I_t$' on the average switching frequency of the equivalent converter, for sinusoidal load. Cases a and c have the same behavior, and can be adequately described by the approximate formula given by [10] for a one-phase VSC.

Table III shows the number of pulses per cycle per phase for the equivalent converter 'p' and for the real switches of the three-phase converter 'pp'. The value of 'p' is higher for the decoupled case. The value of 'pp' depends on the mapping strategy. The proposed one presents values of 'pp' slightly higher than 'p'. The use of synchronous and centered pulses for the three phases, like in [7], would provide an adequate ordering of the sequence of space vector, resulting in p=pp.

The coupled 'case b', which has a lower average switching frequency than 'case c', exhibits a chaotic behavior, especially in the lower and medium range of load currents. The evaluation of the number of transitions in Fig.14,15 was obtained considering only one cycle of the reference voltages. Coupling in 'case b' may cause: **a.)** large variation in the average switching frequency for different reference voltage cycles, (as shown in fig.16), which explains the shape of the surfaces in fig.14,15; and **b.)** the occurrence of small bursts of high frequency, known as 'limit cycles' for low load currents [11].

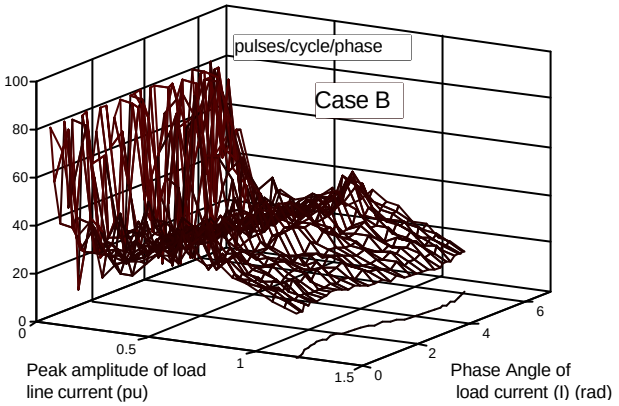

Fig. 14. Number of pulses per cycle per phase as a function of the peak amplitude and phase of the load current I - Case B.

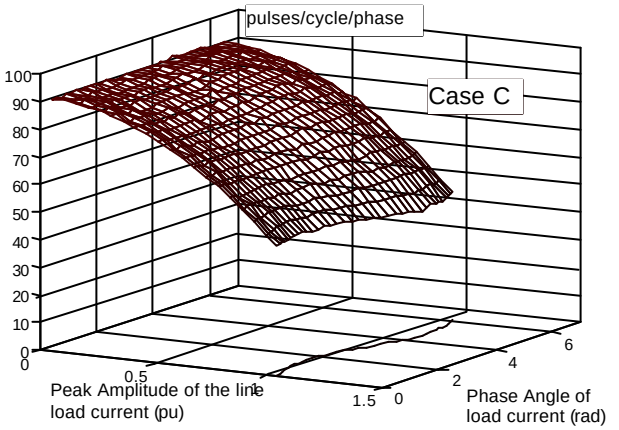

Fig. 15. Number of pulses per cycle per phase as a function of the peak amplitude and phase of the load current I - Case C.

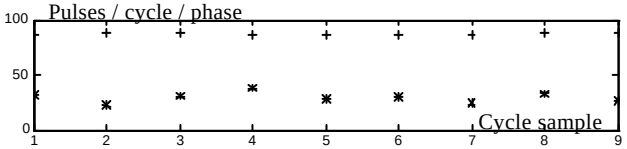

Fig. 16. Pulses/cycle/phase for ten consecutive samples of the reference voltages (+ case c; * case b).

C. Maximum amplitude of the load current

The locus of the load current ($I_r; I_s; I_t$) maximum amplitude (peak values) is represented by the curve plotted in the base of the tri-dimentional graphics of fig.14, 15. The decoupled case imposes a set of reference voltages '$V_{rs\,ref}; V_{st\,ref}; V_{tr\,ref}$' with null zero sequence, which forces the 'locally averaged instantaneous zero sequence components' of the capacitor voltages and the equivalent converter currents 'i_{rs}, i_{st}, i_{tr}', to be null. Therefore, sinusoidal phase currents with a peak amplitude of $I_{dc}/2$, and line currents with a peak amplitude $abs(\vec{i}_x) = \sqrt{3} I_{dc}/2$, can be obtained from the two level ($\pm I_{dc}/2$) currents 'i_{rs}, i_{st}, i_{tr}'. The capacitance value must be evaluated in order to drain a line current with amplitude '$abs(\vec{I}_c)$' (peak value), at 1pu peak amplitude 'line to line' voltage. The maximum current load amplitude (peak value), for a given phase angle is obtained by (6):

$$abs(\vec{I}_x) e^{j\,angle(\vec{I}_x)} = \frac{\sqrt{3}}{2} I_{dc} e^{j\,angle(\vec{i})} - abs(\vec{I}_c) e^{j\,p/2} \qquad (6)$$

Converter line currents up to $abs(\vec{i}_x) = I_{dc}$ (peak value) can be obtained with zero sequence injection PWM strategies, and the new limits for the load current can be obtained from (6), substituting the new value of $abs(\vec{i}_x)$.

The coupled 'case b' has an extended operation range and periods of low switching frequency (see fig.13), which suggest that this control strategy accomplishes zero sequence injection technique.

IX. CONCLUSION

Based on the duality of the equivalent models of the three-phase, three-wire VSC and CSC circuits, this paper analyses the operation of the CSC converter with an hysteresis based, decoupled, voltage controller (case c). With this strategy the converter operates like three independent one-phase converters, providing excellent tracking and transient response. The switching frequency has a deterministic behavior and the capacitor voltage ripple is bounded to $\pm 4\Delta/3$.

The coupled 'case b' (three independent comparators) has an extended admissible load current range and lower average values for the switching frequency than the decoupled 'case c'. However, the switching frequency shows a chaotic behavior.

It is expected that the duality properties and these results can lead to an improved controller, with the merits of both above analyzed cases.

X. REFERENCES

[1] X. Wang; B. Ooi. "Unity PF Current Source Rectifier Based on Dynamic Trilogic PWM"; IEEE-T-PE July, 1993, pp268;

[2] L. Malesani ; P. Tenti "Three Phase AC/DC Converter with Sinusoidal AC Currents and Minimum Filter Requirements" IEEE-T-IA, Jan/Feb 1987;

[3] T. Ohnishi, H. Okitsu "A Novel PWM Technique for Three Phase Inverter/Converter" IPEC Tokyo 1983, pp384;

[4] P. Korondi; L. Nagy; G. Nemeth. "Control of a Three Phase UPS Inverter with Unbalanced and Non Linear Load", EPE 1991 pp 3-180;

[5] Y. Sato; T. Kataoka; "An Investigation of PWM Pattern Generation Methods for High Power Current Type PWM Rectifiers"; IPEC Yokohama-95; pp 748;

[6] Matakas Jr., L.; Kaiser, W. "Low harmonics, decoupled hysteresis type current control of a multiconverter consisting of a parallel transformerless of VSC converters." In: IEEE IAS ANNUAL MEETING IAS'97, USA, 1997. IEEE. V.2 pp 1633-40;

[7] L. Malesani; P. Tenti ; "A Novel hysteresis control method for current controlled voltage source PWM inverters with constant modulation frequency"; IEEE T-IA Jan-Feb/1990, pp 88;

[8] M. Hombu; S. Ueda; A. Ueda. "A Current Source GTO Inverter with Sinusoidal Inputs and Outputs" IAS-85 pp 1033;

[9] J. Holtz "Pulsewidth Modulation for Electronic Power Conversion, "Proceedings of the IEEE, Aug. 1994;

[10] P. A Dahono; Y. Sato; T. Kataoka; "Loss evaluation method for hysteresis current controlled inverters"; Annual Conf. Of IEE Japan, 1992, Int. session, ppE.168;

[11] S. Salama; S. Lennon; "Overshoot and limit cycle free current control method for PWM inverters"; EPE 91, pp 3-247;

[12] J.R. Espinoza, G. Joos; "Current Source Converter on-line pattern generator switching frequency minimization"; IEEE, T-IE; April-1997; pp 198;

[13] Matakas Jr., Lourenço. "A decoupled, hysteresis based, voltage controller for a CSC Converter". In: IPEC 2000, 2000, IPEC 2000. 2000.

APPENDIX A: VSC converter model

Fig.A1 presents the VSC converter connected to a voltage source load through an inductance. Fig. A2 shows its equivalent circuit and (A1) its state space equations.

$$\frac{d}{dt}\begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} = \frac{1}{L}\left(\mathbf{BA}\left(\begin{bmatrix} v_r \\ v_s \\ v_t \end{bmatrix} - \begin{bmatrix} V_r \\ V_s \\ V_t \end{bmatrix}\right)\right) \qquad \text{A.1}$$

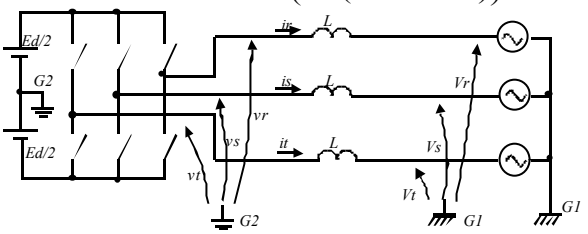

Fig. A1. VSC converter +filter + load

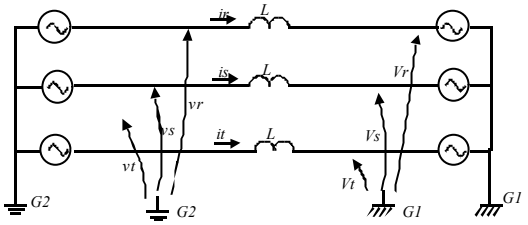

Fig. A2. VSC converter +filter + load

APPENDIX B: Simulation Parameters

$I_{dc} = 1.2\,pu$; $\Delta = \pm 0.15\,pu$ tolerance band;

$w = 1\,pu$

$V_{rs\,ref} = 1 sin(wt); V_{st\,ref} = 1 sin(wt - 2*p/3);$

$V_{tr\,ref} = 1 sin(wt + 2p/3)$ (pu)

$I_r = 0.9 sin(wt + a);\ I_s = 0.9 sin(wt - 2p/3 + a);$

$I_t = 0.9 sin(wt + 2p/3 + a)(pu);$

The capacitor is chosen to drain a line current with peak amplitude '$abs(\vec{I}_c) = 0.2\,pu$', at a line to line voltage peak amplitude of 1pu. Its reactance is $0.2/3\ pu$.