Computer Evaluation of ASD Behavior under Short Interruption and Voltage Sag 6th Brazilian Power Electronics Conference – COBEP'2001

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***Abstract* – One of the most serious problems faced by the industry is the production halt caused by voltage disturbance of power supply. When electrical and electronic equipment are subjected to voltage sag or voltage short interruption it may cause spurious tripping of the equipment. The adjustable speed drives - ASD are notorious for their sensitivity to such disturbances. It is possible to determine how long the equipment will continue to operate after the supply becomes interrupted. This paper evaluates the behavior of single-phase ac ASD when subjected to voltage interruption and voltage sag according to the IEC 61000-4-11 testing and measurement techniques. Simulation test results are presented for different conditions of the voltage disturbances, load and the ASD parameters.**

I. INTRODUCTION

Voltage sag is a sudden reduction of the voltage magnitude followed by voltage recovery after short period of time, mainly caused by a heavy flow of current. Short interruptions represent the most severe condition of voltage sags. Voltage sags are inevitable on the power system, even in the most advanced utility networks.

As industrial plants experiment a globally competitive environment, achieving and sustaining high levels of productivity becomes a critical factor. As the industrial sector increases its dependence on sensitive power electronic based load, the susceptibility to ever-present volatge sag is heightened.

Voltage sags have attracted considerable attention as they cause spurious tripping of electrical and electronic equipment. The mal function and the trip command that takes the equipment off-line have caused economic impacts and annoyance to all class of consumers. The equipment tolerance to voltage sag is primarily dictated by the sag severity and sag duration.

Adjustable speed motor drives – ASD is the most common power electronic-based industrial equipment, which can bring about a more efficient motor control. The ASD are susceptible to volatge sags.

The primary focus of this paper is to examine through computer simulation the response of a single-phase adjustable speed drive - ASD electronic circuit under voltage sags to 0%, 40% and 70% for 5 cycles duration. The behavior of the equipment is tested for different switching frequencies, power loads, capacitances of the dc bus, and phase angles on the mains voltage. The influence of these parameters on the ASD tolerance is evaluated.

The tests have been performed according to IEC 61000-4-11 international standard Edition 1.1 on 'Testing and measurement techniques – voltage dips, short interruptions and voltage variations immunity tests' [1].

The application software PSPICE V6.0 is used for the computer simulation of a generic ASD electronic circuit. The paper is divided into six sections. The first section is an introduction to short duration voltage disturbance and the susceptibility of ASD. It is also presented the purpose of the assessment of the ASD equipment and the guidelines for the evaluation carried out. The second section presents the sensitivity of adjustable speed drives and the common problems faced by them. The third section deals with the fundamentals of the IEC 61000-4-11 standard and the fourth one sets up the simulated ASD circuit configuration. The equipment simulation response to voltage sags is presented in the fifth section, and finally the conclusion in the sixth section.

II. THE SENSITIVITY OF ADJUSTABLE SPEED AC DRIVES

The sensitivity of an ASD to short interruption and voltage sag depends ultimately on its design. Electrical and electronic equipment cannot operate long without electricity. For each piece of equipment it is possible to determine how long it will continue to operate after supply becomes interrupted. The voltage tolerance requirement, obtained by test on the equipment, provides the equipment performance to sudden change on voltage magnitude.

Adjustable speed drives are often extremely sensitive to voltage sags. Tripping of ASD can occur due to [2,3]: the sudden change in operating conditions detected by the drive controller or protection; the reduced dc bus voltage and the consequence lack of energy to carry on the load operation; an ac over-current during the sag or a dc post-sag over-current charging the dc capacitor; and the drop in speed or torque variations by the motor as a result of the sag.

Most often the equipment tolerance is given by the magnitude and duration of the voltage sag it can abide. This study presents the effects of voltage sags on ASD showing up the voltage and current variation at the various stages of the ASD. By means of the ASD behavior it is possible to modify and improve the equipment ride-through.

III. IEC STANDARD TEST DEFINITIONS

The IEC 61000-4-11 is a basic EMC (Electro-Magnetic Compatibility) standard [1] that defines the immunity test methods and range of preferred test levels for electrical

and electronic equipment connected to low-voltage ac power supply networks for voltage sags, and short interruptions. The standard applies to electrical and electronic equipment having a rated input current not exceeding 16A per phase.

Although the standard is limited to 16A it establishes a reference for evaluating the immunity of sensitive equipment when subjected to short duration supply voltage variation. The standard does not set acceptable levels of voltage disturbances to certify the device, equipment or system immunity. It does not establish a pass or fail criteria. It does not assign any voltage tolerance requirements for sensitive equipment. On the contrary, it gives general and fundamental rules for the achievement of electromagnetic compatibility. Performance criteria is used and defined in the equipment technical specifications.

Different types of tests are specified in this standard to simulate the effects of abrupt change voltage. The voltage sag severity suggested for test are to 70%, 40% and 0% of the equipment rated voltage U_T and duration of 0.5, 1, 5, 10, 25, 50 cycles, or any other chosen duration time given in the product specification. One or more of the mentioned test levels and durations may be chosen. Any duration may apply to any test level. If the equipment is tested for voltage sag to 0% it is unnecessary to test for other levels for the same duration [1].

As suggested by the IEC standard, abrupt changes in supply voltage shall occur at zero crossings of the voltage, and at additional angles considered critical preferably selected from 45º, 90º, 135º, 180º, 225º, 270º and 315º on each phase.

IV. ASD Circuit

Figure 1 gives the equivalent circuit of the ASD. The ASD is made up of a single-phase bridge rectifier, a dc link bus, a MOSFET based inverter with a controlled ac output voltage modulated by PWM technique with a switching frequency of 10kHz, and a filter followed by a resistive load. The network power supply is represented by a 60Hz sinusoidal voltage source of rated voltage U_T of 100V in parallel with another voltage source of a% of U_T. With ideal switches, *tclose* (normally open) and *topen* (normally closed), an abrupt commutation between the two voltage sources simulates a voltage sag condition to a% severity. The voltage sag duration considered to evaluate the ASD behavior is 5 cycles. Table I gives the ASD parameters.

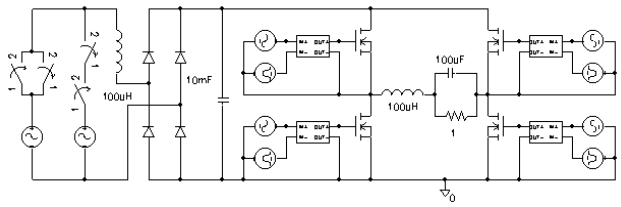

Fig. 1. The equivalent circuit of a single-phase ASD.

TABLE I
PARAMETERS OF A SINGLE-PHASE ASD

Source	Link dc	Filter	Load
V=100V L=100mH	C=10mF	L=100mH C=100mF	R=1Ω

Voltage sag to 0% has been applied at various input voltage phase angles as suggested by the IEC standard. The worst condition as far as the voltage level is concerned was found to a phase angle of 45º corresponding to a dc bus voltage V_0 roughly equal to 50.678V. The voltage V_0 is defined as the dc bus voltage at sag initiation.

These are the basic parameter specifications and simulation condition of the ASD considered in this paper as a basis for comparison.

V. Simulation Results

When the supply voltage of an ASD drops during voltage sag the diodes no longer conduct and the capacitor discharges until the ac supply voltage exceeds the dc bus capacitor. As long as the absolute value of the ac voltage is less than the dc bus voltage, all electrical energy for the load comes from the energy stored in the capacitor. This energy is given by the difference between the energy at sag initiation and the energy consumed by the load [2,3]:

$$\tfrac{1}{2} CV^2(t) = \tfrac{1}{2} CV_0^2 - Pt \qquad (1)$$

Figure 2 shows the voltage response at the dc bus and at the load bus for voltage sag to 0% on the basic circuit referred in section IV. The voltage sag has been applied after the circuit has reached the steady state. Considering a time span until the dc voltage reaches 50% V_0 of 19.232ms, the power supplied by the capacitor to the load as calculated by (1) is equal to 500W.

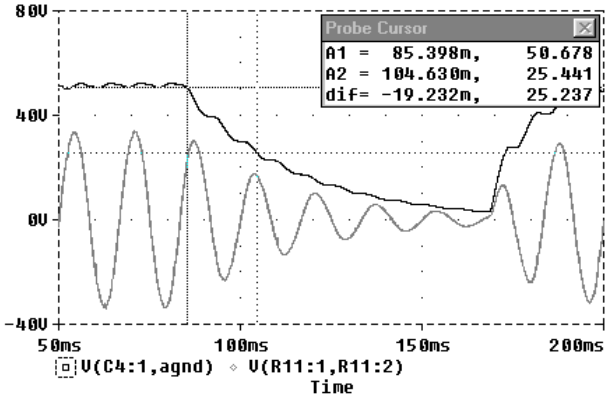

Fig. 2. DC Voltage decay and AC voltage on the load for an interruption of 5 cycles in the reference circuit

Figure 3 gives the power supply current and the dc bus voltage. The current overshoots to 182% above the nominal current after the sag and the over-current may lead to the tripping of the ASD. This high current is required for charging the capacitor and supplying the load. The post sag over-current depends on the source impedance, the dc capacitance, the amount of capacitor energy stored at the switching moment, and the load power.

It can also been noted in Fig. 3 the current waveform distortion.

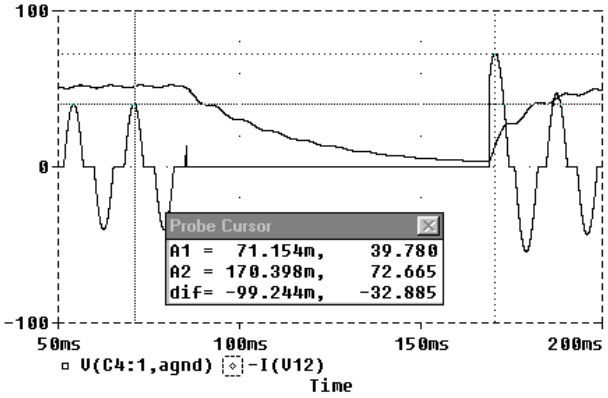

Fig. 3. DC bus voltage and AC input current for voltage sag to 0% at the reference circuit

The voltage ripple is defined as the difference between the maximum and the minimum value of the dc bus voltage. For a supply voltage of 60Hz, Fig. 4 presents the dc bus voltage before the sag with a voltage ripple equal to 1,88V and frequency of 120Hz.

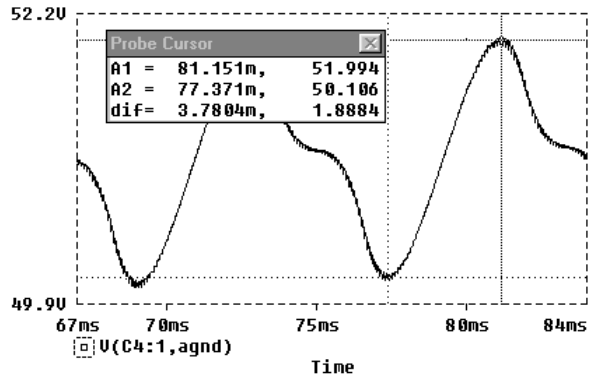

Fig. 4. Voltage ripple of 1,88V and 120Hz at the DC bus on the reference circuit

Figure 5 shows the dc voltage decay when sag to 0%, 5 cycles, occurs at 135º phase angle of the supply voltage. The V_0 for this condition is equal to 52.469V and it is the highest dc bus level found for the phase angles suggested by IEC 61000-4-11. Comparing the two dc voltage plots as shown in Fig. 2 and 5 it can be noted that the time span to reach 50% V_0 is longer in Fig. 5, i.e., 19.232ms for 45º and 22.816ms for 135º. Then, it can be observed that the higher V_0 the longer the decay time. If the dc bus voltage powers the drive control and their electronic, (the dc bus capacitance provides energy storage to maintain the control, and there is a critical dc voltage level and an associated time span to reach it that is of great importance to the equipment tolerance.

If the capacitance size is increased, or the power load is reduced the ripple is smoothed and the angle phase effect on V_0 is lessened. Also if it is considered that the equipment protection is set to trip for a dc bus voltage level given by the worst phase angle condition met, when a sag occurs at other phase angle that means the equipment supportability is higher.

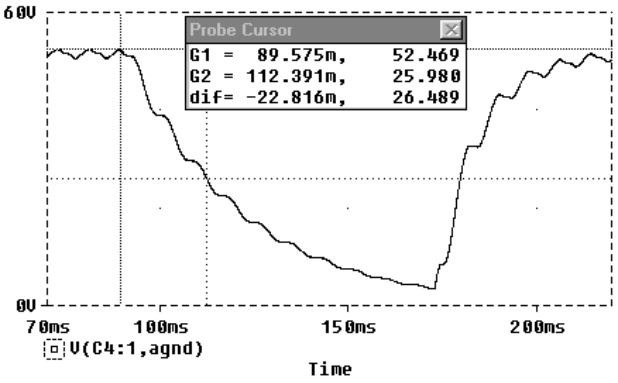

Fig. 5. The decay time of the DC bus voltage for a voltage sag at 135º crossing

When a sag to 40%, phase angle 45º, is tested, the initiating dc bus voltage V_0 is 50.071V and after 5 cycles the dc bus voltage is 38%V_0 (19.165V) as shown in Fig. 6. Two considerations can be drawn from this situation. The first one is that if the sag would last longer, the dc bus voltage would keep at the value of the ac voltage. The second consideration is that for a sag less severe than that represented in Fig. 2 (to 0%), the time need to reach 50%V_0 is longer, i.e., 21.384ms as opposed to 19.232ms to 0% voltage sag.

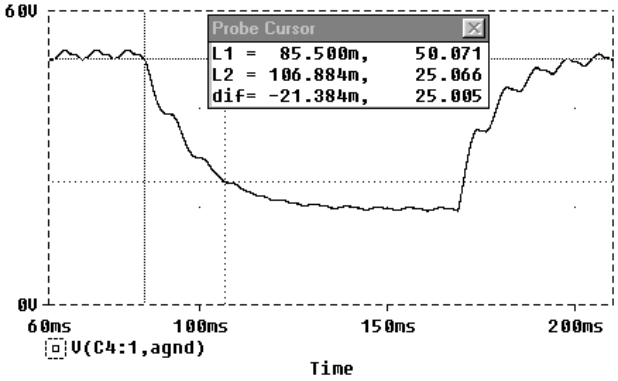

Fig. 6. Effect of voltage sag to 40%, 5 cycles on the DC bus

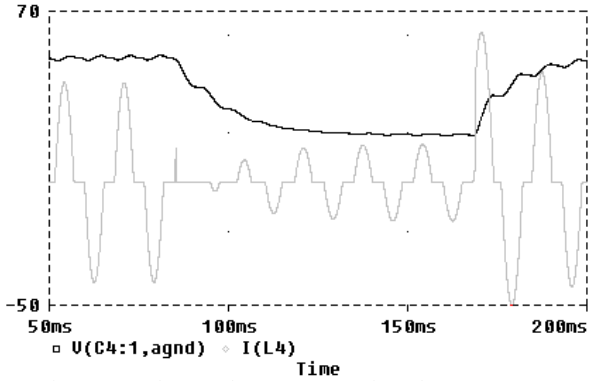

Fig. 7. DC voltage and source current for voltage sag to 40%

Figure 7 depicts the input current waveform. During the dc voltage decay the load is supplied by the energy stored at the dc capacitor and the input current is nil. As the supply voltage exceeds the dc bus capacitor voltage and the diodes are forward biased the ac source once again feeds the load.

On the other hand, when a sag to 70%, 5 cycles, is applied the dc bus voltage reaches the equilibrium in 68.5% V_0 (35.216V) and 42.483ms (2.5 cycles) as shown in Fig.8.

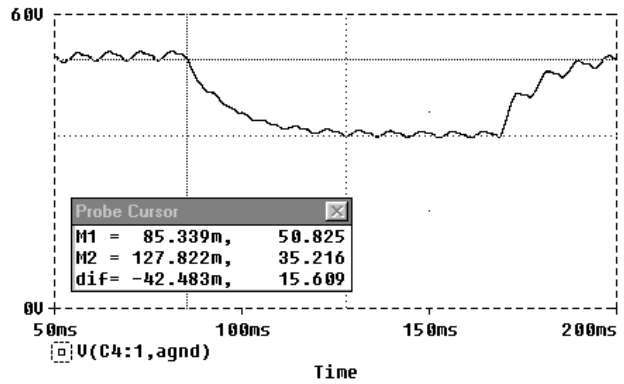

Fig. 8. Effect of voltage sag to 70%, 5 cycles, on the DC bus voltage

Table II presents the dc bus voltage for the basic circuit at the sag initiation (V_0) and after 5 cycles (Vdc) for different voltage sag magnitudes.

TABLE I
DC BUS VOLTAGE

Voltage sag	V_0	Vdc after 5 cycles
0%	50.678V	3.270V
40%	50.071V	19.22V
70%	50.825V	34.70V

Under a supposed 20V and 5 cycles dc bus voltage tolerance the trip command would take the equipment off-line for sag severities to 0% and 40%.

At follows the ASD behavior is evaluated for 0% voltage sag varying the equipment basic circuit parameters one at once.

When the dc bus capacitor is half-sized to 5mF the dc bus voltage, as shown in Fig. 9, decays faster as compared to the ASD behavior of the base case presented in Fig. 2. The time span to reach 50%V_0 is 9.770ms for C=5mF and 19.232ms for C=10mF. In addition to the capacitance the time to reach 50% V_0 is half-sized as well.

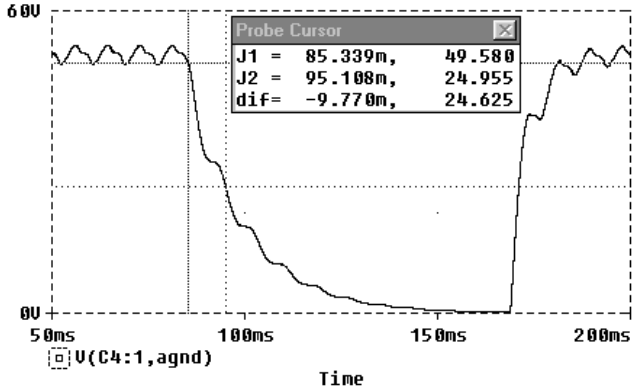

Fig. 9. DC bus voltage for sag to 0%, 5 cycles, and capacitance of 5mF

For a 5mF capacitor at the dc bus, the voltage ripple is twice (3.63V) as that for a 10mF capacitor (1,88V) as it can be seen in Fig. 4 and 10.

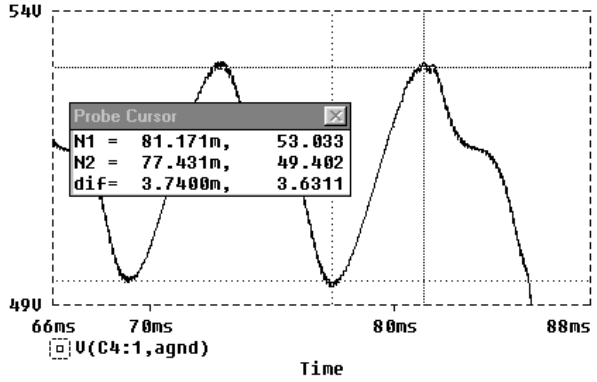

Fig. 10. DC voltage ripple for C=5mF

When the load resistance in the basic circuit changes to 5Ω, the power supplied by the capacitor also changes to 260W, this is about half as that for a load resistance of 1Ω, and the dc bus voltage increases noticeably.

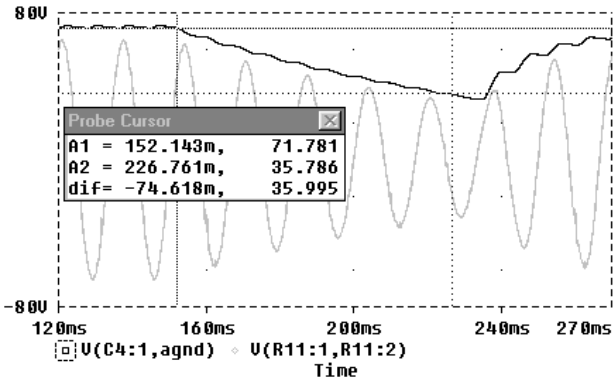

Fig. 11. 5 cycles short interruption with load resistance of 5Ω

Under this consideration the time span to reach 50% V_0 is 74.618ms, as shown in Fig.11, as opposed to 19.232ms for R=1Ω. The ripple at the dc bus is equal to 1.66V, lower than that in Fig. 4. This is reasonable since the power consumed by the load has decreased. It can be concluded that the lighter the load the longer the time to reach 50% V_0 and as a consequence the ASD performance is improved.

In this final evaluation the PWM switching frequency is modified in order to find out the influence on the ASD behavior. Figure 12 gives the ASD response.

The load voltage shows the presence of harmonic voltages of lower order. An adequate filter at the inverter output should be specified in order to filter out the harmonic voltages at the load bus. The presence of harmonics increases the load power losses.

When the PWM switching frequency is lower, the time decay to 50%V_0 is faster than otherwise. As the switching frequency diminishes the capacitor charging frequency by the supply source diminishes as well. Yet, the power drawn by the load is higher due to the presence of harmonic voltages. The ripple voltage at the dc bus is also higher as shown in Fig. 13.

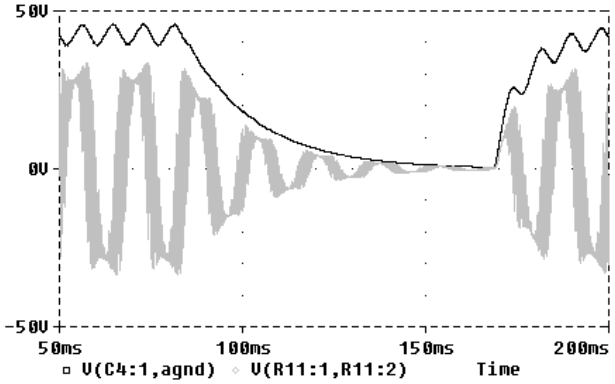

Fig. 12. DC bus and load voltages for a 5 cycles short interruption and 2kHz PWM switching frequency

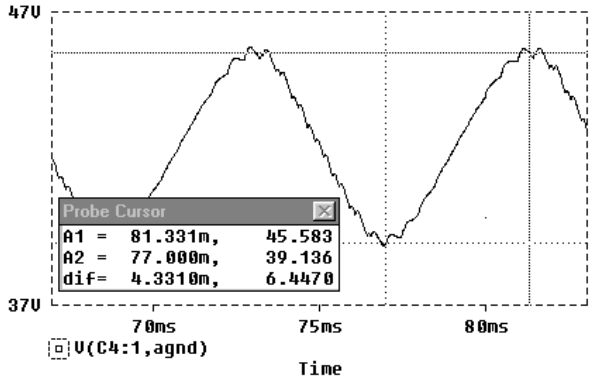

Fig. 13. Ripple voltage of 120Hz for a switching frequency of f=2kHz.

When the filter parameters are modified the load voltage waveform is improved as shows Fig. 14. It is noteworthy that the dc voltage time decay increases and the dc voltage level at the end of the voltage sag is not nil when compared to Fig.12.

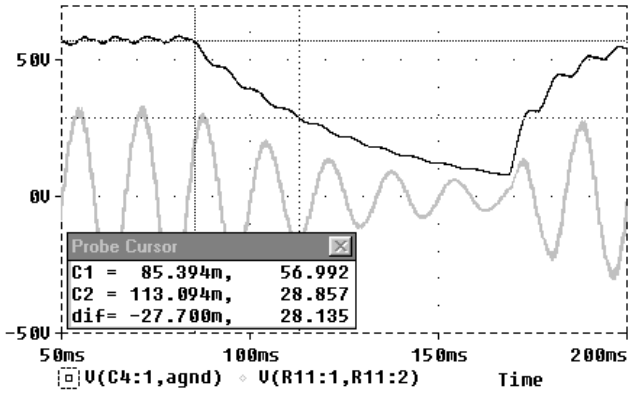

Fig. 14. DC Bus for PWM switching frequency of 2kHz

VI. Conclusion

This paper has presented an evaluation on the influence of an ASD design on its immunity to voltage sag and short interruption. A generic ASD has been tested for different voltage sag characteristics. Factors such as magnitude variation, duration, phase angle, switching frequency, capacitance size and load size are important in determining the behavior of drives during sags.

Lack of stored energy, excessive voltage ripple, over-current, and under-voltage are usually the culprits for the equipment misbehavior.

The typical end-use customer does not consider voltage sag sensitivity in his/her equipment buying decision. However, when the equipment is part of and essential to the process operation it is required to operate properly. To know the equipment sensitivity and the issues that contribute for such is a great deal important.

VII. Acknowledgment

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VIII. References

Standard:

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[2] Bollen, M.H.J., Understanding Power Quality Problems – Voltage Sags and Interruptions, IEEE Press Series on Power Engineering, 2000, ISBN 0-7803-4713-7. IEEE Order Number PC5764. pp.543.

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[3] Bollen, M.H.J., IEEE Tutorial on Voltage Sag Analysis, 1999, ISBN 0-7803-4713-7.