A High Power Factor Single-Phase Rectifier Based on a Current Multilevel Buck Converter

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***Abstract* - This paper introduces a single-phase ac-to-dc converter, which consists of a conventional diode bridge cascaded by a current multilevel buck dc-to-dc converter. Depending upon the switching strategy, the structure input current can present multiple levels and provide a unity displacement factor, leading to a high power factor converter, and a balanced distribution of currents among two or more commutation cells. This low-frequency switching circuit is proper to high-current applications. This paper presents a brief comment about similar rectifiers introduced before and shows simulation results for the proposed arrangement applied to a two-cell, five level converter. Experimental results for a 2-kW prototype are also presented, with a discussion about the pulse generation circuit implemented.**

I. INTRODUCTION

Multilevel converters have emerged as a new breed of power converters during the past few years. Several multilevel converter topologies and modulation technologies have been developed and applied to high power systems. The main motivation for the use of multilevel structures remains on their ability to ensure, besides other features, a safe distribution of the voltage (or current) among a number of associated semiconductor switches. Moreover, there is a possibility to optimize the structure harmonic content, yielding a lower level of conducted and irradiated electromagnetic interference (EMI). These benefits have attracted a tremendous interest in industry. A review of the basic theory regarding voltage or current multilevel converters is presented in [1]. Some topologies based on the association of either converters or commutation cells are also discussed in the same reference.

Current multilevel (CML) converters consist in an alternative way to associate commutation cells in parallel, and have been described in [2]. The new technique has been applied to dc-to-dc (choppers), dc-to-ac (inverters) and ac-to-dc (rectifiers) converters.

Low frequency three-phase switch-mode rectifiers have been recently introduced as a way to improve power factor (PF) of high power ac-to-dc converters [3, 4]. They have been proposed as an alternative for the traditional thyristor bridge rectifiers, which have low PF and introduce excessive harmonic current in the ac line, causing disturbances and loss of quality in electric power systems [5, 6].

Low frequency strategies have been also proposed to improve the harmonic content of the line current in single-phase rectifiers [7, 8]. The technique consists in using a boost converter, for which the main switch is gated a small number of times (often one or two) for a short period of time, within a line voltage cycle.

Another way to increase PF of rectifiers is to employ some kind of high frequency modulation. These techniques are mainly adapted to the boost converter cascading a single-phase diode bridge rectifier [9]. The method has been proposed to provide a better harmonic compliance as compared to conventional single-phase rectifiers employing a simple capacitive filter [10]. Other dc-to-dc stages could be employed. A PF preregulator based on a buck-flyback topology is presented in [11]. Three-phase rectifiers employing high frequency modulation are discussed in [12,13]. High frequency modulation, however, is not proper for high-power applications, due to constraints in technological features of semiconductor switches. Thus, for high-power applications, the low-frequency modulation technique is more recommended.

A PF improvement technique using low-frequency switching can be implemented employing the CML concept. Fig. 1 illustrates expected input current and voltage waveforms for a five-level CML rectifier. It is possible to minimize total harmonic distortion, THD, by means of adjusting α and ϕ. A 12-pulse three-phase rectifier based on the CML technique is presented in [14].

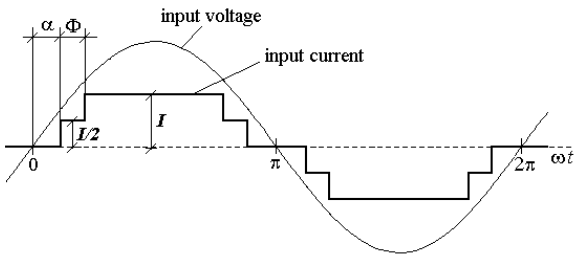


Fig. 1 – A sinusoidal input voltage and a five-level waveform of input current on a CML rectifier

This work proposes a single-phase rectifier that employs low-frequency switching, with unity displacement factor, based on the buck dc-to-dc current multilevel converter. The composite converter provides a balanced distribution of total output current among two or more semiconductor switches, and can be driven to present multiple levels in the rectifier input current. Therefore, the proposed rectifier has a high PF at the rated output voltage, and is proper to high current applications. It may be called a *step down* (or buck) *rectifier*, due to either the presence of a buck converter, which is part of the whole structure, or due to

the average output voltage, which is always lower than the rms input voltage, as shown later in this text.

II. The Single-Phase Current Multilevel Rectifier

Fig. 2 shows the generic CML cell, which is based on the parallel connection of commutation cells (or PWM switches) by means of balance inductors [15]. The PWM switch concept is well described in [16]. It is assumed that upper and lower switches have a complementary operation. Employing suitable displacements among gate pulses, the structure, originally proposed as a safe alternative for parallel association of devices, can have its input current (through T_1 terminal) made of multiple current levels between 0 and I_o. Fig. 3 shows the use of the CML cell in a five-level buck rectifier, as presented in [2]. This rectifier structure is derived from a five-level current source inverter (CSI) [17,18].

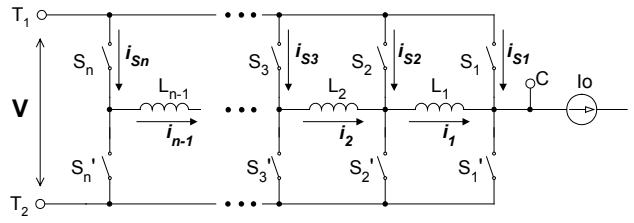


Fig. 2 – The generic CML cell

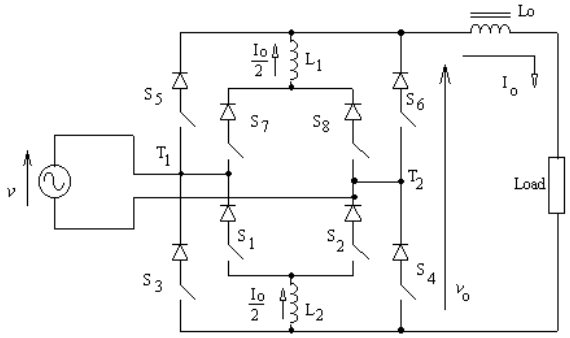


Fig. 3 – A five-level buck rectifier derived from a CSI configuration

The input current of the generic cell (Fig. 2) can be a dc or ac one, depending upon the nature of the converter. For dc-to-dc converters, however, the input current is a dc current and the lower switches are replaced by passive switches (diodes). The structure can be adapted to all non-isolated converters (buck, boost, buck-boost, Ćuk, SEPIC and zeta) [19].

The CML rectifier proposed in this work makes use of the buck dc-to-dc CML converter. A full-bridge rectifier replaces the dc voltage source. Therefore, the voltage applied to the CML dc-to-dc cell is a rectified sine wave voltage. The circuit is shown in Fig. 4.

This rectifier is appropriate for highly inductive loads. Since the circuit operates at low-frequency switching, L_i balance inductors are more properly assembled on silicon-iron cores. An advantage of this new topology is the reduced number of active switches as compared to the alternative shown in Fig. 3. The switching strategy is also simpler than that.

The total output current can be safely distributed among the switches of the converter without incurring the common problems to conventional parallel connection of switches. Depending on the output current value, it may be necessary to use diodes in parallel in the bridge rectifier. Nevertheless, simple diode paralleling can be employed without the hazards that difficult paralleling of active devices.

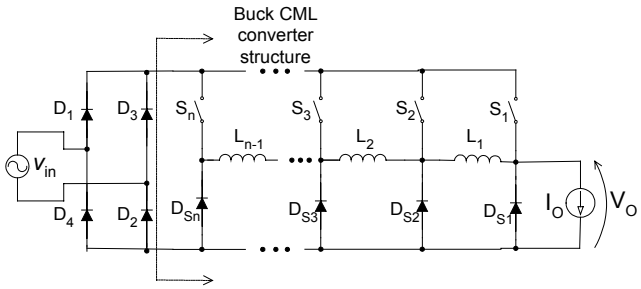


Fig. 4 – The buck rectifier based on the generic dc-to-dc CML cell.

III. Simulation Results

Consider a two-cell, five-level, buck rectifier, as shown in Fig. 5, with the following simulation parameters: $V_{in} = 127V_{rms}$, 60 Hz; R_{load} = 2 Ω; L_o = 100 mH; L_1= 40 mH; $R_{on\ (switches)} = 0.01$ Ω; $\alpha = 12.2^o$, $\phi = 25.9^o$.

Pspice® circuit simulation leads to waveforms plotted in Fig. 6. The harmonic spectrum for the input current is plotted in Fig. 7. For the input current, the obtained THD is 15.4%. The rectifier PF is equal to 0.99.

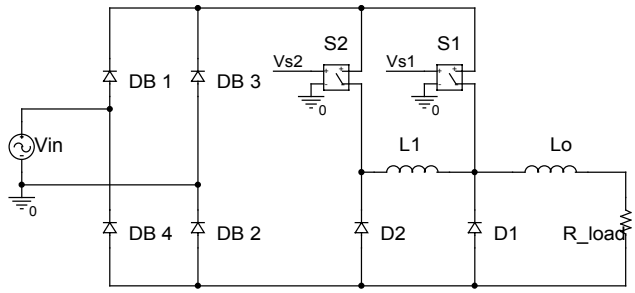


Fig. 5 – A two-cell, five-level rectifier.

The average output voltage value is given by

$$V_O = \frac{1}{\pi} \cdot \int_{\alpha}^{\pi-(\alpha+\phi)} \sqrt{2}.V_{in}.\mathrm{sen}(\theta)\,d\theta = \frac{\sqrt{2}.V_{in}}{\pi} \cdot \left[\cos(\alpha) + \cos(\alpha+\phi)\right]. \quad (1)$$

The values for α and ϕ employed in simulation yield $V_o \cong 94.8$ V, considering voltage drops on the switches. Note that for $\alpha = \phi = 0^o$, (1) provides the same expression given for the output voltage in a conventional single-phase diode bridge rectifier. Note also the step down nature of the circuit (V_o is always lower than V_{in}).

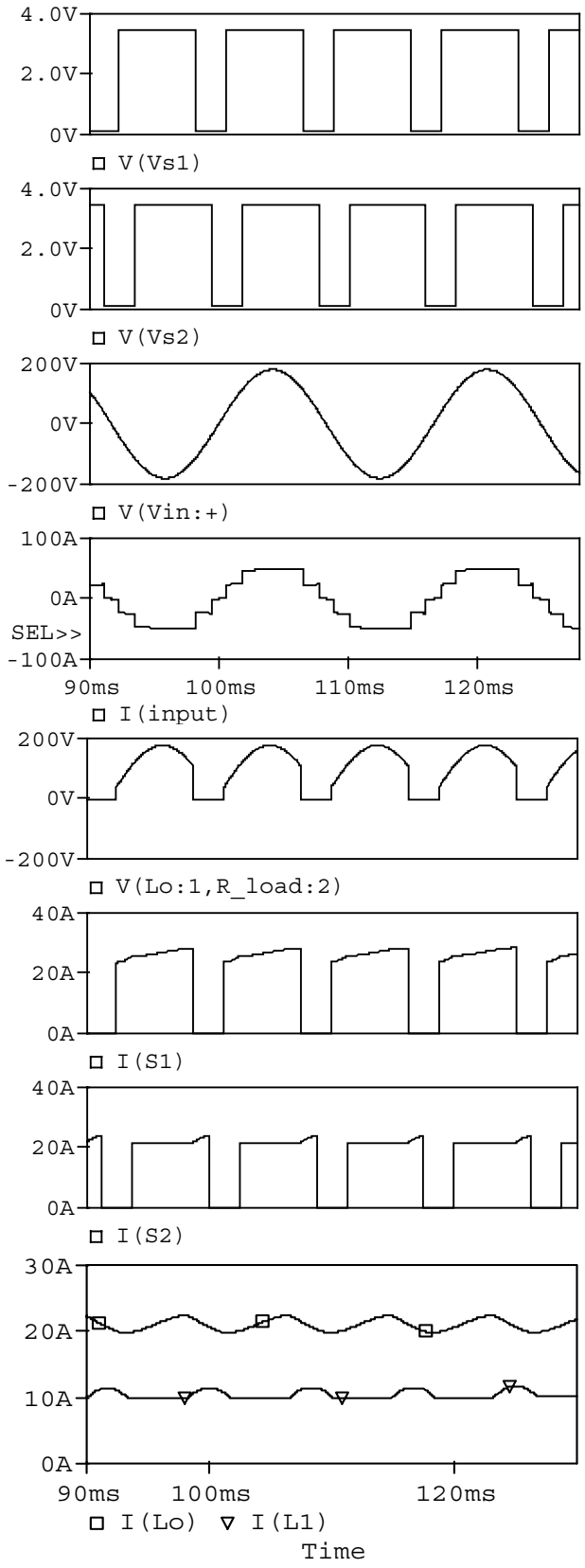


Fig. 6 – Simulated waveforms for the 2 cell buck rectifier. From top to bottom: gate pulses to switches S_1 and S_2; line voltage and input current; output voltage on the load (R_{load} +L_O); current flowing through switches S_1 and S_2; load current and current across balance inductor L_1.

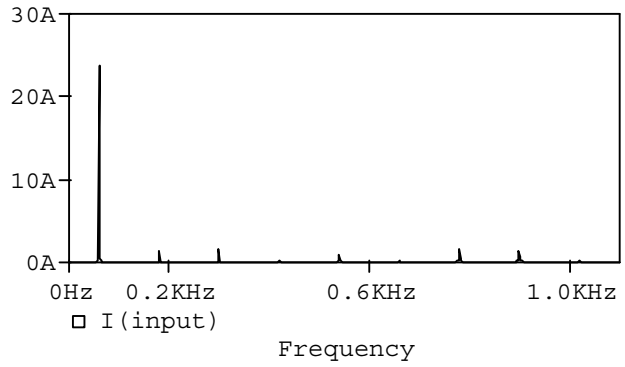


Fig. 7 – Harmonic spectrum for the rectifier input current

IV. Optimizing the Total Harmonic Distortion for a Given Output Voltage

By examining (1), one can see that the proper choice of angles α and Φ allows adjusting the rectifier output voltage V_o. However , there are several pairs of angles that produce a desired output voltage. It is interesting to find, for a given output voltage, a pair of angles that produces a current waveform with a minimum THD.

If the load is assumed as an ideal current source, or L_o is assumed as a near-infinite inductance, and L_1 is assumed large enough to maintain the current $I(L_1)$ almost constant during the time intervals where only one switch is turned on (corresponding to angle Φ), so the current waveform can be considered the ideal waveform shown in Fig. 1. For that waveform, the Fourier Series representation is given by

$$i(t) = \frac{2I}{\pi}\sum_{n=1}^{\infty}\{\cos[(2n-1)\alpha] + \cos[(2n-1)\cdot(\alpha+\Phi)]\}.\text{sen}[(2n-1)\omega t] \quad (2)$$

Where I is the value of the maximum level of input current. The amplitude of the harmonic component of order h, with h = 1,3,5,..., is given by

$$I_h = \frac{2I}{\pi}\{\cos(h\alpha) + \cos[h\cdot(\alpha+\Phi)]\}. \quad (3)$$

The total harmonic distortion is given by

$$THD_{\%} = 100\times\sqrt{\sum_{h=2}^{\infty}\left(\frac{I_h}{I_1}\right)^2}\ . \quad (4)$$

Using (1), (3) and (4), it is possible to compute the angles α and Φ that minimize the THD for a desired value of V_o. The plots showing the minimum THD and optimum angles against output voltage are depicted in Figs. 8 and 9, respectively. It has been assumed that the maximum angle Φ available was 30°, in order to consider the intermediary

level of current flat enough to apply the equations derived earlier. The computing of values has taken into consideration the harmonic components up to 30th order. The output voltages are expressed in percent of the rms input voltage.

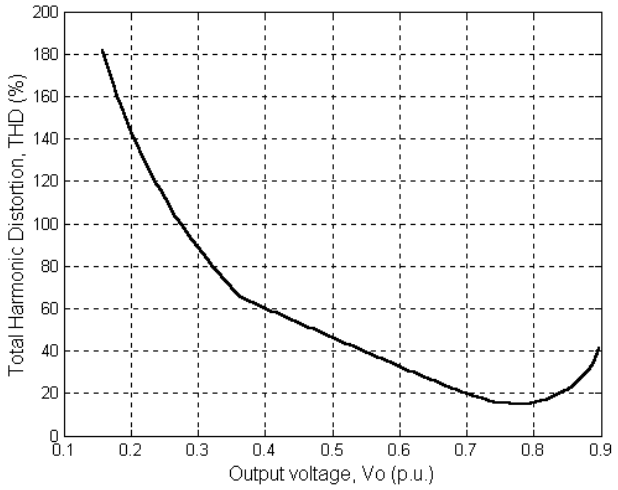


Fig. 8 – Minimum THD x Output voltage, V_o. Vbase=Vin (rms)

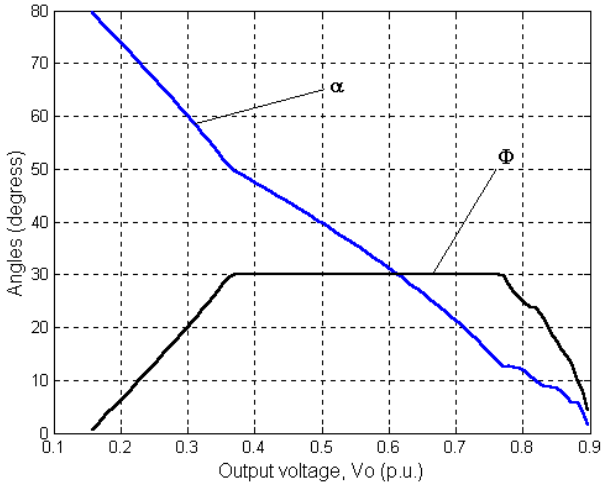


Fig. 9 – Angles α and Φ that provide optimum THD for different values of the output voltage, V_o. Φ was restricted to 30°.

V. The Pulse Generation Circuit

The pulse generation circuit has a fundamental role in the structure proposed here. It must synchronize switch pulses with line frequency and provide identical time intervals $\Delta t_{\alpha(1)}$ and $\Delta t_{\alpha(2)}$, as well as $\Delta t_{\phi(1)}$ and $\Delta t_{\phi(2)}$, as represented in Fig. 10. Small asymmetries between these intervals may determine a current unbalance between switches.

In the pulse generation circuit, described by the block diagram of Fig. 11, the synchronism is achieved by means of a network consisting of a comparator, which converts the sinusoidal input voltage to a square waveform, and a phase-locked loop circuit (PLL). A single chip 8-bit microcontroller, witch uses an internal counter (T/C0), provides the delays between S_1 and S_2 pulses.

It has been chosen the Fairchild CD4046BC circuit to perform the PLL function, while an Atmel AT89S8252 microcontroller has been employed to generate the switching pulses. The use of a microcontroller in the pulse generation circuit was conceived in order to allow adjusting the commutation angles by a numerical keyboard, leading to a reliable and simple interface to adjust the rectifier output voltage.

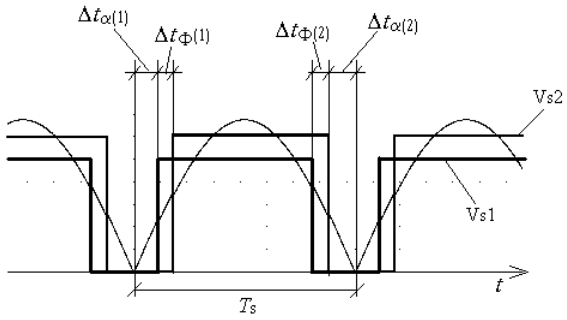


Fig. 10 – Bridge rectifier output voltage and the pulses V_{s1} and V_{s2}. Time intervals $\Delta t\alpha_{(1)}$/ $\Delta t\alpha_{(2)}$ and $\Delta t\Phi_{(1)}$/ $\Delta t\Phi_{(2)}$ must be equal to permit current balance in the switches

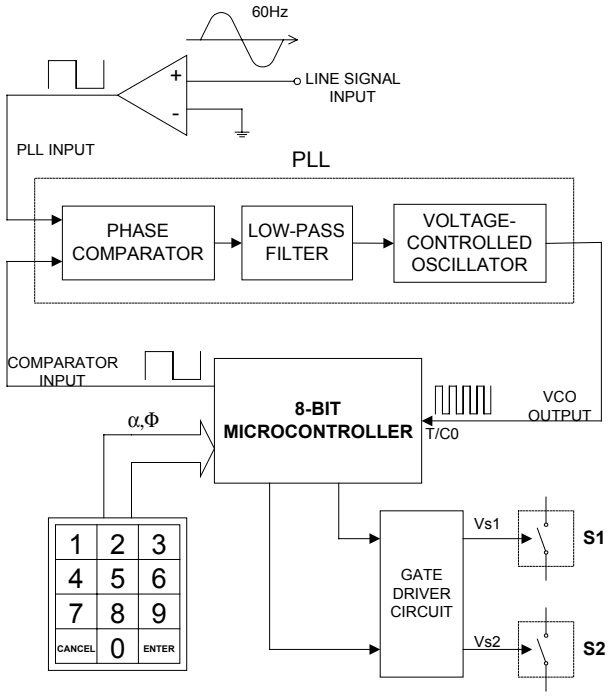


Fig. 11 – The synchronization and pulse generation circuit

VI. Experimental Results

A 2-kW prototype for the buck CML rectifier has been implemented. The International Rectifier IRG4PC30W IGBTs were chosen as active switches $S_1$and S_2 (referred to Fig. 5), while MUR1540 ultra fast diodes were used to implement diodes D_1 and D_2 of CML cell. Although these components are designed for high-frequency applications, the choice of these semiconductor switches for the prototype is justified only by the availability in laboratory. For a practical buck CML rectifier, even the first IGBTs

generation and low-frequency diodes could be employed, because of the low-frequency nature of this circuit.

The waveforms obtained from the lab prototype are plotted in Figs 12, 13 and 14 for the following parameters: $V_S = 127V_{rms}$, 60 Hz; $R_{load} = 4.1\ \Omega$, $L_O = 100$ mH, $L_1 = 60$ mH; $\alpha = 12.2^o$, $\phi = 25.9^o$. A parallel input filter has been used, employing an resistor, $R_f = 10\ \Omega$ in series with a capacitor, $C_f = 1.5\ \mu F$. A small resistor of 0.33 Ω has been used to share output current with L_1 in order to provide a good current balance between switch branches [1]. Note that the commutation angles used in the experimental setup were the same used in the simulation results.

For the input current shown in Fig. 14, the obtained THD was 15.33%, and the rectifier power factor was 0.98.

It can be noted that the input voltage presents a notching effect, which is produced by stray inductances. This technique side effect is also observed in thyristor rectifiers (which presents a very low power factor, however) [20]. The line voltage THD without notches was 2.30%, while a THD = 3.34% was obtained for the voltage in presence of notches.

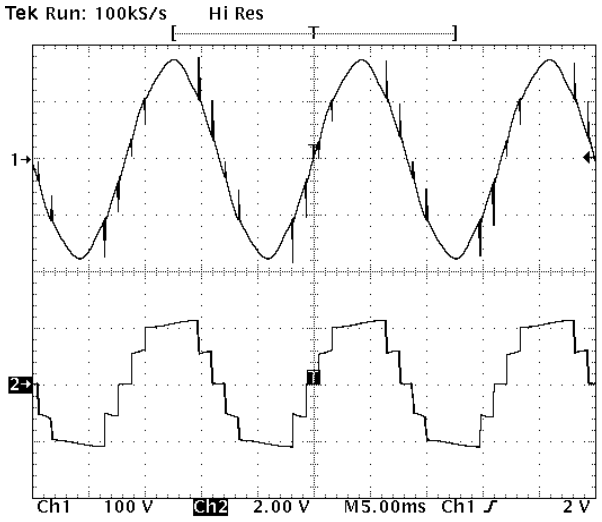


Fig. 12 – Input voltage (100V/div) and input current (20A/div) waveforms for the implemented rectifier

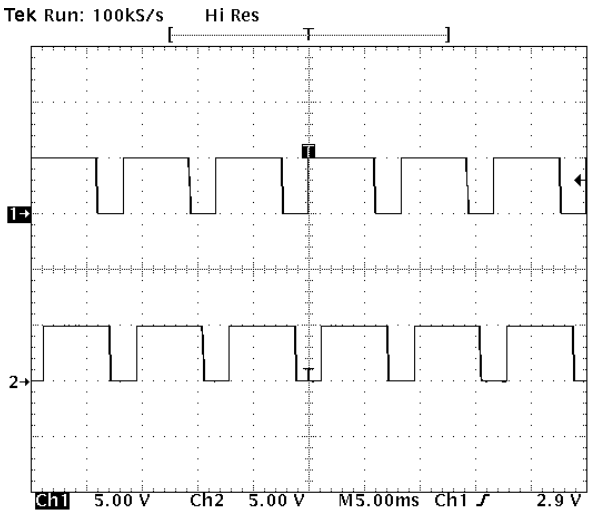
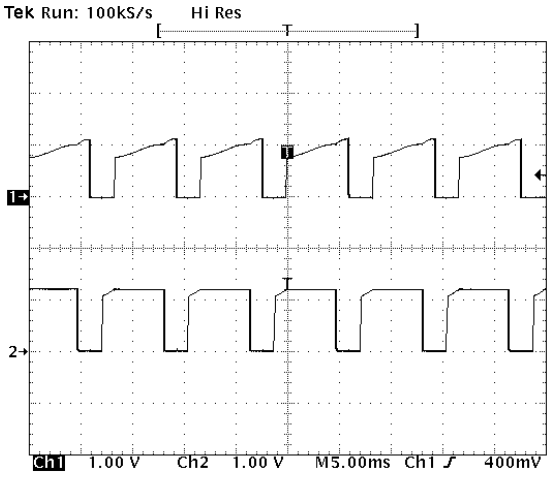
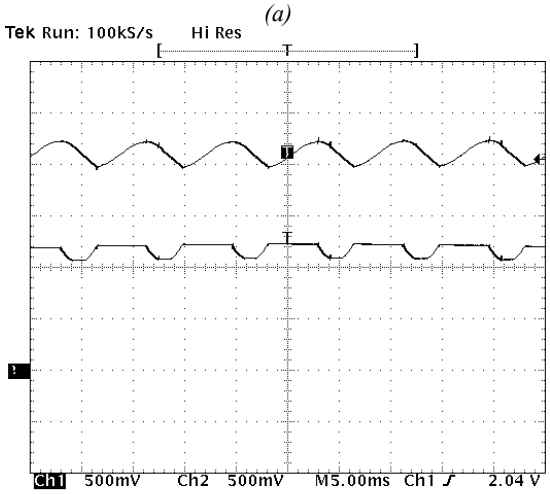


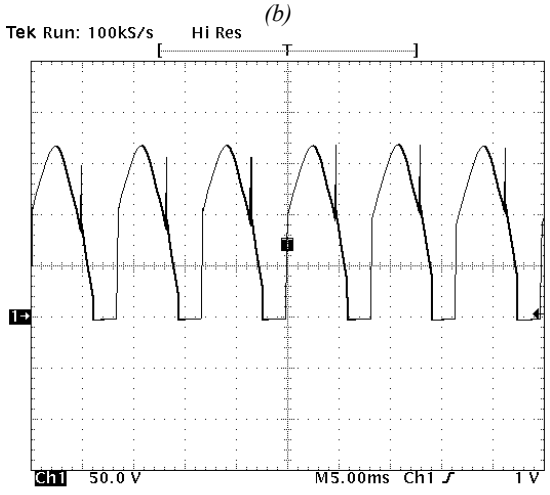
Fig. 13 – Gate pulses (microcontroller output), 5V/div.



(a)



(b)



(c)

Fig. 14 – More experimental waveforms:
(a) Current through S_1 and S_2 (10 A/div);
(b) Current through L_o and L_1 (5 A/div);
(c) Voltage across the load ($R\_load + L_o$) (50V/div).

VII. CONCLUSIONS

This paper introduced a new current multilevel rectifier, based on a two-cell buck converter. The structure was devised to verify the principle of sharing a high output current among a number of cells, using a small number of active devices, as compared to other alternatives. By means of a proper choice of delay angles it is possible to control the output voltage and provide a small THD for the input current, what leads to a high power factor circuit.

The comparison between experimental results plotted in Figs. 12–14 and simulation results shown in Fig. 6 has proven that the present technique can provide a high power factor input current from a single phase (or double phase) rectifier with no need of high frequency switching.

The synchronism strategy associated to the pulse generation circuit has been useful to guarantee the current balance between both switches. The use of a microcontrolled circuit allows the user to set the power delivered to the load and adjust the harmonic content of the input current, by means of choosing angles α and Φ.

Although the simulated and implemented CML rectifier in this work presented five levels in the input current, this technique can be extended to *n*-level rectifiers.

VIII. REFERENCES

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