The ZVS-PWM Active-Clamping CUK Converter

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***Abstract* — A CUK converter featuring clamping action, PWM modulation and soft-switching (ZVS) commutation is proposed to overcome the limitations of conventional CUK converter. As the resonant circuits absorb almost all parasitic reactances of switches, including transistor output capacitances, that converter is suitable for high-frequency operation.**

Principle of operation, theoretical analysis, and simulation results are presented in this paper. Experimental results, taken from a laboratory prototype rated at 400W, input voltage of 150V, output voltage of 200V, and operating at 100kHz, are presented too. The efficiency obtained at full load of power stage was 93%.

I. Introduction

The CUK converter is a good choice when it is necessary to control, in non isolated dc-to-dc converters, the output voltage in a large range of value [1]. It means that, the output voltage can be lower or higher than input voltage. Especially in high power factor applications [2], when a converter with an inductor at the front end is frequently desirable, the CUK converter is useful because the output voltage level can be lower than dc input voltage.

The high frequency operation in CUK converter, as in all dc-to-dc converters, is desirable because of the reduction of reactive component size and cost. As in any power application, high efficiency is essential, and hence the increasing of frequency can be problematic because of the direct dependence of switching losses on frequency. The use of soft-switching techniques, ZVS and ZCS, is an attempt to substantially reduce switching losses, and hence attain high efficiency at increased frequency.

Different techniques have been proposed to operate dc-dc converters in high frequency. The Active Clamping technique [3] has the advantages of PWM modulation, soft-commutation (ZVS) on main switches and low voltage stresses due to the clamping action. Besides operating at constant frequency and with reduced commutation losses there is no significant increasing on circulating reactive energy that would cause large conduction losses.

Thus, this paper presents a CUK converter featuring clamping action, PWM modulation and soft-switching (ZVS) in both active switches. In this converter the major parasitic reactances are absorbed, including transistor output capacitance and track inductance, resulting in high efficiency at high frequency operation without significant increasing in voltage and current stresses on switches. The proposed circuit is shown in Figure 1.

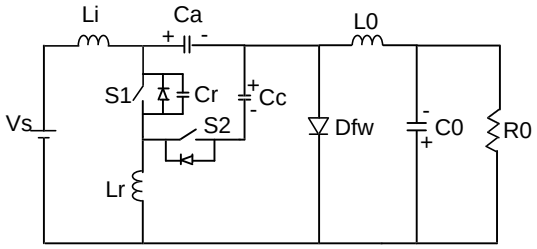
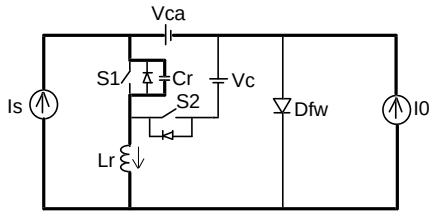


Fig. 1. The ZVS-PWM Active-Clamping CUK Converter.

II. Operation and Analysis of the Cuk Converter

In order to simplify the analysis, the input filter inductance is assumed large enough to be considered as a current source (Is). The capacitor Cc is selected to have a large capacitance so that the voltage Vc, across the capacitor Cc, could be considered as a constant one. The six topological stages and key waveforms, of the proposed CUK converter, to one switching cycle, are shown in Figures 2 and 3 respectively. In those Figures it can be seen that the two switches are switched in a complementary way and soft-switching is achieved for all switches. The main switch S1 is turned off at t=to, when the switching cycle starts.



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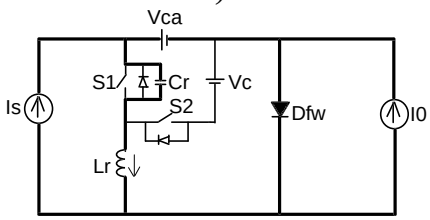

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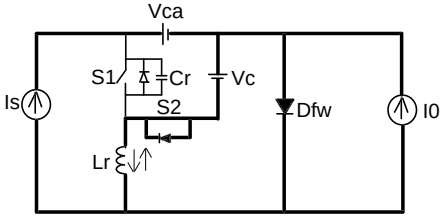

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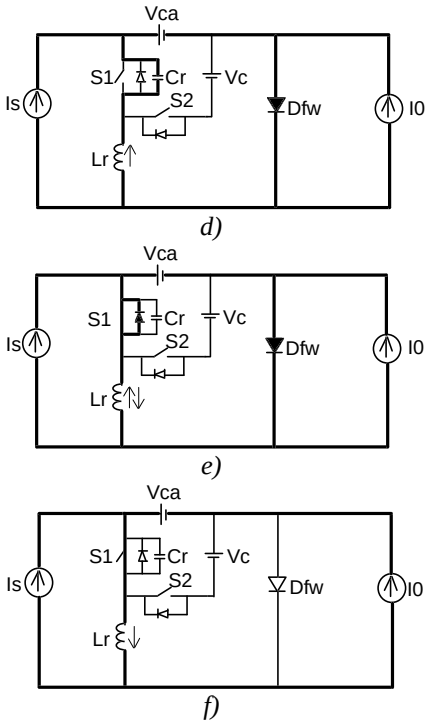


Fig. 2. Topological stages of CUK converter.

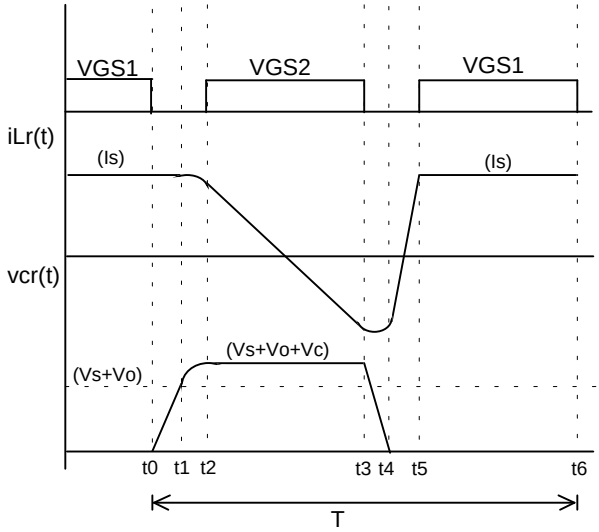


Fig. 3. Theoretical waveforms of CUK converter.

Stage 1 [to, t1]; linear stage Fig. 2a.

Prior to to, the main switch S1 is on, the auxiliary switch is off and the diode Dfw is off. When S1 is turned off, at t=to, the first stage has started, as shown in Fig. 2.a. The capacitor Cr is charged under constant current. When vcr(t) reaches Vca=Vo+Vs, the output diode (Dfw) becomes directly biased and starts conducting.

Stage 2 [t1, t2]; first resonant stage, Fig. 2b.

In this stage, current through Lr and voltage across Cr rings in a resonant way. Voltage vcr(t) increases until it reaches (Vs+Vo+Vc). When vcr(t)=(Vs+Vo+Vc) the antiparallel diode of S2 starts conducting and this stage ends up.

Stage 3 [t2, t3]; linear stage, Fig. 2c.

The Lr current ramps down, because Cc is considered as a constant voltage source, until it reaches zero, when it changes its direction and rises again. In this stage, voltage across Cr is clamped at (Vs+Vo+Vc). When the antiparallel diode of S2 is conducting, the auxiliary switch S2 should be switched on to achieve a loss-less turn-on. This stage ends when S2 is turned off at t=t4.

Stage 4 [t3, t4]; resonant stage, Fig. 2d.

The voltage across Cr falls, due to the resonance between Lr and Cr, until it reaches zero at t=t4. This stage ends when vcr(t) becomes null and the antiparallel diode of S1 begins conducting.

Stage 5 [t4, t5]; linear stage, Fig. 2e.

In stage 5, S1 is turned on without switching losses, in a ZVS way, because vcr(t) became zero. The current through Lr changes its polarity and ramps up to reach Is at t=t5. Then the diode Dfw becomes reversibly biased and turns off.

Stage 6 [t5, t6]; linear stage, Fig. 2.f.

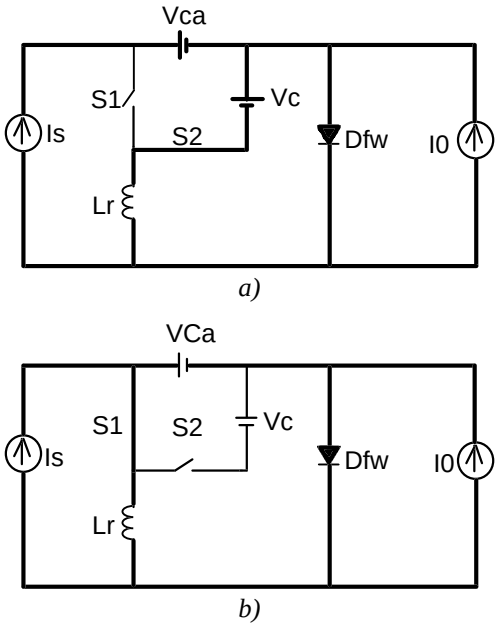
In this stage S1 is conducting a current equal to (Is+Io) and the auxiliary switch is off. The diode Dfw is off and the stage ends when S1 is turned off at the end of period.

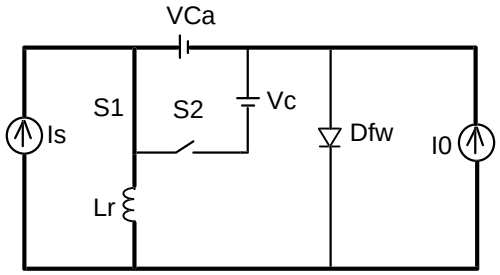
III. Low Frequency Behavior

In order to obtain the low frequency behavior some simplifications are necessary because in the other hand it could be an impossible or extremely hard task. So, as the resonant time intervals are so small when compared to the duration of stages 3, 5 and 6, it is possible to obtain the dc voltage gain from this simplified analysis. So, to proceed this approach we have to consider that:

- all switches are ideal and are switched in a complementary way, without dead time;
- the capacitances Ca and Cc are represented by dc voltages sources;
- the input voltage source and Li, and the output capacitor and Lo are considered as corrent sources;

Therefore, in this way, the converter operation is simplified by three stages as it can be seen in Figure 4.





c)

Fig. 4. Topological stages to simplified operation.

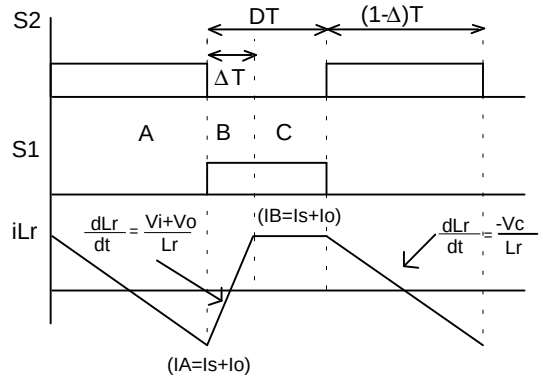


Fig. 5. Main waveforms to simplified operation.

As Is is equal to the average current through Lr , we have:

$$Io(D-\Delta)T = Ii(1-D+\Delta)T \qquad (1)$$

$$q = \frac{Is}{Io} = \frac{Vo}{Vs} = \frac{D-\Delta}{1-D+\Delta} \qquad (2)$$

In order to keep, in stationary stage, a stable operation, IA must be equal IB, because the average current through Cc must be zero. Thus, from Figure 5, we have:

$$\Delta = \frac{2\cdot Lr\cdot(Io+Is)}{T\cdot(Vs+Vo)} \qquad (3)$$

So, if we consider:

$$Ln = \frac{Lr\cdot Io}{Vs\cdot T} \qquad (4)$$

It will result:

$$\Delta = 2\cdot Ln \qquad (5)$$

And, equating (5) in (2), it has:

$$q = \frac{D-2\cdot Ln}{1-D+2\cdot Ln} \qquad (6)$$

Equation (6) represents the dc voltage gain of the converter and D is the duty cycle and Ln is the normalized load current.

Another important parameter to consider is the voltage across the clamping capacitor. So, as the average current across Cc must be zero in a switching cycle, we have:

$$Ic_{med} = \frac{1}{T}\int_0^{(1-D)T}\left[\frac{-Vc}{Lr}t + Is + Io\right]dt = 0 \qquad (7)$$

By solving (7), it results:

$$Vc = (Is+Io)\cdot\frac{2\cdot Lr}{(1-D)\cdot T} \qquad (8)$$

Or,

$$\beta = \frac{2\cdot Ln}{(1-D)}\cdot(1+q) \qquad (9)$$

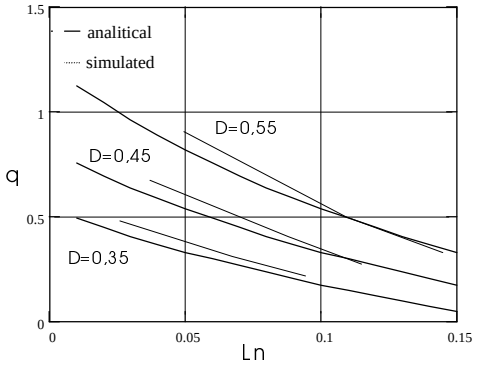
Where,

$$\beta = \frac{Vc}{Vs} \qquad (10)$$

Thus, equating (6) in (9), it results:

$$\beta = \frac{2\cdot Ln}{(1-D)}\cdot\frac{1}{(1-D+2\cdot Ln)} \qquad (11)$$

The dc voltage gain and the normalized clamping voltage, as a function of normalized load current are shown in Fig. 6. As we can see the simulated results are very close to the analitical results.



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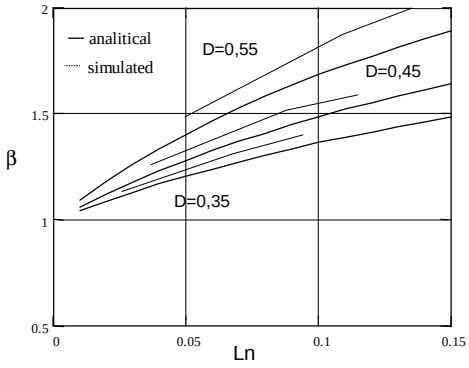


b)

Fig. 6: (a) DC voltage gain; (b) Normalized clamping voltage.

IV. COMMUTATION ANALYSIS

Due to the capacitance Cr, S1 and S2 are turned off with no losses, in a ZVS way. However, S1 and S2 will turn on with no losses, only if there were enough energy stored in Lr to achieve soft commutation. At t=t1, it is necessary to charge Cr from Vo+Vs to Vo+Vs+Vc. At t=t3, it is necessary to discharge Cr from Vc+Vs+Vo to zero. The latter is more difficult because it needs more energy. Thus, if enough energy is guaranteed to achieve soft commutation for S1, then S2 will achieve soft commutation too. Therefore, from energy relationships in Lr and Cr, at t=t3, we have:

$$\frac{1}{2}Lr\cdot(Is+Io)^2 \geq \frac{1}{2}Cr\cdot(Vc+Vs+Vo)^2 \qquad (12)$$

$$Ln \geq \left[\frac{(1-D)}{(1-D)T \cdot \omega o - 2} \right] \quad (13)$$

Where,

$$f = \frac{fo}{fs} \text{ and } \omega_0 = \frac{1}{\sqrt{LrCr}} \quad (14)$$

As that result was achieved on a model with imposed current, then, at t=t3, the current through Lr is equal to the average input current. But, in the real prototype, there is an input inductor that has maximum current greater then average current, so there is more energy stored to commutation. Thus, equation (13) must have a correction factor, which is represented in equation (15).

$$Ln \geq \left[\frac{2Ln}{1-D} + 1 \right] \cdot \left[\frac{1}{(D-2Ln) \cdot \frac{r}{2} + 1} \right] \frac{1}{T \cdot \omega_0 \cdot} \quad (15)$$

Where, (r) is the percentage input current ripple,

$$r = \frac{\Delta Is}{Is} \quad (16)$$

From the analysis before, it is clear that soft-commutation, when S1 turns on, will be achieved depending on Io and Lr. And, as Io depend on the processed power, then that commutation will occur with no losses, only in a range of load that will be established through equation (15). But although that commutation is not completely without losses, the converter will still operate with high efficiency in light load situations, because there will always be enough energy stored in Lr to help the commutation process, and the lost energy never will be so high, as in a completely hard commutation.

As the critical commutation is when S1 turns on, it is important to determine the time interval between the turning on of S1 and turning off of S2. This time interval is necessary for the existence of soft commutation. Then:

$$td \geq \frac{(Vc + Vo) \cdot Cr}{Is} \quad (17)$$

$$td \leq \frac{(Vc + Vo) \cdot Cr}{Is} + \frac{Is \cdot Lr}{(Vo + Vs)} \quad (18)$$

V. Voltage and Current Stresses on Switches

Below, are presented the voltage and current stresses on switches. All current and voltages are normalized. Which means:

$$\bar{I} = \frac{I}{Io} \quad (19)$$

and

$$\overline{V} = \frac{V}{Vs} \quad (20)$$

Switch S1:

$$\overline{Vs1}_{PK} = \frac{1}{(1-D)} \quad (21)$$

$$\bar{Is1}_{PK} = \frac{1}{1-D+2Ln} \quad (22)$$

$$\bar{Is1}_{AVG} = \frac{(D-2Ln)}{[1-(D-2Ln)]} \quad (23)$$

$$\bar{Is1}_{RMS} = \frac{1}{[Ln-(D-2Ln)]} \sqrt{\frac{3D-4Ln}{3}} \quad (24)$$

Switch S2:

$$\overline{Vs2}_{pk} = \frac{1}{1-D} \quad (25)$$

$$\bar{Is2}_{PK} = \frac{1}{1-D+2Ln} \quad (26)$$

$$\bar{Is2}_{AVG} = 0 \quad (27)$$

$$\bar{Is2}_{RMS} = \frac{1}{[1-(D-2Ln)]} \sqrt{\frac{4(1-D)+16Ln}{3}} \quad (28)$$

Diode Dfw:

$$\overline{VDfw}_{PK} = \frac{1}{(1-D)+2Ln} \quad (29)$$

$$\bar{I}Dfw_{PK} = \frac{2}{1-D+2Ln} \quad (30)$$

$$\bar{I}Dfw_{AVG} = 1 \quad (31)$$

$$\bar{I}Dfw_{RMS} = \sqrt{\frac{4(1-D)+8Ln}{3(1-D+2Ln)^2}} \quad (32)$$

IV. Simulation Results of the Proposal Cuk Converter

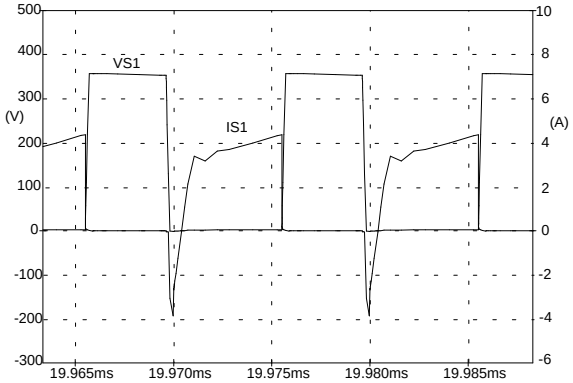
The new CUK converter was simulated with the following specifications:

- output power Po=400W;
- input voltage Vs=150V;
- output voltage Vo=200V;
- switching frequency fs=100kHz.

The power stage consists of the following parameters:

D = 0.63	β =0.557	Ln = 0.048
Lr = 40μH	Cr = 2.12nF	Cc = 1μF

Simulation obtained waveforms of the switches current and voltages can be seen in Fig. 5.a and 5.b. The resonant inductor current and voltage across the resonant capacitor are shown in Fig. 6 a. The voltage across diode Dfw and the current through this diode are shown in Fig. 6 b. These waveforms agree with those predicted theoretically, and as it can be noted from the waveforms shown in Fig. 5, the main switches (S1 and S2) present ZVS commutation with clamped voltages.



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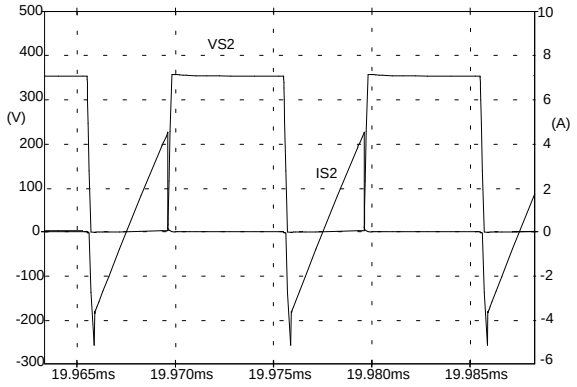

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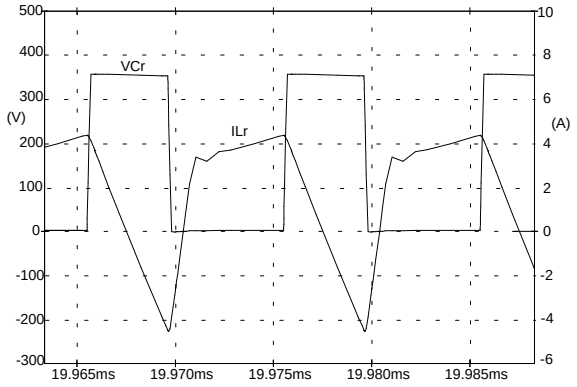
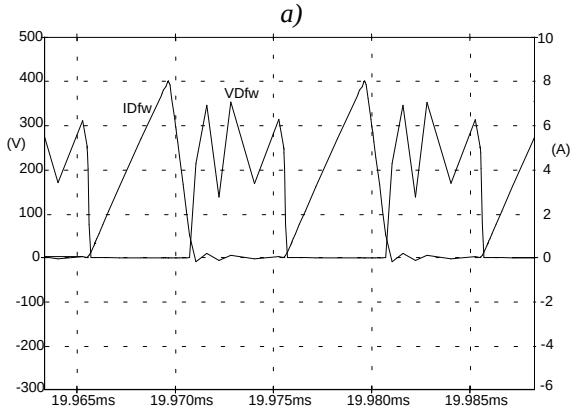
Fig. 5. a) Voltage across S1 and current through S1; b) Voltage across S2 and current through S2.



a)



b)

Fig. 6. a) Voltage across Cr and current through Lr ; b) Voltage across Dfw and current through Dfw.

V. EXPERIMENTAL RESULTS

The new CUK converter was implemented, with the following specifications: output power Po=400W; input voltage Vs=150V; output voltage Vo=200V; switching frequency fs=100kHz. The power stage, shown in Figure 1, consists of the following parameters:

- switches S1 and S2: Power MOSFET's BUZ334;
- diode Dfw: RURP1560;
- extern resonant capacitor Cr_{ext}: 2000pF/1.6kV;
- capacitor Cc: 1.0μF/630V;
- capacitor Ca: 470μF/400V
- output filter capacitor Co: 470μF/400V;
- resonant inductor Lr: 40μH, core (E-30/14)-Thornton;
- input inductor Li: 1000μH, core (E-65/26) Thornton;
- Inductor Lo: 1000μH, core (E-55).

Experimentally obtained main waveforms of the prototype are shown in Figures 7,8, 9 and 10.

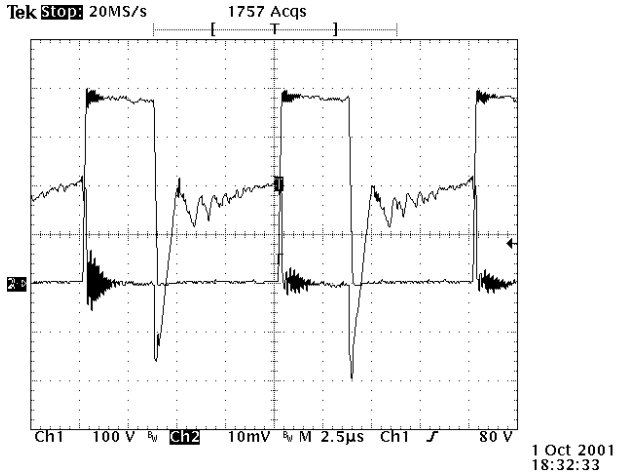


Fig. 7. Drain-to-source voltage across main switch S1 and its current (voltage: 100V/div; current: 2A/div; time scale: 2.5μs/div).

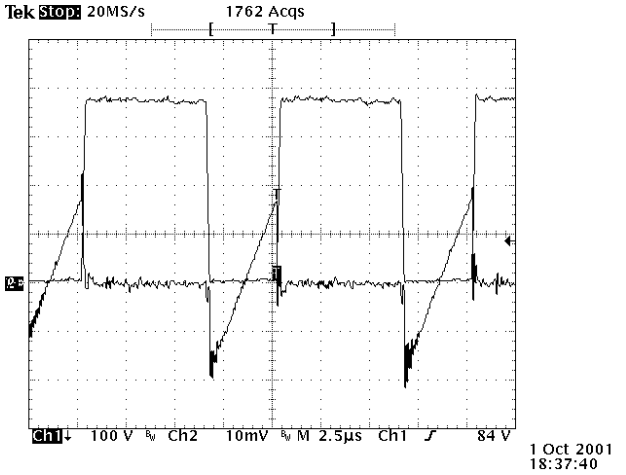


Fig. 8. Drain-to-source voltage across switch S2 and its current (voltage: 100V/div; current: 2A/div; time scale: 2.5μs/div).

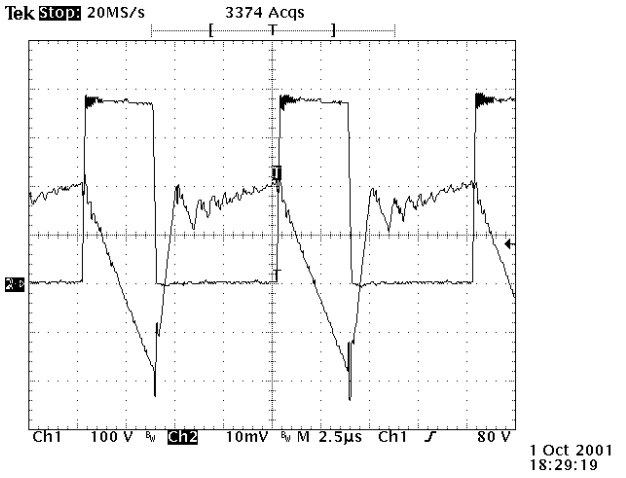


Fig. 9. Voltage across Cr and current through Lr (voltage: 100V/div; current: 2A/div; time scale: 2.5μs/div).

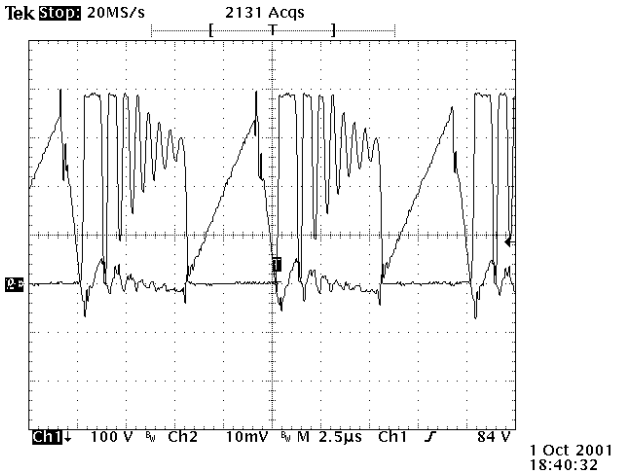


Fig. 10. Voltage across Dfw and current through Dfw (voltage: 100V/div; current: 2A/div; time scale: 2.5µs/div).

These waveforms agree with those predicted theoretically, and as it can be noted from the waveforms shown in Figures 7 and 8, the main switches (S1 and S2) present ZVS commutation with clamped voltages.

In Fig. 11, the DC voltage gain, as a function of output current, is shown, for different duty cycles can be noted.

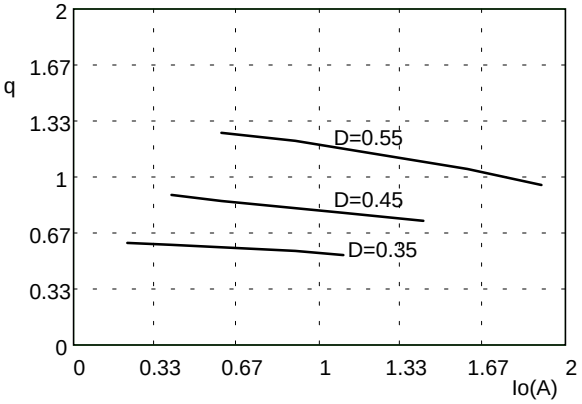


Fig. 11. DC voltage gain with different load conditions and duty cycle.

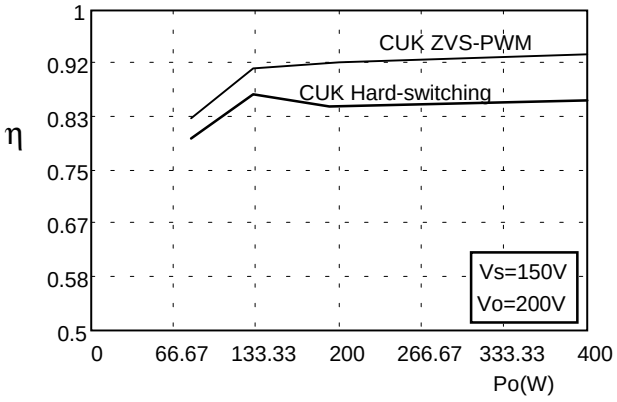


Fig. 12. Experimental efficiency curve with constant output and input voltage.

The experimental efficiency curve of the new converter and the hard-switching counterpart are shown in Fig. 12. The converter presented high efficiency (up to 90%) from 32% to 100% of full load. At full load, the efficiency was 93%. The duty cycle necessary to keep voltages Vs and Vo constant is shown in Figure 13.

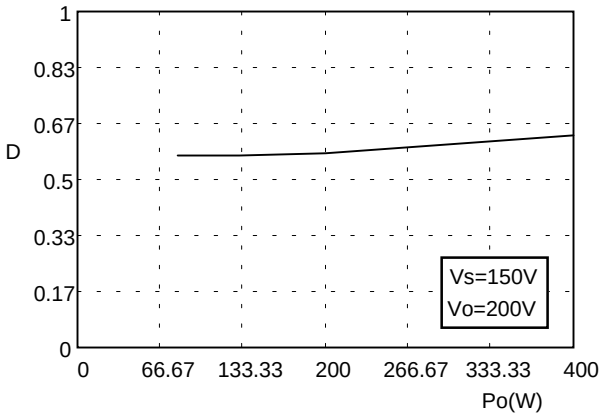


Fig. 13. Experimental duty cycle curve with constant output and input voltage.

VI. CONCLUSION

A CUK converter featuring clamping action, PWM modulation and soft-switching (ZVS) commutation is proposed to overcome the limitations of the conventional CUK converter. As the resonant circuits absorb almost all parasitic reactances, including transistor output capacitance and diode junction capacitance, the new converter operate with favorable switching conditions in all switching devices. Theoretical studies and experimental results allow us to draw the conclusion that the converter is suitable for high frequency operation with high efficiency.

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