Two Alternatives for High-efficiency Isolated DC-DC Converters for High-Voltage Aerospace Applications

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Abstract - Two alternatives for the implementation of an isolated dc-dc converter operating with high output voltage and supplied by an unregulated low input voltage are presented in this paper. The proposed topologies are especially well adapted for the implementation of Travelling Wave Tube Amplifiers (TWTA) utilized in telecommunication satellite applications, due to low mass and volume and the high-efficiency reached by the proposed structures.

The converters studied follow different principles and the main operation aspect of each topology is analyzed.

A two-stage structure composed by a regulator connected in series with a ZVS/ZCS isolated dc-dc converter is the first topology proposed.

The second topology studied is an isolated single-stage converter that maintains high-efficiency even under a large variation of the input voltage.

The experimental results obtained from two prototypes implemented following the design procedures developed are presented, verifying experimentally the characteristics and the analysis of the proposed structures.

The prototypes are developed for an application with 150W of output power, total output voltage of 3.2kV and a variable input voltage from 26V to 44V. The minimum efficiency for both converters operating with the nominal output power occurs for the minimum input voltage, obtaining an efficiency of 93.4% for the two-stage structure and 94.1% for the single-stage converter.

I. INTRODUCTION

There are different applications where is necessary the use of high level DC voltages (thousands volt). Typical examples are CO_2 laser-based systems, medical and industrial X-ray and telecommunication equipment with vacuum tubes, like Travelling Wave Tube (TWT) utilized in communication satellite. Therefore, several high-voltage dc-dc switching power converters are used in different types of electronic equipment. The designer of high voltage power supplies face many problems that are not present in low voltage design and the choice of most adequate solution depends of the design requirements of each specific application.

The design difficulty of high-voltage converters is increased in satellite application due to the severe requirements and specifications that must be attended. The launch cost is very high and there is a permanent interest in the efficiency improvement and reduction of the mass and volume of the satellite equipment. High efficiency is important to achieve since the primary power source of a satellite is a solar array and batteries, presenting an important influence in the total mass, volume and cost.

The final stage amplifier in the transponder of the communication satellite is the Travelling Wave Tube Amplifier (TWTA). In this kind of satellite, the payload mass and power consumption is mainly given by the presence of the TWTA which represent about 35% of the total mass and from 70% to 90% of the overall DC power consumption [1]. Therefore the design of TWTA has been continuously improved in order to realize more light and efficient equipment.

The TWTA consists of a microwave amplifier tube TWT mainly determining the radio frequency (RF) performance and an Electronic Power Conditioner (EPC) for power matching of the DC interface. The high voltage dc-dc converter can be considered the most important part of the EPC because it is the critical point in the design of a high efficiency and competitive TWTA.

II. HIGH-VOLTAGE ISOLATED DC-DC CONVERTERS

The operation of the isolated converter is influenced by the presence of the intrinsic elements of the power transformer. In low-voltage applications, the power transformer can be represented by its magnetizing and leakage inductance, considering its operation without losses. However, in a step-up transformer for high-voltage applications, there is also an equivalent winding capacitance referred to the primary side that must be included in the transformer equivalent model. Due to the high number of turns in the secondary winding and the high transformer turns ratio, this equivalent capacitance becomes important in the converter operation.

Fig.1 presents the high-voltage transformer simplified model constituted by the leakage inductance (L_d), magnetizing inductance (L_m) and the equivalent capacitance referred to the primary side (C_p) [2].

This model is adopted in the principle of operation analysis of the topologies studied.

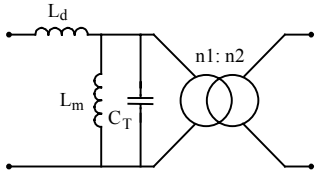

Fig.1. Simplified equivalent circuit of the high voltage and high frequency transformer.

There are some operations characteristics that an isolated topology must presents for its utilization in high output voltage application, maintaining high efficiency, low volume and mass. The main operation characteristics are:

- High switching frequency reducing the reactive elements likes inductors, filter capacitors and the power transformer.
- Soft-commutation in the power switches, avoiding the reduction of the efficiency with the increment of the switching frequency.
- Incorporation of the intrinsic elements of the circuit in the converter operation like switch capacitance, leakage inductance and equivalent capacitance of the high-voltage transformer, avoiding the dissipation of the energy stored in these elements.
- Constant switching frequency, allowing the choice of an optimum switching frequency with respect to the mass, volume and efficiency.
- Voltage source output characteristic, because the multiple high-voltage outputs necessaries for to supply the TWT becomes unfeasible the utilization of output filter inductors in the high-voltage session, for a current source output characteristic.
- Input current source behavior, because the non-pulsating input current allows the reduction of the input filter.
- A step-up output characteristic, reducing the transformer turns ratio and minimizing the effects of the transformer equivalent capacitance referred to the transformer primary side.
- Good load regulation and operation with a large variation of the input voltage.
- Low di/dt in the high-voltage rectifier diodes, minimizing the effects of the recovery current of these diodes.

Considering as choice criterion of the isolated converters all operation characteristics presented above, two topologies were selected and studied for the implementation of a TWTA.

III. The Two-Stage Topology

The input voltage presents a large variation range and the first solution proposed for the implementation of the TWTA power stage is composed by two dc-dc converters connected in series (two-stage topology), presented in Fig.2.

A. Proposed Circuit

The first converter of the two-stage structure is a boost dc-dc converter composed by the input inductor L_1, power switch S_1, diode D_1 and filter capacitor C_1. The boost converter regulates the input voltage variations and operates with PWM modulation and hard switching. However, the operation with low input voltage and the utilization of a schottky diode in the boost output, high-efficiency operating with high switching frequency is reached.

The second stage is an isolated dc-dc converter with resonant operation, generating the different high voltage outputs for supply the TWT [3]. In this case, the isolated dc-dc converter operates in an optimized operation point, with constant switching frequency and fix duty-ratio. The isolated topology is a resonant push-pull current fed dc-dc converter composed by two power switches S_1 and S_2, an input inductor L_2, a resonant capacitor C_T and the push-pull transformer. The intrinsic parameters of the transformer (L_{d1}, L_{d2}, C_{p1} and C_{p2}) are also presented in Fig.2.

A full-bridge rectifier and filter capacitor compose the output.

The push-pull converter operates with zero current and zero voltage switching techniques (ZCS/ZVS). The input current source characteristic of the push-pull converter is obtained with the inductor L_2.

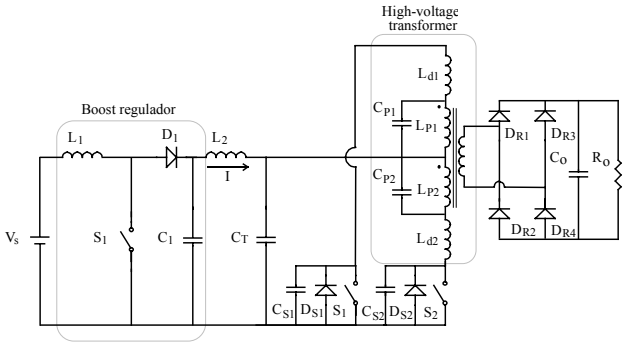

Fig.2. Proposed power circuit of the two-stage topology.

B. Principle of operation

The push-pull ZVS/ZCS principle of operation can be described in two operation stages presented below. For simplification, the components are considered ideal, however the switch capacitance, the leakage inductance and the equivalent capacitance of the high-voltage transformer are included in this analysis.

The output voltage of the boost regulator is substituted by a constant voltage source V_{in}.

1) First operation stage *($[t_o, t_1]$ Fig.3).*

The current in the transformer center tap (i) initially is zero and during the conduction of the switch S_1, the resonance between the center tap capacitance C_T and the leakage inductance L_{d1} occurs. The current (i) increases, reach its maximum value and becomes zero, finishing this operation stage.

During this stage the center tap current (i) is conducted to the filter capacitor and load through the transformer windings and the rectifier diodes D_{R1} and D_{R4}.

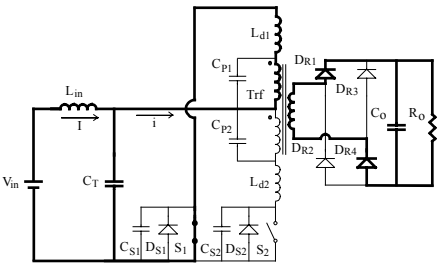

Fig.3. First operation stage (t_o-t_1).

2) Second operation stage *($[t_1, t_2]$ Fig.4).*

When the current in the switch S_1 becomes zero, the rectifier diode is blocked and the energy stored in the magnetizing inductance is transferred to the switch

capacitance and the equivalent capacitance of the high-voltage transformer. The voltage in the equivalent capacitance of the circuit changes in a resonant way and the switch S_2 turn-on occurs with soft-commutation.

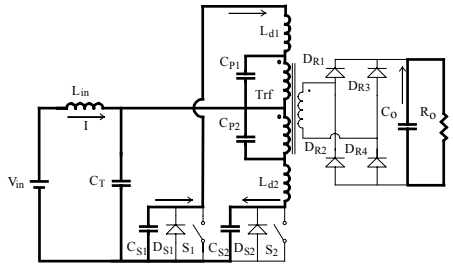

Fig.4. Second operation stage (t_1-t_2).

The main theoretical waveforms of the isolated converter are presented in Fig.5. The commutation loss in the power switches is very low. The maximum voltage across the switches is equal twice the push-pull input voltage (boost output voltage) plus the voltage ripple in the center tap capacitor C_T. Therefore this converter is indicated for low input voltage applications.

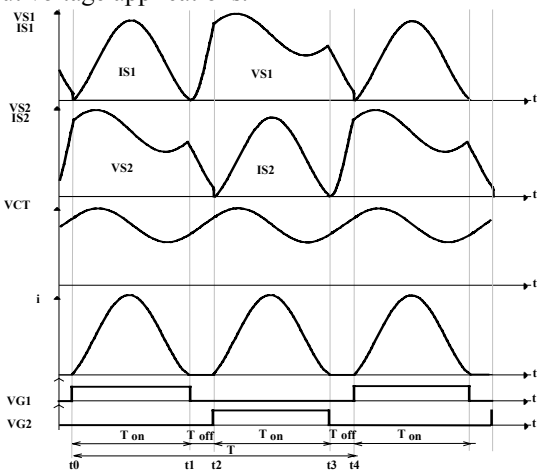

Fig.5. Main theoretical waveforms.

C. Main Mathematical Results and Simplified Design Procedure

The main mathematical results obtained from the theoretical analysis are presented and utilized in a simplified design procedure.

1) Specifications and parameters

The following specifications are considered in the design of the two-stage topology:

Input voltage:	V_s=26/44V
Boost output voltage:	V_2=50V
Total output voltage:	V_o=3200V
Output power:	P_o=150W
Push-pull switching frequency:	F_s=80kHz
Boost switching frequency:	F_b=120kHz

The parameters of the implemented circuit are:

Magnetizing inductance with gap:	L_m=85µH
Leakage inductance:	L_d=1.3µH
Winding capacitance:	C_p=8.75nF
Switch capacitance:	C_s=1nF

2) Operation point of the Push-Pull converter

The switch current must be zero at the end of the period T_{on} (Fig.5 instant t_1) and the voltage across the switch that will be turned-on must reach a low value at the end of the period T_{off} (Fig.5 instant t_2), for the optimized operation of the push-pull converter. These two conditions are defined mathematically by (1) and (2) respectively. The design procedure is simplified solving numerically (1) and (2), and the results obtained are plotted in fig. 6.

$$\cos(\pi.F_r.t_r) - \frac{\pi.F_r.(1-t_r)}{2} \cdot sin(\pi.F_r.t_r) - 1 = 0 \quad (1)$$

$$2 \cdot \cos(\pi \cdot F_{r2} \cdot (1-tr)) - \pi \cdot F_{r2} \cdot tr \cdot sin(\pi \cdot F_{r2} \cdot (1-tr)) + 2 = 0 \quad (2)$$

Where:

$$t_r = \frac{2 \cdot T_{on}}{T} \quad (3)$$

$$F_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_d.C_T}} \cdot \frac{1}{F_s} \quad (4)$$

$$F_{r2} = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_m \cdot C_{eq}}} \cdot \frac{1}{F_s} \quad (5)$$

The relative frequency Fr is the relationship between the resonance frequency of the leakage inductance and the center tap capacitance with the switching frequency. This resonance occurs during the conduction of the power switch. Fr2 is the relationship between the resonant frequency of the magnetizing inductance and equivalent circuit capacitance with the switching frequency. This resonance occurs when both switches are turned off.

Substituting the specification and parameters in (7) yields:

$$C_{eq} = C_{s1} + C_{p1} \quad (6)$$

$$F_{r2} = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot L_m \cdot C_{eq}}} \cdot \frac{1}{F_s} = 1{,}5453 \quad (7)$$

The frequency F_{r2} calculated must be higher than 1.1 for to obtain soft-commutation. The components stresses are reduced for a relative frequency F_r close to 2 and a relative conduction time t_r close to 1. The energy stored in the magnetizing inductance performs the voltage transitions in the equivalent circuit capacitance. Therefore, the magnetizing inductance can be reduced inserting a gap in the transformer, allowing the choice of a good operation point.

With the relative frequency F_{r2} calculated, the value of the switch conduction time (t_r) is defined in Fig.6.

t_r= 0.81

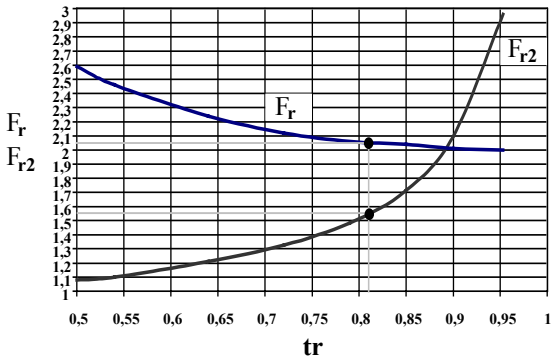

Fig.6. Optimized operation point.

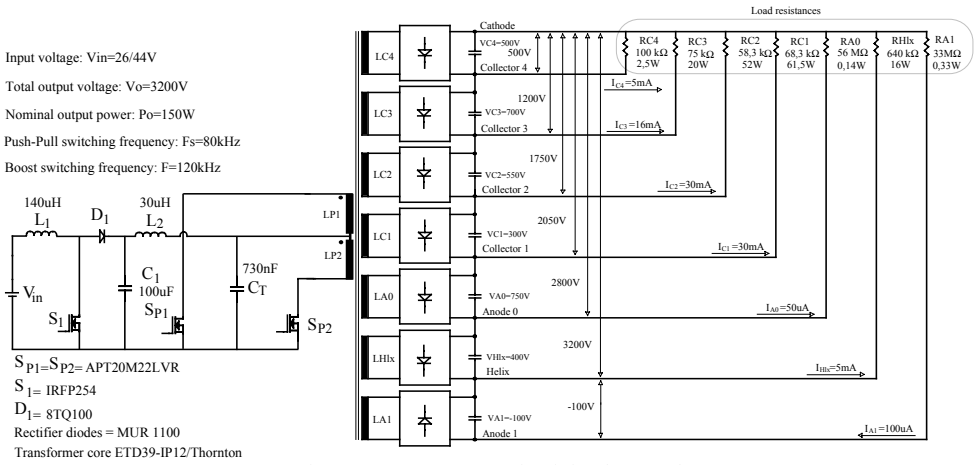

Fig.7. Two-Stage Power circuit implemented.

The switch turn-on and turn-off period are calculated by:

$$T_{on} = \frac{t_r}{2 \cdot F_s} = 5\mu s \tag{8}$$

$$T_{off} = \frac{T}{2} - T_{on} = 1.25\mu s \tag{9}$$

3) Center Tap Capacitance (C_T)

Fig. 6 also defines the relative frequency Fr.

$$Fr = 2.05 \tag{10}$$

$$F_o = F_s \cdot F_r = 164kHz \tag{11}$$

$$\omega_o = 2 \cdot \pi \cdot F_o \tag{12}$$

The center tap capacitance can be calculated by:

$$C_T = \frac{1}{L_d \cdot \omega_o^{\,2}} = 724nF \tag{13}$$

4) Current and voltage stresses

The input current (I) is defined by (14), considering an efficiency of η=95%.

$$I = \frac{P_o}{V_2 \cdot \eta} = 3.158A \tag{14}$$

The switch peak current (I_{pk}) is calculated by:

$$\varphi = a\tan g\left(\frac{\pi . F_r . (1 - t_r)}{2}\right) = 0.549 \tag{15}$$

$$I_{pk} = I \cdot \left[1 + \frac{1}{\cos(\varphi)}\right] = 6.86A \tag{16}$$

The switch RMS current is:

$$iS_{RMS} = \sqrt{\frac{I_{pk} \cdot t_r}{4}} = 3.09A \tag{17}$$

The maximum blocking voltage across the switch (VS_{pk}) is:

$$Zn = \sqrt{\frac{L_d}{C_T}} = 1.34 \tag{18}$$

$$VS_{pk} = \frac{I \cdot Zn}{\cos(\varphi)} + 2 \cdot V_2 = 105V \tag{19}$$

5) Output voltage ripple

The parameterized output voltage ripple is calculated by (20) and (21).

$$\delta = a\tan g\left(\frac{\pi . F_r . (1 - t_r)}{2}\right) \tag{20}$$

$$\overline{\Delta V} = \frac{\Delta V_{Co} \cdot C_o \cdot F_s}{I_o} = \frac{1}{\pi} \cdot \frac{2}{F_r \cdot \cos(\delta)} \tag{21}$$

Where:

I_o – Average current of each output

C_o – Filter capacitor

ΔV_{Co} – Output voltage ripple

C. Experimental Results

A laboratory prototype was implemented following the optimized design procedure developed and some waveforms obtained from this prototype operating with the minimal input voltage and the nominal output power are presented. The details about the power circuit implemented are shown in Fig.7. A typical configuration of load resistance representing the TWT for the test of the power supply is used. The different current and voltage level in each output and the nominal output power are defined by the kind of TWT adopted in the design.

The main experimental results of the push-pull converter operating with nominal output power are presented in Figs. 8 and 9.

Fig.8 presents the soft-commutation obtained in the power switch of the push-pull converter and the peak voltage is about 120V.

Fig.9 shows the voltage and current in a high-voltage rectifier diode of the push-pull. The efficiency curve of the two-stage topology (boost and Push-pull) operating with nominal output power and variable input voltage is presented in Fig.10. The lowest efficiency obtained with nominal output power is equal to 93.4%.

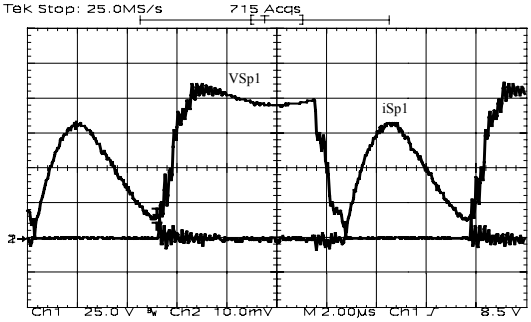

Fig.8. Power switch voltage and current (25V/2A/2µs/div).

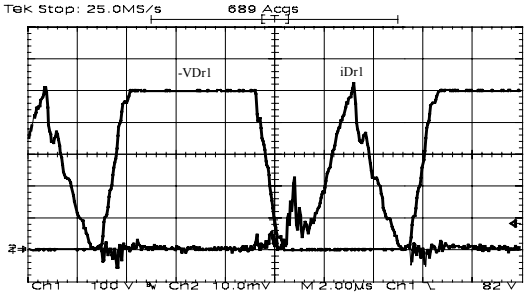

Fig.9. Rectifier diode voltage and current (100V/50mA/2µs/div)

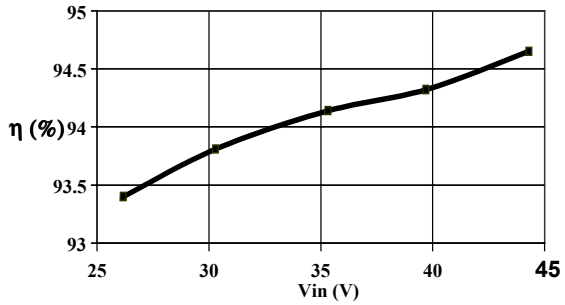

Fig.10. Efficiency operating with nominal output power and variable input voltage

IV-THE SINGLE STAGE TOPOLOGY

A critical point in the utilization of the two-stage topology is the converter series connection that causes a reduction of the overall efficiency. Both converters must present a very high efficiency in order to maintain an adequate efficiency for satellite communication application.

The second solution proposed for the implementation of the TWTA power circuit is a single-stage converter. The isolated dc-dc converter operates with a variable operation point (non-optimum) due to the regulation action of the converter. Thus, the single stage topology must present all suitable operation characteristics for high-voltage applications described in session II and maintain a high efficiency in all range of the input voltage variation.

A. Proposed Circuit

For the implementation of a competitive high-voltage isolated dc-dc converter, a single-stage high-efficiency topology is proposed and presented in Fig.11. The proposed topology is based on the current-fed push-pull dc-dc converter operating with PWM modulation, active clamping and ZVS commutation [4].

Two main switches (S_{P1} and S_{P2}), two auxiliary clamping switches (S_{a1} and S_{a2}), a clamping capacitor C_G and a push-pull transformer compose the converter. The outputs are formed by full-bridge rectifiers and by filter capacitors.

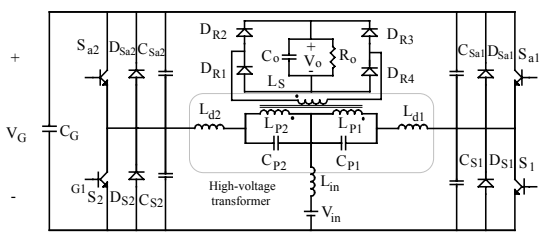

Fig.11. Proposed power circuit of the single-stage topology.

The anti-parallel diode and intrinsic capacitance of the MOSFET are used in the circuit operation. The current feeding is provided by the voltage source V_{in} in series with the input inductor L_{in}. The intrinsic parameters of the transformer are also presented in Fig.11.

B. *Principle of Operation*

Only the operation in continuous conduction mode and with the main switch duty ratio (D) higher than 0.5 is considered in the theoretical analysis (boost operation). The converter duty ratio (d) is defined by the period where both main switches are simultaneously conducting in the switching period.

The seven sequential circuit states that describes the principle of operation are presented below:

1) First Stage ([t_o, t_1] Fig.12).

Both main switches are conducting and the current flowing through the primary windings have the same absolute value and opposite direction. Thus, the rectifier diodes are blocking and the input inductor L_{in} stores energy. The resonance between the leakage inductance and parasitic capacitance of the transformer occurs during this stage but does not present influence in the operation of the converter.

2) Second Stage ([t_1, t_2] Fig.13).

At the instant t_1, switch S_2 is turned off at zero voltage, and the charge and discharge of the capacitors C_{S2} and C_{Sa2} occurs linearly with a constant current. When the currents in the primary windings become different, the power is transferred from the input source to the load. This stage finishes when $VC_{Sa2}(t)=0$.

3) Third Stage ([t_2, t_3] Fig.14).

The voltage across C_{Sa2} becomes zero and the diode D_{Sa2} conducted to the clamping capacitor the energy stored in the leakage inductance. During this stage, the switch S_{a2} must be gated on.

4) Fourth Stage ([t_3, t_4] Fig.15).

The current in i_{Ld2} inverts its direction and the clamping capacitors C_G returns to the converter, through S_{a2}, the energy received during the 3rd stage.

5) Fifth Stage ([t_4, t_5] Fig.16)

The auxiliary switch S_{a2} is turned off. The energy stored in the leakage inductance L_{d2} accomplishes the charge and discharge of the capacitor C_{S2} and C_{Sa2} in a resonant way. The voltage in the main switch decreases to zero.

6) Sixth Stage ([t_5, t_6] Fig.17)

When the capacitor C_{Sa2} reaches the clamping voltage V_G, the diode D_{S2} starts to conduct and the i_{Ld2} current decrease due to the output voltage referred to the primary side (V_{op}). The main switch S_2 must be enabled to conduct during the conduction of the diode D_{S2}.

7) Seventh Stage ([t_6, t_7] Fig.18)

The current inverts its direction flowing through S_2. When the currents in the primary windings become equal, the rectifier diodes are blocked, returning to the first operation stage.

The main theoretical waveforms are presented in Fig.19.

The active clamping allows the operation with soft-commutation in all switches until a minimum load where the energy stored in the leakage inductance is not enough for to accomplish the voltage transitions in the

commutation capacitor. The voltage across the blocking switch is limited to the clamping voltage.

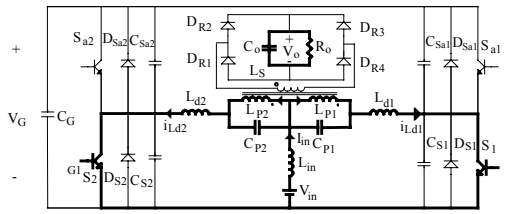

Fig.12. First operation stage (t_o, t_1).

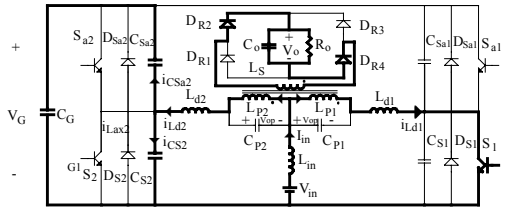

Fig.13. Second operation stage (t_1, t_2).

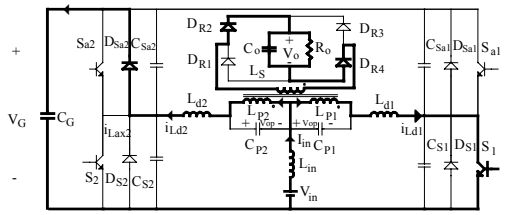

Fig.14. Third operation stage (t_2, t_3).

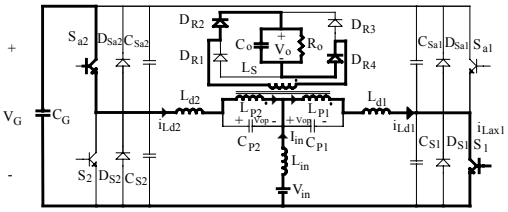

Fig.15. Fourth operation stage (t_3, t_4).

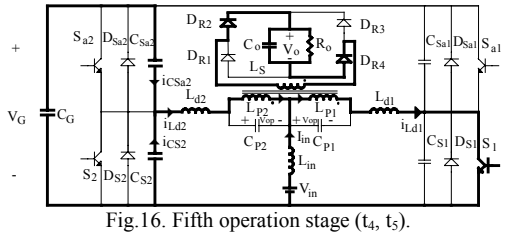

Fig.16. Fifth operation stage (t_4, t_5).

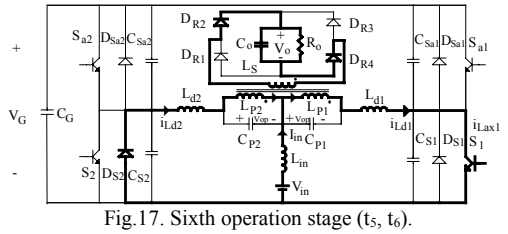

Fig.17. Sixth operation stage (t_5, t_6).

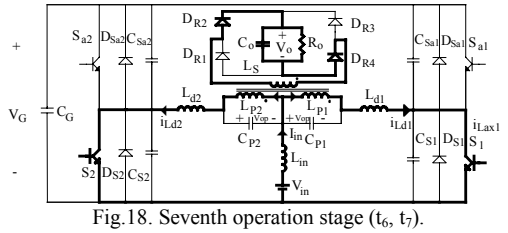

Fig.18. Seventh operation stage (t_6, t_7).

An important characteristic of this structure is to operate with main switch duty-ratio (D) higher than and lower than 0.5 (with overlapping and no overlapping). The auxiliary switches operate in a complementary way in relation the respective main switch. For a main switch duty-ratio lower than 0.5, the converter operates like a sepic dc-dc converter and with a step-down output characteristic. For the operation with a main switch duty-cycle higher than 0.5, the converter operates like an isolated boost converter with a step-up output characteristic. Therefore, this converter does not present inrush current for a progressive variation of the duty-cycle and support a large variation of the input voltage.

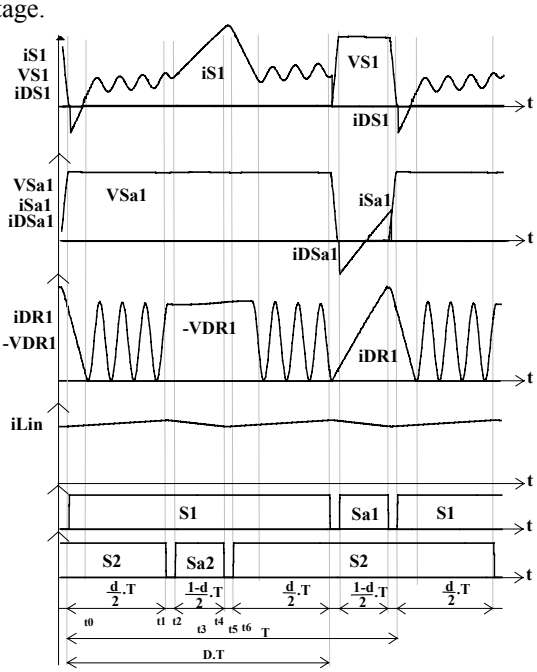

Fig.19. Main theoretical waveforms.

C. Main Mathematical Results and Simplified Design Procedure

A simplified design procedure is presented using the main equations obtained from the theoretical analysis of the proposed converter.

1) Specifications and parameters

The following specifications are considered in the design:

Input voltage:	V_{in}=26/44V
Total output voltage	V_o=3200V
Output power:	P_o=150W
Push-pull switching frequency	F_s=80kHz

The parameters of the implemented circuit are:

Magnetizing inductance:	L_m=85µH
Leakage inductance:	L_d=6µH
Winding capacitance:	C_p=8.75nF

2) Operation point of the Push-Pull converter

The output voltage referred to the primary side (V_{op}) adopted in the design is equal to 50V, considering the main switch duty-ratio higher than 0.5 and a step-up output characteristic.

The static gain, operating with the minimum and maximum input voltage are determined respectively by:

$$q_m = \frac{V_{op}}{Vin_{\min}} = \frac{50}{26} = 1.9231 \qquad (22)$$

$$q_x = \frac{V_{op}}{Vin_{\max}} = \frac{50}{44} = 1.1364 \quad (23)$$

The nominal input current operating with the minimum and maximum input voltage, considering the operation without losses are:

$$Iin_m = \frac{P_o}{Vin_{\min}} = 5.77A \quad (24)$$

$$Iin_x = \frac{P_o}{Vin_{\max}} = 3.41A \quad (25)$$

The parameter γ represents a reduction of the effective converter duty ratio due to the presence of the active clamping circuit. This characteristic is common in the most part of the ZVS-PWM converters. This parameter is proportional to the leakage inductance and output current. For the minimum and maximum input voltage results:

$$\gamma_m = \frac{Iin_m \cdot L_d \cdot F_s}{V_{op}} = 0.08308 \quad (26)$$

$$\gamma_x = \frac{Iin_x \cdot L_d \cdot F_s}{V_{op}} = 0.04909 \quad (27)$$

The nominal converter duty-ratio for the minimum and maximum input voltage are:

$$d_m = \frac{q_m + 2 \cdot \gamma_m - 1}{q_m} = 0.646 \quad (28)$$

$$d_x = \frac{q_x + 2 \cdot \gamma_x - 1}{q_x} = 0.218 \quad (29)$$

2) Voltage stress

The clamping voltage operating with nominal output power and minimum and maximum input voltage are:

$$V_{Gm} = Vin_{\min} \frac{2}{1 - d_m} = 147V \quad (30)$$

$$V_{Gx} = Vin_{\max} \frac{2}{1 - d_x} = 112.5V \quad (31)$$

When the converter operates without load, the clamping voltage is:

$$V_G = 2 \cdot V_{op} = 2 \cdot 50 = 100V \quad (32)$$

Thus, the clamping voltage change from 100V until 147V, and this is the maximum blocking voltage across the active switches.

3) Current stresses operating with the minimum input voltage

Main switch:

$$iSp_{RMS} = Iin_m \cdot \frac{\sqrt{6}}{12} \cdot \sqrt{15 \cdot \gamma_m + 13 - 7 \cdot d_m} = 3.672A \quad (33)$$

Auxiliary switch:

$$iSa_{RMS} = Iin_m \cdot \frac{\sqrt{3}}{12} \cdot \sqrt{1 - d_m} = 0.945A \quad (34)$$

4) Current stresses operating with the maximum input voltage

Main switch:

$$iSp_{RMS} = Iin_x \cdot \frac{\sqrt{6}}{12} \cdot \sqrt{15 \cdot \gamma_x + 13 - 7 \cdot d_x} = 2.432A \quad (35)$$

Auxiliary switch:

$$iSa_{RMS} = Iin_x \cdot \frac{\sqrt{3}}{12} \cdot \sqrt{1 - d_x} = 0.435A \quad (36)$$

5) Soft-commutation range

The auxiliary switches are turned-off when the energy is transferred from the clamping capacitors to the load and only the energy stored in the leakage inductance is available for the accomplishment of the charge and discharge of the commutation capacitors. Thus, the soft-commutation is maintained until a minimal input current where the energy stored in the leakage inductance is lower than the energy stored in the commutation capacitors. The auxiliary switch turn-off is considered as the critical commutation and defines the soft-commutation range of the converter.

Equation (37) allows the determination of the soft-commutation range.

$$\left(\frac{I_{in}}{2}\right) \geq \frac{\sqrt{4 \cdot V_{op}{}^2 - \left(V_G - 2 \cdot V_{op}\right)^2}}{Zn} \quad (37)$$

$$Zn = \sqrt{\frac{L_d}{C_S}} \quad (38)$$

$$L_d = L_{d1} + L_{d2} \quad (39)$$

$$C_S = C_{S2} + C_{Sa2} = C_{S1} + C_{Sa1} \quad (40)$$

6) Output voltage ripple

The parameterized output voltage ripple is variable with the static gain (q) and calculated by (41).

$$\overline{\Delta V} = \frac{2 \cdot \Delta V_{Co} \cdot C_o \cdot F_s}{I_o} = \frac{(2 \cdot q - 1)^2}{4 \cdot q^2} \quad (41)$$

Where:

I_o – Average current of each output

C_o – Filter capacitor

ΔV_{Co} – Output voltage ripple

C. Experimental Results

A laboratory prototype was implemented following an optimized design procedure developed and some waveforms obtained operating with the minimal input voltage and the nominal output power are presented. The details about the power circuit implemented are presented in Fig.20.

The main experimental results obtained operating with the minimum input voltage (26V) are presented in Figs.21 22 and 23. The main switch current and voltage waveforms are shown in Fig.21. The soft-commutation is obtained and the maximum switch voltage is equal the clamping voltage.

The auxiliary switch voltage and current waveforms are presented in Fig.22. The auxiliary switch also presents soft-commutation and the RMS current and the conduction losses are very low.

The maximum switch voltage is equal to 160V.

The voltage and current in a high-voltage rectifier diode is shown in Fig.23.

The efficiency curve operating with nominal output power and variable input voltage is presented in Fig.24. The lowest efficiency obtained with nominal output power is equal to 94.1%.

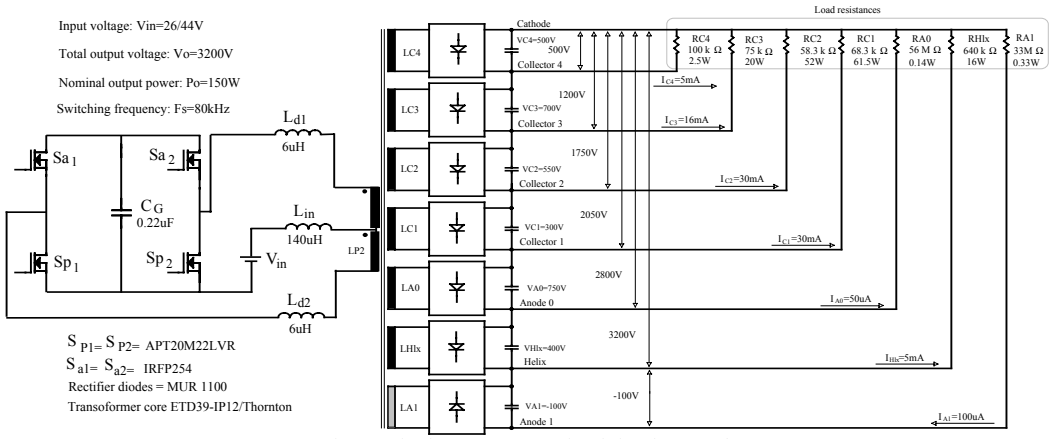

Fig.20. Single-stage power circuit implemented.

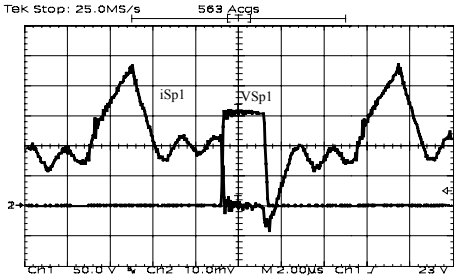

Fig.21. Main switch voltage and current operating with the minimum input voltage (50V/2A/2µs/div).

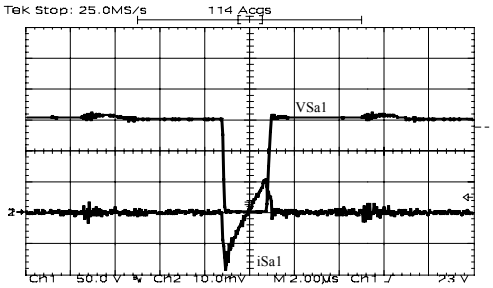

Fig.22. Auxiliary switch voltage and current operating with the minimum input voltage (50V/2A/2µs/div).

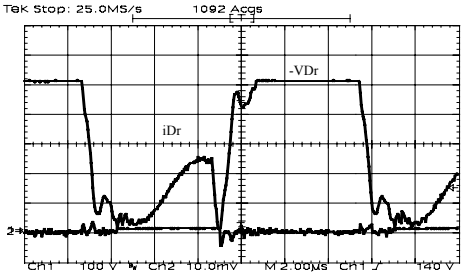

Fig.23. Rectifier diode voltage and current (100V/100mA/2µs/div).

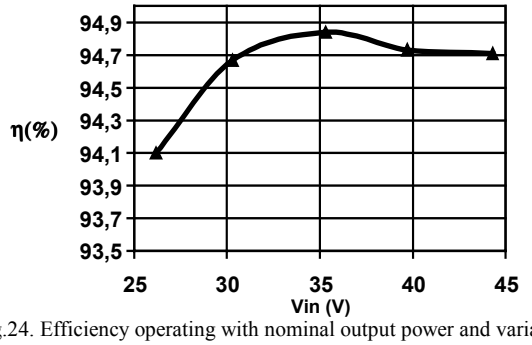

Fig.24. Efficiency operating with nominal output power and variable input voltage.

V. CONCLUSIONS

Two alternatives for the implementation of a high-efficiency isolated dc-dc converter with high-output voltage for TWTA application were proposed and studied. Both structures present several operation characteristics suitable for high output voltage applications supplied by an unregulated input voltage.

The operation characteristics were verified by the implementation of the laboratory prototypes operating with a variable input voltage (26V/44V) and with 3.2kV of total output voltage. The lowest efficiency obtained operating with the nominal output power is equal to 94.1% for the single-stage topology and equal to 93.4% for the two-stage topology.

The two-stage structure presents a output ripple 30% lower that the single-stage topology in its worst operation condition (lowest input voltage) for the same specifications. However, the single-stage topology proposed presents a lower mass and volume and higher efficiency than the two-stage topology studied.

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