Digital Implementation of Three-Phase Rectifier with Deadbeat Controller

Lourenço Matakas Jr., Alisson Dias Junqueira, Wilson Komatsu

Dept. of Electrical Energy and Automation Engineering - PEA
University of São Paulo - USP
Av. Prof. Luciano Gualberto, trav. 3, no. 158 – 05508-900 - São Paulo, SP – BRAZIL
Phone: +55 (11) 3818-5483 - Fax: +55 (11) 3818-5719 - e-mail: matakas@pea.usp.br

***Abstract* –A three-phase PWM rectifier with deadbeat controller is presented. Rectifier modeling and a DSP (Digital Signal Processor) based digital controller project are shown. Numerical simulations, as well as some experimental results, are also presented.**

I. INTRODUCTION

The growing use of non-linear loads in the electric power system (e.g. diode rectifiers) has increased concern with the quality of electrical energy. For low power, one-phase applications, the "full bridge diode rectifier + boost converter" topology has proved to be a good performance low cost solution [6]. For three-phase, lighter power applications, requiring bi-directional power flow, a three-phase, full bridge self commutated converter operating in PWM (pulse width modulation) mode is a convenient choice [7]. Typical applications include rectifiers for AC drives, telecommunication equipments, etc.

This digest presents a PWM three-phase rectifier with DSP (digital signal processor) control, which aims the reduction of reactive power and harmonics.

Section II describes the mathematical modeling of the VSC (voltage source converter). Section III presents the digital controller project, with the description of its main parts, the interconnection of current and voltage control loops, and the PLL (Phase Locked Loop) strategy. Numerical simulation results are presented in section IV, and preliminary experimental results in section V.

II. MODELING OF VSC

A. AC side

Fig. 1 shows VSC model and its connection to the mains (three wire system) through equivalent inductors (*L*). Terminal G_2, not present in the real converter, is used here in order to simplify the equivalent circuit modeling.

Fig. 2 introduces the simplified AC side model of the VSC. As:

$$v_r + v_s + v_t = 0, \quad (1)$$

and the equivalent voltages at converter's AC side:

$$\overline{v_{cr}} + \overline{v_{cs}} + \overline{v_{ct}} = 0, \quad (2)$$

G_1 and G_3 can be connected for modeling purposes.

Equation (3) can be obtained from Fig. 2:

$$\frac{d\mathbf{I}}{dt} = \frac{1}{L}\cdot\left(\mathbf{V} - \overline{\mathbf{V}_c}\right) = \frac{1}{L}\cdot\left(\mathbf{V} - \mathbf{B}\cdot\mathbf{V}_c\right) \quad (3)$$

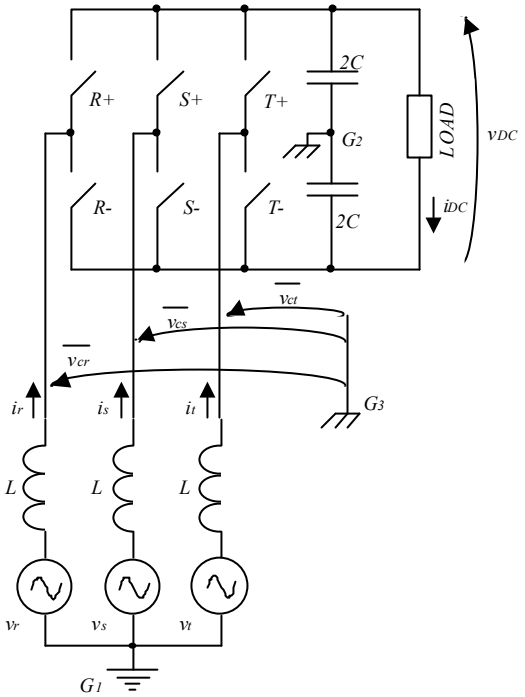

Fig. 1: Three-phase VSC model.

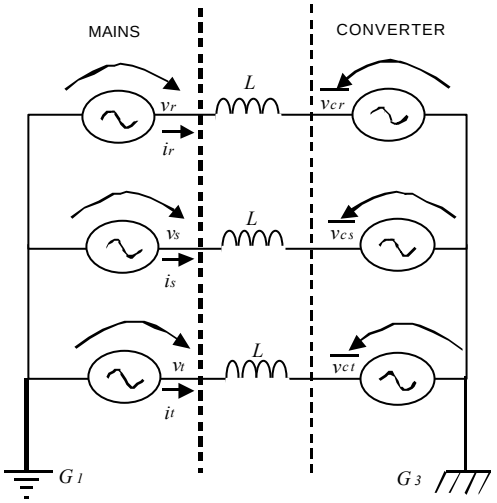

Fig. 2: Simplified AC side model.

Inside (3):

$$\mathbf{I} = \begin{bmatrix} i_r \\ i_s \\ i_t \end{bmatrix} \quad (3.1), \quad \mathbf{V} = \begin{bmatrix} v_r \\ v_s \\ v_t \end{bmatrix} \quad (3.2), \quad \overline{\mathbf{V}_c} = \begin{bmatrix} \overline{v_{cr}} \\ \overline{v_{cs}} \\ \overline{v_{ct}} \end{bmatrix} \quad (3.3), \quad \mathbf{V}_c = \begin{bmatrix} v_{cr} \\ v_{cs} \\ v_{ct} \end{bmatrix} \quad (3.4) \text{ and}$$

$$\mathbf{B} = \frac{1}{3}\cdot\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}. \quad (3.5)$$

As the converter output voltages v_{cr}, v_{cs}, v_{ct} can assume the values $-v_d$ and $+v_d$ (v_d is the voltage over each 2C capacitor drawn in Fig. 1), one can apply:

$$\mathbf{V}_c = \begin{bmatrix} v_{cr} \\ v_{cs} \\ v_{ct} \end{bmatrix} = \begin{bmatrix} m_r \\ m_s \\ m_t \end{bmatrix} \cdot v_d \qquad (3.6)$$

where the modulation index m is in the range $m_i = \pm 1$ (3.7), and

$$\mathbf{m} = \begin{bmatrix} m_r \\ m_s \\ m_t \end{bmatrix} \qquad (3.8)$$

Replacing in (3.6) at (3) one gets:

$$\frac{d\mathbf{I}}{dt} = \frac{1}{L} \cdot \left(\mathbf{V} - \mathbf{B} \cdot \mathbf{m} \cdot v_d \right) \qquad (4)$$

B. DC side

Fig. 3 presents the simplified model of VSC at the DC side. The PWM converter is represented by the PWM current sources $\frac{m_r}{2} \cdot i_r$, $\frac{m_s}{2} \cdot i_s$ and $\frac{m_t}{2} \cdot i_t$, and the DC load by a constant current i_{DC}. v_{DC} is the total DC voltage, thus

$$v_{DC} = 2v_D \qquad (4.1)$$

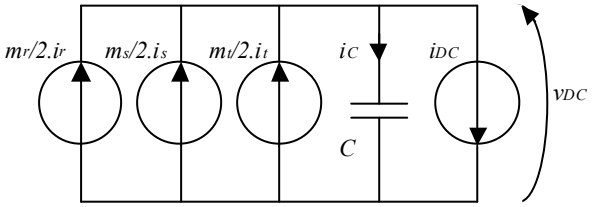

Fig. 3. Simplified model of VSC, at DC side.

Equation (5) can be written for Fig. 3 circuit:

$$\frac{dv_{DC}}{dt} = \frac{1}{C} i_C = \frac{1}{C} \left(\frac{m_r}{2} \cdot i_r + \frac{m_s}{2} \cdot i_s + \frac{m_t}{2} \cdot i_t - i_{DC} \right) =$$

$$= \frac{1}{C} \left(\frac{1}{2} \mathbf{I}^t \cdot \mathbf{m} - i_{DC} \right) \qquad (5)$$

III. CONTROL STRATEGY

A. General outline

The control strategy objective is to obtain converter AC side sinusoidal currents in phase with AC voltages (unitary power factor). DC side voltage is boosted above AC side peak voltage, and is regulated within controller limits.

For the AC side current tracking, a deadbeat control strategy was used. The DC side voltage control adopts a proportional-integral controller (PI). There are, thus, current and voltage control loops [1][2][4][5][6].

Fig. 4 schematically exhibits the previously described blocks, and also the PLL block, which generates reference sinusoidal signals $\overline{v_r}, \overline{v_s}, \overline{v_t}$ with unitary amplitude, synchronized with mains voltages v_r, v_s, v_t. With this method, the PWM and sampling pulses are synchronized with the mains [2].

B. Current loop

The AC current control strategy (deadbeat) is illustrated in Fig. 5 for a one phase case. The controller aim is to nullify the error in the $(k + 1)$ sampling instant, independent of the error in the previous k instant.

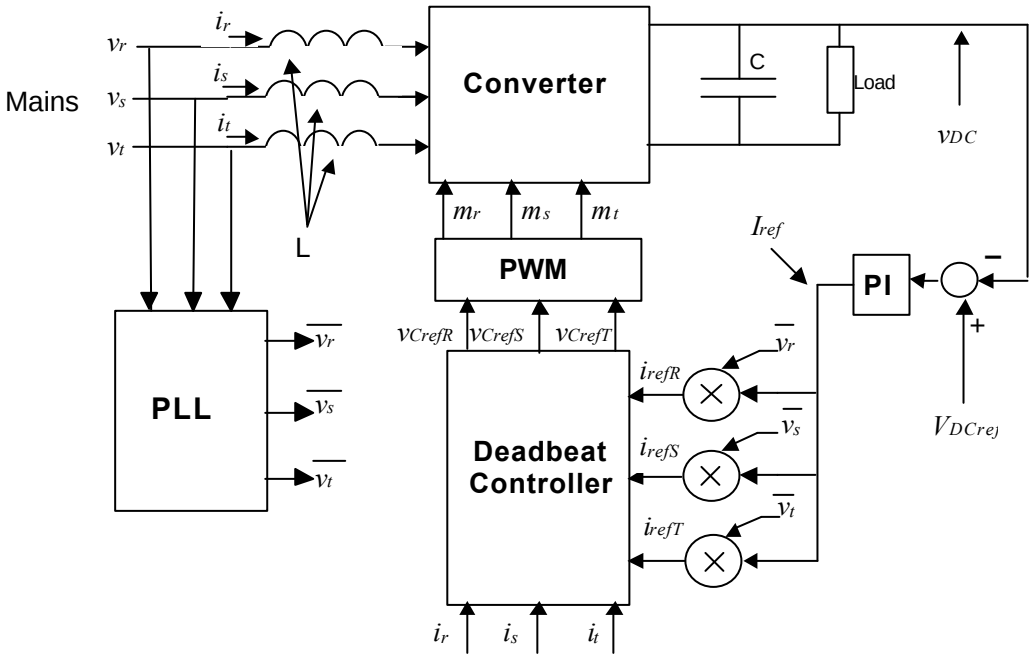

Fig. 4. Block diagram of system: converter and control blocks.

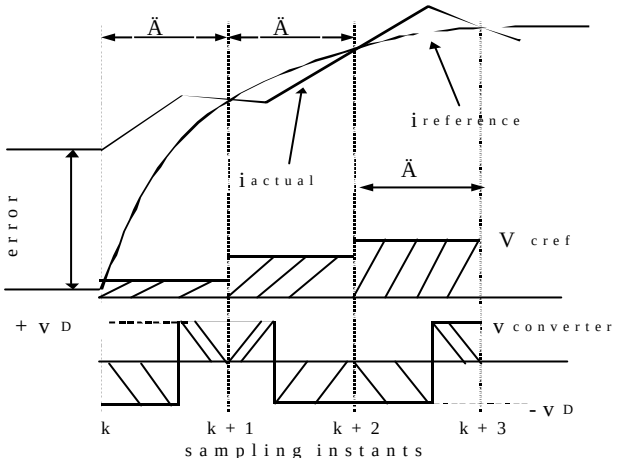

Fig. 5. Deadbeat behavior diagram.

In order to obtain the deadbeat behavior, it is necessary that $v_c(k)$ is imposed, resulting in

$$i(k+1) = i_{ref}(k+1) \tag{6}$$

For each one of the phases, one has:

$$\frac{di}{dt} = \frac{1}{L} \cdot \left(v - \overline{v_c}\right) \tag{7}$$

Integration of (7) results:

$$\int_{i(k)}^{i(k+1)} di = \frac{1}{L} \cdot \int_{t(k)}^{t(k+1)} (v - \overline{v_c}) dt \tag{8}$$

If mains voltage can be considered constant during the time interval Ä, the left side of (8) can be written:

$$i(k+1) - i(k) = \frac{1}{L} \cdot (v(k) \cdot \Delta - v_{cref}(k) \cdot \Delta) \tag{9}$$

Where Δ is the sampling period.

The imposition of (6) on (9) results:

$$i_{ref}(k+1) = i(k) + \frac{1}{L} \cdot (v(k) - v_{cref}) \cdot \Delta \tag{10}$$

From (10), v_{cref} can be written as:

$$v_{cref}(k) = -\frac{L}{\Delta} \cdot \left(i_{ref}(k+1) - i(k)\right) + v(k) \tag{11}$$

Thus, one has three reference voltages v_{CrefR}, v_{CrefS}, v_{CrefT} updated twice each switching cycle and applied to a PWM generator with asymmetric sampling.

C. DC voltage loop

The DC voltage control loop is implemented with the DC voltage feedback through a PI controller, which generates a reference current I_{ref}, multiplied by voltage references generated by PLL block ($\overline{v_r}$, $\overline{v_s}$, $\overline{v_t}$) providing the reference currents (i_{refr}, i_{refs}, i_{reft}) for the deadbeat controller. Thus, the DC voltage acts, indirectly, in the AC current amplitude (see Fig. 4).

D. PLL block

PLL block generates three sinusoidal references ($\overline{v_r}$, $\overline{v_s}$, $\overline{v_t}$) in phase with each one of the reference voltages v_r, v_s and v_t (measured at the AC side of the converter) [2]. PLL block also synchronizes the sampling and switching pulses and, together with the deadbeat controller, guarantees null phase displacement between current and voltage signals at the AC side.

Fig. 6 illustrates PLL operation at one phase.

Given a fixed number of sampling pulses per cycle of the mains voltage (PPC), PLL monitors zero crossing in the rise transition of AC voltage. At the beginning of each cycle it calculates the error, which is

$$error = |PPC - CA|, \tag{12}$$

where *CA* is the sampling pulse number counter (CA is reset each cycle). With this error information, the PLL recalculates the next sampling period width Ä that forces the next pulse with CA=0 to be coincident with a positive zero crossing of the mains voltage, ensuring synchronization.

IV. NUMERIC SIMULATION

The system was simulated using MATLAB. Following results show simulation with DC capacitor initially charged with nominal DC voltage and inductors with null current at initial instant.

Simulation values are:

- DC voltage: $v_{DC}=350(V)$
- DC load: $R=350(\Omega)$
- DC capacitor: $C=400(\mu F)$

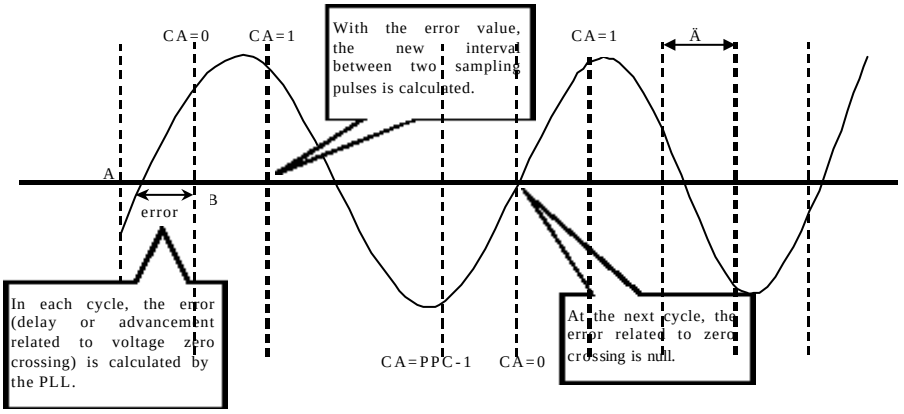

Fig. 6. PLL operation diagram.

- Line frequency: $f=60(Hz)$
- Line voltage: $v_{AC}=220(V)$
- PWM frequency: $f_{PWM}=6(kHz)$
- Line inductors: $L=165(mH)$
- Asymmetric sampling

Fig. 7 shows AC currents and Fig. 8 shows voltage and current at one of the AC phases (phase *r*).

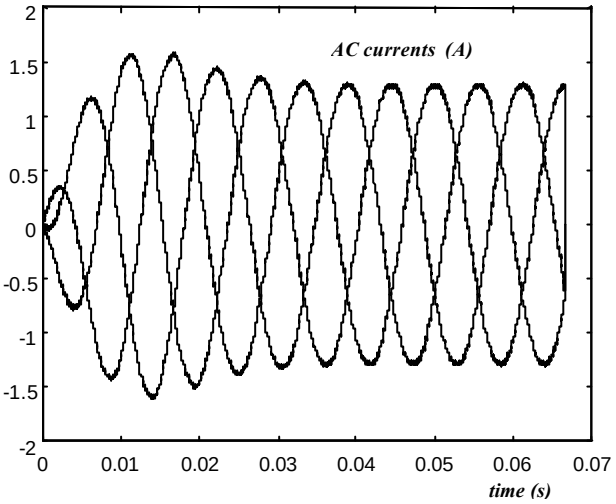

Fig. 7. Currents i_r, i_s and i_t , AC side (simulation).

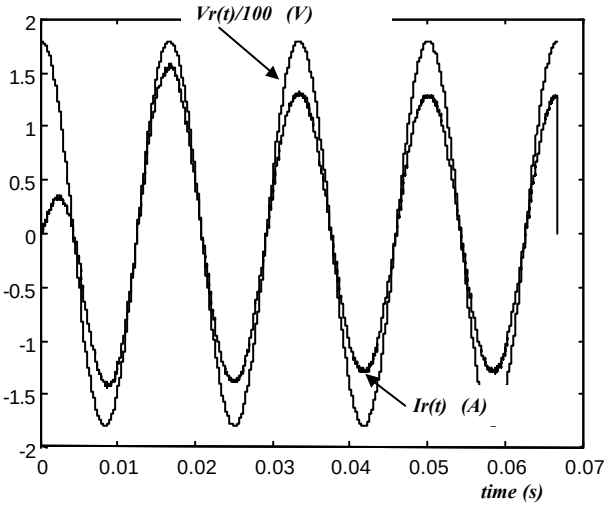

Fig. 8: Voltage (V/100) and current, phase r (simulation).

System behavior with plant disturbances was also simulated. Fig. 9 shows voltage and current waveforms at a phase, with the system subject to the disturbances. Fig. 10 shows the result of these same disturbances at the output DC voltage. Five perturbation stages can be distinguished: A. System is energized; B. 10% over voltage step at AC side; C. returns to the nominal voltage; D. DC load is removed (load rejection); and E. load is reintroduced.

Fig. 11 shows harmonic content for AC line current *ir(t)*. One can see harmonic components around hundred times AC frequency, which corresponds to switching frequency.

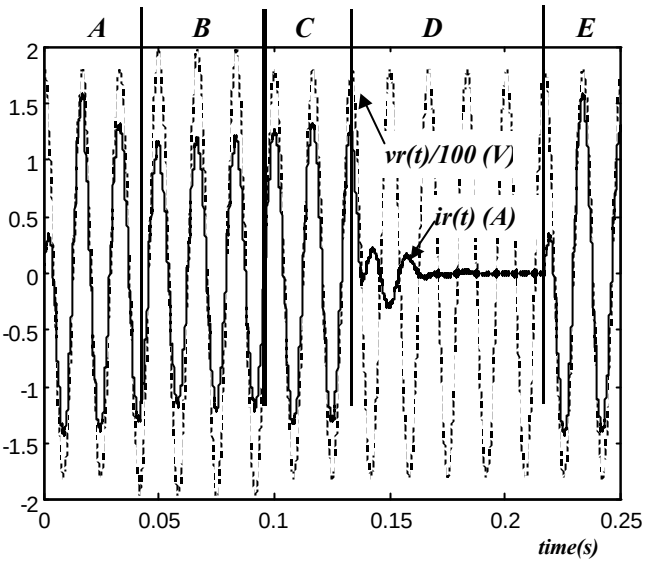

Fig. 9. Waveforms of voltage (V/100) and current in r phase, with disturbance (simulation).

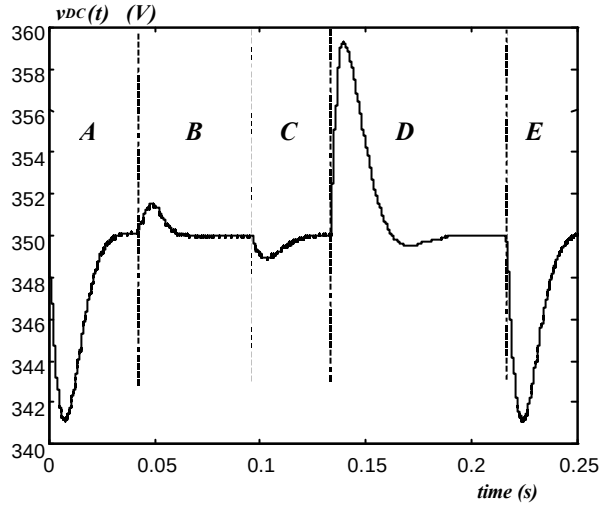

Fig. 10. Waveform of DC voltage in the output rectifier, with disturbance (simulation).

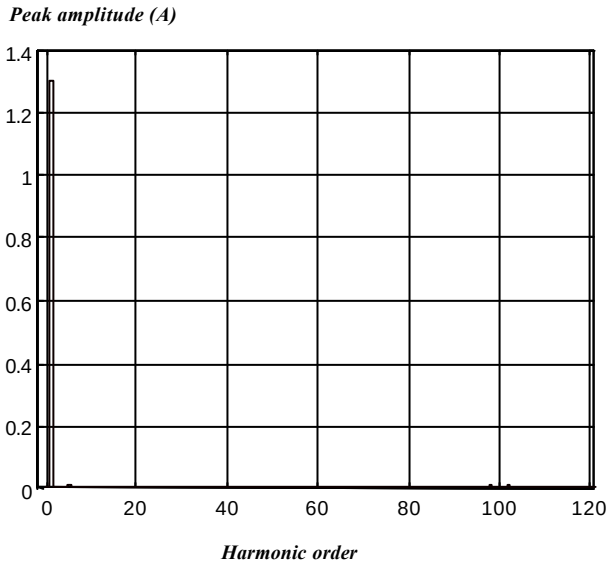

Fig.11: Harmonic content of current ir(t) (simulation).

V. EXPERIMENTAL SETUP

The control algorithm was implemented in a DSP (Analog Devices ADMC-401 [3], 16 bits, fixed point, 26MHz clock) which has some facilities for power electronics, as an internal three-phase PWM generator and analog to digital (A/D) and digital to analog (D/A) converters.

Two AC voltages and two AC line current are measured, allowing for the calculation of the third line voltage and line current. Measurements are done with Hall effect voltage and current sensors (LEM LV25-P and LA25-NP).

The three-phase bridge converter, "in-house" developed, employs MOSFET transistors (IRF 840) and IRF2110 drivers.

This section introduces some experimental results.

Experimental values are:

- DC voltage: $v_{DC}=350(V)$
- DC load: $R=400(\Omega)$
- DC capacitor: $C=400(\mu F)$
- Line frequency: $f=60(Hz)$
- Line voltage: $v_{AC}=220(V)$
- PWM frequency: $f_{PWM}=6(kHz)$
- Line inductors: $L=100(mH)$
- Symmetric sampling

The AC high frequency (switching frequency) filter is still absent.

Fig. 12 show DC voltage, AC line voltage and AC line current waveforms. One can observe AC voltage distortion due to relatively low line regulation at the point of common coupling, as well as high frequency noise due to the lack of AC filter. Fig. 13 shows AC line current alone.

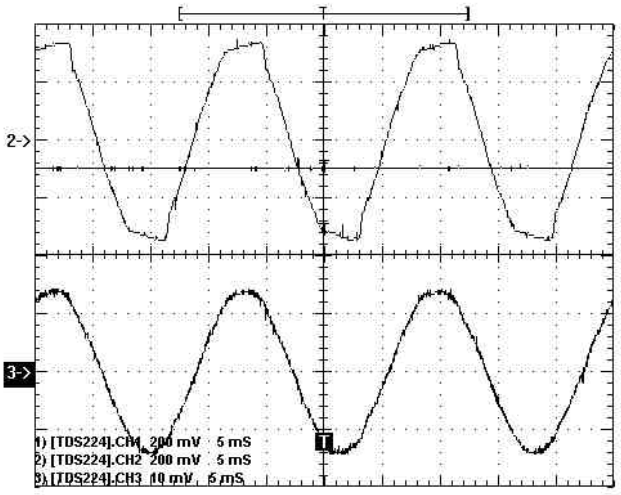

Fig. 12. Experimental waveforms of DC voltage (CH1) phase voltage (CH2) and line current (CH3). (Scales: CH1: 100V/div; CH2: 100 V/div; CH3: 1A/div).

DC load variation was done changing load from $R=490(\Omega)$ to $R=360(\Omega)$ and vice-versa (Figs. 14 and 15). Test conditions show negligible DC voltage variation with load (partial) insertion and (partial) rejection.

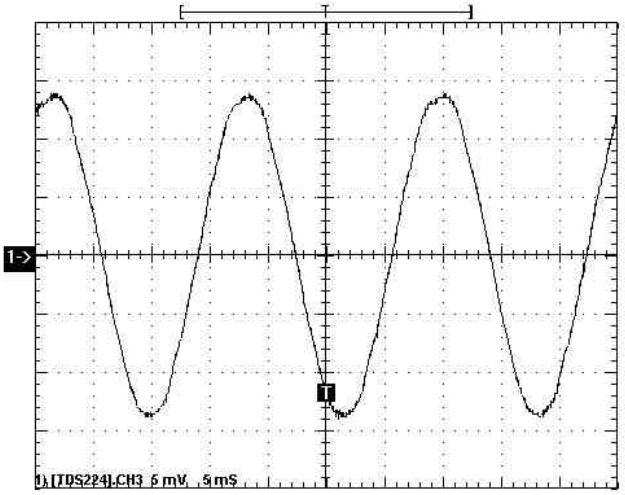

Fig. 13. Experimental waveform of AC line current (Scales: 1A/div).

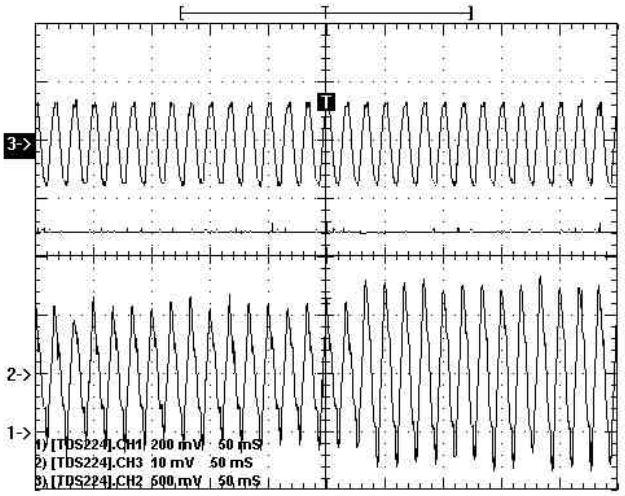

Fig. 14. Experimental waveforms of AC phase voltage (up), DC voltage (center) and line current (down), during a DC load insertion. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).

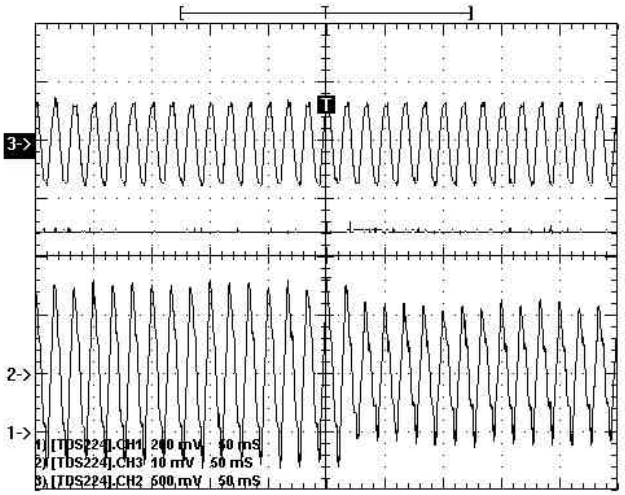

Fig. 15. Experimental waveforms of AC phase voltage (up), DC voltage (center) and line current (down), during a DC load partial rejection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).

Figs. 16 and 17 show complete DC load insertion and rejection (load value $R=400\ (\Omega)$). As figs. 14 and 15, it is difficult to see the effect on DC voltage variation. One can see that with no load current there is AC current, imposed by the voltage control loop in order to keep DC voltage constant, and to feed converter (low) losses.

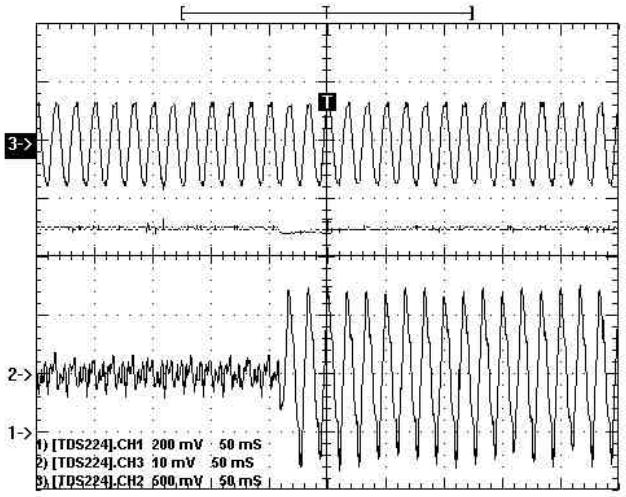

Fig. 16. Experimental waveforms of AC phase voltage (up), DC voltage (center) and line current (down), during a DC load connection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).

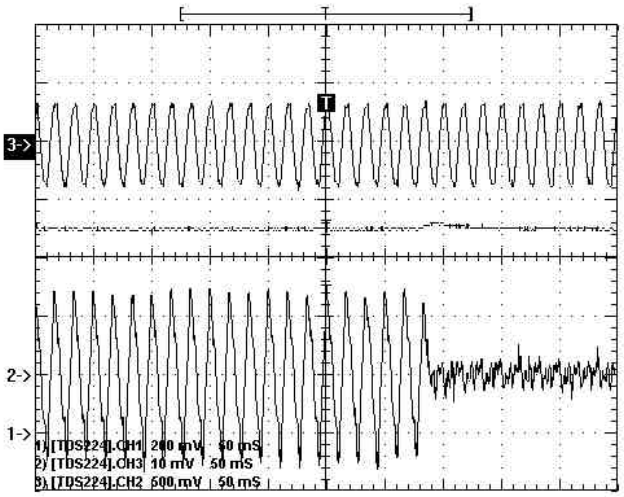

Fig. 17. Experimental waveforms of AC phase voltage (up), DC voltage (center) and line current (down), during a DC load connection. (Scales: up: 250V/div; center: 100 V/div; down: 1A/div).

VI. CONCLUSIONS

A three-phase PWM rectifier with deadbeat controller is presented. Rectifier modeling and DSP (Digital Signal Processor) digital controller project are shown. Numerical simulations, as well as some experimental results, are also presented.

VI. REFERENCES

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