A Novel Unity Power Factor Rectifier Based on the Boost Converter with the Three-State Switching Cell

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***Abstract.*- This paper presents a novel high efficiency single-phase PFC 3kW converter using a three-state switching cell operating in continuous conduction mode. The main advantages of this converter are low conduction and commutation losses and the frequency of the reactive elements is twice of the switching frequency. Due to these features, the proposed converter presents reduced input and DC-link current ripple, smaller inductor and output filter capacitor, low weight and reduced volume. The converter is suitable for high power applications (>1.5 kW) as pre-regulator stage. Theoretical analysis and experimental results demonstrate the feasibility of the proposed rectifier.**

I. INTRODUCTION

The increasing diversity of possible applications and the continuous demand for smaller, lighter and more efficient power converters have spurred the interest in fundamental topological properties of PWM networks and the constructions of new converter topologies. In a search for other configurations, elementary converters were modified by various circuit manipulation techniques [1].

A new family of DC-DC converter topologies with three-state switching cell converters was proposed [2]. In this work, it was chosen one DC-DC boost topology to apply in power factor correction. Thus, the input DC source was replaced by input AC source followed by full-bridge diodes. The proposed converter presents the following advantages: capable to operate with high power; high efficiency in hard switching, reduced input and output current ripples; smaller input inductor and output capacitor; low weight and reduced volume. Hence, this converter is suitable for commercial and industrial applications, specially where pre-regulator stages are required.

The topological circuit and operation principle of the converter is **different** from the interleaving boost converter [4]; with the proposed structure a percentage of the power is transferred to the load via magnetic coupling (transformer T) without circulating trough the switches.

II. PROPOSED POWER CIRCUIT AND PRINCIPLE OF OPERATION IN POWER FACTOR CORRECTION

The proposed three-state switching cell boost converter and its control strategy is illustrated in Fig. 1. The circuit is composed of a single-phase AC input voltage (Vin), full wave diode rectifier (DR), inductor (L), transformer (T), two main switches (S1, S2), two diodes (D1, D2), output filter (Co), and load (Ro). The control technique applied to the circuit is average current mode control [3], using the inductor current as control parameter. The input current is sampled through a current sensor and compared with I_{ref}, the error signal, Vc, is then sent to the PWM comparator, where the command signals for the main switches are generated. The topological circuit and operation principle of this is converter is different from the interleaving boost converter; with the proposed structure a percentage of the power is transferred to the load via magnetic coupling (transformer T) without being processing in the switches.

Each half cycle of AC mains, the converter presents two different operation modes as can be observed in Fig. 2. Initially, when the rectified input voltage is lower than half output voltage ($Vin < \frac{Vo}{2}$), switches S1 and S2 operate in **Overlapping Mode** with duty cycle greater than 0.5. Later, when that voltage becomes greater than ($Vin > \frac{Vo}{2}$), switches operate in **Non-Overlapping Mode** with duty cycle lower than 0.5.

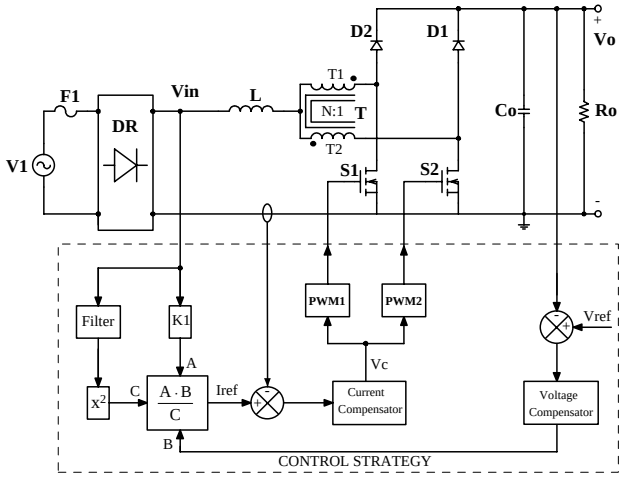


Fig. 1 - Proposed boost converter in PFC.

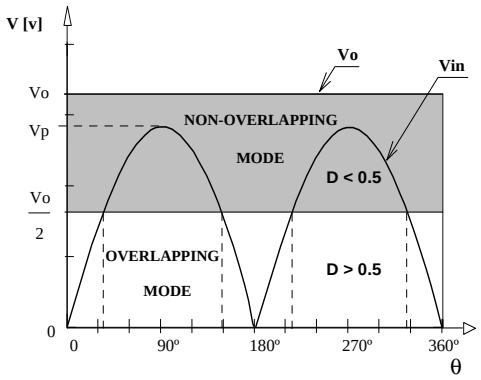


Fig. 2 - Two different operation modes.

A. *Analysis In Non-Overlapping Mode (D < 0.5)*

1) Principle of Operation

Stage 1 ($t_0<t<t_1$): at instant $t=t_0$, switch S1 is turned on and switch S2 is turned off. Since the turns ratio of both central tap transformer windings are the same, current I1 is equally divided between these windings. Half of the current flows through diode D2 to the load and half flows through switch S1. In this stage, current I1 grows linearly and energy is stored in L. The voltages across the transformer windings T1 and T2 are half of the output voltage Vo. The current paths can be seen in Fig 3a.

Stage 2 ($t_1<t<t_2$): at instant $t=t_1$, switch S1 is turned off, while switch S2 remains in off state. Diodes D1 and D2 are directly biased. In this stage, energy from the voltage source V1 and energy stored in inductor L are transferred to the load through T1, T2, D1 and D2. The voltage across the transformer windings is zero since their currents are equal with opposite directions. The current paths are shown in Fig. 3b.

Stage 3 ($t_2<t<t_3$): due to topological symmetry of the circuit, this stage is similar to the first stage (Fig. 3c).

Stage 4 ($t_3<t<T$): This stage similar to the second stage (Fig. 3d).

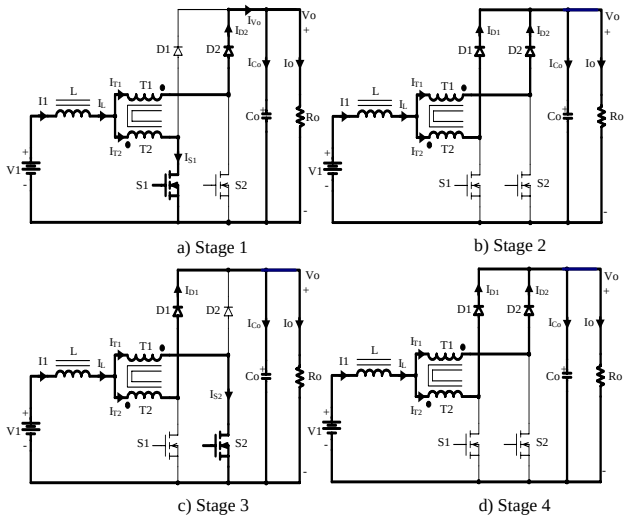


Fig. 2 – Operation stages in non-overlapping mode.

2) Ideal waveforms

The ideal waveforms are shown in Fig. 4.

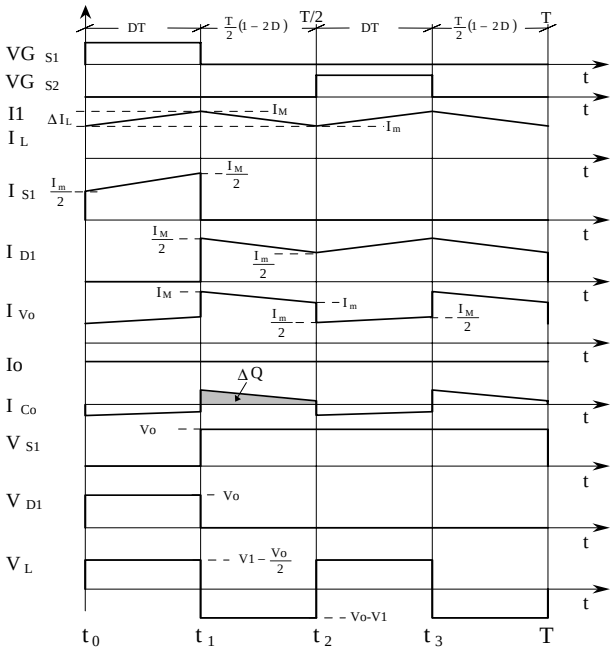


Fig. 4 - Boost converter waveforms in non-overlapping mode.

3) Voltage Gain

The ideal gain is illustrated trough expression (1) and plotted in Fig. 5.

$$G = \frac{V_0}{V_1} = \frac{1}{1-D} \qquad (1)$$

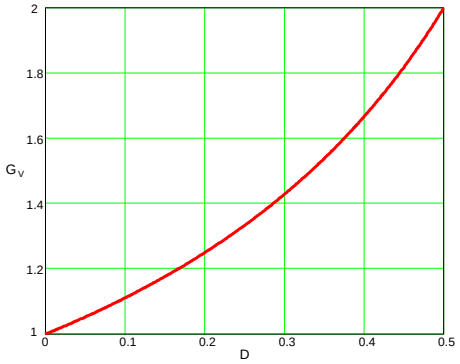


Fig. 5 – Ideal voltage gain as a function of D in non-overlapping mode.

B. *Analysis In Overlapping Mode (D > 0.5)*

1) Principle of Operation

Stage 1 ($t_0<t<t_1$): - At instant $t = t_0$, when S1 is turned on, S2 is still in conduction state. D1 and D2 remain reverse biased. Since the magnetic fluxes of each winding of the transformer are in opposite directions, this transformer is short-circuited. As a result, V_{in} is applied across inductor L. In brief, this is an energy storage stage. The current paths are shown in Fig. 6a.

Stage 2 ($t_1<t<t_2$): at instant $t=t_1$, switch S2 is turned off, while switch S1 remains in conduction state. Since the turns ratio of both central tap transformer windings are the

same, current I1 is equally divided through these windings. Half of the current flows through diode D2 to the load and other half flows through switch S1. Diode D1 remains reverse biased. In steady state, inductor L delivers to the load all the energy it stored during the previous stage. The current paths are shown in Fig. 6b.

Stage 3 (t_2<t<t_3): due to topological symmetry of the circuit, this stage is similar to the first stage (Fig. 6c).

Stage 4 (t_3<t<T): This stage similar to the second stage (Fig. 6d).

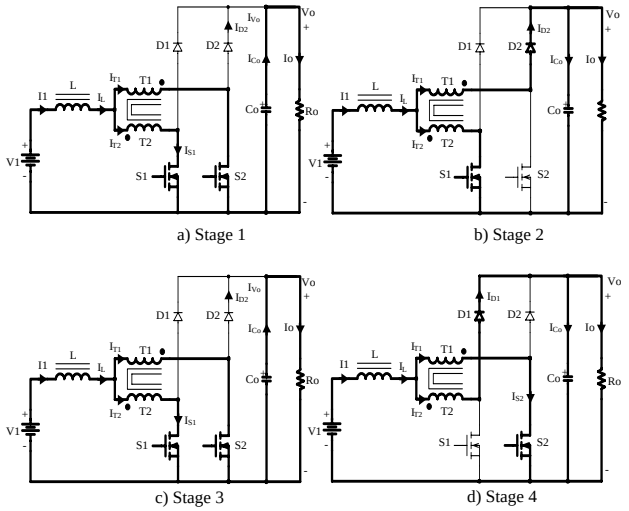


Fig. 6 – Operation stages in overlapping mode.

2) Theoretical Waveforms

The ideal waveforms for overlapping mode are shown in Fig. 7.

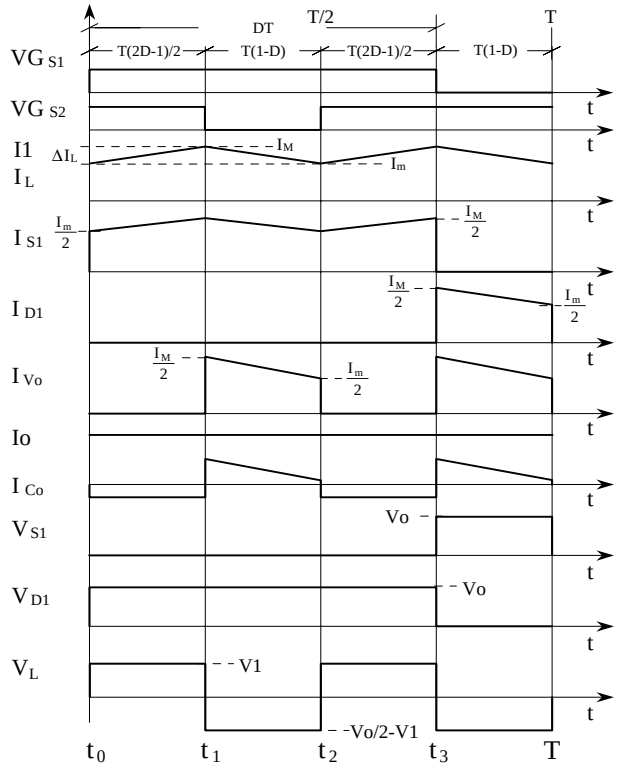


Fig. 7 - Boost converter waveforms in overlapping mode.

3) Voltage Gain

The ideal gain is illustrated trough expression (2) and plotted in Fig. 8.

$$G = \frac{V_0}{V_1} = \frac{1}{1-D} \qquad (2)$$

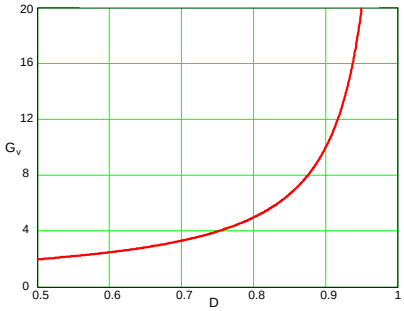


Fig. 8 – Ideal voltage gain as a function of D in overlapping mode.

C. Static Gain and Output Characteristic

The ideal voltage-gain G_V as a function of the converter duty cycle D is shown Fig. 9. The ideal output characteristic of the converter is shown in Fig. 10, where the voltage gain is shown as a function of the load having the duty cycle as parameter. In Fig. 10 the discontinuous conduction mode is shown in region 1 whereas region 2 refers to the continuous conduction mode.

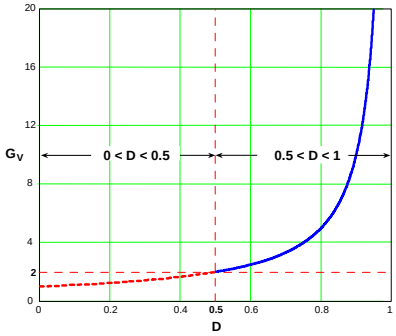


Fig. 9 – Static gain of the converter.

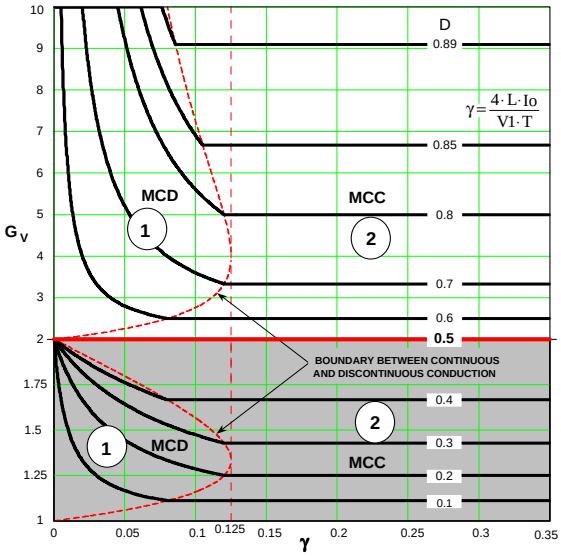


Fig. 10 – Output characteristic of the converter.

III. Modulation Technique

The modulation to obtain power factor correction of the converter is based on two sawtooth functions V_1 and V_2 phase-shifted one from another by 180º, but with constant frequency (Fs). These signals are the inputs to two different comparators that generate the command signals by comparing with the same control voltage V_C; details can be seen in Fig. 11. When control voltage V_C is lower or equal to $\frac{Vp}{2}$, (V_p is the peak value of V_1 and V_2), the converter switches operate in **Non-Overlapping** mode $\left(0 \le V_C \le \frac{Vp}{2}\right)$. When the control voltage V_C is greater or equal to $\frac{Vp}{2}$, the switches operate in **Overlapping** mode $\left(\frac{Vp}{2} \le V_C \le Vp\right)$.

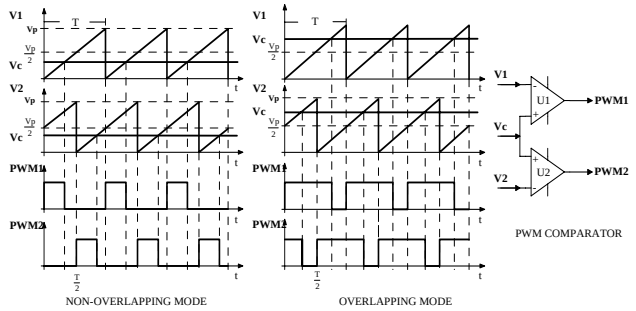
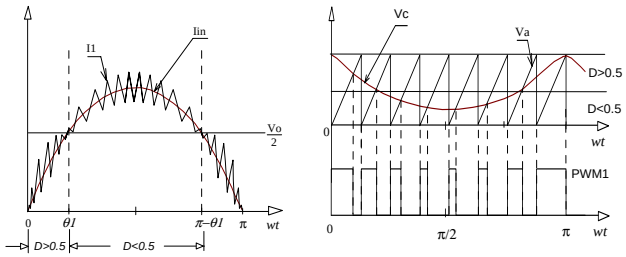


Fig. 11 - PWM modulation technique.

Fig. 12 shows the waveforms of input current and PWM modulation for mains half cycle.



a) b)

Fig. 12 - a) input current, b) PWM modulation for half cycle.

IV. Duty Cycle and Input Current Ripple

The duty cycle for AC-DC mode is defined by the expression (3) and is plotted in Fig. 13 for different values of the parameter α.

$$D(\theta) = 1 - \frac{|sen(\theta)|}{\alpha} \qquad (3)$$

Where α is the ratio of the DC output voltage to the peak AC input voltage:

$$\alpha = \frac{Vo}{Vp} \qquad (4)$$

The parameterized inductor ripple current for duty cycle lower and greater than 0.5 are defined by expressions (5) and (6) respectively. These currents are plotted in Fig. 14 for different values of the parameter α.

Duty cycle lower than 0.5.

$$\overline{\Delta I_L}(\theta) = \frac{\Delta I_L(\theta)\cdot L \cdot Fs}{Vo} = \frac{(2\cdot sen(\theta) - \alpha)\cdot(\alpha - sen(\theta))}{2\cdot\alpha^2} \qquad (5)$$

Duty cycle greater than 0.5.

$$\overline{\Delta I_L}(\theta) = \frac{\Delta I_L(\theta)\cdot L \cdot Fs}{Vo} = \frac{(\alpha - 2\cdot sen(\theta))\cdot sen(\theta)}{2\cdot\alpha^2} \qquad (6)$$

Where F_S is the switching frequency.

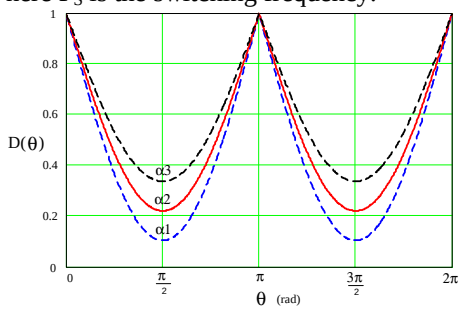


Fig. 13 – Duty cycle variation during one mains cycle.

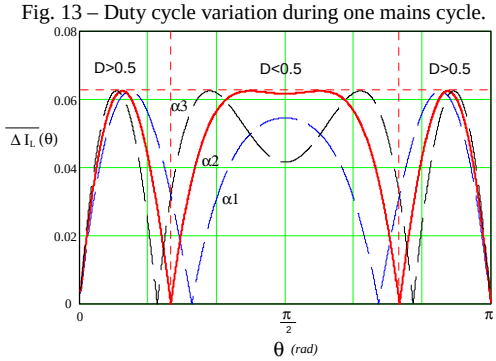


Fig. 14 Parameterized ripple current during a mains half cycle.

The maximum ripple current is given by the expression (7).

$$\Delta I_{L\,max} = \frac{Vo}{16\cdot L\cdot Fs} \qquad (7)$$

V. Design Procedure

The design procedure of the pre-regulator with high power factor and lower THD is presented in this section. Furthermore, average current mode control is applied to the three-states boost converter. The design is accomplished in base the proposed converter of Fig. 1.

A. *Specifications*

Input date:

Po = 3000W	output power;
V1 = 220V	rms input voltage;
Vo = 400V	output voltage.

For the design are adopted the following parameters:

Fs = 30kHz	switching frequency;
ΔIL = 4A	ripple current (20% of I1p);
ΔVo = 10V	output ripple voltage;
η = *97%*	efficiency;
$\alpha = \frac{Vo}{Vp} = 1.286$	parameter;

$$\theta 1 = \text{sen}^{-1}\left(\frac{\alpha}{2}\right) = 0.6982\,\text{rad}$$ transition angle between the two operation modes.

B. *Determination of passive components*

Inductor L:

$$L = \frac{Vo}{16 \cdot \Delta I_{L\,max} \cdot Fs} = 208.30\ \mu H$$

Capacitor C:

$$C \geq \frac{Po}{4 \cdot \pi \cdot F_r \cdot Vo \cdot \Delta Vo} = 994.7\,\mu F$$

C. *Voltage and current stress*

a) Inductor L

RMS current

$$Ir_{ef\,L} = \frac{\sqrt{2} \cdot \alpha \cdot Io}{\eta} = 14.06\,A$$

Peak current

$$I_{pL} = \frac{2 \cdot \alpha \cdot Io}{\eta} = 19.88\,A$$

b) Transformer

Voltage

$$V_{T1} = \frac{Vo}{2} = 200\,V$$

RMS current

$$I_{ef\,T1} = \frac{\sqrt{2} \cdot \alpha \cdot Io}{2 \cdot \eta} = 7.03\,A$$

Peak current

$$I_{pT1} = \frac{\alpha \cdot Io}{\eta} = 9.94\,A$$

c) Switches S1 and S2

Voltage

$$V_{S1} = 400\,V$$

RMS current

$$I_{efS1} = \frac{Io}{\eta} \cdot \sqrt{\frac{\alpha \cdot (3 \cdot \pi \cdot \alpha - 8)}{6 \cdot \pi}} = 4.10\,A$$

Peak current

$$I_{pS1} = \frac{\alpha \cdot Io}{\eta} = 9.94\,A$$

d) Diodes D1 and D2

Voltage

$$V_{D1} = Vo = 400\,V$$

Average current

$$I_{mD1} = \frac{Io}{2 \cdot \eta} = 3.87\,A$$

Peak current

$$I_{pD1} = \frac{\alpha \cdot Io}{\eta} = 9.94\,A$$

e) Bridge rectifier diodes

Voltage

$$V_{DR} = V_p = 311.12\,V$$

Average current

$$I_{mDR} = \frac{2 \cdot \alpha \cdot Io}{\pi \cdot \eta} = 6.33\,A$$

Peak current

$$I_{pDR} = \frac{2 \cdot \alpha \cdot Io}{\eta} = 19.89\,A$$

f) Capacitor C

Voltage

$$V_C = Vo = 40$$

Ripple current

$$\Delta I_C = I_p = \frac{2 \cdot \alpha \cdot Io}{\eta} = 19,89\,A$$

RMS current

$$I_{ef\,C} = \frac{Io}{\eta} \cdot \sqrt{\frac{16 \cdot \alpha + 12 \cdot \alpha^2 \cdot \text{sen}^{-1}\left(\frac{\alpha}{2}\right) + \alpha \cdot \sqrt{4 - \alpha^2} \cdot (16 - \alpha^2) - 6 \cdot \pi \cdot \alpha^2 - 9 \cdot \pi}{6}} = 3.21\,A$$

With those values calculated of voltage and current stresses the components of the converter are specified, as shown the Fig. 15.

VI. Experimental Results

In this section, experimental results obtained with the proposed boost converter circuit are presented. Aiming to verify the principle of operation as well as the control and the modulation technique a prototype was implemented, as shown in Fig. 15. Figs. 16 to 24 show the results obtained with the prototype.

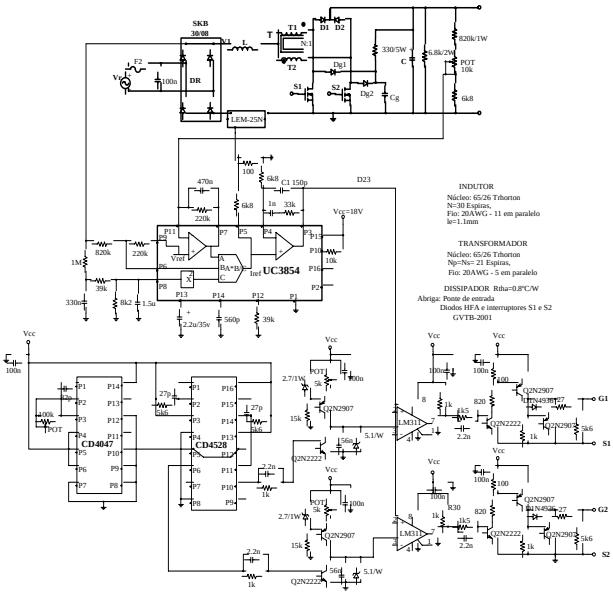


Fig. 15 – Circuit schematic of the implemented prototype.

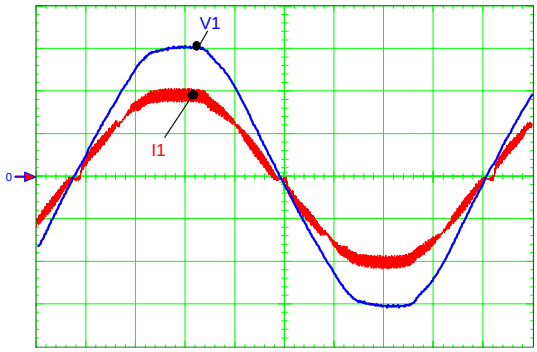


Fig. 16 – Input voltage and current.
Scale: V1 (100V/div.) I1 (10A/div.), time (2ms/div.)

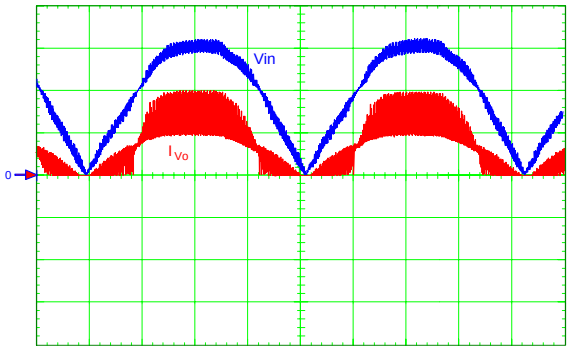


Fig. 17 – Voltage Vin and current before the filter capacitor C.
Scale: Vin (100V/div.) I_{Vo} (10A/div.), time (2ms/div.)

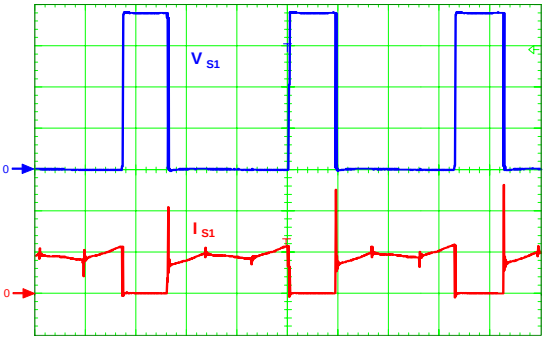


Fig. 18 – Voltage and current in S1 for duty cycle greater than 0.5.
Scale: V_{S1} (100V/div.) I_{S1} (5A/div.), time (10us/div.)

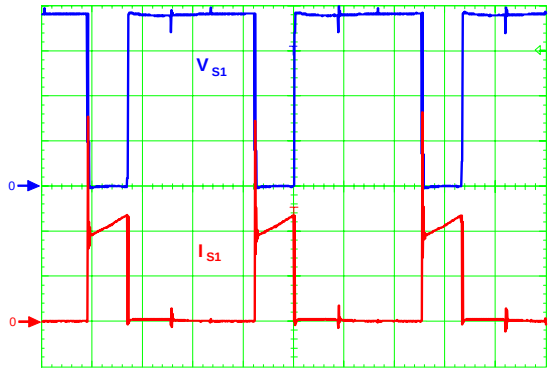


Fig. 19 – Voltage and current in S1 for duty cycle lower than 0.5.
Scale: V_{S1} (100V/div.) I_{S1} (5A/div.), time (10us/div.)

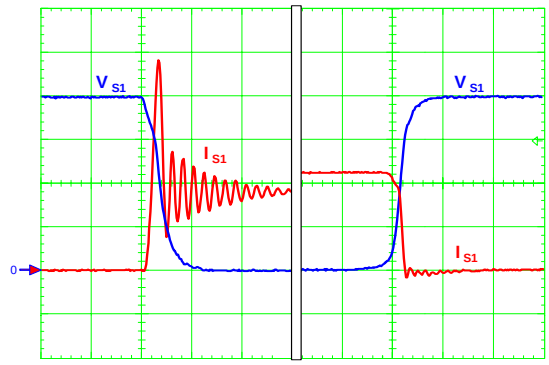


Fig. 20 – Details of the commutation of S1.
Scale: V_{S1} (100V/div.), I_{S1} (5A/div.), time (200ns/div.)

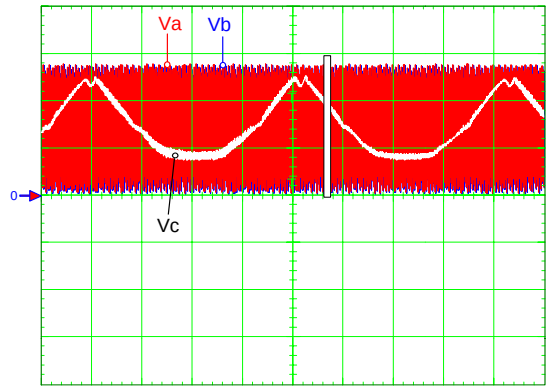


Fig. 21 – Saw-tooth carriers V1 and V2 and control voltage Vc
Scale: Va-Vb-Vc (2V/div.), time (2ms/div.)

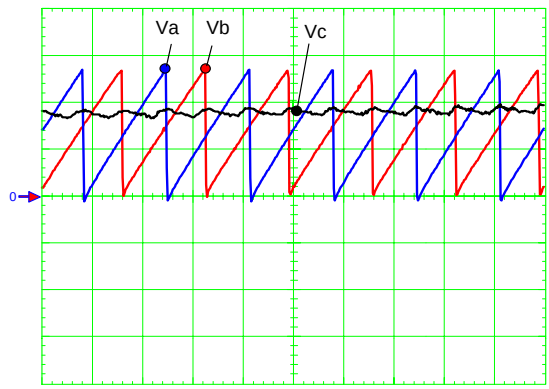


Fig. 22 – Details of the saw-tooth carriers Va and Vb and control voltage Vc
Scale: Va-Vb-Vc (2V/div.), time (20us/div.)

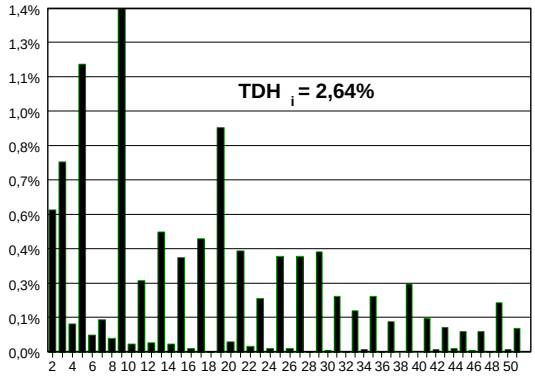


Fig. 23 – Input current harmonic analysis.

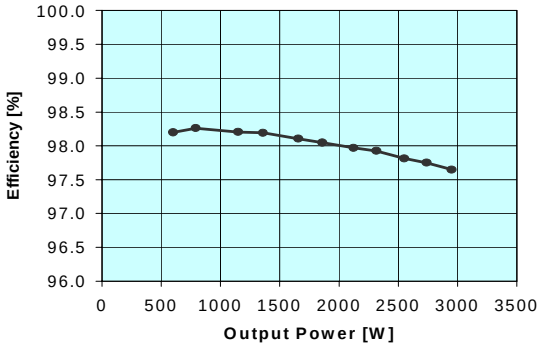


Fig. 24 – Efficiency of the proposed converter.

VII. Conclusion

From the study presented in this paper, we can draw the conclusions as follows.

The new boost converter behaves as predicted theoretically. It is suitable for commercial and industrial applications, where high power AC-DC conversion is required with power factor correction.

The proposed rectifier presented high efficiency, greater than 97.5 %, at full load. This high efficiency is obtained because only 50% of the power is processed in the switches, the reminder power is transferred to the load directly from magnetic coupling in T.

The proposed technique allowed high power factor operation (about 0.999) and low THD (lower than 2 %).

VIII. References

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[2] G. V. Torrico Bascopé, and Ivo Barbi, “Generation of a Family of Non-Isolated DC-DC PWM Converters Using New Three-State Switching Cells”, IEEE PESC, 2000 Record, pp. 858-863, June 2000 Galway, Ireland.

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[4] Po-Wa Lee, Yim-Shu Lee, David k. W. Cheng, and Xiu-Cheng Liu, “Steady-State Analysis of an Interleaved Boost Converter with Coupled Inductors,” IEEE Trans. Industrial Electronics, vol. 47, pp. 787-795, august 2000.