High Frequency AC Regulator for Non-linear Loads

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***Abstract* – This paper presents a new high frequency AC voltage regulator, to provide energy to linear and non-linear loads. The proposed regulator can also operate as an active filter, correcting the distortions from the input AC voltage and providing a low harmonic distortion AC output voltage. Principle of operation, theoretical analysis and simulation results are shown. Laboratory experimental results are also presented, which demonstrate the feasibility of the study carried.**

1 INTRODUCTION

The use of voltage regulators has been spreading in all of the areas that involve the use of electronic equipments, as residential, commercial or industrial areas. So, the national industry has been trying to fulfil this potential market with simple and reliable solutions.

There are several topologies, already dominated, available to industrial factoring. Basically, those topologies can be classified into two groups: Serials and Non-serials. The first ones [1], [2], [3] and [4] present the great advantage of processing only a percentage of the load power, acting in truth as a compensator. However, in most cases, they are not isolated. The second ones [5, 6] process the total load power and in most cases they are isolated. Trying to make the commutation better, topologies without dead time [7] and with soft switching [8, 9] were developed. The disadvantage of the last ones is the great number of active switches.

There is no known information regarding topologies that join simplicity, high efficiency and capability to provide energy to non-linear loads. Also, there is a lack of topologies that can operate simultaneously as a regulator and as an active filter.

This paper presents a new topology, that can provide energy to non-linear loads, isolate the load from the AC line voltage and act as an active filter using only two active switches and presenting high efficiency.

2 THE PROPOSED TOPOLOGY AND PRINCIPLE OF OPERATION

The topology presented in [1] and shown in Fig. 1, in its simplified form, has a good static gain, is isolated and allows to correct positive and negative variations of the input voltage. However, this topology, due to the presence of dead time, needs the use of snubbers, resulting in low efficiency. The topology presented in [7] and shown in Fig. 2, eliminates the dead time problem, solving the matter of high voltage across the components. However, this structure is not isolated and does not allow the increment of the output voltage.

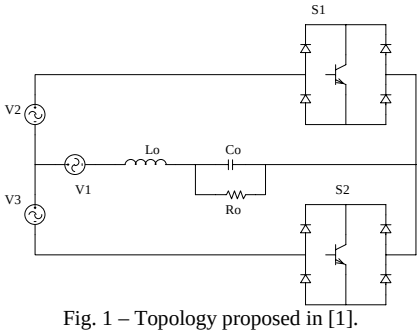

Fig. 1 – Topology proposed in [1].

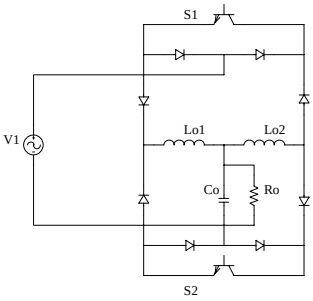

Fig. 2 – Topology proposed in [7].

In Fig. 3 the proposed topology is shown. In order to simplify the description of the operation stages, a simplified topology is adopted, as shown in Fig. 4.

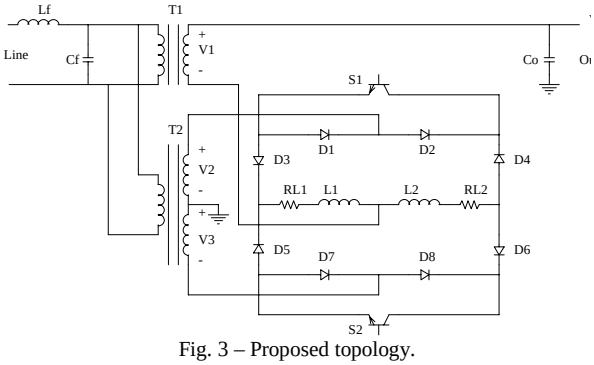

Fig. 3 – Proposed topology.

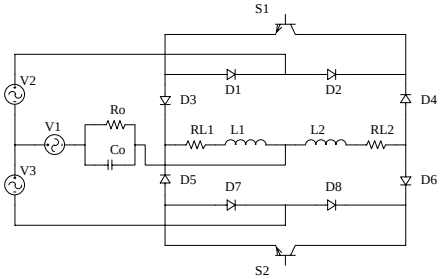

Fig. 4 – Proposed topology simplified.

The inductors L_1 and L_2, and the capacitor C_o, constitute the output filter. The resistances of the filtering inductor's windings are represented by R_{L1} and R_{L2}. The inductor L_f and the capacitor C_f form the input filter. The load is represented by R_o. Actually, this load is non-linear and is constituted by a rectifier with a capacitive filter.

In order to describe the operation of the circuit, it is assumed that:

- The power switches are ideal;
- During a switching period, the input and output voltages are considered constant, because the switching frequency (F_s) is considerably higher than the line frequency (F_r);
- The load is purely resistive.

The operation stages are as follows:

1st stage (t_0, t_1), (Fig. 5): S_1 is in ON state. The load current flows through V_1, V_2, D_2, S_1, D_3, R_{L1}, L_1 and $R_o//C_o$. The current i_{L2}, through inductor L_2, flows through L_2, R_{L2}, D_4, S_1, D_3, R_{L1} and L_1. During this stage energy is transferred from V_1 and V_2 to the load. This stage is finished at time t_1, when S_2 is commanded to turn-on.

2nd stage (t_1, t_2), (Fig. 6): This stage starts when S_2 is turned-on. The switches S_1 and S_2 are ON. The current through inductor L_1, i_{L1}, flows through V_1, V_2, D_2, S_1, D_3, R_{L1}, L_1 and $R_o//C_o$. The current through inductor L_2, i_{L2}, flows through L_2, R_{L2}, D_6, S_2, D_7, V_3, V_1 and $R_o//C_o$. The load receives energy from V_1, V_2 and V_3. This stage is finished when S_1 is ordered to turn-off, at time t_2.

3rd stage (t_2, t_3), (Fig. 7): At time t_2, when S_1 is switched-off, the third stage begins. The switch S_2 is in the ON state. The load current flows through V_1, V_3, D_8, S_2, D_5, R_{L1}, L_1 and $R_o//C_o$. The current i_{L2} flows through L_2, R_{L2}, D_6, S_2, D_5, R_{L1} and L_1. The load receives energy from V_1 and V_3. The voltage applied across the load is the difference between V_1 and V_3. This stage is finished at time t_3 when the switch S_1 is commanded to turn-on.

4th stage (t_3, t_4), (Fig. 8): The fourth state of operation begins when S_1 is turned-on, at time t_3. As in the second stage, S_1 and S_2 are ON. The current i_{L1}, through inductor L_1, flows through V_1, V_2, D_2, S_1, D_3, R_{L1}, L_1 and $R_o//C_o$. The current i_{L2}, of inductor L_2, flows through L_2, R_{L2}, D_6, S_2, D_7, V_3, V_1 and $R_o//C_o$. The load receives energy from V_1, V_2 and V_3. This stage is finished when the switch S_2 is commanded to turn-off, at time t_4.

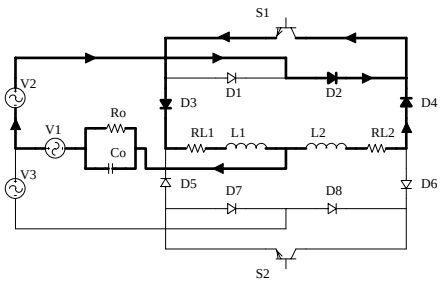

Fig. 5 – 1st stage.

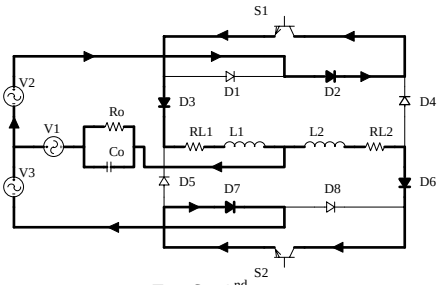

Fig. 6 – 2nd stage.

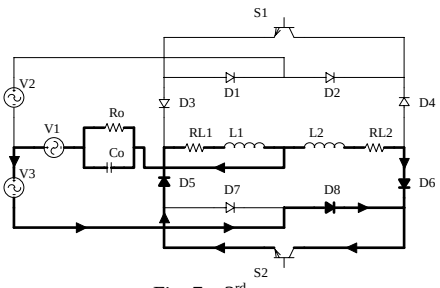

Fig. 7 – 3rd stage.

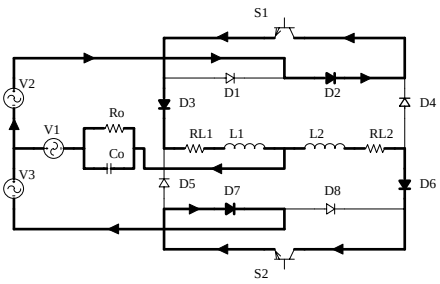

Fig. 8 – 4th stage.

The main idealized waveforms, for a switching period, considering the input voltage in its peak value, are shown in Fig. 9.

3 Analytical Study

The input voltages of the power stage are sinusoidal, obtained from the secondary windings of two transformers. The transformation ratios are n_1, for transformer T_1, and n_2 and n_3, for transformer T_2. The voltages V_1, V_2 and V_3 are given by expressions (1), (2) e (3), respectively. V_{in_p} is the voltage peak value of the AC line.

$$V_1(t) = n_1 \quad V_{in\_p} \quad \sin(\omega t) \qquad (1)$$

$$V_2(t) = n_2 \quad V_{in\_p} \quad \sin(\omega t) \qquad (2)$$

$$V_3(t) = n_3 \quad V_{in\_p} \quad \sin(\omega t) \qquad (3)$$

To determine the static gain of the power stage, it will be neglected the stages where both switches are ON, that means, the intervals Δt in Fig. 9. These intervals are very small, if compared with a switching period, so its influence in the static gain can be neglected.

The ON intervals of the switches S_1 and S_2 are given by expressions (4), (5) and (6).

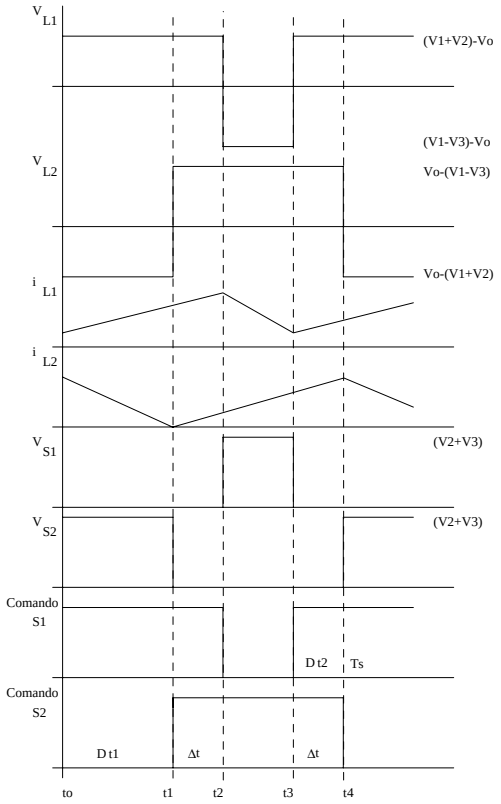

Fig. 9- Main waveforms for a switching period.

$$\Delta t = (t_2 - t_1) = (t_4 - t_3) \quad (4)$$

$$\Delta t_1 = t_1 - t_{0\cong}(t_1 - t_0) + 2\Delta t \quad (5)$$

$$\Delta t_2 = t_3 - t_{2\cong} T - \Delta t_1 \quad (6)$$

The static gain is given by expression (7) as a function of the voltages in the secondary side of transformers T_1 and T_2, and by expression (8) as a function of the input voltage and the transformation ratios of T_1 and T_2:

$$Vo = V_1 - V_3 + (V_2 + V_3)D \quad (7)$$

$$Vo = V_{in}\left[n_1 - n_3 + (n_2 + n_3)D\right] \quad (8)$$

The current ripple through inductors L_1 and L_2 is given by expressions (9) and (10), respectively:

$$\Delta i_{L1\max} = \frac{(V_1 + V_2) - V_o}{L_1 \quad F_s} D_{\max} \quad (9)$$

$$\Delta i_{L2\max} = \frac{V_o - (V_1 - V_3)}{L_2 \quad F_s}(1 - D_{\max}) \quad (10)$$

The expression that determines the voltage ripple over the capacitor C_o is given by (11):

$$\Delta V_{Co\max} = \frac{4}{\pi^3 \quad F_s{}^2 \quad C_o \quad L_o} \bullet \left[\begin{array}{l} V_o - (V_1 - V_3) + \\ (2V_1 + V_2 - V_3 - 2V_o)D_{\max} \end{array}\right] \quad (11)$$

The transfer function of the circuit, necessary to design the compensator, is given by expression (12), neglecting the series resistances of the output capacitors. V_s is the maximum value of the ramp voltage in the generation of the PWM command signals.

$$G(j\omega) = \frac{V_o(j\omega)}{V_C(j\omega)} = \frac{(V_2 + V_3)}{V_S} = \frac{1}{(j\omega)^2 \quad L_o \quad C_o + (j\omega) \quad \frac{L_o}{R_o} \quad +1} \quad (12)$$

A compensator, which diagram is shown in Fig. 10, is designed using the classical structure, normally used for Forward converters [10]. Another possibility, considering a sliding mode control was used [12, 13]. The corresponding diagram is shown in Fig. 11.

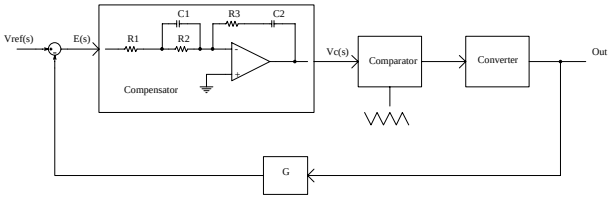

Fig. 10 - Conventional system control.

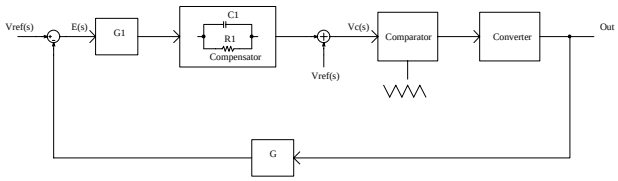

Fig. 11 - Sliding mode control.

4 SIMULATION RESULTS

In order to demonstrate the operation of the proposed topology and to validate the mathematical expressions previously presented, the circuit shown in Fig. 4 has been simulated, with closed loop operation and a PWM modulation. The used parameters values were:

$V_1(t) = 311V$ (Peak value);

$V_2(t) = 120V$ (Peak value);

$V_3(t) = 70V$ (Peak value);

$V_o = 311V$ (Peak value of the output voltage);

$n_1 = 1$ (Transformation ratio of T_1);

$n_2 = 0,386 \quad n_3 = 0,225$ (Transformation ratio of T_2);

$P_o = 1kW$ (Output power);

$L_1 = L_2 = 100\mu H$ (Filter inductors);

$R_{L1} = R_{L2} = 3,6m\Omega$ (Series resistance of the filter inductors);

$C_o = 100\mu F$ (Output capacitor);

$R_o = 10k\Omega$ (Output resistance, in parallel with a non linear load of 1 kW);

$F_r = 60\,Hz$ (Line frequency);

$F_s = 20\,kHz$ (Switching frequency);

$\Delta t = 500\,ns$ (Simultaneous conduction time of S_1 and S_2).

The transformation ratio of T_2 was obtained by simulation, as a function of the voltage drops on the circuit components, aiming to optimise the performance of the control circuit. The transformation ratio of T_1 is one, because the transformer T_1 is used only to isolate the load from de AC line.

In Fig. 12 the voltage across the switches are presented and it can be observed that they have a good behaviour, without voltage spikes.

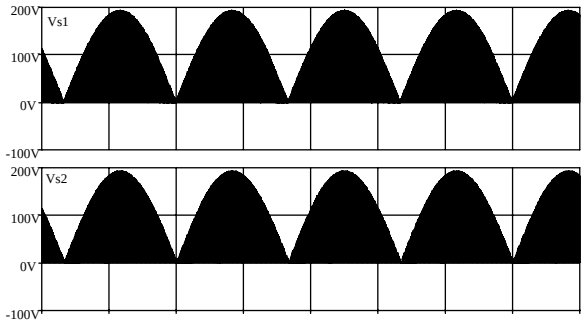

Fig. 12 – Voltage across switches S_1 and S_2.

In Fig. 13 the output voltage is shown with the converter operating at minimal, nominal and maximum input voltage. This simulation was done with linear load and a sliding mode controller. The output voltage has a good regulation when a variation of ± 20% of the input voltage is considered.

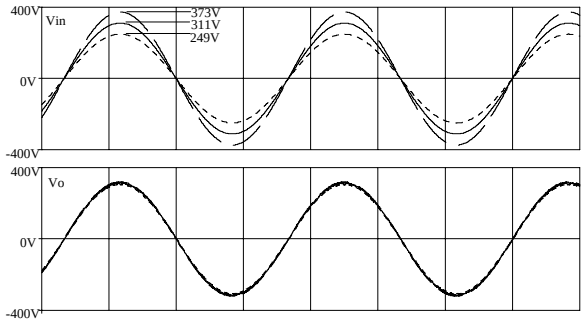

Fig. 13 – Output voltage for three different input voltages.

In Fig. 14 the output voltage is shown with the converter operating with distorted input voltage, that is, with high harmonic content. It can be verified that the converter as an active filter behaviour.

In Fig. 15 the converter's output voltage is shown with non linear load. In this case the input voltage is considered purely sinusoidal. It is also shown in Fig. 15 the controller's output voltage. It can be seen that the output voltage has a low harmonic content, with a waveform without overvoltages.

The non linear load's current is shown in Fig. 16.

In Fig. 17 the simulation results for non linear load with distorted input voltage are shown. It can be noted the good quality of the waveforms of output voltages, showing the good performance of this topology when operating as active filter an voltage regulator.

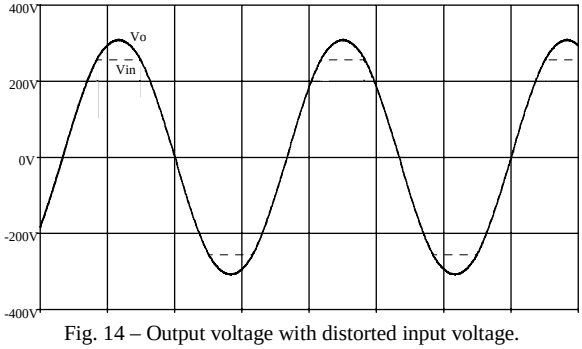

Fig. 14 – Output voltage with distorted input voltage.

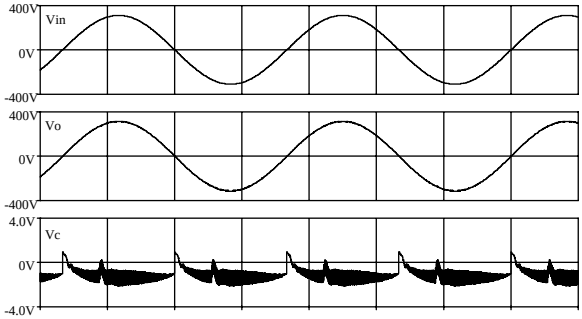

Fig. 15 – Output voltage for non linear load.

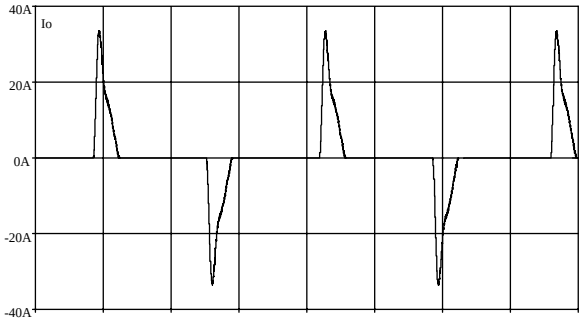

Fig. 16 – Current through non linear load.

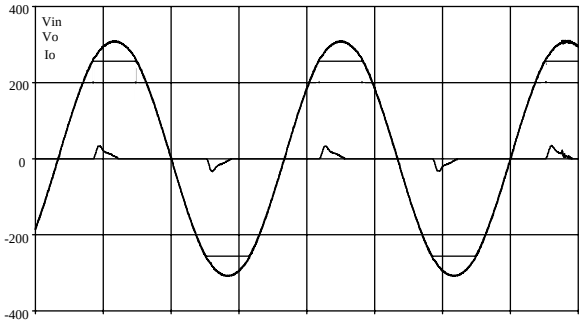

Fig. 17 – Output voltage for non linear load with distorted input voltage.

5 EXPERIMENTAL RESULTS

In order to verify experimentally the principle of operation, some tests were made on a 1 kW prototype providing energy to a linear and to a non linear load.

The power semiconductors used on the prototype were:

- S_1 and S_2 - IRG4PSC71U from IR;
- D_1 to D_8 - HFA30PA60C from IR.

To eliminate the influence of the leakage inductance of T_1 and T_2 a small RC clamper, in parallel with S_1 and S_2, was used. The other components are similar to those shown in Section four.

In Fig. 18 the voltage across the switches is presented and it can be observed that they have a good agreement with the simulation results. The current through the switch S_1 is also shown in Fig. 18.

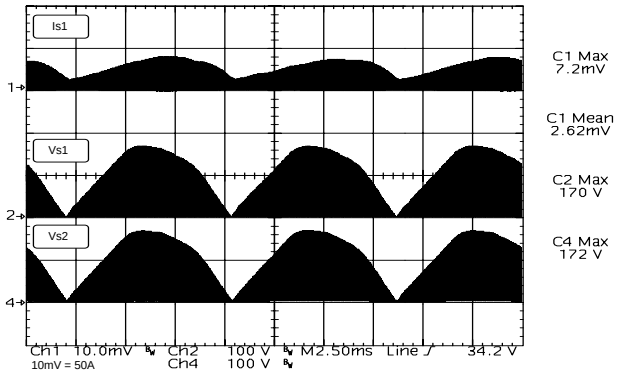

Fig. 18 – Voltage across switches S_1 and S_2 and current through the switch S_1.

In Fig. 19 the details of the voltages across switches S_1 and S_2 and the current through the switch S_1 are shown.

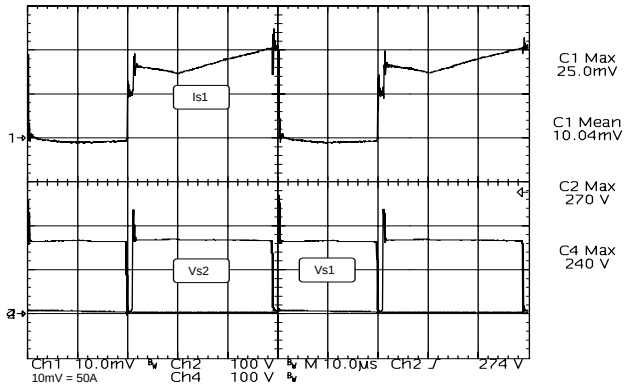

Fig. 19 – Detail of the voltage across switches S_1 and S_2 and current through the switch S_1.

In Fig. 20 the output voltage for a linear load is shown. The control system used in that test was a conventional PID compensator.

Fig. 21 shows the output voltage for linear load with sliding mode control. It can be observed that the output voltage has a good quality and small harmonic distortion. The voltage V_1 is the output voltage of the transformer T_1.

In Fig. 22 the output voltage for linear load and the AC line voltage are shown. The output voltage has a low harmonic content, showing that the converter acts as an active filter.

Fig. 23 shows the output voltage for non linear load with sliding mode control. The low quality of output voltage is caused by the leakage inductance of transformers T_1 and T_2. In order to obtain better quality of output voltage, those transformers (T_1 and T_2) must be built using techniques for reduction of leakage inductance and of windings resistances.

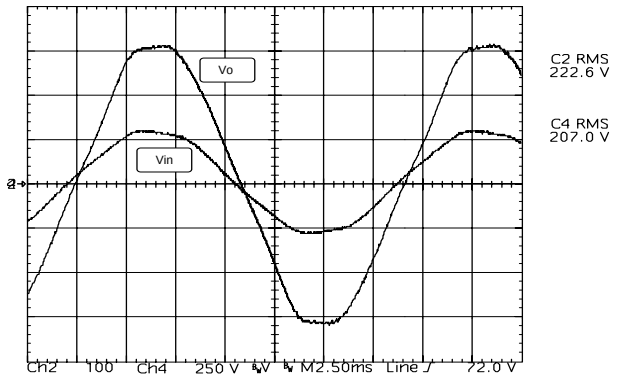

Fig. 20 – Output voltage for linear load with conventional control system.

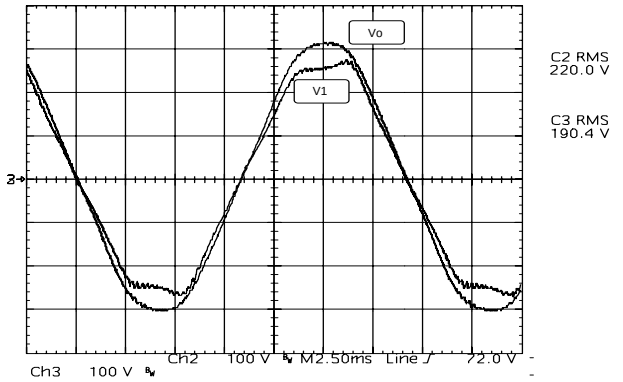

Fig. 21 – Output voltage for a linear load with sliding mode control.

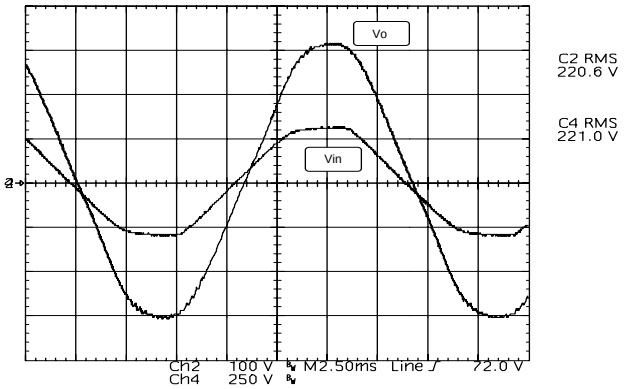

Fig. 22 – Output and AC line voltage for linear load.

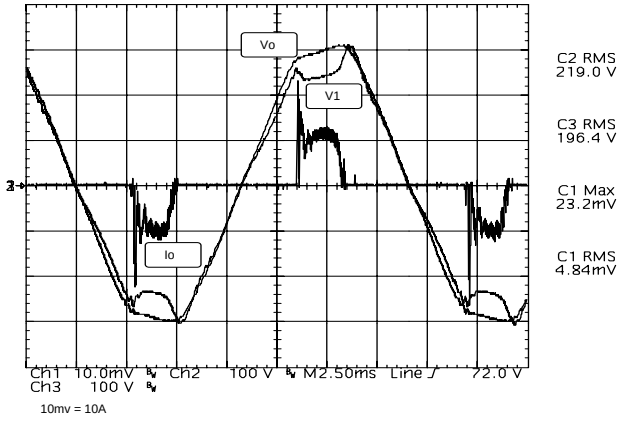

Fig. 23 – Output voltage for a non linear load with sliding mode control.

In Fig. 24 the harmonic spectrum of the output voltage for non linear load is shown. It can be observed that the results present a good accordance with the standard.

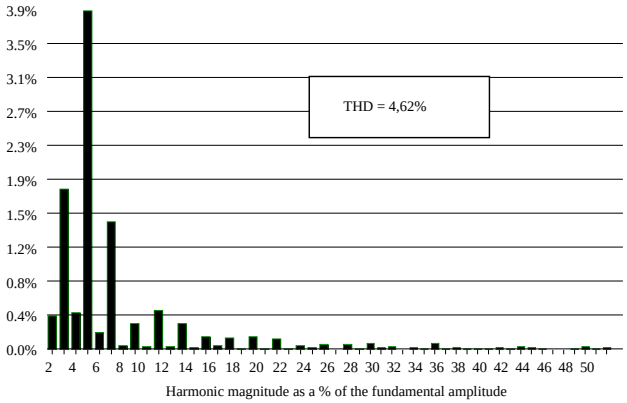

Fig. 24 – Harmonic content of output voltage.

6 CONCLUSIONS

In this paper a new AC voltage regulator was presented, operating at high frequency and providing energy to a linear and non-linear load. The proposed topology has performed an effective regulation of the output voltage. The harmonic distortion of the output voltage is very low (<5%). The proposed topology can also act as an active filter, compensating distortions in the input voltage.

Using the proposed converter to provide energy to linear loads, high efficiency can be obtained. However, in the case of non-linear loads this efficiency decreases significantly, because the increase of RMS current due to this load.

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