An Optimization Method to Minimize Switches Conduction Losses of DC-DC ZVS Full-Load-Range Converters

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***Abstract* - This paper presents an optimization method to minimize switches conduction losses of DC-DC converters operating with ZVS in the entire load. The converters considered have characteristics similar to well-known isolated ZVS full-bridge converter. The proposed method optimizes the values of series and parallel inductors, minimizing the conduction losses in the converter. Experimental results of a series converter and of a full-bridge converter, operating with 1.5 kW @ 100 kHz with isolated 60V/25A output are presented to demonstrate the feasibility of the proposed method.**

I. INTRODUCTION

In last decades much efforts have been made to increase the converters efficiency. This tendency can be observed in the large number of publications about soft commutation techniques, which allow converters efficiency improvement. In spite of these techniques produce efficiency improvement, the use of optimization methods can provide an extra improvement in the converter efficiency. Furthermore, optimization methods can be utilized to minimize conduction losses, minimize the converter volume, minimize the converter heating, etc.

The present work presents an optimization method to minimize switches conduction losses in isolated dc-dc ZVS converters. Basic procedures are demonstrated for the isolated ZVS full-bridge (ZVS-FB) dc-dc converter that is among the most utilized converters. The full-bridge converter can operate with ZVS in a wide-load-range due to the presence of the leakage and magnetizing inductances of the transformer [1,2,3]. Like the ZVS-FB converter, many others isolated dc-dc converters can operate with ZVS in a load-range, only making use of the transformer inductances [1,5,6,8,9].

The main drawback of this commutation technique is the increase of the conduction losses when ZVS in wide load range is required, penalizing the converter efficiency [1,2,3]. However, the designer can sacrifice the soft-commutation at light load to achieve higher efficiency at full load. Otherwise, the ZVS capability of these converters can be easily extended to full-load-range by the inclusion of an auxiliary circuit that performs ZVS with low load current. A simple way to implement this auxiliary circuit is the use of an auxiliary inductor as presented in [10,11].

The main procedure adopted to design the converters that utilize this approach consists in determine the minimum load (I_{crit}) in which series inductance perform ZVS and subsequently design the auxiliary inductor to perform ZVS from no load to I_{crit}.

The proposed optimization method allows obtaining the best values of series and parallel inductors to minimize switches conduction losses. The proposed method is applied to two dc-dc isolated converters: the ZVS Full-bridge converter and a converter composed of the series arrangement of two half-bridges controlled by pulse width modulation (PWM) [6]. The two converters are represented in Fig. 1 and 2 respectively.

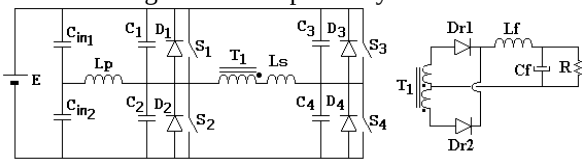

Fig. 1 – Improved full-load-range ZVS full-bridge converter.

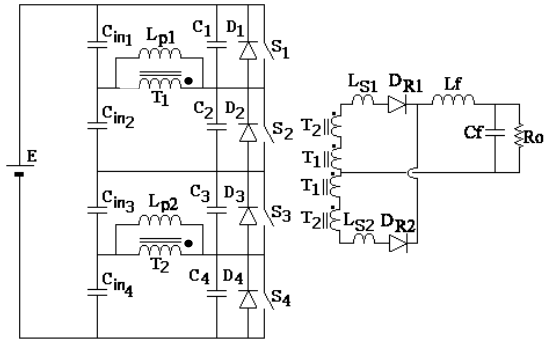

Fig. 2 - Improved full-load-range ZVS-PWM series converter.

II. THE ZVS IN DC-DC CONVERTERS

The ZVS full-bridge converter (ZVS-FB) dispenses detailed presentation, since it is among the most popular converters. However, some considerations about the series converter shown in Fig. 2 are necessary.

Two half-bridge converters share the input voltage at primary side and two auxiliary inductors, one in series and the other in parallel with each transformer allow ZVS in the full-load range. The series inductors L_{s1} and L_{s2} guarantee ZVS in a wide load range (like the ZVS-FB), however at light load, only these inductors do not assure ZVS [6]. This way, parallel inductors L_{p1} and L_{p2} are included to guarantee ZVS at light-load or even at no-load. It must be noticed that the series inductors (L_s) can be placed as in the secondary side (as shown in Fig. 2) as in the primary side, in series with each transformer.

Secondary windings of the T_1 and T_2 transformers are connected in series, therefore their output voltages add up. Two diodes D_{R1} and D_{R2} make the voltage rectification, and L_f and C_f form the second order output filter.

An important characteristic of this converter is connected to the use of PWM, being the voltage on input capacitors a function of the duty-cycle (D) as presented in (1) and (2).

$$V_{Cin1} = V_{Cin4} = \frac{E}{2}.D \quad (1)$$

$$V_{Cin2} = V_{Cin3} = \frac{E}{2}.(1-D) \quad (2)$$

Due to this fact, the peak currents (I_{Lpmax}) through parallel inductors are not linearly dependent of the duty-cycle, as in the ZVS-FB converter. Furthermore, the design of the parallel inductors (L_p) must be done considering the smallest duty-cycle, since in this case the parallel inductor has the smallest current to perform the ZVS. The relation I_{Lpmax} x D can be observed in Fig. 4.

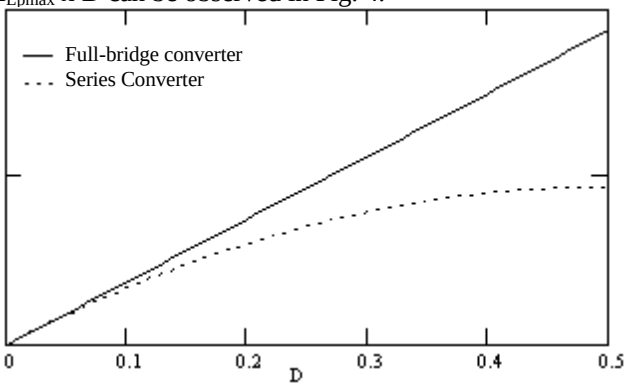

Fig. 3 – Parallel inductors peak current as a fuction of the duty-cycle

Operation stages of the series converter are similar to that presented in [6], with the main difference resulting from the addition of the parallel inductors. Therefore, only main switches commutations stages are analyzed here.

For both converters, the ZVS-FB and the series converter, the load current reflected to the primary side has the proper polarity to operate with ZVS for one commutation of each leg. In order to illustrate the above mentioned, Fig. 4 shows the commutation from S_3 to S_4 for both the ZVS-FB and the series converter.

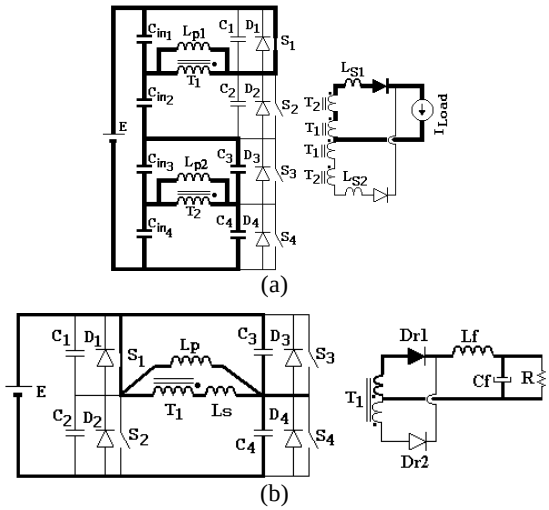

Fig. 4 – Switches commutation when the load current is favorable for the ZVS: (a) series converter; (b) Full-bridge converter.

On the other hand, when the load current freewheels through the output rectifiers diodes, the commutation depends of the energy stored in the series inductor to perform ZVS. Without L_p inductor, this commutation is among the most critical ones. However, with the parallel inductor, it is possible operate with ZVS even in this case. Fig. 5 illustrates this commutation and (3) represents the voltage across the commutation capacitor of the series converter.

$$v_{C_4}(t) = \frac{E.D.\left[1-\cos\left(w_{eq}t\right)\right]}{2} + Iop(Ls-Leq).w_{eq}.\sin\left(w_{eq}t\right) + I_{Lp2_{max}}.L_{eq}.w_{eq}.\sin\left(w_{eq}t\right) \quad (3)$$

where I_{op} is the load current referred to the primary side and $L_{eq} = \frac{L_{s2}.L_{p2}}{L_{s2}+L_{p2}}$, $w_{eq} = \sqrt{\frac{1}{L_{eq}.C}}$, $C=C_1=C_2=C_3=C_4$.

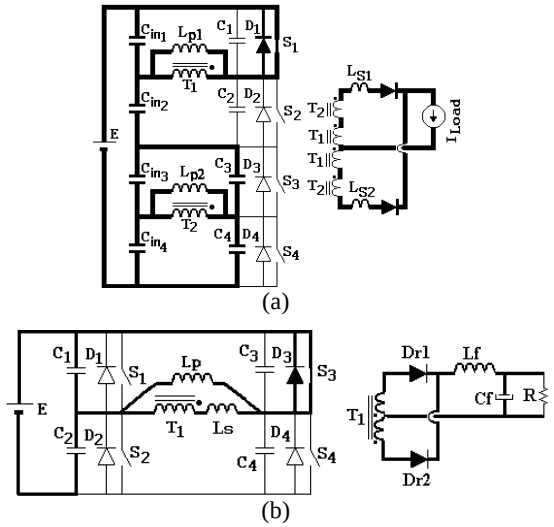

Fig. 5 – Commutations stages of one leg of the converter.

From the above discussion, it can be concluded that the series and the parallel inductors must be designed to ensure ZVS at different operation conditions, and in addition, their values should be selected to minimize the current stresses in the circuit. Next section addresses the issue of the series and the parallel inductors design.

III. The Optimization Method

Without lost of generality, the procedures presented below are based on an application with specifications given in Table I.

TABLE I - DESIGN SPECIFICATIONS

Input dc voltage for the series converter (E)	600V
Input dc voltage for the full-bridge converter (E)	300V
Output voltage (V_0)	60V
Output power (P_{out})	25A
Switching frequency (*fs*)	100kHz
Main Switches	MOSFETs

Figure 6 represents the load current and the capability of each inductor (L_s and L_p) alone to perform the ZVS.

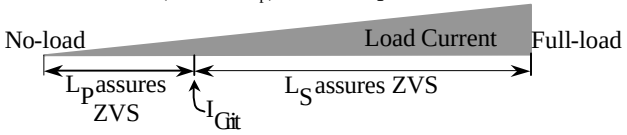

Fig. 6 – ZVS operation range versus load current.

Note that there is a degree of freedom for the selection of the critical current (I_{crit}), shown in fig. 6. Hence, there will be different sets of Ls and Lp that will insure ZVS in the

entire load range. On the other hand, only one critical point allows minimize the rms current through main switches.

An optimization method to obtain the values of the series and parallel inductors that minimize the rms current through main switches is presented below. The optimization method is developed for the series converter.

Equation (4) represents the maximum voltage across C_4, which must be at least equal to $E/2$, to ensure ZVS. From this equation, the parallel inductor value can be obtained by (5).

$$v_{C4}(t) - \frac{E.D}{2} = \sqrt{\left(\frac{-E.D}{2}\right)^2 + \left[\sqrt{\frac{Leq}{2.C}}\left(Iop + \frac{k_1}{Lp2}\right)\right]^2} \quad (4)$$

$$L_{P1} = L_{P2} = \frac{-B + \sqrt{B^2 - 4.A.k_3}}{2A}, \quad (5)$$

where

$$A = 2.k_2.C - Ls.Iop^2, \quad B = 2.k_2.C.Ls + 2.Iop.k_3,$$

$$k_1 = \frac{E.T.D.(1-D)}{4}, \quad k_2 = \frac{E^2.(1-2.D)}{4}, \quad k_3 = -k_1.Ls.$$

From (6) it can be seen that the parallel inductors values are a function of the load current, of the duty cycle, of the series inductance, as well as of the resonant capacitor value. In the worst case, the load current is zero, so, a minimum duty cycle must be adopted to define an L_p value in function of the series inductor value.

Figure 7 presents an abacus to determine the value of the parallel inductor as a function of the series inductor for three values of minimum duty-cycle.

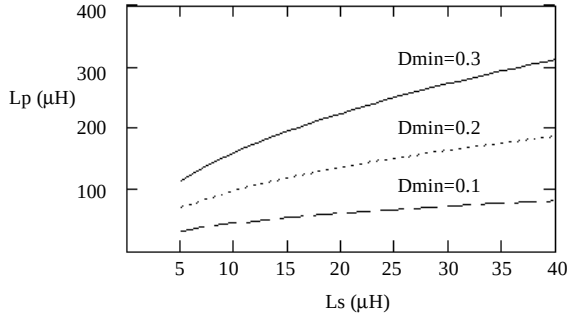

Fig. 7 – L_p value in function of L_s value.

Based on this abacus, it can be deduced that when L_s value increases, the L_p value also increases, thus the reactive energy in the circuit is reduced.

However, the converter effective duty-cycle D_{ef} is function of the series inductor, as defined in (6).

$$D_{ef} = D - \frac{8.fs.Ls.io}{n.E}, \quad (6)$$

where fs is the switching frequency, n is the transformer turns-ratio (N1/N2) and i_o is the load current.

Fig. 8 presents the effective duty-cycle D_{ef} versus series inductor for D = 0.5. Due to the effective duty-cycle loss, the transformers turns-ratio must be selected to obtain the required output voltage. The transformer turns-ratio in function of the series inductor is presented in Fig. 9. It can be seen that as the series inductance is increased, smaller values of transformer turn-ratio are required, resulting in higher values of load current reflected to the primary side.

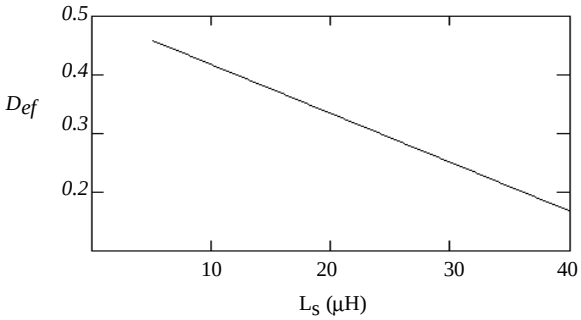

Fig. 8 – Effective duty-cycle versus series inductor value.

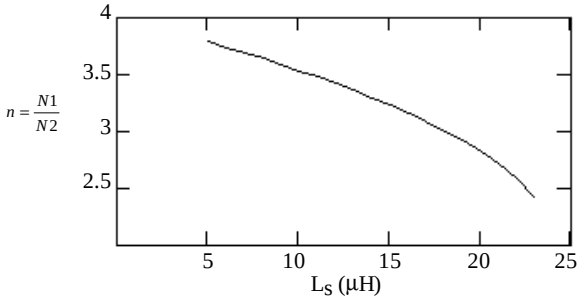

Fig. 9 – Transformer turns-ratio versus series inductance.

From the previous presented analysis, it can be concluded that by reducing the value of L_s, the reactive circulating energy added to the circuit by L_p is decreased. On the other hand, increasing L_s, the transformers turn-ratio must be reduced, increasing the load current value reflected to the primary side, and consequently, increasing the rms current through main switches. To solve this problem and obtain optimum inductor values, the rms current through main switches can be used as a design criterium.

The abacus presented in fig. 10 gives the rms current through S_1 and S_4 for three different values of L_s. In a similar way, the rms current through S_2 and S_3 are presented in fig. 11.

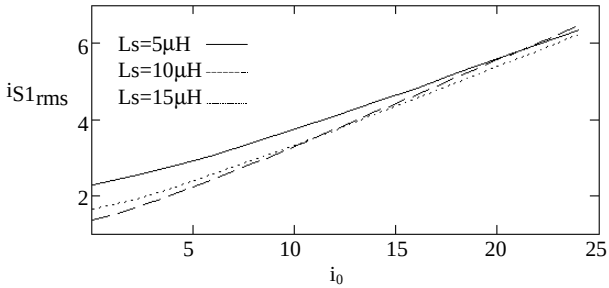

Fig. 10 – S_1 rms current versus load current.

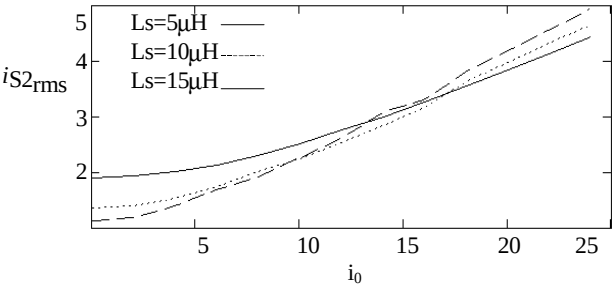

Fig. 11 – S_2 rms current versus load current

The conduction losses in main switches can be calculated by (7), considering the use of MOSFETs as main switches,.

$$P_{loss} = R_{DS_{on}} . I_{rms}{}^2 . \quad (7)$$

Therefore, the total power dissipation at main switches (P_{cond}) is given by (8).

$$P_{cond} = P_{loss_{S1}} + P_{loss_{S2}} + P_{loss_{S3}} + P_{loss_{S4}} . \quad (8)$$

Figure 12 presents the conduction losses at main switches versus the load current, for three values of series inductance, as a function of the load current.

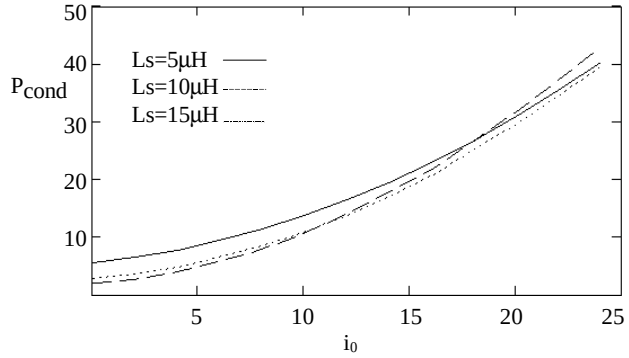

Fig. 12 – Conduction losses at main switches versus Io.

Here, the average conduction losses (9), which has been computed over the entire load range, on main switches is adopted as the optimization criterious. Figure 13 gives the average conduction losses as a function of the series inductance. From this figure, it is seen that the use of a series inductance of 10µH presents the minimum switches conduction losses for C=400pF (MOSFETs capacitance).

$$\overline{P_{cond}} = \frac{1}{26} \sum_{io=0}^{25} P_{cond}(io) . \quad (9)$$

By using the same procedure to the ZVS-FB converter, the average of conduction losses can also be obtained, as depicted in Fig. 14.

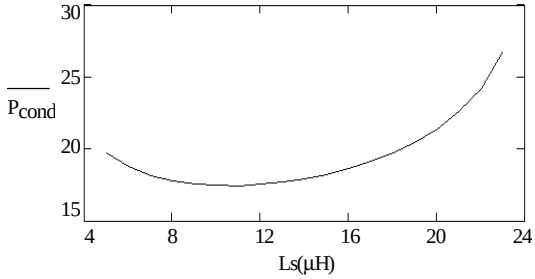

Fig. 13 – Average power of conduction losses at main switches versus series inductance for the Series converter.

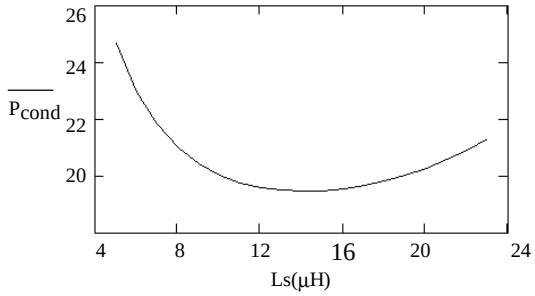

Fig. 14 – Average power of conduction losses at main switches versus series inductance, for the ZVS-FB converter.

IV. Experimental Results

Two prototypes have been implemented based on the presented design procedures. Table II presents the main parameters used.

The sum of the leakage inductance of transformers T_1 and T_2 has been measured, and the value found was 5µH. To obtain the value of the series inductance L_s (10 µH), an external inductor of 5µH (EE-30/07) has been added in series with T_2 transformer.

Table II
Parameters and Components utilized in the prototype

Device	Parameter
S_1, S_2, S_3, S_4	IRFP 360
D_1, D_2, D_3, D_4	MOSFETs intrinsic diodes
C_1, C_2, C_3, C_4	MOSFETs intrinsic capacitors
L_s	10 µH
C_{in1-4}	5 x 1µF - Icotron
D_{r1}, D_{r2}	MUR 3060
T_1, T_2	EE 65/26 Thornton – 12:3 turns
L_{p1}, L_{p2}	98 µH – EE 30/14Thornton – 20 turns
Lf	100µH –EE 55/21
Cf	2 x 220 µF- Icotron

Figures 15 and 16 present the voltage across switch S_2 and its gate-source voltage for full-load and no-load, respectively. In these figures, it can be seen that the gate signals are applied only after the voltage across the switches reach zero, characterizing the ZVS commutation.

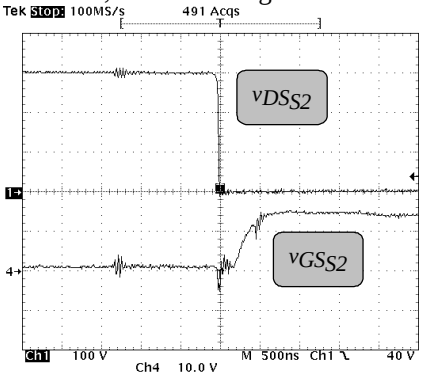

Fig. 15 – S_2 drain-source voltage and gate-source voltage, at full-load.

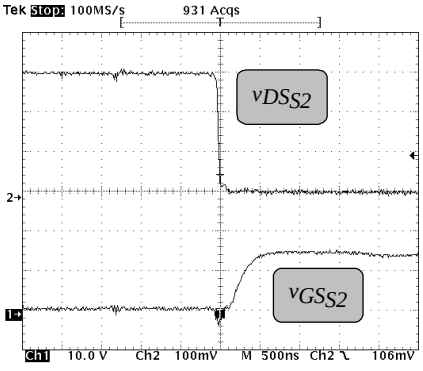

Fig. 16 – S_2 drain-source voltage and gate-source voltage, at no-load.

Figure 17 shows S_2 drain-source voltage and L_{p1} current at full-load. It can be seen that the peak current I_{Lp1max} is

greater than the minimum current necessary to the achieve ZVS. This occurs because the parallel inductors are designed for a minimum duty-cycle, and the peak current in parallel inductors increases in function of the duty-cycle.

Figure 18 presents the efficiency of the series converter, as well as of the ZVS-FB converter; being achieved a maximum efficiency of 92%, for both converters.

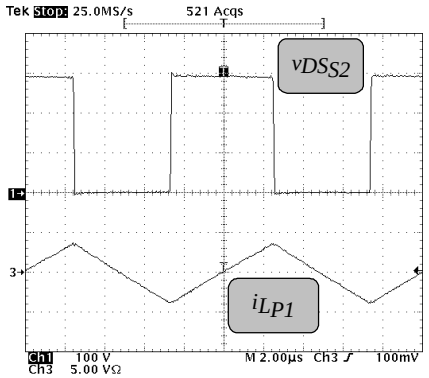

Fig. 17 – S_2 drain-source voltage and L_{p1} current.

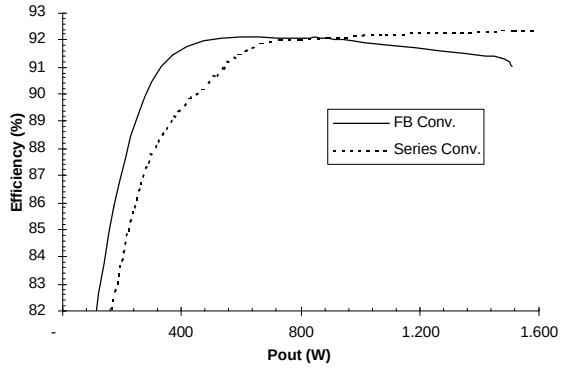

Fig. 18 – Efficiency versus output power.

V. CONCLUSIONS

This paper presents an optimization method to minimize the rms current through main switches of dc-dc converters with ZVS in entire-load range The proposed method gives the optimal set of series and parallel inductors values, in a way to minimize conduction losses at main switches.

The presented procedures can be extended to others converters that present similar characteristics to the full-bridge ZVS converter. Experimental results obtained from a dc-dc series converter and from a ZVS-FB converter, both operating with 1.5kW@100kHz are presented to demonstrate the feasibility of the proposed technique.

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