A ZVS PWM INVERTER WITH ACTIVE CLAMPING TECHNIQUE USING ONLY A SINGLE AUXILIARY SWITCH

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Abstract - This paper presents a ZVS PWM inverter with voltage clamping technique using only a single auxiliary switch. The structure is particularly simple and robust. It is very attractive for single-phase high power applications. Conduction and switching losses are reduced due to implementation of the simple active snubber circuit, that provides ZVS conditions for all switches, including the auxiliary one. Its main features are: Simple control strategy, robustness, lower weight and volume, lower harmonic distortion of the output current, and high efficiency. The principle of operation for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.

I. INTRODUCTION

Many efforts have been made by the researchers all over the world, in the attempt to reduce the harmonic distortion and the audible noise in the output of the inverters.

These objectives have been attained with the increase of the inverter commutation frequencies and an appropriate modulation strategy. These measures give some benefits like the reduction of the weight and volume of the magnetic elements; nevertheless they cause some difficulties due to the high commutation losses in the switches and the electromagnetic interference appearing. These factors occur mainly in inverter topologies that use the bridge inverter configuration. At the moment that the main switch turn on, the antiparallel diode of the bridge complementary switch begins its reverse recovery phase. During this stage the switches are submitted to a high current ramp rate **(di/dt)** and a high peak reverse recovery current **(Ir)**. Both contribute significantly to the increasing of the commutation losses and procedure electromagnetic interference.

A great number of works have been developed with the aim to diminish these problems [1], [2], [3].

Recently, some researches were made using the reverse-recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [4], [5].

In this paper a ZVS PWM inverter with voltage clamping across the switches, using only a single auxiliary switch, is presented. The proposed structure utilizes the diode reverse recovery energy technique to obtain soft commutation in all switches, such as the rectifier shown in reference [5].

This topology presents some advantages in comparison with the conventional soft commutation inverters studied in the literature, which we can print out:

- Soft commutation in all load range;
- Simple topology with a low number of components;
- Use a classical PWM modulation;
- Auxiliary switch works with constant duty cycle in all operation stages;
- Use of slow and low cost rectifiers diodes;
- Low clamping voltage across the capacitor;
- Low current stress through the main switches;
- Simple design procedure with low restrictions;
- High efficiency.

II. PROPOSED CIRCUIT

The proposed circuit is shown in Fig.1. It presents a half bridge inverter configuration, where Q1, Q2 are the main switches, and Qa is the auxiliary switch.

The snubber circuit is formed for one switch **Qa**, one small center-tapped inductor **Ls1**, **Ls2** and one capacitor **Cs**. **C1, C2** and **Ca** are the commutation capacitors. The capacitor **Cs** is responsible by the storage of the diode reverse recovery energy and by the clamping of switches voltage. The inductors **La1** and **La2** can be constructed in the same ferrite core, and they are responsible for the control of the **di/dt** during the diode reverse recovery time. The main advantage of this converter consists in the use of only one auxiliary switch, which provides the clamping of the voltage and the ZVS conditions for all switches, including the auxiliary switch in the snubber circuit.

III. OPERATION STAGES (FOR THE FIRST HALF CYCLE)

The principle operation of both semicycle of the inverter load current is symmetrical. Thus, only for the first half cycle of the operation the circuit analysis will be made.

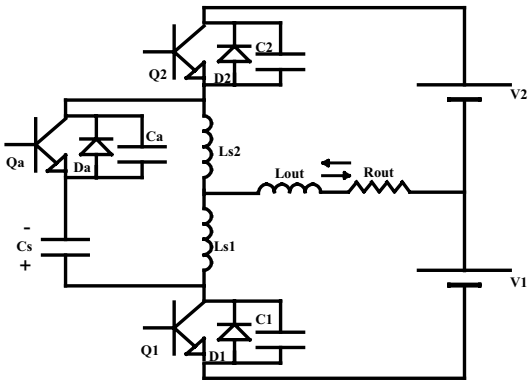

Fig. 1. Proposed Circuit.

To simplify the analysis, the following assumptions are made: the operation of the circuit is steady state; the components are considered ideal; excluding the reverse recovery of the diodes D1, D2. The voltage across the capacitor **Cs**, and the current in the output inductor **Lout** are considered constant during the switching period. The parameter **E** represents the total bus voltage **(E=V1+V2)**, and **Vcs** is the voltage across the clamping capacitor **Cs**. The parameter **Ls** is defined as the sum of the auxiliary inductors **(Ls=Ls1+Ls2)**.

In the following paragraphs the operation stage of the first positive half cycle of the output current is described in detail.

First stage (t0-t1): During this interval the output current $\mathbf{I_{out}}$ is increasing, and delivering energy to the source **V2** via diode **D2**. At the same time, the additional current $\mathbf{i_{Ls1}}$ flows around the mesh, formed by **Ls2, Qa, Cs,** and **Ls1.**

Second stage (t1-t2): This stage starts when the auxiliary switch **Qa** is blocked. The current $\mathbf{i_{Ls1}}$ begins the charge of the capacitor **Ca** from **zero** to $\mathbf{E+V_{Cs}}$, and discharges **C1** from $\mathbf{E+V_{Cs}}$ to **zero**.

Third stage (t2-t3): At this stage the voltage across **C1** reaches **zero,** and it is clamping by the diode **D1.** So, the switch **Q1** conducts with ZVS condition. At this moment, the voltage **E = V1+V2** is applied across the inductors **Ls1** and **Ls2**, and the currents $\mathbf{ï_{Ls1}}$ and $\mathbf{i_{Ls2}}$ decrease linearly.

Fourth stage (t3-t4): It begins when the current $\mathbf{i_{Ls1}}$ inverts its direction and flows through the switch **Q1**. The current $\mathbf{i_{Ls2}}$ continues to decrease until inverting its direction, and begins the reverse recovery phase of the diode **D2.** The inductor **Ls2** limits the $\mathbf{di_{Ls2}/dt}$.

Fifth stage (t4-t5): This stage starts when the diode **D2** stops conducting. The current $\mathbf{i_{Ls2}}$ begins the charge of the capacitor **C2** from **zero** to $\mathbf{E + V_{Cs}}$ and the discharge of **Ca** from $\mathbf{E + V_{Cs}}$ to **zero**.

Sixth stage (t5-t6): At this stage the voltage across the capacitor **Ca** reaches **zero**, and it is clamped by the diode **Da.** Thus, the auxiliary switch **Qa** conducts with zero-voltage switching. The currents $\mathbf{i_{Ls1}}$ and $\mathbf{i_{Ls2}}$ increase, due the application of the voltage $\mathbf{V_{Cs}}$ across the inductors **Ls1** and **Ls2**.

Seventh stage (t6-t7): This stage begins when the current $\mathbf{i_{Ls2}}$ changes its direction and flows through the switch **Qa**. The current $\mathbf{i_{Ls1}}$ continues to increase linearly.

Eighth stage (t7-t8): At this stage the switch **Q1** is blocked, and the current in **Cs** inverts its direction and flows through the diode **Da.** The capacitor **C1** charges itself from **zero** to $\mathbf{E + V_{Cs}}$ and the capacitor **C2** discharges from $\mathbf{E + V_{Cs}}$ to **zero**.

Ninth stage (t8-t0): It begins when the voltage across the capacitor **C2** reaches **zero,** and it is clamped by the diode **D2**. The current $\mathbf{i_{Ls1}}$ continues increasing. This stage finishes when $\mathbf{i_{Ls1}}$ inverts its direction, and flows through the auxiliary switch **Qa**, restarting the first operation stage.

For the second half cycle the operation stage is analogous and can be described in an identical way.

The main waveforms are shown in Fig. 2, and Fig.3. shows the main operation stages.

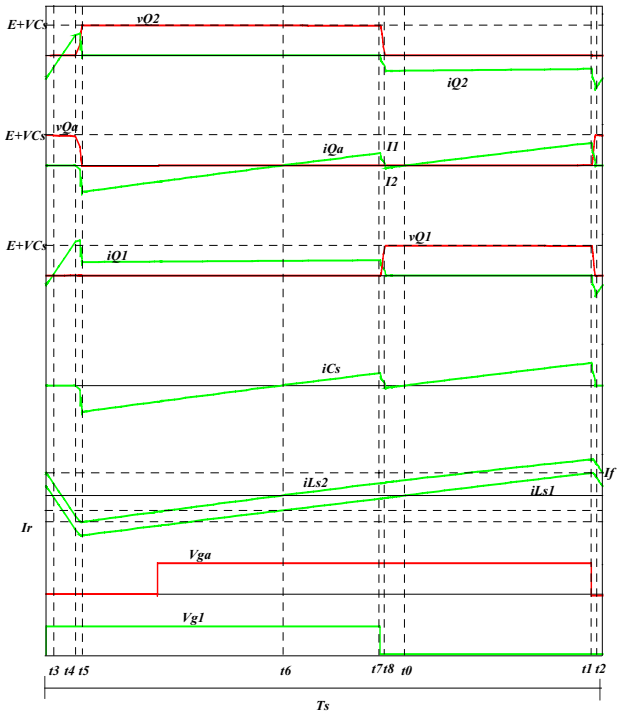

Fig. 2. Main Waveforms.

IV. Mathematical Analysis of the Soft-Switching Circuit

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor Ls=Ls1+Ls2 be sufficient to discharge the capacitor C1 and to charge Ca. Thus, by inspection of Fig. 3 (Interval t1-t2) the following condition can be formulated:

$$Ls \cdot If^2 \geq (Ca + C1)(E + V_{Cs})^2 \qquad (1)$$

Where ***If*** is the maximum current in **Ls2,** and $\mathbf{V_{Cs}}$ is maintained constant during a switching period. Assuming $\mathbf{V_{Cs}}$**<<E** we have:

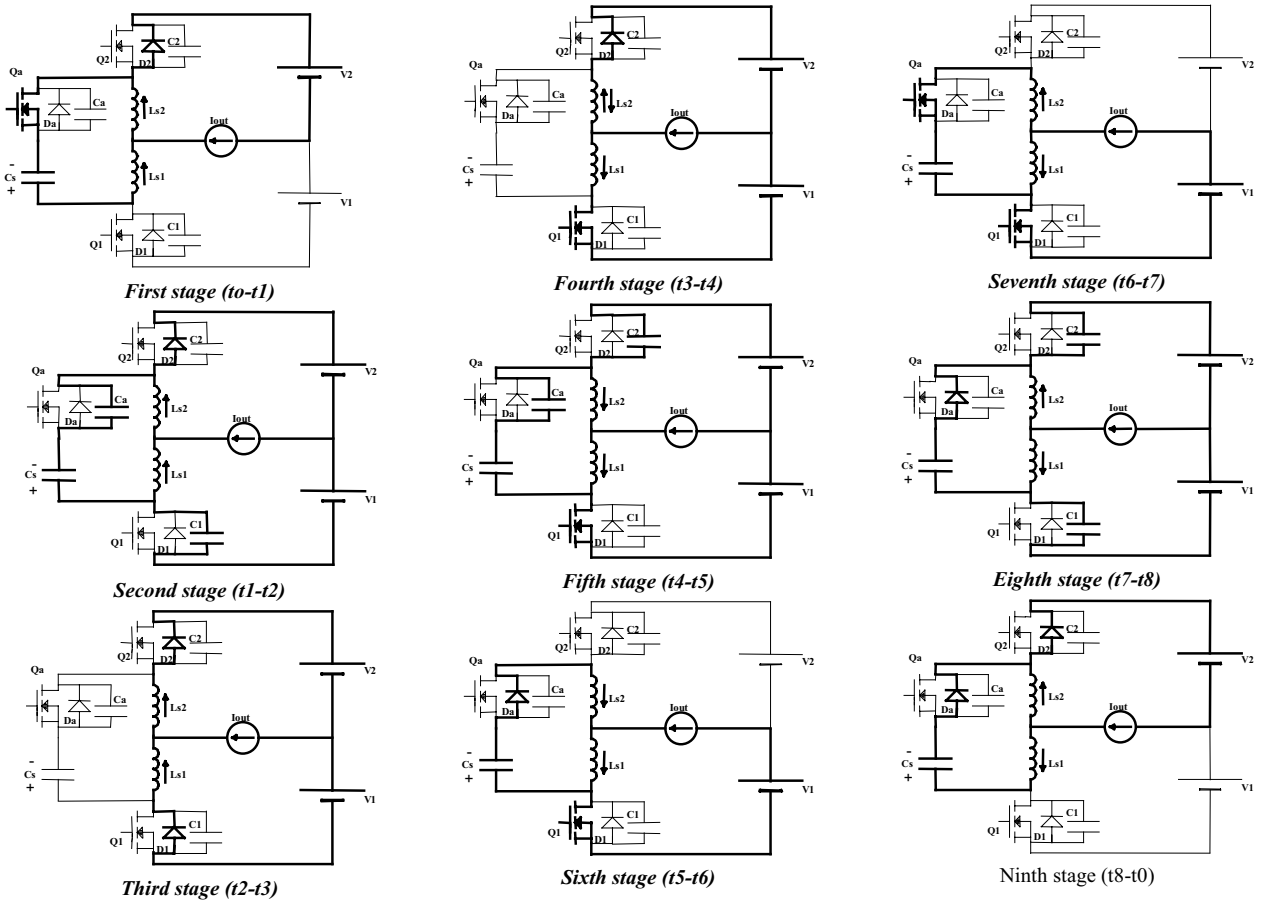

Fig. 3. Operation Stage

$$If \min \geq E\sqrt{\frac{C1+Ca}{Ls}} \tag{2}$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor **Cs**.

In the steady state conditions the clamping capacitor average current must be zero. Thus:

$$iCs_{av} = \frac{1}{Ts}\left[\int_0^{t7}\left(\frac{Vcs}{Ls}\cdot t - Ir\right)dt + \int_{t7}^{t1}\left(\frac{Vcs}{Ls}\cdot t - Iout - Ir\right)dt\right] \tag{3}$$

Where **Ts** is the switching period

Solving the integral equation, and considering:

$$D = \frac{t7}{Ts} \tag{4}$$

$$t1 \approx Ts \tag{5}$$

$$iCsav_{av} = 0 \tag{6}$$

We have:

$$Vcs = \frac{2\,Ls}{Ts}\left[Ir + Iout\ (1 - D)\right] \tag{7}$$

Considering that the output current will be sinusoidal and in phase with the output voltage, thus:

$$Iout = \frac{E \cdot ma}{2 \cdot Zout} \cdot sen\omega t \tag{8}$$

where ***Zout*** is the load impedance given by:

$$Zout = \sqrt{Rout^2 + (\omega \cdot Lout)^2} \tag{9}$$

Rout – Load resistance

Lc – Load inductance

The duty cycle ***D*** can also be defined as:

$$D = ma \cdot sen\omega t \tag{10}$$

Where ma represents the modulation factor of amplitude.

Combining Eqs. 7, 8 e 10 we obtain the expression of the ***Vcs*** voltage.

$$Vcs(t) = \frac{2 \cdot Ls}{Ts}\left[Ir + \frac{E \cdot ma}{2 \cdot Zout} \cdot sen\omega t \cdot (1 - ma \cdot sen\omega t)\right] \tag{11}$$

Where ***Ir*** is the peak reverse recovery current of the antiparallel diode, which can be given by:

$$Ir = \sqrt{\frac{4}{3} \cdot Qrr \cdot \frac{E}{Ls}} \tag{12}$$

Qrr – Reverse Recovery Charge

From the analysis of the current behavior in the capacitor **Cs** , the expression of the current ***If*** can be obtained :

$$If(t) = \frac{Vcs}{Ls} \cdot Ts - Iout - Ir \qquad (13)$$

Combining Eq. 11 with Eq. 13 and making some simplifications we obtain the expression that represents the evolution of the current ***If***.

$$If(t) = Ir + \frac{E \cdot ma}{2 \cdot Zout} \cdot sen\omega t - \frac{E \cdot ma^2}{Zout} \cdot sen^2 \omega t \qquad (14)$$

To guarantee ZVS condition in all load range the minimum value of the current ***If*** obtained from Eq. 14 must be bigger than the value obtained from Eq. 2.

V. Design Example

A. Input Data

E = 400V	Bus Voltage
Vout = 127 V	RMS Output Voltage
Pout = 1000VA	Output Power
Iout = 7.88A	Output Current
fs = 20KHz	Switching Frequency
f = 60Hz	Output Frequency
Lout = 2.5mH	Load Inductance
Rout = 16Ω	Load Resistance
ma=0,9	Modulation Factor

B. Calculation of the auxiliary inductors.

The auxiliary inductors are responsible for the di/dt limit during the turn off of the main diodes. The di/dt is directly related with the peak reverse recovery current ***Ir*** of the antiparallel diodes. A “snappy” di/dt produces a large amplitude voltage transient and contributes significantly to Electro-magnetic interference.

In the design procedure it is chosen a di/dt that is usually find in the diode data book. This is a simple way to obtain the diodes fundamental parameter for the design of the inverter. In such case the di/dt chosen for this example was 40A/us. Knowing that the current ramp rate is determined by the external circuit, thus:

$$Ls = \frac{E}{di/dt} = \frac{400V}{40\,A/\mu s} = 10\mu H \qquad (15)$$

The auxiliary inductors are given by:

$$Ls1 = Ls2 = \frac{Ls}{2} = 5uH \qquad (16)$$

C. Load Impedance.

The load impedance is obtained from Eq. 17

$$Zout = \sqrt{16\Omega^2 + (2 \cdot \pi \cdot 60Hz \cdot 2{,}5mH)^2} = 16.11\Omega \qquad (17)$$

D. Diode Choose.

For the performance of the inverter it is important to choose a slow diode. So, we opt to use the body diode of the MOSFET IRFP460, which has the following characteristics:

Vdss = 500V	Maximum Reverse Voltage
Is = 20A	Diode Average Current
Qrr = 5.7µC	Reverse Recovery Charge

E. Switching Period

$$Ts = \frac{1}{fs} = \frac{1}{20KHz} = 50\mu s \qquad (18)$$

F. Reverse Recovery Current.

The reverse recovery current is given by the Eq. 12.

$$Ir = \sqrt{\frac{4}{3} \cdot 5{,}7\mu C \cdot \frac{400V}{10\mu H}} = 17{,}4A \qquad (19)$$

G. Capacitor Clamping Voltage Behavior

Using a Eq. 11 the curves described in Fig. 4 are obtained.

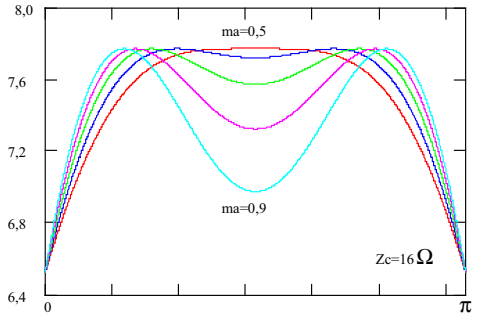

Fig 4. Capacitor Clamping Voltage Behavior

For Zout=16Ω and ma=0,9, the maximum clamping voltage is ***8V***.

We can observe that the voltage increment across the switches is smaller than conventional inverter.

H. Current If Behavior.

The current ***If*** behavior, obtained from Eq.14 and Eq. 2, can be seen in Fig. 5.

It is observed that the current ***If*** has a minimum point that is located in π/2, and the intensity of the current diminishes with the increase of the load. To guarantee ZVC condition in all range load, the minimum value of the current ***If***, obtained from Eq. 14, must be bigger than the value of the traced straight line from Eq. 2.

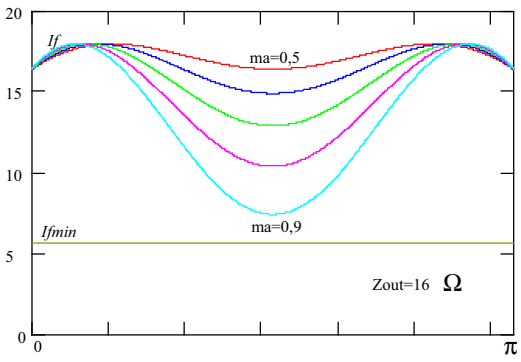

Fig. 5. Current ***If*** Behavior

VI. Experimental Results

An inverter prototype rated 1kVA operating with PWM commutation was built to evaluate the proposed circuit. The main specifications and components are given below:

A. Prototype Specifications

Pout = 1500 W	(Output Power)
E = 400V	(Bus Voltage)
Vout = 127V	(Rms Output Voltage)
f = 60Hz	(Output Frequency)
fs = 20 kHz	(Switching Frequency)
Q1, Q2, Qa	(IGBT IRG4PC50W)
D1, D2, Da	(Mosfet Body Diode IRFP460)
C1, C2, Ca	(Components Intrinsic Capacitance)
Ls1, Ls2	(5uH each; Ferrite Core EE30/7; N=16 turns, 13 wires #20AWG)
Cs	(220uF/35V; Electrolytic Capacitor)
Lout	(2.5mH, Output Inductor)
Rout	(16Ω; Output Resistor)

B. Experimental Waveforms

In the figures presented below we can observe the experimental waveforms obtained from the laboratory prototype. Figs. 6, 7 and 8 show the voltage and current in the switches.

In Fig. 9 it can be observed the current in the commutation auxiliary inductors for a switching period.

The voltage across the clamping capacitor **Cs** is shown in Fig. 10. . We can note a very low voltage across **Cs**.

The output voltage and current are presented in Fig. 11.

Fig. 12 and 13 show the efficiency and losses as function of the load range.

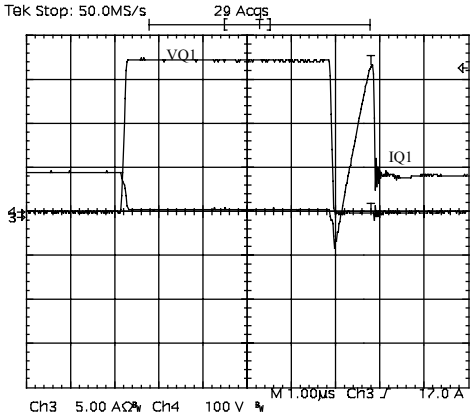

Fig. 6. Voltage and current in Q1, D1.
(100V/div, 5A/div, 1us/div

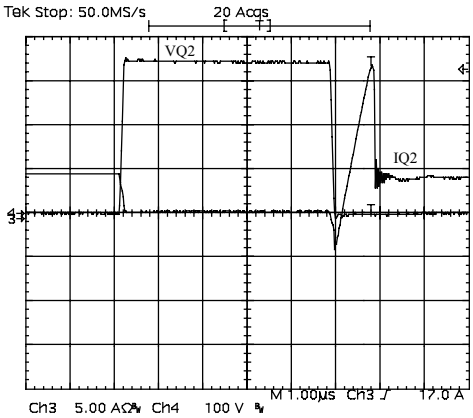

Fig. 7. Voltage and current inQ2, D2.
(100V/div, 5A/div, 1us/div)

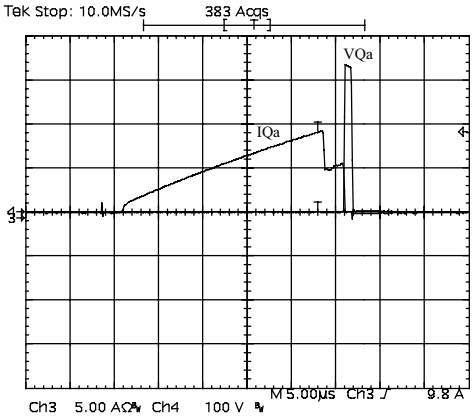

Fig. 8. Voltage and current in Qa.
(100V/div, 5A/div, 1us/div)

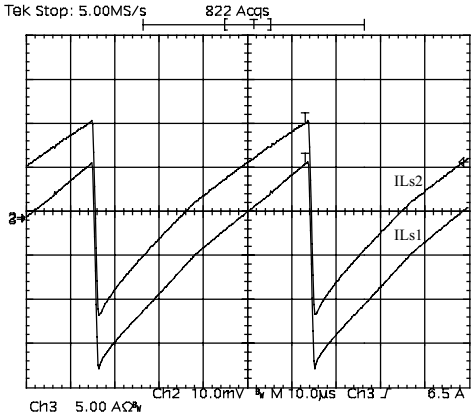

Fig. 9. Current in Ls1 and Ls2.
(5A/div, 10us/div)

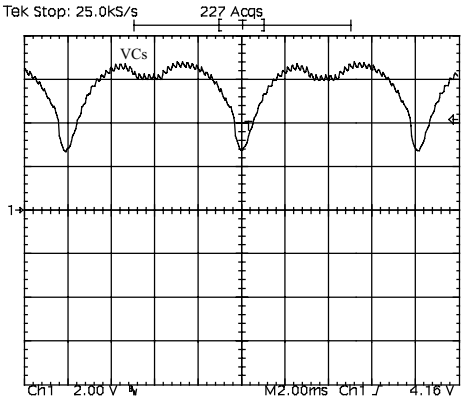

Fig. 10. Voltage in Cs.
(2V/div, 2ms/div)

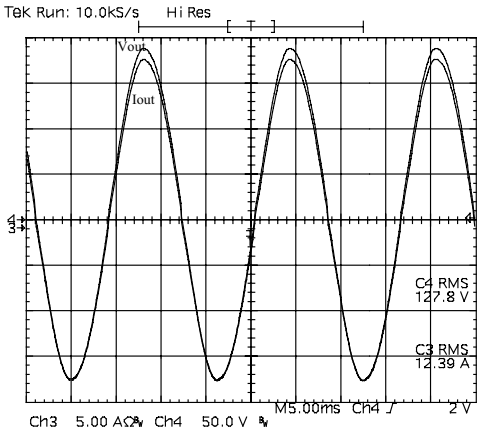

Fig. 11. Output voltage and current.
(50V/div, 5A/div, 5ms/div)

VII. Conclusions

A ZVS PWM inverter with voltage clamping using a single auxiliary switch has been developed. The operation stages for steady-state condition, mathematical analysis, main waveforms and experimental results were presented. The experimental results show a low voltage in the clamping capacitor. Conduction and switching losses are reduced due to the implementation of the simple active snubber circuit, that provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability, and make it suitable for practical applications. The proposed circuit presents soft commutation for all load range, confirming the theoretical studies.

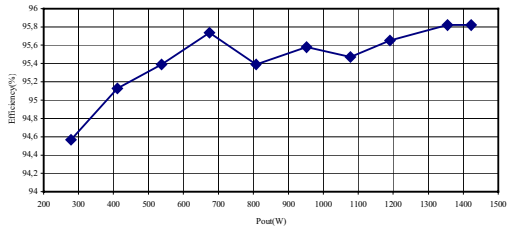

Fig. 12. Efficiency over the output range.

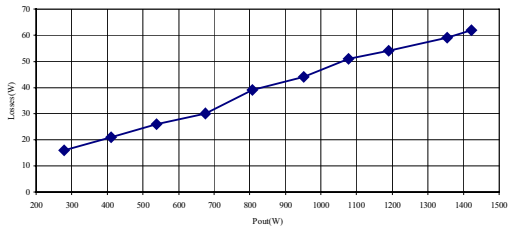

Fig. 13. Inverter losses

VIII. References

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