Implementation Aspects of Digital Control Algorithms for Cascaded Converter Systems

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***Abstract* – Cascaded converters are the essential part of modern energy conversion systems like uninterruptible power supplies, photovoltaics and other regenerative power systems. Starting from a description of the special converter system the implementation process of the developed algorithms is presented. The detailed structure of the hardware platform, designed as a low-cost solution, is also given. The particular tasks of the control unit like the calculation of the different control variables, the generation of the gate signals and the real time demands for a multitasking operation are explained. Finally the implementation of frequently used control algorithms is demonstrated.**

I. INTRODUCTION

Besides the regenerative energy systems, wherein cascaded converter configurations are used to transform the primary energy into grid compatible waveforms, they are also used in series or parallel connected high power converters to achieve among others a high availability [1], [2]. These configurations ensure an improved quality of the input and/or output values due to their higher operating frequencies compared to conventional solutions. Furthermore applying a superposition of series or paralleled modules a decrease of the resulting ripple, caused by the switching actions, is obtainable [3].
Following the tendencies of development in power electronics the power density of new devices becomes more and more important. Especially the passive components like transformers, inductors and capacitors determine the dimensions and the costs of the products. To decrease their sizes higher operating frequencies are indispensable.

Together with these rapidly growing requirements and the rising amount of power switches the digital control units have to operate under forced real time conditions. For a complete operation both computational and peripheral like timers and PWM-channels and logic functionality is necessary. The choice of the most suitable components thereby depends on the number of power switches and analog input signals, the required resolution of the duty cycles and last not least on the costs of the system.

The investigated system, discussed in this paper, is a battery supplied uninterruptible power supply [4], [5], [12]. It has to provide two different isolated sinusoidal output voltages with high quality and availability. Compared to conventional topologies the necessary transformer is included in a dc-dc converter, whereby the output inverter can be directly connected to the load side. Due to the higher amount of active switches the resulting topology is more difficult to control like the classical full bridge inverter with a low frequency output transformer [12].

The architecture of the control unit is based on several components. Different tasks like the analog-to-digital conversion, calculation of the control variables, pulse width modulation and circuit protection are solved by different components. This allocation leads to the design presented in this paper. After a short description of the power stage the developed control algorithms are given. The last sections contain besides the hardware structure some detailed timing description and software implementation considerations.

II. POWER STAGE

Uninterruptible Power Supplies (UPS) are needed to provide a source of electrical energy with high quality, stability and disposability in case the public mains cannot fulfil these demands. Fig. 1 shows a block diagram of a transformerless online-UPS, which consists besides the input rectifier of an isolated full bridge boost converter to adjust the uncontrolled battery voltage to the dc-link level and an output inverter. The most important benefit of this topology is the absence of the large low frequency output transformer.

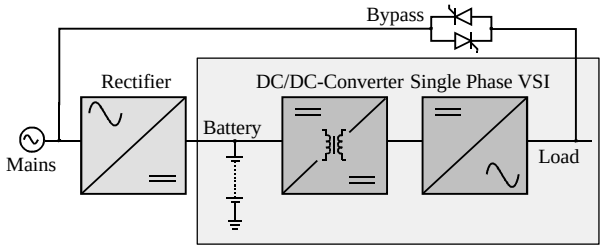


Fig. 1. Transformerless online-UPS

To achieve a compatibility of the UPS to different public mains configurations like 230V/50Hz and 115(120)V/60Hz the output inverter topology consists of two half bridge inverters in parallel as shown in Fig. 2b. Depending on the chosen voltage the gate signals of one half bridge and the load connectors 0,1 and 2 have to be changed. Except for the fundamental frequency the utilization factor of all elements is independent of the generated output voltage at the same power [4], [12]. Another benefit of the system in Fig. 1 is the controlled dc-link voltage ensured by the dc-dc converter. The special

inverter topology requires a divided dc-link to operate with three voltage levels. Fig. 2a shows the power stage of the dc-dc converter, which consists of an isolated full bridge boost converter including two secondary sides.

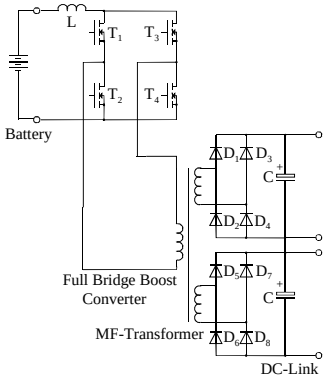


Fig. 2a. Full bridge boost converter

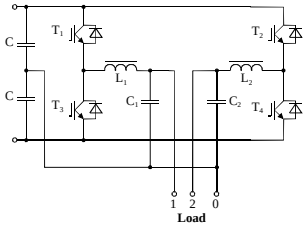


Fig. 2b. Single phase voltage source inverter

The basic principles of operation of the ups are described in [4], [5] and [12]. The only disturbances, whose influence is to be eliminated by the inverter control, are load generated harmonics due to the regulated dc-link voltage. Hence the presented concept promises in spite of the relatively large amount of active switches a satisfying performance.

III. Modeling And Control Design

The first step in deriving control laws for any plant is to find suitable models for the technical procedures. In the present case the systems are swichted electric circuits, which can be described by different approaches. Assuming a constant high switching frequency for both systems in relation to the natural frequencies of the electric circuits, the state space averaging approach will be used [6], [7], [8], [9]. The mathematical model for the dc-dc converter and the output inverter can be in general formulated as

$$\dot{\vec{x}}(t) = \underline{A}\vec{x}(t) + \underline{B}\vec{u}(t) + \underline{E}\vec{z}(t) \qquad (1)$$

with the state vector $\vec{x}(t)$, the control vector $\vec{u}(t)$, the disturbance vector $\vec{z}(t)$ and the system, control and disturbance matrices $\underline{A}$, $\underline{B}$ and $\underline{E}$.

Because the boost converter and the output inverter are second order systems, the state vector contains two components and the system matrix becomes two-dimensional. In opposition to the inverter due to the non-linearity of the boost converter therefor a small signal approximation is needed. It must be noticed that the state vector of the linearized model contains only the deviations *Dx* of the state variables. The single phase inverter regarding Fig. 2b owns two different state equations depending on the chosen output voltage. Since the analysis of both power stages is detailed described in [4] and [5], (2) represents for example the normalized matrices of the output inverter model with the definition of the state vector $\vec{x}(t) = \begin{pmatrix} i_L & v_C \end{pmatrix}^T$, the control variable $u(t) = 2D(t) - 1$ with the duty cycle *D(t)* and the disturbance vector $\vec{z}(t) = \begin{pmatrix} 0 & i_{LOAD} \end{pmatrix}^T$.

$$\underline{A} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \begin{pmatrix} -\dfrac{R_{L_\Sigma}}{L_\Sigma} & -\dfrac{V_{C_{MAX}}}{I_{L_{MAX}} L_\Sigma} \\ \dfrac{I_{L_{MAX}}}{V_{C_{MAX}} C_\Sigma} & 0 \end{pmatrix}$$

$$\underline{B} = \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} \dfrac{V_{DC}}{I_{L_{MAX}} L_\Sigma} \\ 0 \end{pmatrix} \qquad (2)$$

$$\underline{E} = \begin{pmatrix} e_1 \\ e_2 \end{pmatrix} = \begin{pmatrix} 0 \\ -\dfrac{I_{LOAD_{MAX}}}{V_{C_{MAX}} C_\Sigma} \end{pmatrix}$$

The parameters in (2) are the concentrated loss resistance R_{L_Σ} and the effective inductances L_S and output capacitances C_S depending on the chosen output voltage. The normalization factors are the maximum values of the state and disturbance variables $V_{C_{MAX}}$, $I_{L_{MAX}}$ and $I_{LOAD_{MAX}}$. Summarizing there are three different models to consider while deriving the control laws for the complete UPS.

A. Boost Converter Control

The small signal model of the boost converter is used to calculate a linear-quadratic state feedback matrix K_{DC} to achieve a good stability and dynamic response of the closed-loop system [9]. To reduce the amount of sensors only the input and output voltage of the dc-dc converter are measured. The missing state variable i_L is estimated by a *Luenberger* observer of reduced order. Fig. 3 shows a block diagram of the boost converter control structure.

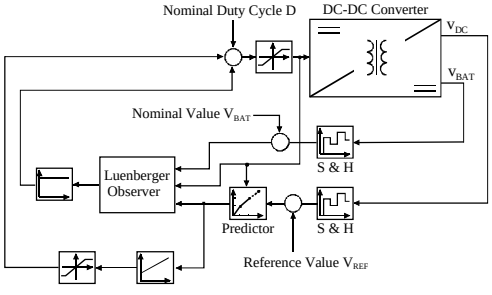


Fig. 3. Observer based state feedback control

B. Inverter Control

The control laws of the two possible inverter configurations are calculated in a similar manner to the boost converter [12]. Besides the linear state feedback matrix K_{AC} some additional control loops are necessary. To avoid the steady state error of first-order integrators under alternating reference values, which are usually added to proportional state feedback loops, a second-order integrator must be applied in the inverter control. Its transfer function can be derived from the space vector modulated three phase system with *park*-transformed phase values and PI-control of both resulting components [12] and is

$$G_{2I}(s) = \frac{K_P}{w_N} \cdot \frac{\frac{w_N}{s}}{1 + \frac{w_N^2}{s^2}} \tag{3}$$

with the integrator gain K_p and the fundamental frequency of the inverter output voltage w_N.

Due to the absence of an output transformer an offset-compensator is furthermore needed. Because the UPS has to be protected against short circuit and overload a current control loop has to get in the lead if these cases occur. To ensure a synchronous output voltage compared to the public mains a PLL-algorithm has to predetermine the voltage reference. That task will be described more detailed in the following section. Fig. 4 gives an overview of the inverter control structure.

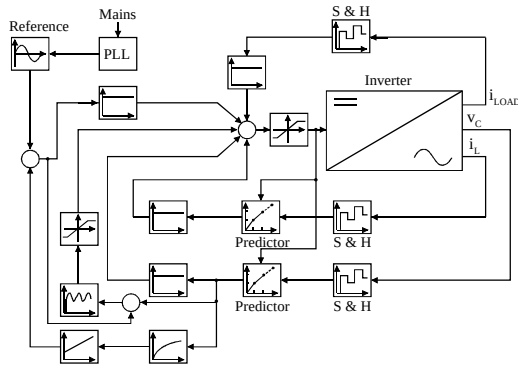


Fig. 4. State feedback control of the proposed VSI

In addition to the named control loops a disturbance variable feedforward supports the elimination of load generated voltage harmonics.

To reduce the influence of the delay time caused by the digital calculation and the zero-order-hold effect the measured state variables in both systems are predicted using a linear extrapolation technique [11]. Equation (4) represents the general approach to predict the input values of the control loops:

$$x_{k+1} \approx 2x_k - x_{k-1} + C_x T_S (D_k - D_{k-1}) \tag{4}$$

with the sample time T_S and a system dependent constant C_x. An estimated value of the state variable x_{k+1} at the end of the sample period $k+1$ can be calculated using present and past values of the state variable itself and a correction term, consisting of present and past values of the control variable D.

C. Synchronization

In order to provide a high quality, high reliability supply the UPS has to be fully functional in any of two modes of operation. The first is the UPS working online (with or without the public mains) using the inverter to supply the loads. The second is the public mains connected directly to the output of the UPS using the bypass. This might be needed if malfunctions occur in hard- or software or maintenance has to be done. Changing these modes makes it necessary to synchronize both public mains and UPS generated to avoid phase shifts on connected appliances.

A second reason for a strict synchronization is the optional feature of the parallel use of several UPS without any communication. One possible way to generate one unique output is to synchronize to the public mains.

To add the synchronization task to the implemented control algorithms it has to run at the same frequency as the inverter. Depending on the fundamental frequency of the public mains (50 or 60Hz) a Discrete Fourier Transformation (DFT) uses 240 or 200 sample points, respectively.

The synchronization algorithm has to deliver two results. At first it has to extract the exact fundamental frequency of the public mains which can vary in a certain range. The second is to get the accurate phase angle of the mains. Using a 16 bit Integer for storing phase information one will have a precision of $2 \cdot p \cdot 2^{-16} = 9.59 \cdot 10^{-5}$ which leads to 0.0055° for the tiniest angle.

Using a constant sampling frequency to run in a multitasking controller environment it is necessary to vary the Fourier frequency in order to synchronize to the public mains. The reason is the presented approach of the synchronization. Based on any mains as the sum of sinusoidal functions of a fundamental frequency and its odd numbered multiples the coefficients of the Fourier Integrals can be expressed as follows:

$$\mathrm{Re} = \int \sum_{n=0}^{\infty} A_{2n+1} \sin\left[(2n+1) w_p t + a_{2n+1}\right] \cos(w_F t + a_F) dt \tag{5}$$

$$\mathrm{Im} = \int \sum_{n=0}^{\infty} A_{2n+1} \sin\left[(2n+1) w_p t + a_{2n+1}\right] \sin(w_F t + a_F) dt \tag{6}$$

whith w_P as the fundamental frequency of the public mains, w_F as the Fourier Frequency, a_{2n+1} and a_F as the belonging phase shifts and A_{2n+1} as the amplitudes of the contained sine functions of the public mains.

The (not shown) borders of the integrals are defined by the time window, which includes the measurement points (almost exactly one period). The solutions of both integrals are

$$\mathrm{Re} = \left\{ \frac{1}{2} \frac{A_1}{w_F - w_p} \cos\left[(w_F - w_p)t + (a_F - a_1)\right] - \right.$$

$$-\frac{1}{2}\frac{A_1}{w_F+w_p}\cos\left[\left(w_F+w_p\right)t+\left(a_F+a_1\right)\right]\Bigg\}\Bigg|_{t_1}^{t_2} \quad (7)$$

$$\mathrm{Im}=\left\{\frac{1}{2}\frac{A_1}{w_F+w_p}\sin\left[\left(w_F+w_p\right)t+\left(a_F+a_1\right)\right]+\right.$$

$$-\frac{1}{2}\frac{A_1}{w_F-w_p}\sin\left[\left(w_F-w_p\right)t+\left(a_F-a_1\right)\right]\Bigg\}\Bigg|_{t_1}^{t_2} \quad (8)$$

As a result the two parts of the Fourier Coefficients Re(t) and Im(t) are shown in Fig. 5. One represents a sinusoidal function with a frequency equal to the sum of fundamental and Fourier Frequency and the other with the frequency resulting of the difference of these values. The amplitudes of these functions are inversely proportional to their frequencies. Based on these results the criteria for finding the fundamental frequency of the mains is the equality of fundamental and Fourier Frequency: the Fourier Frequency needs to be modified until coefficients consist only of the sinusoidal function representing the sum of the frequencies and an offset. Thus Fourier and fundamental frequency are equal. The remaining offset is representing the difference of the phase shifts of fundamental (a_1) and Fourier Function (a_F). By varying a_F to get the offset to zero a_F will equal a_1. Following w_F and a_F are used to generate the alternating reference for the inverter.

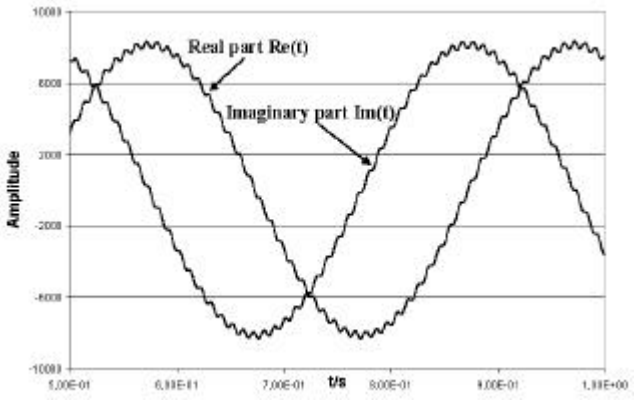


Fig. 5. Time graph of the Fourier Coefficients

IV. CONTROL IMPLEMENTATION

The described hardware platform is based on a low-cost TMS320LF2407 / 30 MHz DSP [13] connected to a XILINX Spartan XCS05 [14] running at 48 MHz.

All analog signals are measured by external 12bit ADCs to improve the speed and accuracy of the measurement procedure, because the internal ADC units of the DSP have only 10bit resolution. Fig. 6. shows a block diagram of the developed hardware platform.

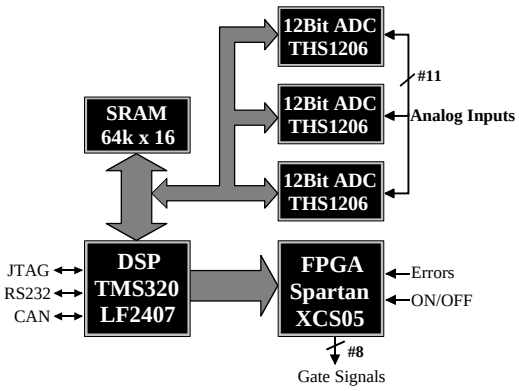


Fig. 6. Hardware platform

Using the DSP for PWM generation the On-Chip PWM channels turned out to be too slow for the dc-dc converter switching frequency of approximately 100 kHz with a resolution of at least 8 bit. So the FPGA was added to the design delivering almost 9 bit at 48 MHz.

Due to the limitation of computational power and the aim to implement all algorithms in one DSP the tasks had to be arranged in a time slicing method. That means to avoid conflicting access to DSP resources by different tasks there needs to be a certain amount of time for every algorithm to complete and after that starting the next. This has to be done in a way that every task is running at a constant frequency even to the appropriate measurements to be taken.

By letting the FPGA generate the PWM signals the newly computed duty cycle needs to be reloaded from the DSP. This happens at the same frequency the duty cycle is calculated. Using a synchronized topology the switching frequency is equal or a multitude of the control algorithm frequency. That combined with the time slice based multitasking leads to the following frequencies:

- Inverter PWM and regulation algorithm: 12 kHz using 12 bit resolution
- DC-DC converter regulation algorithm: 24 kHz
- DC-DC converter PWM: 96 kHz using 9 bit
- Synchronization to main net: 12 kHz

Fig. 7 shows the arrangement of those tasks:

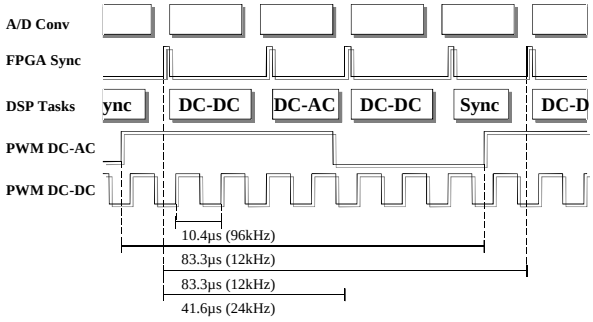


Fig. 7. Timing diagram

By arranging the tasks according to Fig. 7 it is ensured that every algorithm will be completed in time without any concurrence between any of them. The start of such a frame is initiated by an interrupt signal sent from the FPGA every fourth pulse of the dc-dc converter (24kHz = 41.6µs). Beginning with the transfer of the digitized measurement data to the DSP the control algorithm for the boost converter is computed. After finishing this task the DSP is waiting for the next interrupt from the FPGA signalizing the measurement data for the inverter is to be read. Continuing with the belonging algorithm the DSP is set in wait mode again. Following another run of the dc-dc converter algorithm is the synchronization task.

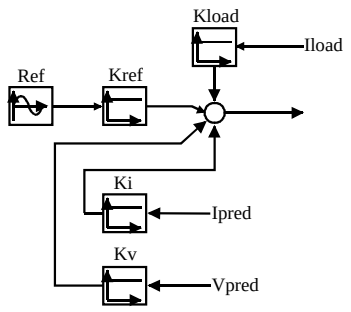
Communication between the DSP and the peripherals is done using the external memory interface of the processor.

For the calculation of the PWM and synchronization at first AD conversions of the measurement signals need to be done. Table I shows which signals are simultaneously to be measured and their appendant sample frequency.

TABLE I
ANALOG INPUT SIGNALS

Task	Signals	Sampling rate
DC-DC	$V_{DC\text{-}LINK} = V_{DC\text{-}LINK1} + V_{DC\text{-}LINK2}$ V_{BAT}	24kHz
DC-AC	$V_{C\text{-}OUT1}$, $V_{C\text{-}OUT2}$ $\Delta V_{DC\text{-}LINK}^{*} = V_{DC\text{-}LINK1} - V_{DC\text{-}LINK2}$ I_{LOAD1}, I_{LOAD2} I_{L1}, I_{L2}	12kHz
Sync	V_{MAINS}	12kHz

To fulfil the named realtime demands programming is completely done in assembler.




```
          .data              ; DATA MEMORY
Ref:      .word 0000h        ; Alternating voltage reference
Ipred:    .word 0000h        ; Predicted inductor current
Vpred:    .word 0000h        ; Predicted output voltage
Iload:    .word 0000h        ; Load current

          .text              ; PROGRAM MEMORY
Kref:     .word xxxxh        ; Reference gain
Ki:       .word xxxxh        ; Inductor current gain
Kv:       .word xxxxh        ; Output voltage gain
Kload:    .word xxxxh        ; Disturbance variable feedforward gain

          .
          .
          .
Adding:                      ; ASSEMBLER PROGRAM
          LAR   AR0, #Ref    ; Load Auxiliary Register 0 with Pointer to Ref
          LARP  AR0          ; Load Auxiliary Register Pointer with AR0
          RPT   #03          ; Repeat the following command 3 (+1) times
          MAC   Kref, *+     ; Multiply Ref with Kref and accumulate previous content of
                             ; P-register and increment program counter and AR0
          APAC               ; Add content of P-register to accumulator
```

Fig. 8. Assembler listing

To increase the program speed and referring to the basic structure of the control algorithms an extensive use of the *MAC* command was made to implement the algorithms according to Fig. 3 and 4. Combined with the *RPT* instruction this leads to one-cycle multiply and accumulate of two 16 bit arguments delivering a 32 bit result accelering the program execution [15]. Fig. 8 shows an assembler listing for the calculation of the control variable for the inverter state feedback.

To verify the timing and to validate the principle of operation of the control unit the complete UPS-structure has been simulated using SIMPLORER®. All measurement signals in the simulation were stored and then transfered to the control unit, which had to pass the gate signals for the main switches back to the simulation. Fig. 9 shows as an example the corresponding output waveforms of the inverter generating a 230V/50Hz voltage on nominal resistive load conditions.

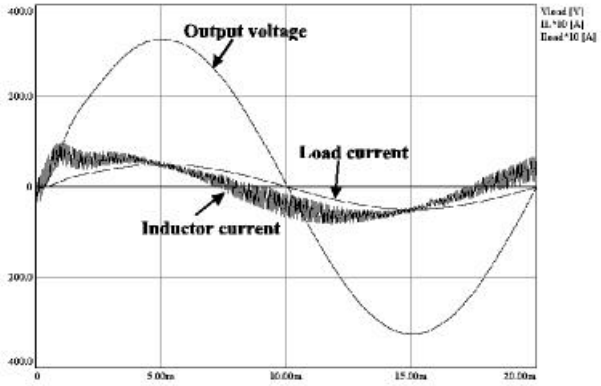


Fig. 9. Simulated waveforms of the inverter

The results show the ability of the proposed system to work as a digital control system for UPS applications. The higher resolution of the used external Analog-to-Digital Converters leads to an improved dynamics and steady state accuracy of the generated output voltage.

V. CONCLUSION

In this paper some implementation aspects of digital control algorithms for a cascaded converter system were discussed. Based on the developed feedback laws and a low-cost hardware solution the segmentation into the different tasks was demonstrated. Special attention was given to the real time demands and the opportunities in programming the applied components. The enlargement of the peripheral assemblies like the external ADC units and the PWM-channels, implemented by a programmable logic device, makes it possible to use small low-cost processors for a multitasking system, which is required in cascaded converter systems.

The presented hardware platform is also suitable for other power electronic converters and converter systems.

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