An Integrated Class-D Audio Power Amplifier Using Standard CMOS Technology

Paulo Augusto Dal Fabbro[1], Murilo Pilon Pessatti[1], José Antenor Pomilio[2] and Saulo Finco[3]

[1]Dept. of Semiconductors, Instruments and Photonics – DSIF
[2]Dept. of Energy Control and Systems – DSCE
School of Electrical and Computer Engineering – FEEC
State University of Campinas – UNICAMP
Av. Albert Einsten, 400 – 13083-970 – Campinas – SP – Brazil
pauloau@hotmail.com, mpessatti@hotmail.com, antenor@dsce.fee.unicamp.br

[3]National Institute of Information Technology – ITI
P.O. Box 6162 – 13089-500 – Campinas – SP – Brazil
saulo.finco@iti.br

Abstract - **A class-D audio power amplifier integrated using available standard CMOS technology is presented in this document. This amplifier is implemented in a single monolithic chip, which comprises both logical and power structures. Its intention is showing the possibility of using the concept Smart Power in technologies not developed specifically for it and for some applications with power ratings up to 1W.**

I. Introduction

Packaging reduction and increasing efficiency is becoming mandatory in most of the applications in electronics industry nowadays, including the extensive use of audio amplifiers with power ranging from 0.1 to 1W in notebooks, wireless speakers, and hearing aids. Taking into account these two issues, an integrated class-D audio power amplifier becomes an attractive solution in comparison to the common class-AB power amplifiers due to its high efficiency. In order to integrate power elements and control logic altogether, a new microelectronic fabrication technology emerged in the eighties, which made possible to have the integration of standard and power transistors in a single monolithic chip. This technology is called *Smart Power* [1]. However, it is passing through a maturing process that makes its access not so trivial as the standard CMOS technology due mainly to its cost and also to its higher complexity. To carry out this dilemma, the use of available standard CMOS technology with some arrangements to bear higher voltages and currents has shown to be a reasonable solution [2]. In this context, this document proposes the implementation of an integrated class-D audio power amplifier using standard CMOS technology.

II. Achieving Power Needs

The standard CMOS microelectronic technology has some fabrication characteristics that make it not appropriate to power integration. Commonly, its analog and digital CMOS devices support a maximum voltage level of 5V due to the physical fabrication characteristics of the PN junctions and gate oxide thickness. To achieve a voltage level of up to 35V, that can be useful in some power applications, two main problems must be solved: the avalanche rupture of PN junctions and gate oxide rupture.

The first one can be minimized in standard technology using the n-well region, which is intended to be primarily the substrate of PMOS transistors. The low concentration of free electron carriers of this region is used to interface the P region to the N one, allowing the PN junction to be submitted to higher voltages without suffering avalanche rupture [3]. The other one is the proximity of the gate edges with the drain and source due to a thin and short oxide layer, that makes standard technology support low voltage levels between gate-drain terminals without exhibiting oxide rupture. This is because the thin and short oxide concentrates the electric field, making the gate-drain interface not ideal for use in voltages higher than 5V. A solution in this kind of technology for this problem is making the oxide gate thicker and longer in the gate-drain overlapping region, minimizing though the electric field in this region and allowing the application of up to 35V on the device.

Fig. 1 shows the LDD-NMOS (Light Doped Drain NMOS) transistor improved to support higher voltages. In the figure the n-well region that is normally used as bulk for PMOS transistors can be observed as the DRAIN-WELL region and the longer and thicker gate-drain oxide that overlaps the drain is also shown. In this project, the symmetric version of the LDD, called LDSD (Light Doped Source and Drain) was used for the power transistors.

It is worth to remember that the inclusion of the n-well region increases the conduction resistance of the channel due to its higher resistivity. Paralleling MOSFETs is possible to minimize this effect, once the equivalent channel resistance decreases. Another improvement with this configuration is the possibility of having higher current levels since the density current in each device is lower when the number of paralleled devices increases.

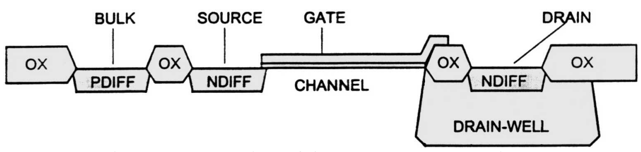

Fig. 1. Cross-section of the LDD-NMOS transistor.

III. THE AUDIO AMPLIFIER

A class-D topology of amplifier was chosen because of its efficiency of typically 80% - with possibility to be increased up to 90% in optimized systems - what facilitates its integration. High efficiency is due to the operation of the output power transistors as switches. They are always either totally on or totally off, making the power dissipation as low as possible. The basic operation of a class-D amplifier can be described as follows: the audio signal to be amplified is compared to a sawtooth waveform resulting in a square signal with frequency equal to the sawtooth waveform and pulse width proportional to the amplitude of the audio signal [4]. This pulse width modulated (PWM) signal is then used to drive the output power transistors. The output of this arrangement of transistors is connected to the load (speaker) after being filtered by a common passive filter. The configuration used to implement the class-D amplifier here proposed comprises two stages divided by their power ratings, although they share the same die: an input stage composed by a pre-amplifier and a pulse width modulation (PWM) signal generator, and an output stage that contains a gate drive circuit and the output power transistors.

A. Input Stage

Two important features are performed by the input stage: the conditioning of the input audio signal and its modulation for driving the output stage.

In order to accomplish these basic functions, the input stage is comprised of a pre-amplifier, a sawtooth wave generator and a comparator as shown in the block diagram of Fig. 2. The pre-amplifier in turn is composed by a simple operational amplifier that provides a volume control for the audio signal and adequate its DC level, allowing its comparison to the sawtooth wave. The sawtooth wave is generated internally using two current sources and an oscillator with logic control.

The comparison between the signals above mentioned results in a PWM signal with a frequency equal to the sawtooth waveform and a pulse width proportional to the amplitude of the audio signal. This signal and its inverted counterpart will drive the output stage.

B. Output Stage

The power amplification of the PWM signal is provided by a H-bridge of power MOSFETs as depicted in the block diagram of Fig. 2. They use the layout configurations described in section II to achieve the power requirements.

A level shifter supplied by a charge pump is used to drive the high side transistors of the bridge. This ensures that the gate voltage will be sufficiently higher than the source voltage and thus will properly drive these power MOSFETs. The low side transistors are driven directly from the PWM generator output as they do not require special treatment since their source terminals are grounded.

The power transistors are driven in such a way that the current through the load flows in both directions and therefore the output voltage signal exhibits dual polarity what is desired for proper operation of the speaker.

To accomplish this, the PWM signal drives M2 and M3 (through one level shifter) and the inverted PWM signal drives M1 (through the other level shifter) and M4. Then, the overall operation is: when M2- M3 are turned on (M1-M4 turned off) the current flows in a opposite way than when M1-M4 are in conduction (M2-M3 turned off).

The last part of the output stage is the filter, which is responsible for drastically reducing the undesired switching component and reconstituting the original audio signal at the speaker terminals

Now, a consideration about the PWM signal frequency is pertinent. In order to correctly represent an audio signal, the PWM signal must have a frequency about 250kHz, considering the whole audio frequency range. This ensures that the output filter eliminates all the modulating frequency components and just keeps the frequency components of the input, applying it to the speaker. Although it was stated before that the output transistors operating as switches makes the power dissipation very low, this becomes not true when the switching frequency and power needs increase above a certain value. This happens because the dissipation in the transition between on and off states of the transistors becomes considerable. Taking into account all this, the main audio frequency range target of this project was chosen to be the voice band, which ranges from 300Hz to 3kHz.

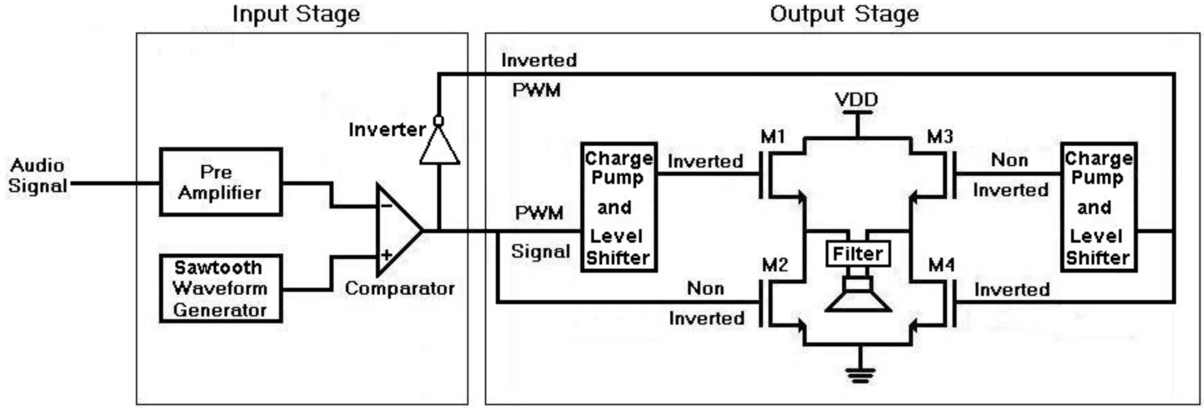

Fig. 2. The audio power amplifier block diagram

A potential application for this amplifier is a hands-free telephone kit that is used in cars for safety and comfort issues. Considering this frequency range, the current limit of the power transistors and the maximum power dissipation of the die, up to 1W of power can be delivered to the speaker.

IV. The Integrated Circuit Layout

In order to integrate the audio power amplifier, an array of power MOSFETs was designed together with some other blocks constituted by standard transistors, forming a matrix of integrated devices in a single chip. These other blocks are operational amplifiers, comparators, current sources, inverters and NAND gates, which were used to implement the processing functions of the audio amplifier. The passive components and signal diodes used in the amplifier are not included in the chip and thus they were connected externally to it. Fig. 3 shows the layout of the matrix of the integrated devices.

Along all the perimeter of Fig. 3 are localized the pads for connection with the integrated circuit pins. The upper and bottom parts contain the blocks of standard transistors and the power transistors form the biggest region found in the middle. Some of the interconnection among the components inside the matrix will be also made externally to the chip. This allows the use of the integrated circuit for other power applications, since the blocks present in it are basic blocks used in a great variety of power electronic circuits.

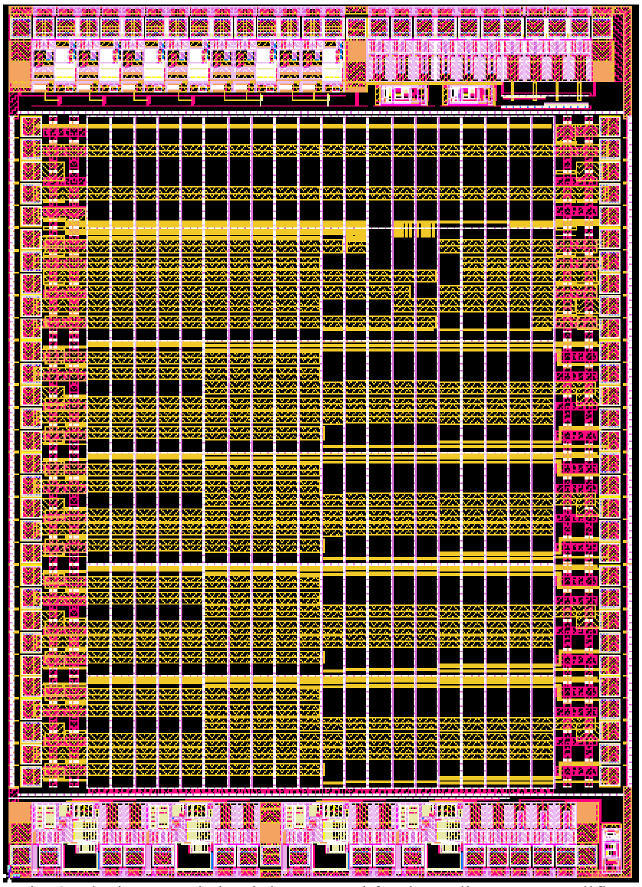

Fig. 3. The integrated circuit layout used for the audio power amplifier

V. Simulation and Experimental Results

A. Simulation Results

The projected circuit for the audio power amplifier was simulated using the models supplied by the foundry responsible for the chip manufacturing. The sources used in the circuit were a 5V-power supply for the input stage and a 12V-power supply for the output stage, what simplifies the use of this device in vehicles.

The obtained waveforms for the sawtooth wave generator and the PWM signal, which are the desired signals in this stage, can be observed in Fig. 4. Together with them, appears the 10kHz sine input signal (after pre-amplification) for a better visualization of the modulation scheme. The sawtooth wave has a frequency of 110kHz and varies from 1V to 4V. The PWM signal varies from 0V to 5V and its frequency is 110kHz too.

In the output stage, a charge pump was used, as mentioned earlier, to provide a 15V-voltage level from the 12V-power supply. A second order low pass passive filter was designed to have a –3dB cut-off frequency of 4kHz in order to recover signals with frequencies up to 3kHz and reject signals of upper frequencies, specifically the 110kHz modulation frequency.

The waveform of the output signal delivered to the 8Ω load obtained in the simulation is shown in Fig. 5 (top). The 1kHz sine input signal can also be observed in this same figure (bottom). A quick comparison of the two signals shows that the signal after amplification correct reproduces the original signal. In the output signal, one can notice the presence of a small ripple due to the residual 110kHz component not totally attenuated by the second order filter. Nevertheless, even if this component is present in the output signal it will not be listened because of its high frequency.

B. Experimental Results

The first step in this practical stage was testing the components inside the chip to certify if they were operating in a proper manner. After this was guaranteed, the input stage was tested in a breadboard with some passive components and signal diodes externally added. The waveforms obtained experimentally for the sawtooth generator and the PWM signal are shown in Fig. 6.

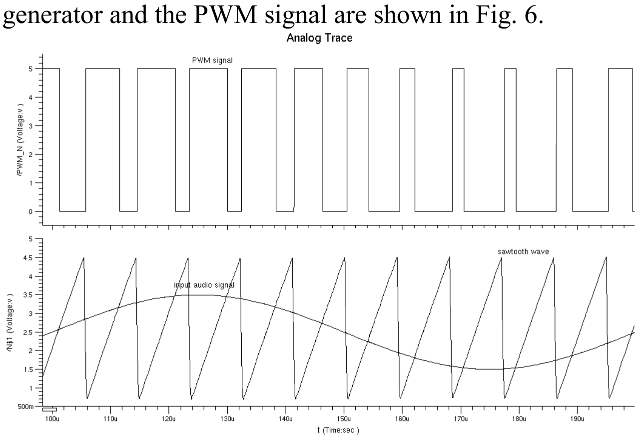

Fig. 4. Simulation waveforms for the input stage

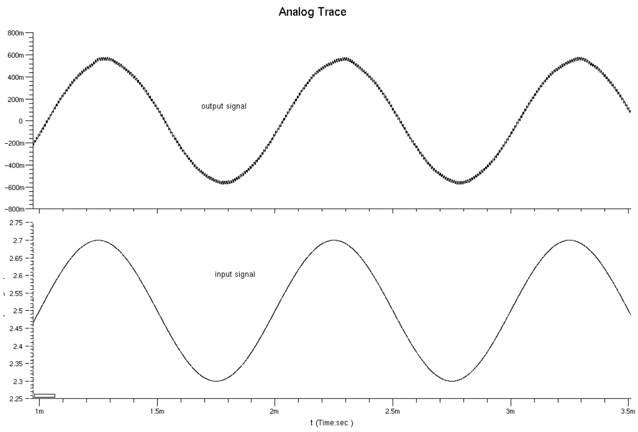

Fig. 5. Simulation waveforms for the output stage

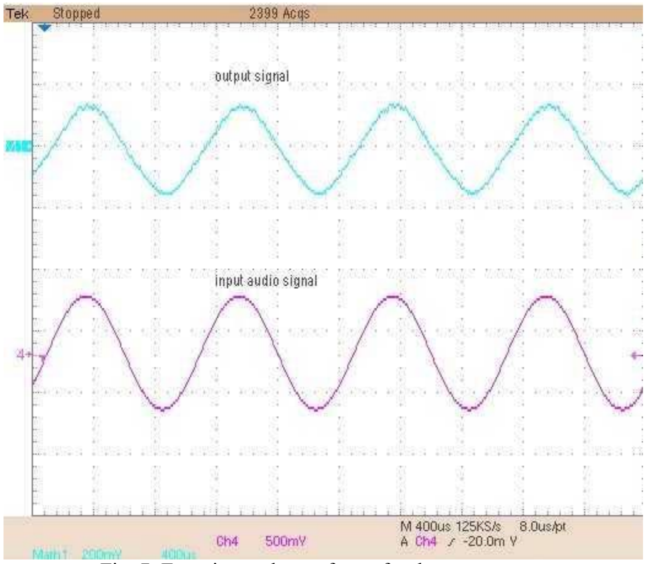

Fig. 7. Experimental waveforms for the output stage

It can be seen in Fig. 6 that the linearity of the sawtooth wave required for a good modulation of the input signal was achieved. Also, the PWM waveform is in accord with the theoretical expected result, showing the proper operation of the comparator.

Once the input stage was working properly, the output stage was attached to it completing the circuit for the audio amplifier. Before connecting the filter and the speaker, a 100Ω resistance was connected as the load to the power bridge. So, it was possible to test the power transistors and assure that they could deliver 1W of power to the load without overheating . Then the 100Ω load was replaced by the filter and a 8Ω speaker, and a 1kHz test sine wave was applied to the input of the amplifier. The output signal corresponding to this test can be observed in Fig. 7.

As shown in this figure, a small ripple in the output signal (top) was also observed in the practical implementation as was predicted by simulation. But the overall operation of the power amplifier is very satisfactory as it well reproduces the input test signal.

As a sine wave exhibits only one frequency component, it is useful to perform a real test where a wide range of audio frequencies is present altogether. In order to perform this test, nothing more realistic than amplifying the output of a CD player. Although this amplifier was designed for voice frequency range, this test is also valid as it puts the amplifier in a more exhaustive situation. The result of this test is shown in Fig. 8 and is very satisfactory.

VI. Conclusions

Considering the satisfactory quality of the audio power amplifier observed in the graphics found in section V, together with the low cost process involved in the fabrication of the chip and its power and voltage ratings, the use of this device in applications such as hands-free telephone car kits is very reasonable.

However, as this project lacks in some tests generally required for their use by the automotive industry, as is the case of total harmonic distortion (THD) and efficiency tests, it is not a commercial product and is still under study.

As was briefly exposed before, the integrated circuit used to implement this audio amplifier is a generic chip. Besides allowing its use in other applications, the main reason for its design was to serve as the working matter in

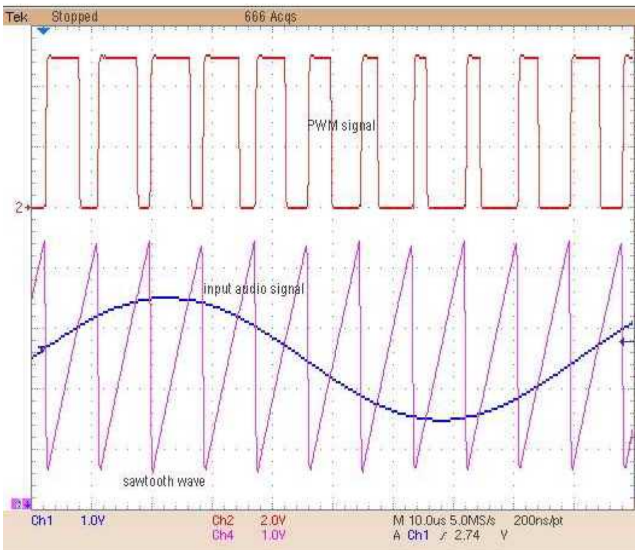

Fig. 6. Experimental waveforms for the input stage

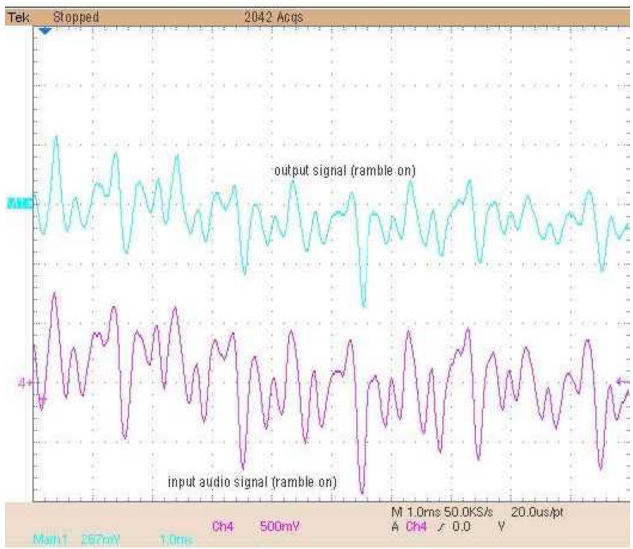

Fig. 8. Original (bottom) and amplified (top) versions of a small part of Led Zeppelin's song "Ramble On"

an experimental academic program for Smart Power training based in standard CMOS technology in which this project is included. Therefore, a successful result in the implementation of this integrated audio power amplifier is due to this program and even more, it shows that the program itself is very pertinent and valuable.

VII. Acknowledgements

The authors would like to thank Prof. Carlos Alberto dos Reis Filho for idealizing and turning this Smart Power training into a real program. Thanks are also to PMU (Programa Multi-Usuário) and CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico) for supporting the fabrication of the chip.

VIII. References

[1] B. J. Baliga, "An Overview of Smart Power Technology", *IEEE Trans. on Electron Devices,* vol. 38, no. 7, pp. 1569-1575, Jul. 1991.

[2] S. Finco, *Projeto de um Circuito Integrado Inteligente de Potência Implementado em Tecnologia Convencional CMOS*. Master Thesis, State University of Campinas (UNICAMP), no. F492P, Feb. 1996.

[3] A. Nakagawa, N. Yasuhara, and Y. Baba, "Breakdown Voltage Enhancement for Devices on Thin Silicon Layer/Silicon Dioxide Film" , *IEEE Trans. on Electron Devices*, vol. 38, no. 7, pp. 1650-1654, Jul. 1991.

[4] R. Palmer, "Design Considerations for Class-D Audio Power Amplifiers", *Application Report,* Texas Instruments, no. SLOA031, Aug. 1999.