An Optimum Loss Less Commutation PWM Two Level Forward Converter Operating like a Full Bridge

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***Abstract* - This paper presents an optimum topology for the combination of two forward structures, attached to the same transformer and operating like a full bridge. Transformer and output filter operating frequencies are twice of each forward switching frequency.**

Each one of the forward converters has a loss less commutation cell that allows for high switching frequency, high power operation and high efficiency to a wide load range.

I. Introduction

Isolated converters have been developed with high switching frequency in order to decrease the transformer size. Moreover, most of these converters use just one cycle of the transformer hysteresis, which does not make use of its full capacity. The proposed converter uses entire hysteresis cycle, resulting in a smaller transformer. The switching frequency is half of the operating frequency in the transformer.

Full-bridge topologies, which have the same characteristic [1,2,3,4], will be used like a comparison parameter.

II. Presenting the Proposed Converter

Fig. 1 presents the proposed converter.

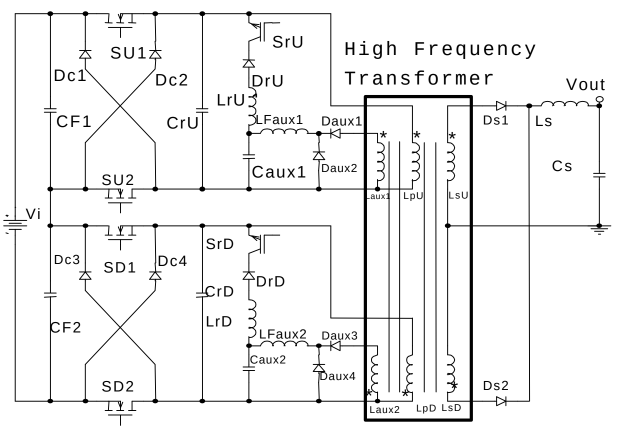


Fig. 1 – Proposed loss less Two Level Forward Converter.

Two forward structures, working in a complementary way, are used to achieve the full-bridge operation mode. The auxiliary switches, S_{rU} and S_{rD}, operate in ZCS mode to charge the resonant capacitors C_{rU} and C_{rD}, respectively. When these capacitors are charged to Vi/2 the main switches can turn-on ZVS mode. The use of only one resonant capacitor for each forward structure represents a gain in terms of reduction of components. Besides, the circuit control for this converter will not need to consider the “dead time”, that is required in full bridge controllers.

Further, an additional advantage of this converter, in comparison to those conventional full-bridges, is the reduced voltage over the main semiconductors equal to $V_{in}/2$.

Since, the forward converters work alternately, the operating frequency of each forward is reduced to half, $f_s/2$. Therefore, the switching losses are proportionally reduced, but the transformer and inductor frequency are still operating with f_s.

The components C_{aux1}, D_{aux1}, D_{aux2}, L_{Faux1}, L_{aux1} and C_{aux2}, D_{aux3}, D_{aux4}, L_{Faux2}, L_{aux2} implement two auxiliary DC sources needed by the resonant circuit, V_{aux1} and V_{aux2}. To make easier the operating stage analysis, the auxiliary voltage sources will be replaced by 2 DC voltage sources of Vi/4. These auxiliary DC voltage sources feed the load resonant circuit and the load with only 10% of the total power transferred to the load. This power is totally used to transfer energy to the load, which means that the energy used in the resonant circuit is also used to transfer power to the load.

A. Operating Principles.

In order to simplify the analysis, the following conditions are assumed:

- ‘I_c’ is the load current referenced to the primary winding of the high frequency transformer and it is constant.
- V_{AuxU} and V_{AuxD} must be, at least, equal to Vi/4 to guarantee that the C_{rU} and C_{rD} can reach Vi/2 during the resonance. V_{Aux1} and V_{Aux2} can be set to 1.3* Vi/4.
- C_{F1} and C_{F2} can be replaced by DC voltage sources of Vi/4 for one switching cycle.

Fig. 2 shows the main waveforms for this converter and Fig. 3 shows the equivalent circuit for each operating stage.

The analysis of the two forward converters is identical but phase shifted by the controller. So, it will be presented for only one of them.

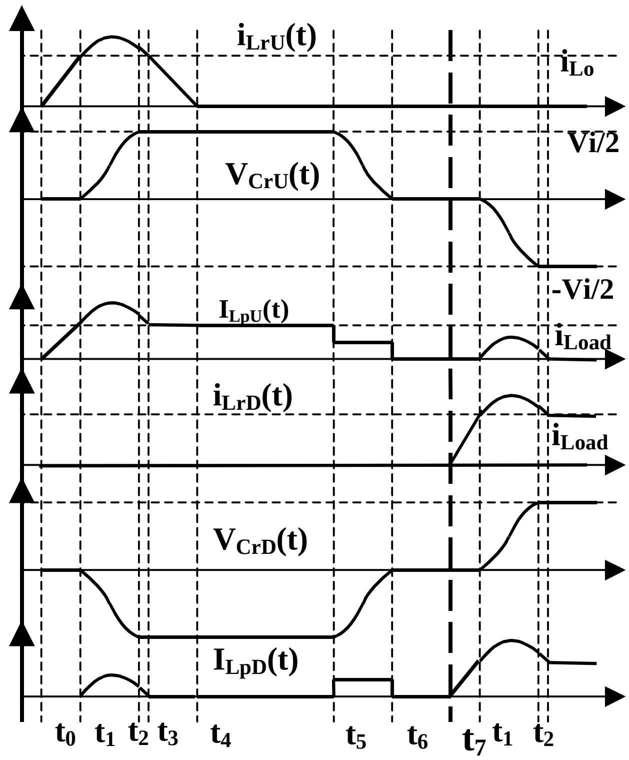


Fig. 2 – Main waveforms.

Stage 1 [$t_0 - t_1$] → Linear Stage

Fig. (3.a) presents the equivalent circuit for this stage. Before the beginning of this stage, Ds1 and Ds2 are conducting the load current, S_{U1}, S_{U2}, S_{D1} and S_{D2} are not conducting, C_{rU} and C_{rD} are discharged.

At $t = t_0$, S_{rU} is turned on in ZCS (Zero Current Switching) mode. The resonant current, $i_{LrU}(t)$, starts to increase linearly from zero to I_L, when this stage ends.

The secondary winding is in free welling until $i_{LrU}(t) = I_L$ at $t = t_1$. This stage can be mathematically described by (1).

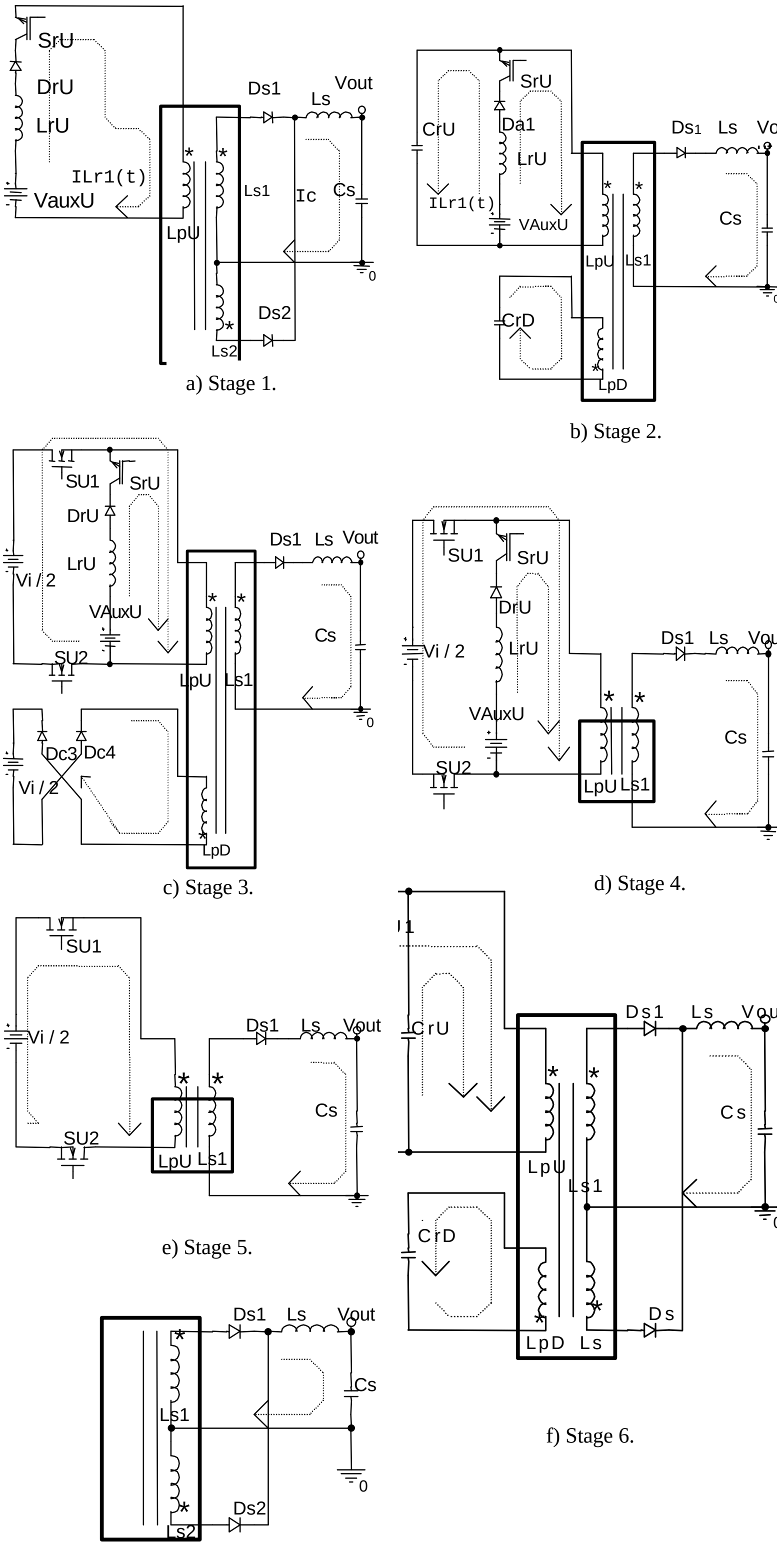
$$i_{LrU}(t) = \frac{V_{AuxU}}{L_{rU}} \cdot t \tag{1}$$

Stage 2 [$t_1 - t_2$] → Resonant Stage.

Figure (3.b) presents equivalent circuit for this stage. At $t = t_1$, C_{rU} starts to charge positively and C_{rD} starts to charge negatively.

During the time $i_{LrU}(t) > I_L$, L_{pD} starts to conduct the current $i_{LrD}(t)$ due to the induction of L_{pU} over L_{pD}. For this stage $i_{LrD}(t) = i_{LrU}(t) - I_L$.

This stage ends when $Vc_{rU}(t) = Vi/2$ and $Vc_{rD}(t) = -Vi/2$ at $t = t_2$, when S_{U1} and S_{U2} are turned-on in ZVS (zero voltage switching) mode.



a) Stage 1.

b) Stage 2.

c) Stage 3.

d) Stage 4.

e) Stage 5.

f) Stage 6.

g) Stage 7

Fig. 3 (a – b) Operating Stages.

This stage can be mathematically described by (2) and (3), (4) and (5).

$$i_{LrU}(t) = I_c + \frac{V_{AuxU}}{Z_o}\,\text{sen}(w_o \cdot t) \qquad (2)$$

$$Z_o = \sqrt{\frac{L_{rU}}{2 * C_{rU}}} = \sqrt{\frac{L_{rD}}{2 * C_{rD}}} \qquad (3)$$

$$V_{AuxU} = k \cdot \frac{V_{in}}{4} \qquad (4)$$

$$v_{CrU}(t) = k \cdot \frac{V_{in}}{4} \cdot \left(1 - \cos(w_o \cdot t)\right) \qquad (5)$$

Stage 3 [$t_2 - t_3$] → Linear.

Fig. (3.c) presents the equivalent circuit for this stage. If V_{AuxU} and V_{AuxD} were equal to Vi/4, this stage would not exist. For practical circuits, V_{AuxU} and V_{AuxU} must be higher than Vi/4 due to conduction losses. Since V_{AuxU} and V_{AuxU} are higher than Vi/4, the current $i_{LdP}(t_2) \neq 0$. This stage exists to let $i_{LrD}(t)$ reach zero. When $i_{LrD}(t) = 0$ at $t = t_3$ the stage ends.

In the winding L_{pD}, diodes Dc_3 and Dc_4 conduct the remaining current. These diodes clamp $Vc_{rD}(t)$ at –Vi/4.

In the winding L_{pU}, $i_{LpU}(t) = I_L$ again at $t = t_3$.

S_{U1} and S_{U2} are turned-on at $t = t_3$ but they will not get into conduction until $i_{LrD}(t) = I_L$ at $t = t_3$. They are turned-on at $t = t_2$ to facilitate the control.

This stage can be mathematically described by (6).

$$i_{LrU}(t) = \left[I_c + \frac{k \cdot V_{in}/4}{Z_o} \cdot \left[1 - \frac{k-1}{k}\right]\right] - \frac{V_{in}(k-2)}{4 \cdot Lr} \cdot t \qquad (6)$$

Stage 4 [$t_3 - t_4$] → Linear

Figure (3.d) presents the equivalent circuit for this stage. In this stage, the source starts to feed the load. The current in S_{U1} and S_{U2} starts to increase linearly from zero to I_L and $i_{LrU}(t)$ decreases linearly from I_L to zero.

This stage ends when $i_{LrU}(t) = 0$ at $t = t_4$ and S_{rU} is turned-off in ZCS mode.

This stage can be mathematically described by (7).

$$i_{LrU}(t) = I_c - \frac{V_{in}(k-2)}{4 \cdot Lr} \cdot t \qquad (7)$$

Stage 5 [$t_4 - t_5$] → Feeding the load

Figure (3.e) presents the equivalent circuit for this stage. In this stage, the source feeds completely the load. The PWM (pulse width modulation) controller defines the time duration of this stage. This stage ends at $t = t_5$ when S_{U1} and S_{U2} are turned-off.

Stage 6 [$t_5 - t_6$] → Linear.

Figure (3.f) presents the equivalent circuit for this stage. This stage represents the soft turn-off of S_{U1} and S_{U2}. Capacitor C_{rU} discharges linearly from Vi/2 to zero and capacitor C_{rD} discharges linearly from-Vi/2 to zero.

This stage can be mathematically described by (8).

$$v_{CrU}(t) = \frac{V_{in}}{2} - \frac{I_c}{2 \cdot Cr} \cdot t \qquad (8)$$

Stage 7 [$t_6 - t_7$] → Free wheeling

Figure (3.f) presents the equivalent circuit for this stage. On this stage all main switches are turned-off. The controller defines the operation time of this stage.

III. SIMULATION RESULTS

The proposed converter has been simulated with the following parameters:

- C_{rU} and C_{rD} = 2.2nF
- L_{rU} and L_{rD} = 2μH
- C_{F1} and C_{F2} = 330μF
- V_{in} = 400V
- L_{sU} and L_{sD} = 600μH
- L_{AuxU} and L_{AuxD} = 600μH
- L_{pU} and L_{pD} = 1mH
- P_{Out} = 2400W
- L_{FauxU} and L_{FauxD} = 50μH
- C_{FauxU} and C_{FauxD} = 33μF
- L_S = 50μH
- C_S = 100μF

A frequency of 75kHz has been adjusted for each forward converter. Fig. 4 presents the main waveforms in the resonant elements. The peak values of $i_{LrU}(t)$ and $i_{LrD}(t)$ are depended from the load current and from $L_{rU} - C_{rU}$ and $L_{rD} - C_{rD}$, respectively. These elements can be calculated to make it as low as possible to reduce the conduction losses in S_{Aux1} and S_{Aux2}.

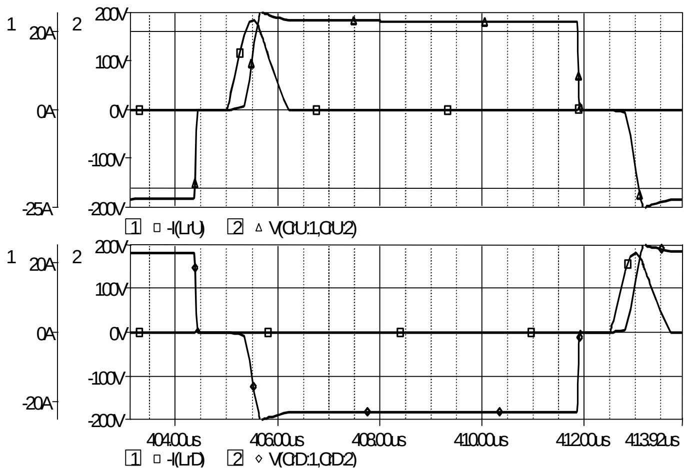


Fig. 4 – Main waveforms in the resonant elements.

Fig. 5 presents the switching details of the main switches S_{U1} and S_{D1}. S_{U2} and S_{D2} have the same operation of S_{U1} and S_{D1}, respectively. All main switches are turned on and off in ZVS mode.

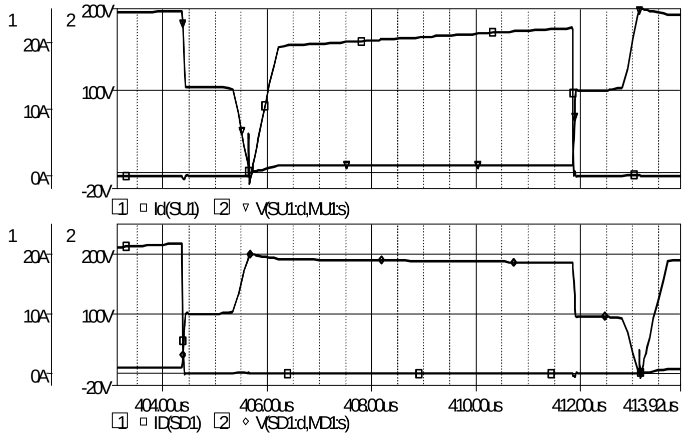


Fig. 5 – Switching detail of S_{U1} and S_{D1}

Fig. 6 presents switching details for auxiliary switches S_{Aux1} and S_{Aux2}. Both are turned on and off in ZCS mode.

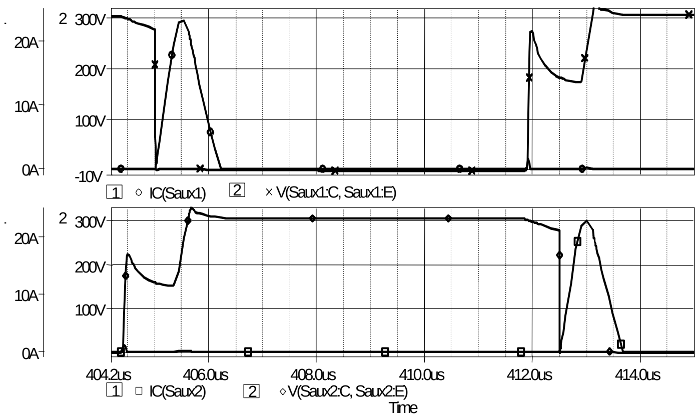


Fig. 6 – Switching detail of S_{rU} and S_{rD}.

IV. CONCLUSIONS

This paper proposed an optimum converter that, as a full bridge, uses all the hysteresis cycle of the transformer, with an easy implementation commutation cell. The main advantages over the conventional full bridge are the decrease of the voltage over the main switches and the easier control.

V. REFERENCES

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