A Family of Unit Power Factor Active Clamping Single Phase Three Level Rectifier

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***Abstract* – This paper introduces a family of single phase rectifier, which present the following features: unit power factor, regulation by PWM technique, ZVS commutation and clamping action in all converter switches, instantaneous average input current control and output regulation. Each converter consist of a single-phase three level rectifier incorporated with a ZVS-PWM, Buck, Boost and Buck-Boost Active Clamping converter cell. Experimental results are presented, take from a designed prototype for 1.6 kW output power, input RMS voltage 127 V, output DC voltage 800 V, and operating at 40 kHZ.**

I. INTRODUCTION

In power factor correction one of the most common circuit used is the full bridge diode rectifier associated with a boost converter [1].

Substantial power dissipation occurs in the switch because it is subjected simultaneously to increasing current and full output voltage, during turn on commutation. Besides, the reverse recovery mechanism in the boost diode produces high di/dt and high current peak through the switch. Since the switch is specified for high voltage it normally has high conduction resistance. The current always flows through three power semiconductors simultaneously causing appreciable conduction losses, thus this converter presents low efficiency

A single phase three level rectifier, see Fig. 1, can be advantageous for many applications. In this converter only half of the output voltage is applied across the switch and current flows through only one or two power semiconductors simultaneously. Therefore this converter presents less conduction losses.

Active clamping technique has been employed to solve commutations problems in boost based converters and increasing its efficiency [2].

The Buck-Boost active clamping boost based rectifier [3] was proposed to replace a conventional hard switch boost based high power factor rectifier. This converter presents ZVS commutation in both switches, without significant increasing in circulating energy inside the converter.

This paper introduces a family of single-phase three level rectifier version with ZVS commutation for all switches, employing the active clamping technique. The proposed family of rectifiers was obtained from the fundamentals buck, boost and buck-boost active clamping commutation cells, described in [2]. Fig. 2 shows the fundamentals cells. The buck, boost and buck-boost cells based rectifiers, converters are shown in Fig. 3,4 and 5 respectively.

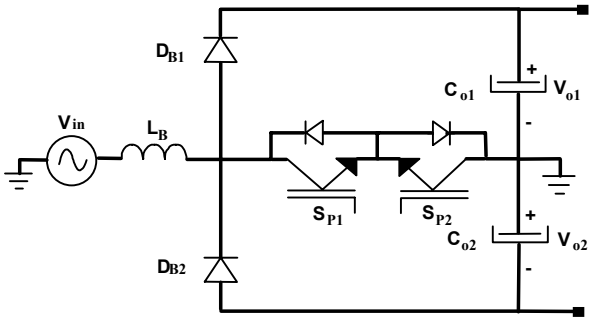


Fig. 1.Single phase three level rectifier

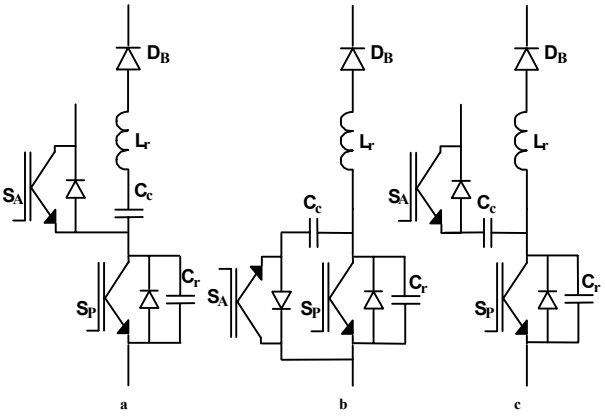


Fig. 2. Active Clamping commutation cells: a) buck cell; - b) boost cell; - c)buck-boost cell.

Principles of operation and circuit description are presented in sections II, simplified design example in section III and finally, results from a laboratory prototype and conclusion about this converter are described in sections IV and V respectively.

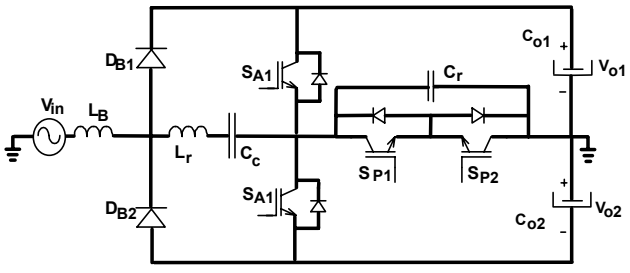


Fig. 3. Buck cell based rectifier.

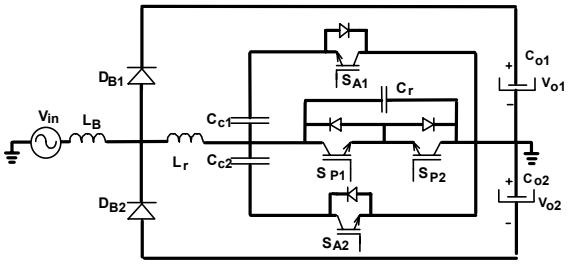


Fig. 4. Boost cell based rectifier.

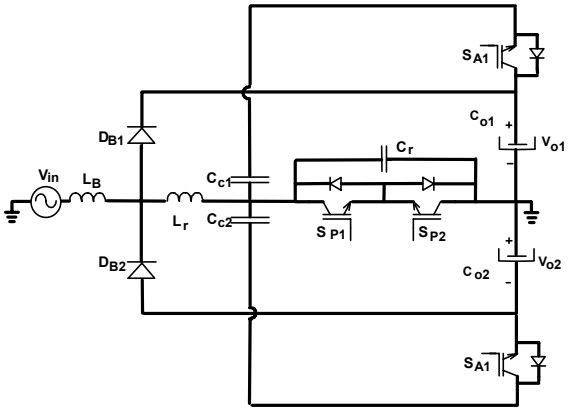


Fig. 5. Buck-boost cell based rectifier.

II. Principle of Operation and Circuit Description

To operate with unit power factor the Unitrod PFC controller, UC3854 [4], was used. It was possible because the converter operates in continuous current mode with constant switching frequency.

The block diagram, including converter power stage and control, for a buck-boost based rectifier, is shown in Fig. 6.

In this approach the gate signals in switches S_{P1} and S_{A1} are complementary and it's occur in the interval $0 \le \theta \le \pi$, and S_{P2} is kept turned on and S_{A2} turned off. In the other hand, during the interval $\pi \le \theta \le 2 \cdot \pi$, the switches S_{P2} and S_{A2} are commutating in complementary form, S_{P1} is kept turned on and S_{A1} turned off.

Input voltage and current are sinusoidal waveforms, then we have:

$$V_{in}(\theta) = V_{inpk} \cdot sin(\theta) \qquad (1)$$

And

$$I_{in}(\theta) = I_{inpk} \cdot sin(\theta) \qquad (2)$$

Where:

$$\theta = \omega \cdot t \quad \text{and} \quad \omega \cdot t = 2 \cdot \pi \cdot 60 \qquad (3)$$

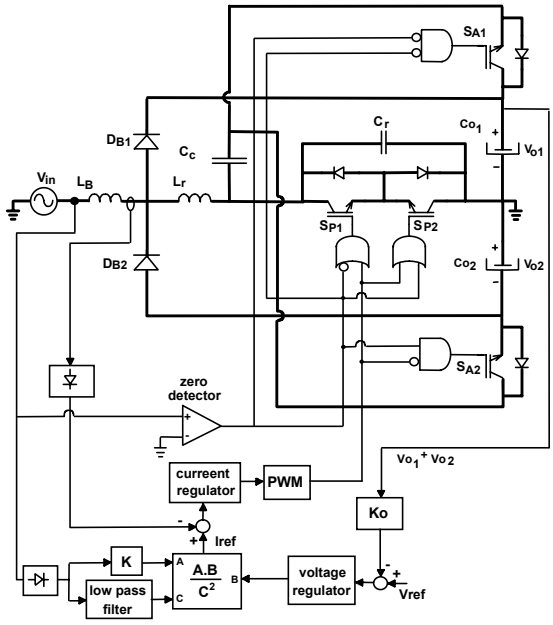


Fig.6. Complete block diagram of the power stage and control circuit for buck-boost based rectifier

A. Stages of Operation

The following simplifications are made to the commutation stages analysis:

1) Input voltage source and boost inductor are represented by a constant current source, I_S;

2) Output stages are represented by constant voltage sources, V_{o1}, V_{o2};

3) The capacitor C_c is selected to have a large capacitance so that the voltage V_C across the capacitor C_c could be considered as a constant one.

Stage 1 (t_0-t_1): at $t=t_0$ the main switch is turned off and the capacitor C_r is linearly charged by I_s to V_{o1}. Due to the presence of C_r, S_{P1} is turned off with no switching loss.

Stage 2 (t_1-t_2): when the voltage across C_r equal V_{o1}, the boost diode D_{B1} starts conducting. The current through L_r and C_r evolves in a resonant way and V_{Cr} rises from V_{o1} up to $V_o + V_C$. After that, the voltages are clamped.

Stage 3 (t_2-t_3): the diode D_{A1} starts conducting when V_{Cr} reaches $V_o + V_C$ at $t=t_2$. The voltage across S_{A2} is zero then its turns on with out loss. The L_r current ramps down util it reaches zero, when it changes its direction and rises again. This stage ends when S_{A1} is turned off at $t=t_3$.

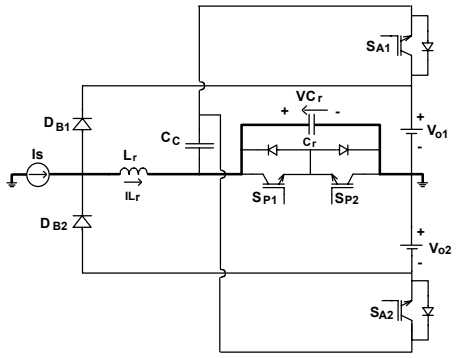
Stage 4 (t_3-t_4): The voltage across C_r decreases, due the resonance between L_r e C_r until its reaches zero at $t=t_4$.

Stage 5 (t_4-t_5): at $t=t_4$ S_{P1} is turned on with no switch loss, because V_{Cr} became null. The current through L_r changes its polarity and ramps up to reaches I_S, when the boost diode D_{B1} becomes reversibly biased.

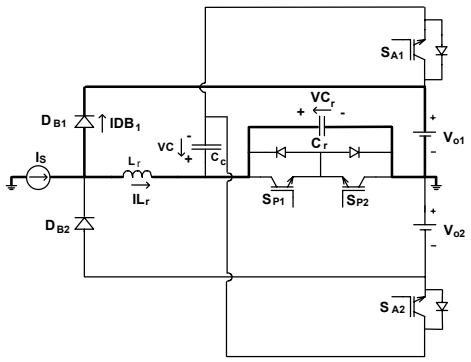
Stage 6 (t_5- t_0):after D_{B1} turns off the input current flows through S_{P1} and power is not transferred to the load. This stage ends when S_{P1} is turned off at the end of switching cycle.

The six topological stages are shown in Fig. 7. In those figures it can be seen that the two switches are switched in a complementary way.

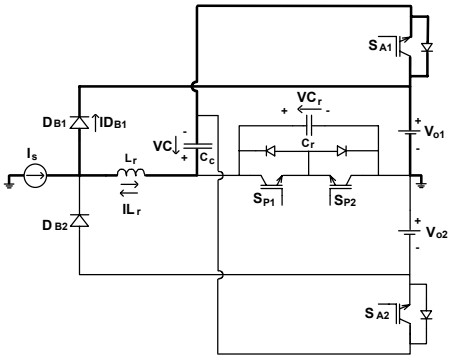
Fig. 8 shows the relevant waveforms to commutation analysis.



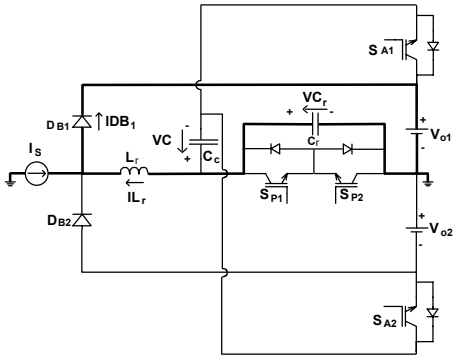
Stage 1 (t_0-t_1)



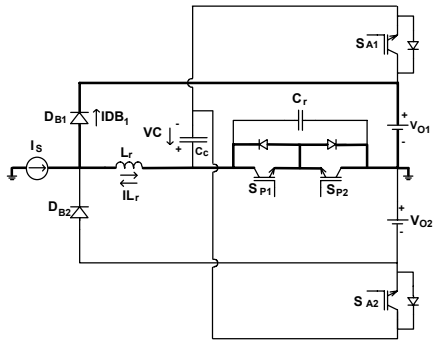
Stage 2 (t_1-t_2)



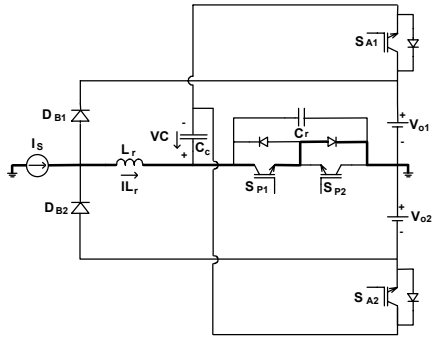
Stage 3 (t_2-t_3)



Stage 4 (t_3-t_4)



Stage 5 (t_4-t_5)



Stage 6 (t_5-t_0)

Fig. 7. Stages of operation

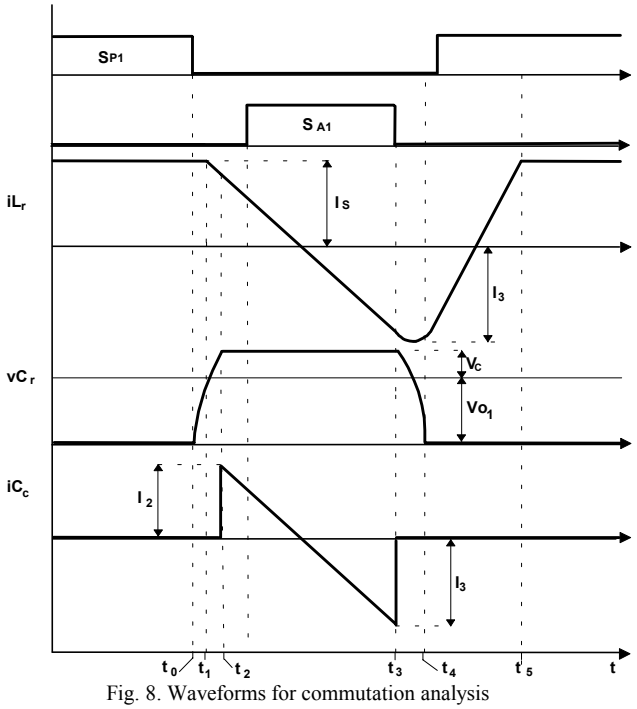


Fig. 8. Waveforms for commutation analysis

B. DC voltage clamping and DC voltage conversion ration

Since the time intervals $(t_1 - t_0)$, $(t_2 - t_1)$ and $(t_4 - t_3)$ are very short, in relation to the switching period, they will no be considered in this analysis. Thus, the current through C_c capacitor can be considerate:

$$I_2 = I_{in}(\theta) \tag{4}$$

In a commutation cycle the average current through clamping capacitor is zero, then:

$$\int_0^{[1-D(\theta)]}\left[I_{in}(\theta)-\frac{V_C(\theta)}{L_r}\cdot t\right]dt=0 \quad (5)$$

Then

$$\beta=\frac{V_C(\theta)}{V_{o1}}=\frac{\Delta D(\theta)}{[1-D(\theta)]} \quad (6)$$

Where

$$\Delta D(\theta)=\frac{2\cdot L_r\cdot I_{in}(\theta)}{V_{o1}\cdot T_s} \quad (7)$$

is the duty cycle reduction.

The average voltage across the boost inductor, L_B must be zero in a commutation cycle, thus DC voltage conversion ratio is given by:

$$\frac{V_{o1}}{V_{in}(\theta)}=\frac{1}{[1-(D(\theta)-\Delta D(\theta))]} \quad (8)$$

From (8) we can know how duty cycle vary in a input voltage half cycle:

$$\Delta D(\theta)=1-\left[\frac{V_{inpk}}{Vo1}-\Delta D_{pk}\right]\cdot sin(\theta) \quad (9)$$

Where:

$$\Delta D_{pk}=\frac{2\cdot L_r\cdot I_{inpk}}{V_{o1}\cdot T_s} \quad (10)$$

is the maximum duty cycle reduction in input voltage half cycle.

From (7), (9) and(10) it is possible to determinate that the clamping voltage is constant for a input voltage half cycle, as

$$V_C(\theta)=\frac{V_{o1}\cdot\Delta D_{pk}}{\frac{V_{inpk}}{V_{o1}}-\Delta D_{pk}} \quad (11)$$

C. Commutation Analysis

For the correct operation of the converter according to the stages described above, the passive elements, L_r and C_r, must be projected as following:

- In stage 3, the energy accumulated in L_r must be enough

to discharge the capacitor C_r, from $V_o + V_C$ to zero. Thus, from energy relationships in L_r and C_r, at $t=t_3$ we have:

$$\frac{1}{2}\cdot L_r\cdot\left[(I_{inpk})^2\cdot sin^2(\theta_{min})\right]>\frac{1}{2}\cdot C_r\cdot(V_{o1}+V_C)^2 \quad (12)$$

Where θ_{min} define the minimum input current limit for soft commutation, then:

$$\sqrt{\frac{L_r}{C_r}}>\frac{V_C+V_{o1}}{I_{inpk}\cdot sin(\theta_{min})^2} \quad (13)$$

III. Simplified Design Example

A simplified design example is described in this section, according to the analysis presented in Section II. The specification are as follows:

V_{inef}=127 V RMS (input voltage); V_{o1}=V_{o2}= 400 V (output voltage); P_o=1600 W (output power); f_s= 40kHz (switching frequency).

Choosing $V_C=80V$, and $\theta_{min}=30^o$ then:

$$\Delta D_{pk}=\frac{V_C}{\frac{V_{o1}}{V_{inpk}}\cdot\left(V_{inpk}+V_C\right)}=0.075$$

Once the claming voltage, θ_{min} and maximum duty cycle reduction are defined, resonant inductor and capacitor are calculated

$$L_r=\frac{\Delta D_{pk}\cdot V_{o1}}{2\cdot I_{inpk}\cdot f_s}=20\cdot\mu H$$

$$C_r<\frac{L_r\cdot I_{inpk}\cdot sin(\theta_{min})^2}{V_C+V_{o1}}<7.6nF$$

IV. Experimental Results

In order to verify the principle of operation the designed prototype was built. The parameter and power components specifications are as follows:

Switches S_{P1}, S_{A1}, S_{P2} and S_{A2}: IGBT's IRG4PF50W

All diodes MUR8100

Clamping capacitor C_c: 2.2 µF / 250 V

Resonant capacitor C_r: 4.1 nF / 1.6 kV

Output filter capacitor C_{o1} and C_{o2}: 660 µF / 450 V

Resonant inductor L_r: 20 µH

Input filter inductor L_B: 650 µH

Experimentally obtained waveforms of input current and input voltage for the prototype operant at full load are shown in Fig. 9. It can be noted that the converter operates with a high power factor.

Fig. 10 shows output voltages V_{o1} and V_{o2}.

Fig. 11 shows the current through resonant inductor and voltage across the resonant capacitor. Those waveforms agree with those predicted theoretically.

Fig. 12 shows the voltage across the switch S_{P1} and the current through the switch S_{P1}, and as can be noted from these waveforms, the mains switches (S_{P1} and S_{P2}) presents ZVS commutation and its voltages are clamped at a specified value.

In Fig. 13 a detail of the switch S_{P1} turn-off process is show. Fig. 14 shows a detail of the switch S_{P1} turn-on process

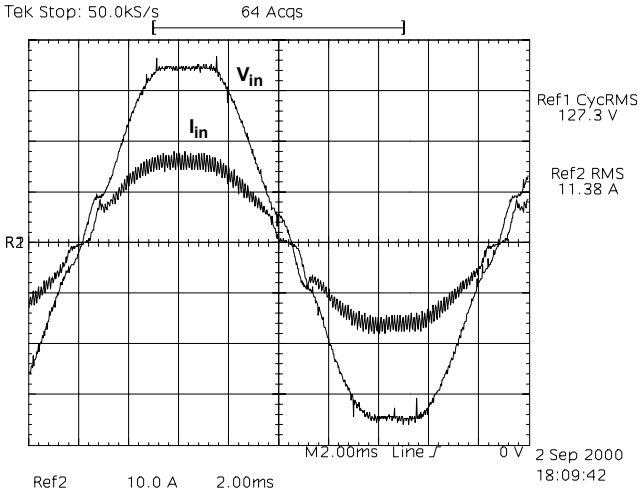


Fig. 9. Input voltage and input current (50 V/div, 10 A/div, 2ms/div)

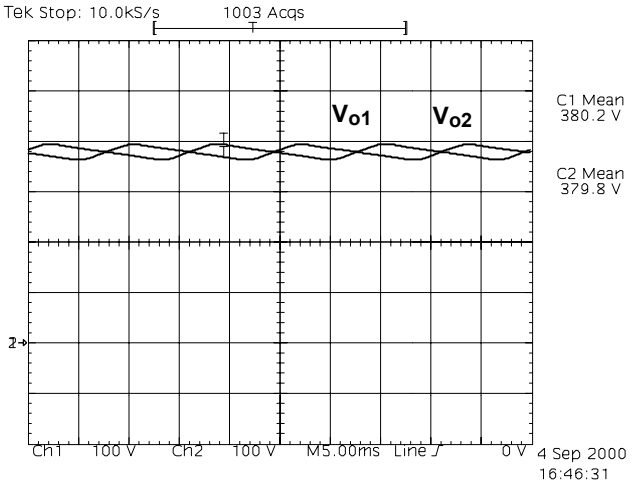


Fig. 10. Output voltages V_{o1} and V_{o1} (100 V/div, 5ms/div)

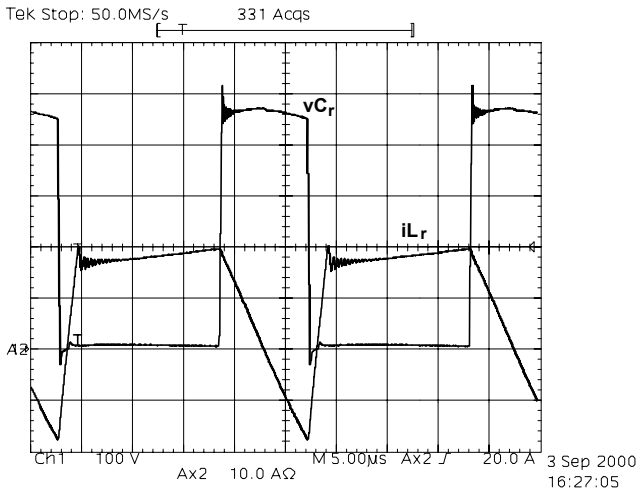


Fig. 11. Resonant capacitor voltage and resonant inductor current (100V/div, 10 A/div, 5 µs/div)

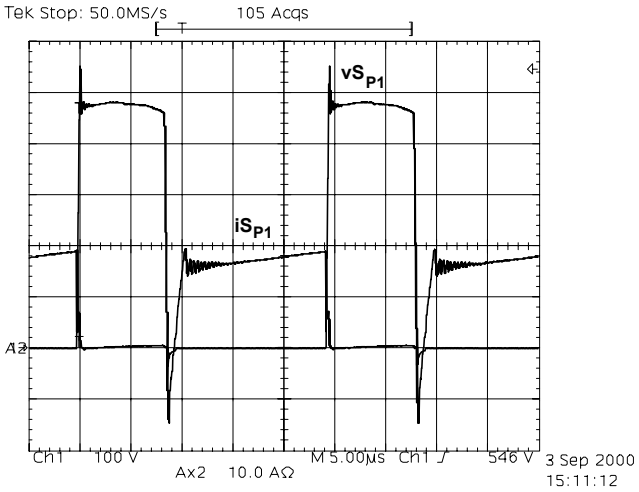


Fig. 12. Drain-to-source voltage across S_{P1}. and current through S_{P1}.(100V/div, 10 A/div, 5 µs/div)

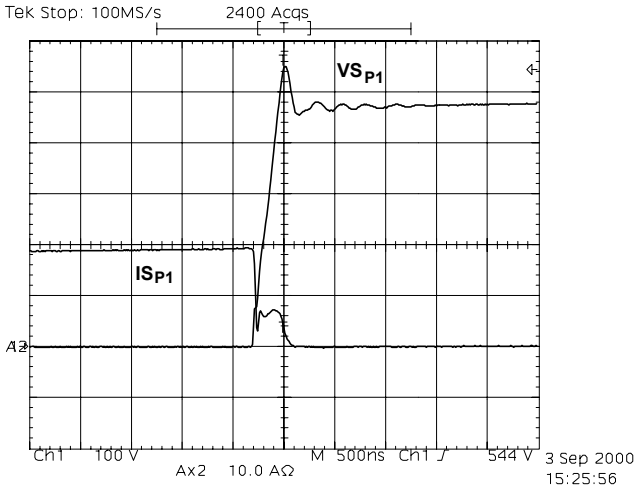


Fig. 13. Detail of the S_{P1}.turn-off process.(100V/div, 10 A/div, 1 µs/div)

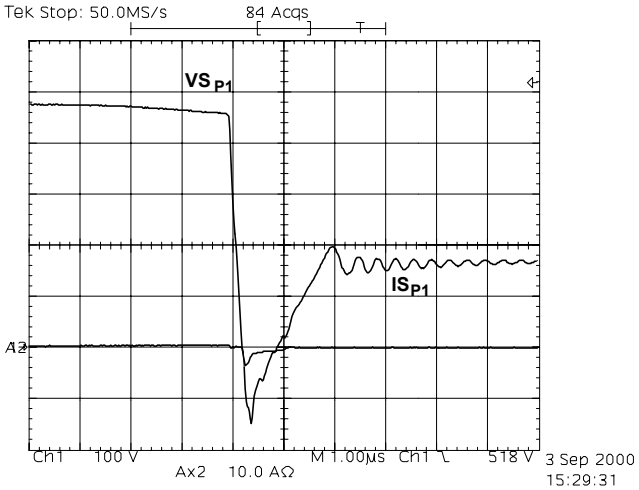


Fig. 14. Detail of the S_{P1}.turn-on process.(100V/div, 10 A/div, 1 µs/div)

Fig.15 shows the waveforms for S_{A1} commutations.

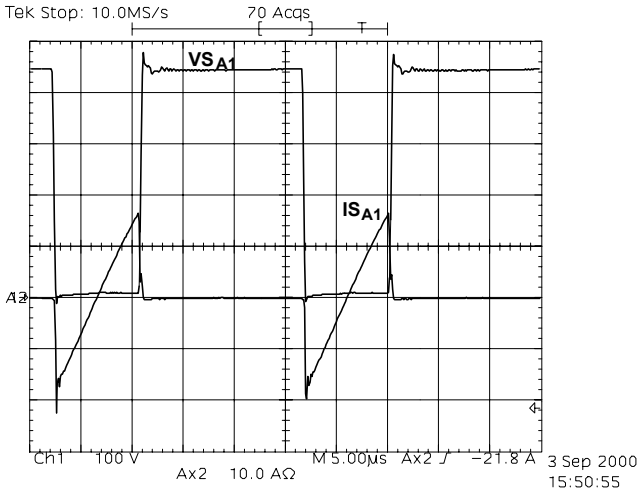


Fig. 15. Drain-to-source voltage across S_{A1}. and current through S_{A1}.(100V/div, 10 A/div, 5 µs/div)

V. CONCLUSIONS

The results obtained with the proposed PFC circuit le

ad to the following conclusions:

- the converter operates with ZVS commutation in all switches;

- soft commutation occurs for a large range of input current;

- half of the output voltage across the switches makes this converter suitable for high voltages applications;

VI. REFERENCES

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[2] C.M.C. Duarte and I. Barbi, "A New Family of ZVS-PWM Active-Clamping DC-to-DC Boost Converters: Synthesis, Analysis, and Experimentation", *INTELEC, 1996 Proceedings, pp 305-312*.

[3] C.M.C. Duarte and I. Barbi, "A New ZVS-PWM Active-Clamping High Power Factor Rectifier: Analysis, Design and Experimentation", *APEC, 1998 Proceedings, pp 230-233.*

[4] C.S.Silva, "Power Factor Correction with UC3854", *Unitrode Application. Note*