A Series-Parallel Compensated Line-Interactive UPS System Implementation with Active Power-Line Conditioning

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***Abstract*-This paper presents a three-phase line-interactive uninterruptible power supply (UPS) system with series-parallel active power-line conditioning capabilities, using synchronous reference frame (SRF) based controller, which allows an effective power factor correction, load harmonic current suppression and output voltage regulation. The three-phase UPS system is composed by two active power filter topologies. The first one is a series active power filter, which works as a sinusoidal current source in phase with the input voltage. The other is a parallel active power filter, which works as a sinusoidal voltage source in phase with the input voltage, providing to the load a regulated and sinusoidal voltage with low total harmonic distortion (THD). Operation of a three-phase phase-locked loop (PLL) structure, used in the proposed line-interactive UPS implementation, is presented and experimentally verified under distorted utility conditions. The control algorithm using SRF method and the active power flow through the UPS system are described and analytically studied. Design procedures, digital simulations and experimental results for a prototype are presented to verify the good performance of the proposed three-phase line-interactive UPS system.**

I. INTRODUCTION

To improve the power source quality, UPS systems have been employed, providing clean and uninterruptible power to critical loads such as, computers, medical equipment, etc, against power supply disturbances [1-7]. In [6, 7] three-phase parallel processing UPS have been presented with harmonic and reactive power compensation, but the output voltages and the input currents can not be controlled simultaneously. Three-phase UPS systems with series-parallel active power-line conditioning have been proposed using different control strategies [1-3]. In [3] the three-phase UPS system was employed for three-wire systems, and in [1-2] it was employed for three-wire and four-wire systems. In these works two different approaches to control three-phase UPS systems using synchronous reference frame (SRF) based controllers were proposed, but only simulations results were presented.

This paper presents experimental results for three-phase line-interactive UPS system with series-parallel active power-line conditioning using SRF based controller, for three-phase, three-wire and four-wire systems. The series active power filter acts as a sinusoidal current source and the parallel active power filter acts as a sinusoidal voltage source [2]. In this line-interactive UPS system, an effective power factor correction is carried out. The output voltages are controlled to have constant rms values and low total harmonic distortion (THD) and the source currents are controlled to be sinusoidal quantities with low THD, too.

Operation of a three-phase phase-locked loop (PLL) structure, used in the line-interactive UPS implementation, is presented and experimentally tested under distorted utility conditions. A PLL model is shown and design procedures to achieve the PI controller gains are presented.

The control algorithm using SRF method and the active power flow through the UPS system are described and analytically studied. Design procedures, digital simulations and experimental results for a prototype are presented to verify the good performance of the proposed three-phase line-interactive UPS system.

II. OPERATION OF THE LINE-INTERACTIVE UPS TOPOLOGY

The topology of the line-interactive UPS system is shown in Fig. 1. Two PWM converters, coupled to a common dc bus, are used to perform the series active filter and the parallel active filter functions. A battery bank is placed in the dc bus and a static switch '*sw*' is used to provide a fast disconnection between the UPS system and the power supply when an occasional interruption of the incoming power occurs.

A control algorithm using synchronous reference frame based controllers is used to control the series PWM converter making the three-phase line currents (i_{sa}, i_{sb}, i_{sc}) sinusoidal and balanced.

The parallel PWM converter is controlled to acts as a sinusoidal voltage source. The output UPS voltages v_{fa}, v_{fb} and v_{fc} are controlled to be in phase with respect to the input voltages v_{sa}, v_{sb} and v_{sc}, respectively.

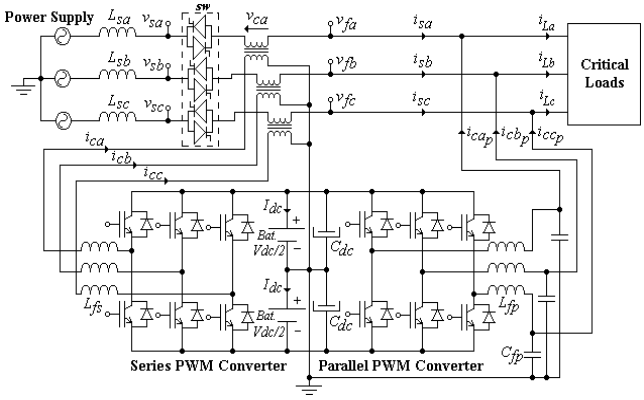

Fig. 1. Line-interactive UPS system topology.

III. Synchronous Reference Frame and State Feedback Controllers

A. Current SRF Controller (Standby Mode)

The block diagram of the control scheme for current compensation is shown in Fig. 2. The control algorithm should be developed to provide, by software, the compensating reference currents (i_{ca}^*, i_{cb}^*, i_{cc}^*) for the series active filter. The three-phase uncompensated currents (i_{La}, i_{Lb}, i_{Lc}) are measured and transformed into two-phase stationary reference frame $(dq)^s$ quantities (id^s, iq^s). Then, these quantities are transformed from the two-phase stationary reference frame $(dq)^s$ into a two-phase synchronous rotating reference frame $(dq)^e$, based on the transformation (1), where $\theta = \omega.t$, is the angular position of the reference frame. The inverse transformation matrix from two-phase synchronous reference frame to two-phase stationary reference frame is given by (2). The components of the unit vector $sin\theta$ and $cos\theta$ are obtained from a PLL system that will be discussed in the next section.

The current at the fundamental frequency ω is now a dc value and all the harmonics are transformed into non-dc quantities and can be filtered using a low pass filter (LPF) as shown in Fig. 2. Now, id_{dc}^e and iq_{dc}^e represent the fundamental active and reactive component of the load currents, respectively, both in dq axis. In this line-interactive UPS system implementation the reactive power will be compensated and then, k_q is made equal to zero in Fig. 2. The series filter reference currents in the stationary reference frame is then given by (3).

$$\begin{bmatrix} id^e \\ iq^e \end{bmatrix} = \begin{bmatrix} \cos\theta & sin\theta \\ -sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^s \\ iq^s \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} id^s \\ iq^s \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\theta \\ sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^e \\ iq^e \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} id_f^s \\ iq_f^s \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\theta \\ sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id_c^e \\ 0 \end{bmatrix} \quad (3)$$

Thereby, the dc components of the synchronous reference frame are transformed into the stationary reference frame $(dq)^s$ and yield all fundamental components of the input uncompensated ac currents. The matrices that provide the linear transformation from three-phase system to two-phase stationary reference frame system and from two-phase system to three-phase stationary reference frame system are given by equations (4) and (5), respectively. An additional dc bus controller is responsible for regulating the current I_{dc} and the voltage V_{dc}. Different from the conventional active power filter applications, in which only the dc bus voltage is controlled, the UPS dc bus controller must be able to control the dc bus current too. The dc bus controller is responsible by the control of the power flow through the UPS system. Its output is added to the active current in the d axis id_{dc}^e, and thus the amplitude of the input currents is controlled as shown in Fig. 2.

$$\begin{bmatrix} id^s \\ iq^s \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} i_{ca}^* \\ i_{cb}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} id_f^s \\ iq_f^s \end{bmatrix} \quad (5)$$

B. State Feedback Current Controller (Standby Mode)

The single-phase block diagram of the current controller is shown in Fig. 3. The load currents ($i_{La,b,c}$) are measured and from the current SRF controller the sinusoidal current references ($i_{ca,b,c}^*$) are obtained. From Fig. 3, the closed loop transfer function $i_c(s)/i_c^*(s)$ is found as (6) and the output dynamic stiffness is given by (7), which shows the effect of the difference between the output voltage v_f and input voltage v_s on the compensated input current i_c (i_s). The difference between the input and output voltages is treated as a disturbance.

$$\frac{i_c(s)}{i_c^*(s)} = \frac{K_{Ps}s + K_{Is}}{L_{fs}s^2 + (K_{Ps} + R_{L_{fs}})s + K_{Is}} \quad (6)$$

$$\frac{v_f(s) - v_s(s)}{i_c(s)} = -\frac{L_{fs}s^2 + (K_{Ps} + R_{L_{fs}})s + K_{Is}}{s} \quad (7)$$

The frequency response of equation (6) is shown in Fig. 4 (a) and (b). At the power system frequency (ω = 377 rad/s), the gain of the system transfer function is about 0 dB and the phase shift is nearly zero degree. The bandwidth of the system is about 1600 Hz. Fig. 5 shows the dynamic stiffness of the system. It is noted that the series active filter has high impedance in a large range of the frequency spectrum.

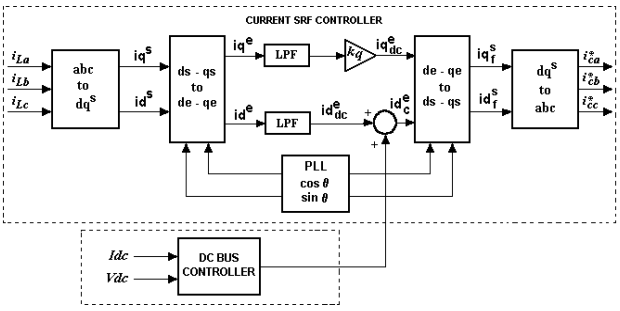

Fig. 2. Block diagram of the current SRF based controller.

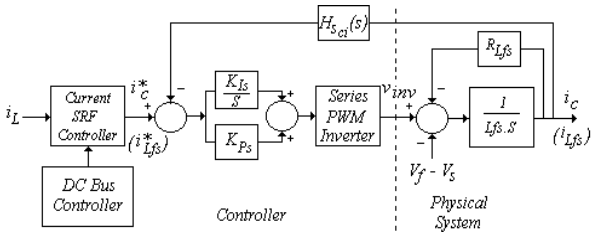

Fig. 3. Single-phase current controller of the series active filter.

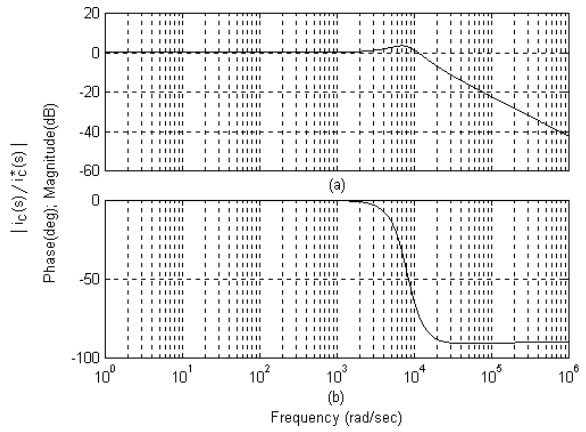

Fig. 4. Frequency response of the series active filter $i_c(s)/i_c^*(s)$: (a) Amplitude response, (b) Phase response.

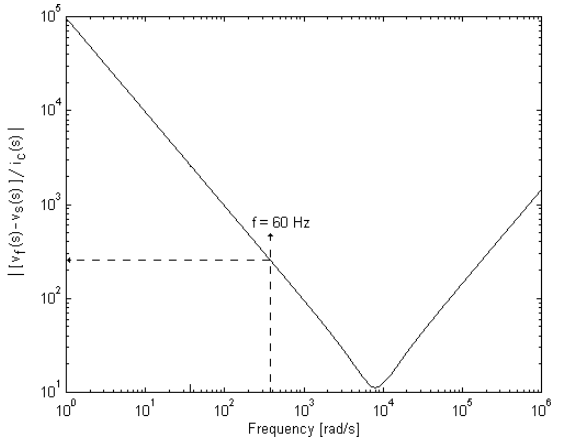

Fig. 5. Dynamic stiffness of the current controller $\left|(v_f(s)-v_s(s))/i_c(s)\right|$: Amplitude response.

C. State Feedback Voltage Controller (Standby and Backup Mode)

The parallel active filter is responsible by the control of the output voltages. Thus, the output voltages must have constant rms values with low THD and will be controlled to be in phase with the input voltages. As the control algorithm for input current compensation, the reference voltages ($v^*_{f\,a,b,c}$) are generated by software using a PLL system. The single-phase block diagram of the voltage controller is shown in Fig. 6, in which a classical PI controller with inner current loop and outer voltage loop is used.

From Fig. 6, the closed loop transfer function $v_f(s)/v_f^*(s)$ is found as (8) and the output dynamic stiffness is given by (9), which shows the effect of the difference between the load current i_L and the compensated input current i_s on the regulated output voltage v_f. The difference between the load current i_L and the compensated input current i_s is treated as a disturbance.

$$\frac{v_f(s)}{v_f^*(s)} = \frac{X_1 s^2 + X_2 s + X_3}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \tag{8}$$

$$\frac{i_L(s) - i_s(s)}{v_f(s)} = -\frac{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4}{Z_1 s^2 + Z_2 s} \tag{9}$$

$$\left.\begin{array}{lll} X_1 = \hat{C}_{fp}.K_{Pi} & Y_1 = L_{fp}.C_{fp} & Z_1 = L_{fp} \\ X_2 = K_{pv}.K_{Pi} & Y_2 = C_{fp}.(K_{Pi} + R_{Lfp}) & Z_2 = R_{Lfp} \\ X_3 = Y_4 = K_{Iv}.K_{Pi} & Y_3 = K_{pv}.K_{Pi} + 1 & \end{array}\right\} \tag{10}$$

The frequency response of equation (8) is shown in Fig. 7 (a) and (b). At the power system frequency (ω = 377 rad/s), the gain of the system transfer function is about 0 dB and the phase shift is nearly zero degree. The bandwidth of the system is about 6000 Hz. Fig. 8 shows the dynamic stiffness of the system. It is noted that the parallel active filter has low impedance in a large range of the frequency spectrum.

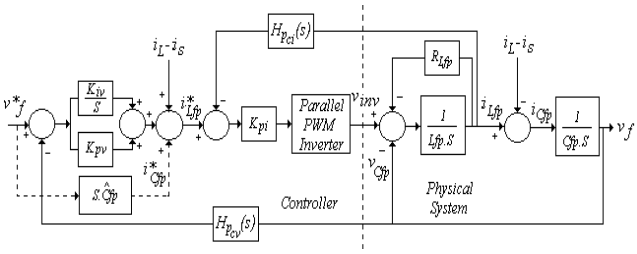

Fig. 6. Single-phase voltage controller of the parallel active filter.

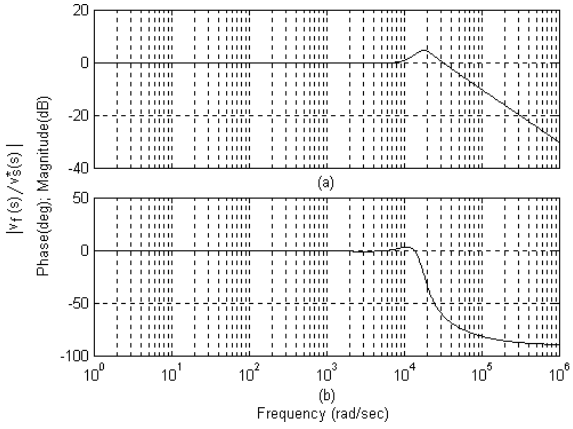

Fig. 7. Frequency response of the parallel active filter $v_f(s)/v_f^*(s)$: (a) Amplitude response, (b) Phase response.

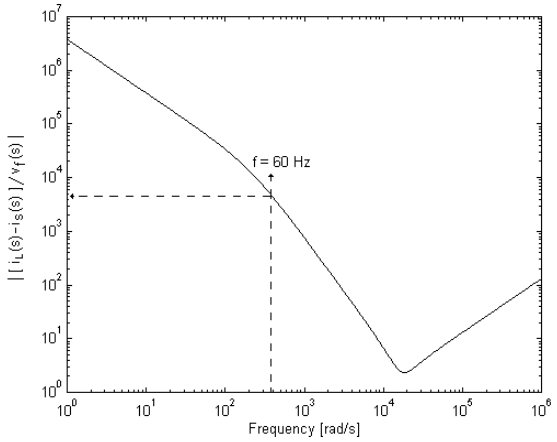

Fig. 8. Dynamic stiffness of the voltage controller $\left|(i_L(s)-i_s(s))/v_f(s)\right|$: Amplitude response.

IV. The Three-Phase PLL System

The three-phase PLL structure implemented in this work is shown in Fig. 9. It is completely implemented in software.

The input signals of the PLL system are the sampled voltages v_{sa}, v_{sb} and v_{sc}. The principle of operation of the presented PLL structure is to annul the dc component p'_{dc} of the instantaneous power p' (Fig. 9). The dynamic of the PLL system will set the output of the PI controller to the angular frequency reference $\omega^* = 2.\pi.f$, where *f* is the utility frequency. The angle $\theta^* = \omega^*.t$ is obtained by integration of the frequency reference ω^* that will be identical to the utility frequency ω. Thus, the angle θ^* is used to calculate the feedback signals i'_{sa} and i'_{sc} that will be orthogonal to the sampled voltages v_{sa} and v_{sc}, respectively, such that the dc component of p' is annulled.

A. Control Model of the Three-Phase PLL System

The instantaneous input power of the power system is found as

$$p = v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = p_{dc} + p_{ac}. \tag{11}$$

Assuming that the sum of the input currents i_{sa}, i_{sb} and i_{sc} is equal to zero, equation (11) can be found as

$$p = (v_{sa} - v_{sb})i_{sa} + (v_{sc} - v_{sb})i_{sc} = V_{ab}i_{sa} + V_{cb}i_{sc} \tag{12}$$

where

$$\left.\begin{aligned} V_{ab} &= \sqrt{3}V_m sin(\theta + 30^o) \\ V_{cb} &= \sqrt{3}V_m sin(\theta + 90^o) \end{aligned}\right\}. \tag{13}$$

Thus, from Fig. 9, the PLL instantaneous power p' is given by (14), where the quantities V'_{ab}, V'_{cb}, i'_{sa} and i'_{sc} are given by (15).

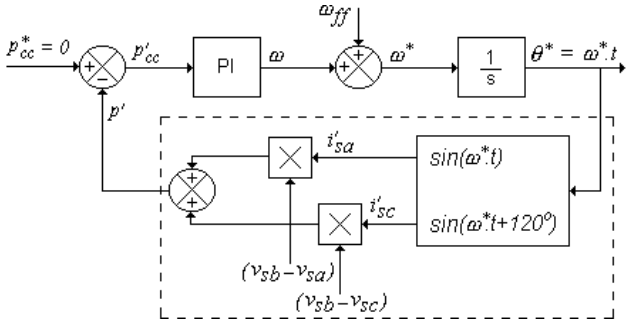

Fig. 9. Three-phase PLL control diagram.

$$p' = V'_{ab}i'_{sa} + V'_{cb}i'_{sc} \tag{14}$$

$$\left.\begin{aligned} V'_{ab} &= k_1 sin(\theta + 30^o) \\ V'_{cb} &= k_1 sin(\theta + 90^o) \\ i'_{sa} &= k_2 sin(\theta^*) \\ i'_{sc} &= k_2 sin(\theta^* + 120^o) \end{aligned}\right\} \tag{15}$$

To annul the dc component of p', the PLL system will set the output of the integrating element as

$$\theta^* = \theta' + 90^o. \tag{16}$$

The error between the utility angle θ and the PLL angle θ' is given by (17). Then, substituting the equations (15), (16) and (17) in (14), the power p' can be found as (18). As constant *k* varies when either input voltages or input currents change, it is assumed in the PLL model to be equal to one.

$$\Delta\theta = \theta - \theta' \tag{17}$$

$$p' = k.sin(\Delta\theta) \tag{18}$$

Thus, the PLL control diagram shown in Fig. 9 can replaced by the simplified PLL model shown in Fig. 10. For small values of $\Delta\theta$, the term $sin(\Delta\theta)$ behaves linearly [8], that is, $sin(\Delta\theta) \approx \Delta\theta$.

The open loop transfer function $G_{oL}(s)$ is found as (19), which accounts for the sampling time T_S that introduces a lag in the forward path of the PLL model. As it contains a double integration, a standard design procedure called "symmetrical optimum" method is used to determine the PI controller gains [9]. This method consists in choosing the crossover frequency ω_c at the geometric mean of the two corner frequencies of $G_{oL}(s)$. The magnitude and the phase plot of $G_{oL}(s)$ should be symmetrical with respect to the crossover frequency.

$$G_{oL} = \frac{sK_{Ppll} + K_{Ipll}}{s^3\tau_s + s^2} \tag{19}$$

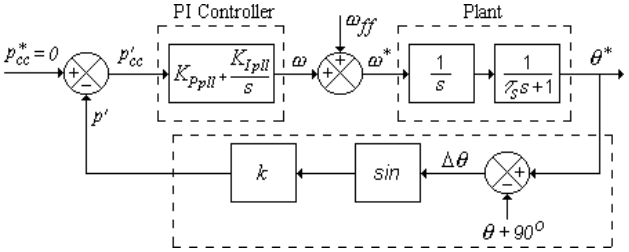

Fig. 10. Control model of the three-phase PLL.

Therefore, using the "symmetrical optimum" method discussed above and from (19), equations (20) and (21) are found, where δ is a normalizing factor. Thus, from (19), (20) and (21) the proportional gain can be selected by (22).

$$\left.\frac{1}{\delta}\omega_c = \frac{K_{Ipll}}{K_{Ppll}},\quad \delta\omega_c = \frac{1}{\tau_s},\quad \tau_s = \frac{T_s}{2\pi}\right\} \tag{20}$$

$$\left.\begin{aligned} &|G_{oL}(j\omega_c)| = 1 \\ &G_{oL}(j\omega_c)_{dB} = 20\log|G_{oL}(j\omega_c)|_{s=j\omega_c} = 0 \end{aligned}\right\} \tag{21}$$

$$K_{Ppll} = \frac{\omega_c}{k} \tag{22}$$

The closed loop transfer function $G_{cL}(s)$ is given by (23) and its poles are found by (24).

$$G_{cL}(s) = \frac{\omega_c^2\delta(s+\omega_c/\delta)}{(s+\omega_c)(s^2+\omega_c(\delta-1)s+\omega_c^2)} \tag{23}$$

$$\left.s_1 = -\omega_c,\ s_{2,3} = \omega_c - \left[\left(\frac{\delta-1}{2}\right) \pm j\sqrt{1-\left(\frac{\delta-1}{2}\right)^2}\right]\right\} \tag{24}$$

Hence, the relationship between damping ratio ς and the factor δ is

$$\delta = 2\varsigma + 1 \tag{25}$$

Thereby, with an adequate choice of the damping ratio ς and from equations (20), (22) and (25), it is possible to select the appropriate PI controller gains.

In Table I are shown the parameters and the controller gains used in the PLL simulation and experimentation. In Figs. 11 and 12 the experimental results and the model simulation results of the three-phase PLL system are shown. Fig. 11 and 12 show the PLL instantaneous power p' and PLL frequency ω^*, respectively. In Fig. 13 the distorted input voltage v_{sa} and the clean PLL voltage v_{pll} are shown.

TABLE I
PARAMETERS AND CONTROLLER GAINS

Factor δ	35
Sampling Time (T_s)	200 μs
Crossover Frequency (ω_c)	898 rad/s
Proportional gain (K_{Ppll})	898 rad/Ws
Integral gain (K_{Ipll})	23021 rad/Ws^2

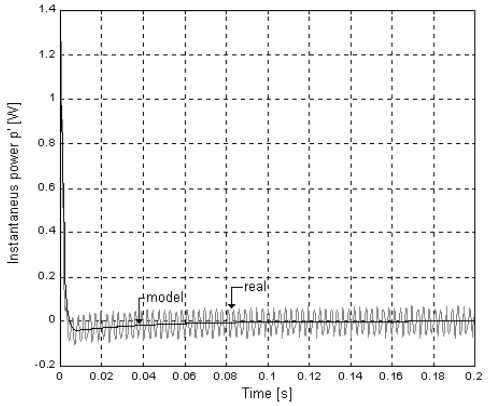

Fig. 11. PLL instantaneous power p'.

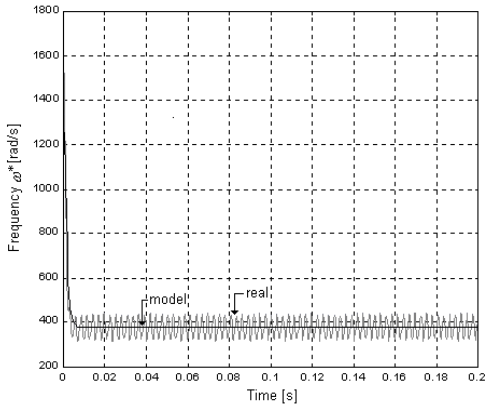

Fig. 12. PLL frequency ω^*.

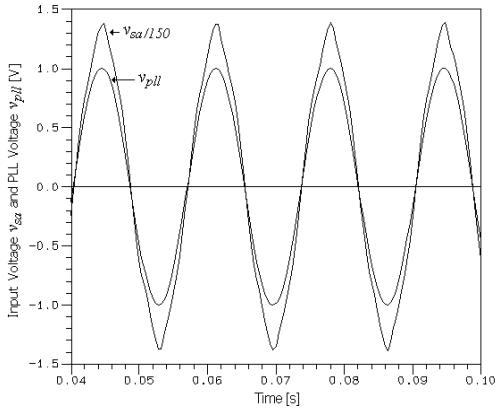

Fig. 13. Input sampled voltage v_{sa} and PLL voltage v_{pll}.

V. ACTIVE POWER FLOW OF THE THREE-PHASE UPS SYSTEM

Active power flow of the UPS system is shown in Fig. 14. The direction of the power flow can ever change because the amplitude of the input voltages is variable.

Both the apparent powers S_s and S_p, handled by the series and by the parallel converters, respectively, depend of the ratio between the output and input rms voltages (V_f/V_s), the displacement factor ($\cos\phi_1$) and the THD of the load current i_L (THD_{iL}). In steady state, assuming a balanced sinusoidal system, the normalized powers

handled by the parallel converter $|S_p/S_L|$ and by the series converter $|S_s/S_L|$ are given by equations (26) and (27), respectively. The quantities S_L, P_L, Q_L and H_L are the apparent, active, reactive and harmonic powers of the load, respectively.

In Fig. 15 (a) and (b) the normalized powers handled by the parallel converter $|S_p/S_L|$ and by the series converter $|S_s/S_L|$ are plotted for two different displacement factors. These curves can be used to determine the power rate of the PWM converters.

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P_L^2\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P_L^2+Q_L^2+H_L^2}} = \frac{\cos\phi_1\sqrt{\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{1+TDH_{i_L}^2}} \tag{26}$$

$$\left|\frac{S_p}{S_L}\right| = \sqrt{\frac{\cos^2\phi_1\frac{V_f}{V_s}\left(\frac{V_f}{V_s}-2\right)}{1+TDH_{i_L}^2}+1} \tag{27}$$

If the charging of the batteries is taking into account, additional active power P_b, given by (28), must be included in the analysis. Thus, equations (29) and (30) replace (26) and (27), respectively, where the charging factor $k_b \geq 0$.

$$P = P_L + P_b = P_L + k_b P_L \tag{28}$$

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P^2\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P_L^2+Q_L^2+H_L^2}} = \frac{\cos\phi_1\sqrt{\left[(1+k_b)\left(1-\frac{V_f}{V_s}\right)\right]^2}}{\sqrt{1+TDH_{i_L}^2}} \tag{29}$$

$$\left|\frac{S_p}{S_L}\right| = \sqrt{\frac{\cos^2\phi_1\frac{V_f}{V_s}(1+k_b)\left(\frac{V_f}{V_s}(1+k_b)-2\right)}{1+TDH_{i_L}^2}+1} \tag{30}$$

The plots of the normalized powers for two different values of k_b are shown in Fig. 16 (a) and (b). Depending of the k_b value and the input voltage deviation from the desired output voltage, the batteries charging can be realized either from the series or parallel PWM converters or from both.

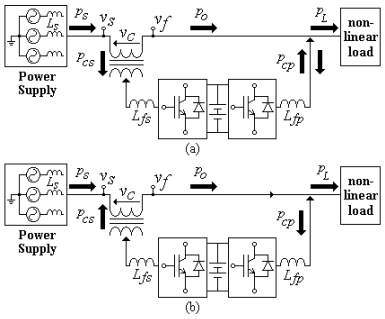

Fig. 14. Power flow of the UPS system: (a) $V_s > V_f$, (b) $V_f > V_s$.

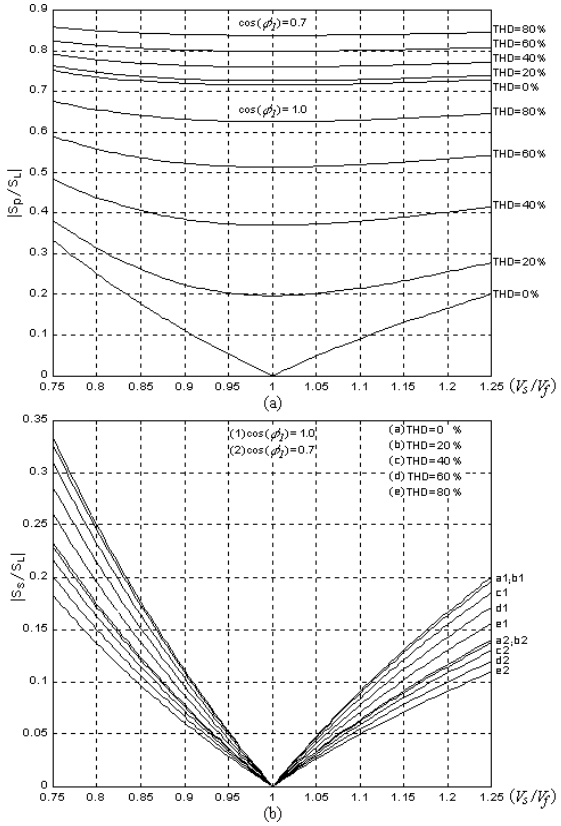

Fig. 15. Normalized powers: (a) Parallel converter $|S_p/S_L|$, (b) Series converter $|S_s/S_L|$.

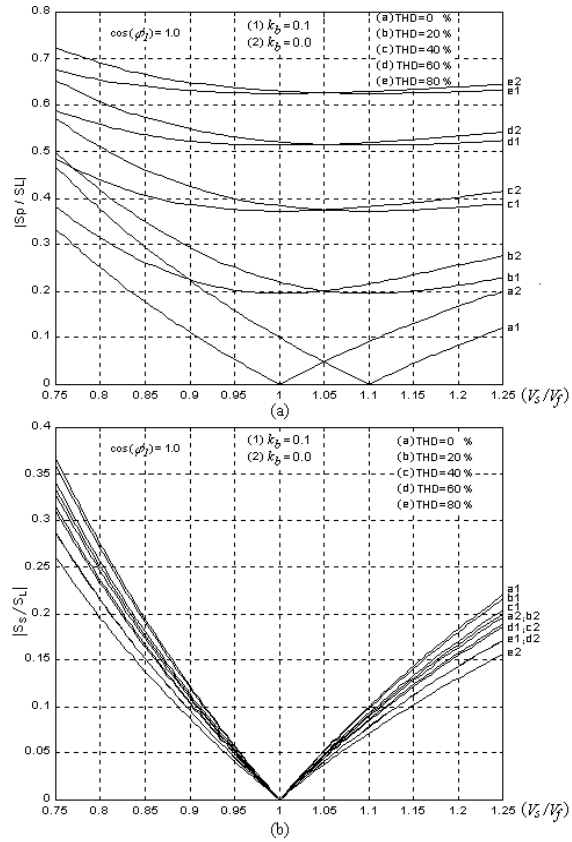

Fig. 16. Normalized Powers for $k_b = 0$ and $k_b = 0.1$ ($\cos\phi_1 = 1$): (a) Parallel converter $|S_p/S_L|$, (b) Series converter $|S_s/S_L|$.

VI. EXPERIMENTAL RESULTS

The complete scheme of the three-phase line-interactive UPS system is shown in Fig. 17. To verify the performance of the UPS system, a prototype was developed and tested. A 2.5 kVA non-linear load ($THD_{iL} \cong$ 30%) used to test the UPS system is a there-phase diode rectifier. The parameters used in the prototype are: L_{fp} = 300µH, L_{fs} = 1.4mH, C_{fp} = 130µF; R = 30 Ω (dc load); C_{dc} = 2200µF, nominal rms line-to-neutral output voltages - $V_{fa,b,c}$ = 115V and dc bus voltage - V_{dc} = 570V.

The part of the scheme shown in the shaded area uses a 400MHz PC computer, a 12 bits resolution data acquisition system and a 12 bits resolution D/A converter board. Both current SRF controller (Fig. 6) and PLL scheme (Fig. 2) are implemented in software and are responsible to generate the current and voltage references for the current and voltage analog controls. Both data acquisition systems and digital controllers run at 5kHz frequency.

The output voltages ($v_{f\,a,b,c}$) and source currents ($i_{s\,a,b,c}$) are shown in Figs.18 (a) and (b), respectively. The source currents $i_{s\,a,b,c}$ are almost sinusoidal and balanced. The output voltages ($v_{f\,a,b,c}$) are almost sinusoidal with constant rms values and low THD.

Fig. 18 (c) shows the phase 'a' input current i_{sa} and the input voltage v_{sa}. It is noted that a high power factor is obtained. Figs. 18 (d) shows the phase 'a' compensated current i_{sa} and the output voltage v_{fa}, respectively. The quantities $v_{s\,a,b,c}$ and $i_{s\,a,b,c}$ are controlled to be in phase with respect to $v_{f\,a,b,c}$. The UPS stabilization capability of the output voltages is shown in Figs. 18 (e) and (f).

In Fig. 18 (g) shows phase 'a' uncompensated current i_{La}, parallel compensation current i_{ca_p} and compensated source current i_{sa}. It is noted the presence of a fundamental component in i_{ca_p} that is responsible by charging of the battery bank. Figs. 18 (h) and (i) show the quantities v_{fa}, i_{sa}, i_{La} and i_{sa}^* (reference input current), for the transition from standby to backup mode (0.1 s) and from backup to standby mode (0.6 s), obtained from data acquisition software.

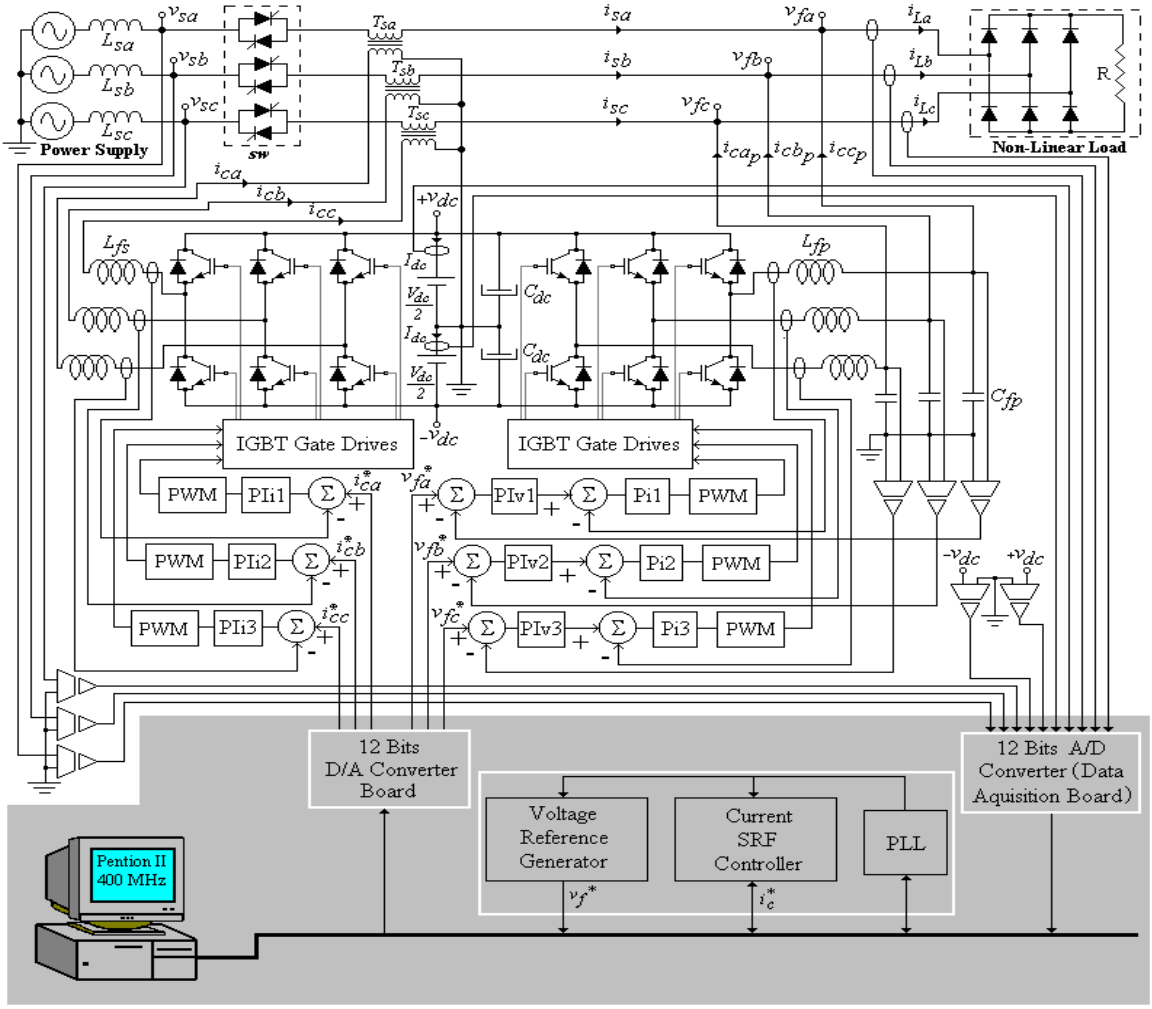

Fig. 17. Complete scheme of the line-interactive series-parallel UPS system.

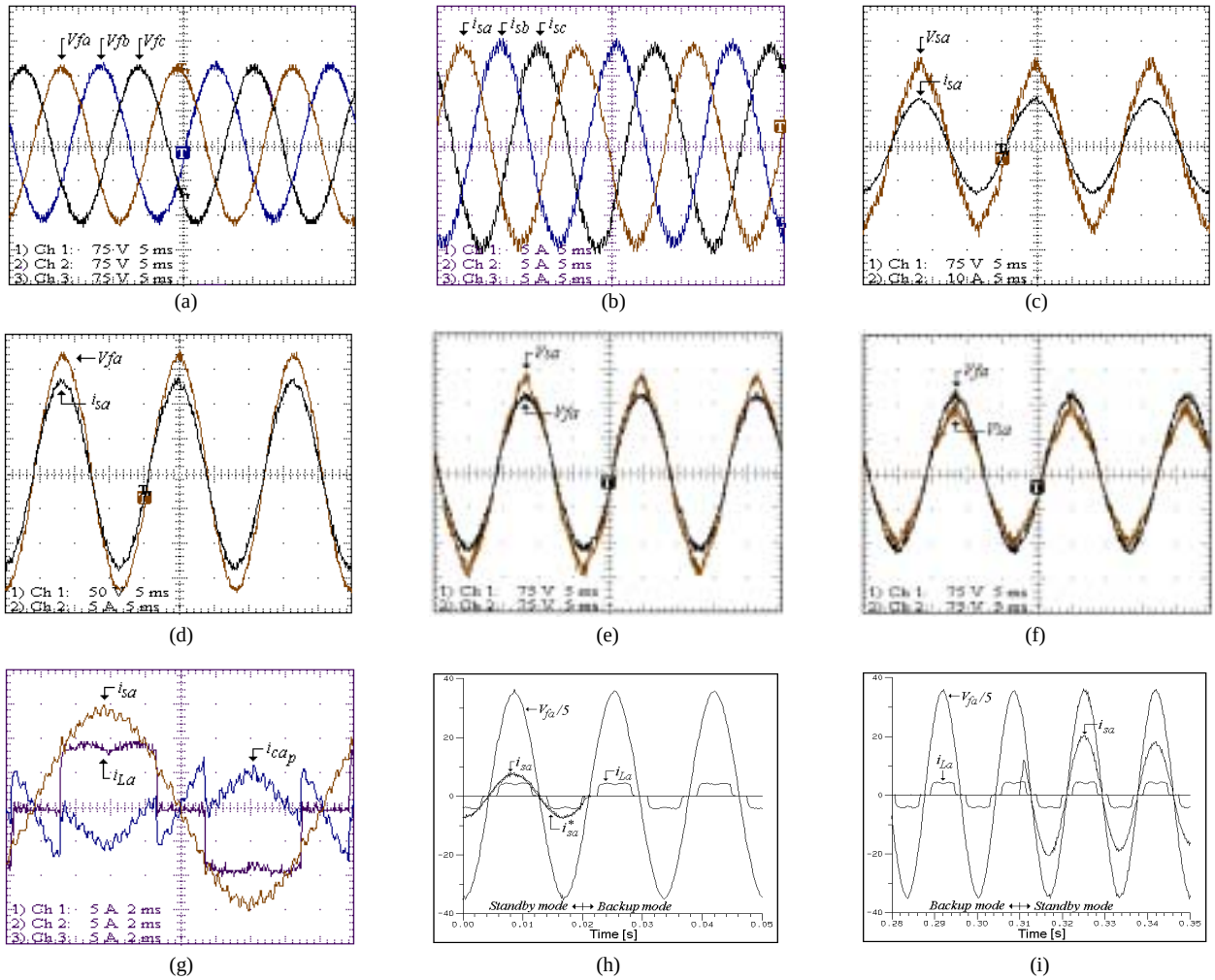

Fig. 18. Experimental results: (a) Output voltages $v_{f\,a,b,c}$; (b) Input currents $i_{s\,a,b,c}$; (c) Input voltage v_{sa} and input current i_{sa} ; (d) Output voltage v_{sa} and input current i_{sa} ; (e) Boost action - Input and output Voltages; (f) Buck action - Input and output voltages; (g) Currents i_{sa} , i_{cap} and i_{La} ; (h) Standby-Backup transition mode; (i) Backup-Standby transition mode.

VII. Conclusions

A three-phase line-interactive UPS system topology with active series-parallel power-line conditioning capabilities has been implemented and tested. Sinusoidal and regulated output voltage, sinusoidal input current and high input power factor were obtained. A model of a PLL system was presented and both PLL system and the algorithm of the SRF based controller were implemented in software without the use of any hardware filters.

The main advantage of the presented line-interactive UPS topology, as compared to the on-line topology, which uses two cascaded PWM power converters working at full power rating, is the smaller power rating handled by both series and parallel converters during the standby mode, increasing the efficiency of the UPS. Depending of the load VA rating, the presented line interactive UPS system can be an attractive and practical solution.

It has been demonstrated that the experimentally obtained results agree with good approximation with the theoretically predicted results.

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