Voltage-Doubler Rectifier with PFC, Regulation and Balancing of the Output Voltages Using DSP

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Abstract: This article presents the study and implementation of a single-phase pre-regulator rectifier, which can be applied to telecommunications sources with digital control using a DSP. The control technique used aims to obtain power factor correction (PFC) and regulated and balanced output voltages. The rectifier is a single-phase voltage doubler with a center tap at the voltage output. The DSP used is the ADMC331 of ANALOG DEVICES. The greatest advantages of this topology over the standard boost rectifier are: reduction in the number of components, the voltage across the switches is half of the total output voltage, lower conduction losses, single command for the switches and the presence of a center tap at the voltage output.

I. INTRODUCTION

The telecommunications rectifiers are normally composed by two stages connected in series, a rectifier with power factor correction and dc-dc converter. The proposal of this work is the use of a single-phase voltage-doubler PWM boost rectifier with power factor correction whose main characteristics are: high power factor in the input, regulation and balance of the output voltages.

The operational basic principle of this converter consists in imposing adequately a sinusoidal reference, which is established through a signal set that brings within itself the necessary characteristics to obtain a high power factor as well as regulated and balanced output voltage.

Several control techniques and topologies have been proposed to achieve the requirement of PFC [4,6].

The implemented control of the single-phase rectifiers was based on the average current mode control technique [6], which imposes to each period commutation the average current value in the inductor.

II. PRINCIPLE OF OPERATION

The topology of the voltage-doubler rectifier used is shown in fig.1. Its main characteristics are:

- The utilization of two diodes commuted in high frequency constituting the rectifier stage;
- Common capacitive center point;
- Bi-directional switch in current with single command;
- Blocking voltage in the switches is equal to half of the DC-link voltage.

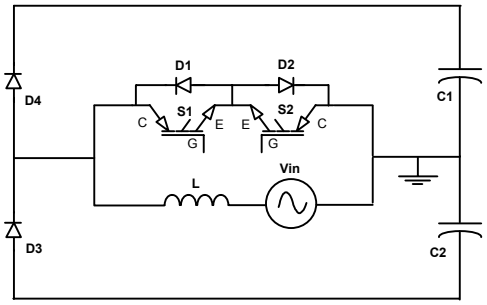

Fig.1 – Topology of the rectifier.

This converter behaves as if composed of two boost type converters operating in a complementary manner, since each half cycle of the AC-mains voltage will have the combination of a diode and a switch. In the half cycle where the boost diode (D3, D4) remains blocked, the connected load on this output is supplied exclusively by the capacitor.

The operating stages of this structure can be divided into four (4), being two (2) for each half cycle of the AC-mains voltage.

A. During the positive half cycle of the input voltage, switch S2 remains turned off

Switch S1 is ordered to conduct, initiating the energy accumulation stage of L (fig.2). On the output stage, each capacitor (C1 and C2) provides energy to the load.

Switch S1 is cut off, inductor L and source Vin provides energy to the capacitor C1 and its associated load, through diode D4 (fig.3).

These two stages occur in switch frequency during positive half cycle. The duration of each stage is proportional to the duty cycle.

B. During the negative half cycle of the input voltage, switch S1 remains turned off

Switch S2 is ordered to conduct, initiating the energy accumulation stage of L. At the output DC-link, each capacitor is responsible for providing energy to its associated load, (fig.4).

Switch S2 is cut off, source Vin and inductor L provide energy to the capacitor C2, through diode D3 (fig.5).

These energy transfer and accumulation cycles occur in switch frequency, also proportionally to the PWM period.

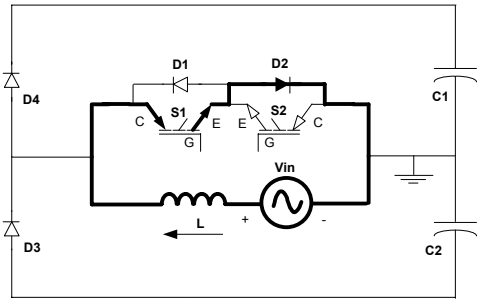

Fig.2 – Stage 1.

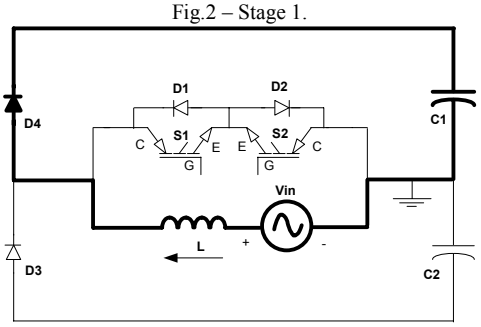

Fig.3 – Stage 2.

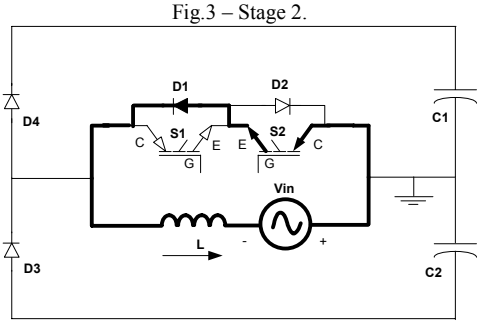

Fig.4 – Stage 3.

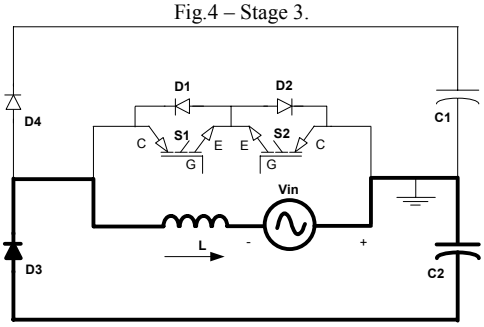

Fig.5 – Stage 4.

Table 1

Half-Cycle	Voltage in Switch S1, S2	Switching Command	Switch Turn on
Positive	Voltage in C1	(1-D)	D4
	0	D	S1,D2
Negative	Voltage in C2	(1-D)	D3
	0	D	S2,D2

Table 1 synthesizes the single-phase voltage-doubler boost rectifier operational stage, showing the semiconductors that conduct and the respective voltage applied to the same for each half-cycle of converter operation. It is possible to verify that there is always one (1) or two (2) semiconductors conducting during of the AC-mains voltage period.

A. Duty Cycle Variation

The converter pre-regulator used in the power factor correction is going to operate in the continuous conduction mode (CCM).

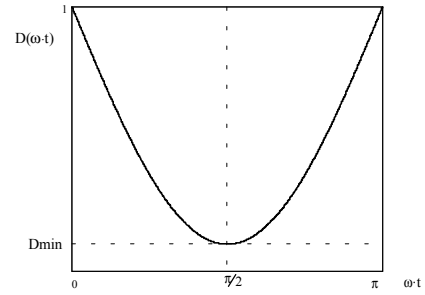

Fig.6 –Duty cycle variation.

The duty cycle must vary to each commutation period for switch frequency constant in order to control the average value of the output voltages desirable. Departing of the valid relation for the boost converter static gain, output voltage by the input voltage, it has:

$$\frac{Vo}{Vin} = \frac{1}{1-D} \tag{1}$$

Replacing adequately *Vin's* values and *D*, it arrives the following variation duty cycle term:

$$D(\omega.t) = 1 - \frac{1}{\beta}.sen(\omega.t) \tag{2}$$

Being β defined as the relation between output voltage and the input peak voltage, of the following form:

$$\beta = \frac{Vo}{Vin_p} \tag{3}$$

The fig. 6 represents the duty cycle variation expressed by the (2).

B. Input current Ripple

The input current ripple varies to each commutation period, or be, is going to vary along the AC-mains voltage period. The boost inductor value depends on the knowledge of this ripple. Admitting constant the voltage applied on L during the switches conduction S1 and S2, it arrives the (4) that represents the input current ripple normalized by $\frac{L}{Vin_p.T_s}$.

$$\overline{\Delta I_L}(\omega.t) = sen(\omega.t).\left[1 - \frac{1}{\beta}.sen(\omega.t)\right] \tag{4}$$

The fig.7 represent graphically (4), the normalized current ripple $\overline{\Delta I_L}(\omega.t)$ in function of β.

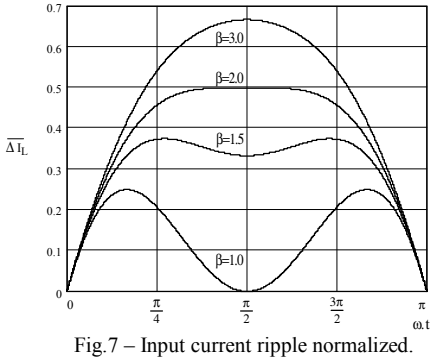

Fig.7 – Input current ripple normalized.

The maxim ripple point of current is obtained through the derivative analysis of (4). This value is replaced back in the (4) and solving for *L* then becomes:

$$L = \frac{Vin_p . \overline{\Delta I_L max}}{f_S . \Delta I_L} \quad (5)$$

Where:

f_S : Commutation frequency.

ΔI_L : Input current variation specified by the projector.

Vin_p : Input peak voltage.

The $\overline{\Delta I_L max}$, represents the maxim current ripple in the inductor, that depends on the value of β. If $\beta \leq 2$, then $\overline{\Delta I_L max}$ is $\frac{\beta}{4}$ or else $(1 - \frac{\beta}{4})$.

III. Average Current Mode Control Technique

The modulation strategy used is based on the appropriate variation of the duty cycle at a constant frequency. The control technique applied is called control by means of instantaneous average values of the input current. It is one of the most used in the power factor correction in pre-regulators with high power factor providing an input current with low harmonic distortion [4].

This technique consists of monitoring the input current of the converter making it follow a sinusoidal reference with the smallest error possible. This imposition is achieved through the appropriate high frequency switching control of the switches of converter. This control automatically regulates the output voltages and keeps them in balance. The control algorithm described was implemented using the ADMC331 DSP.

Figure 8 shows, using a block diagram, the control circuit used to command and control the rectifier.

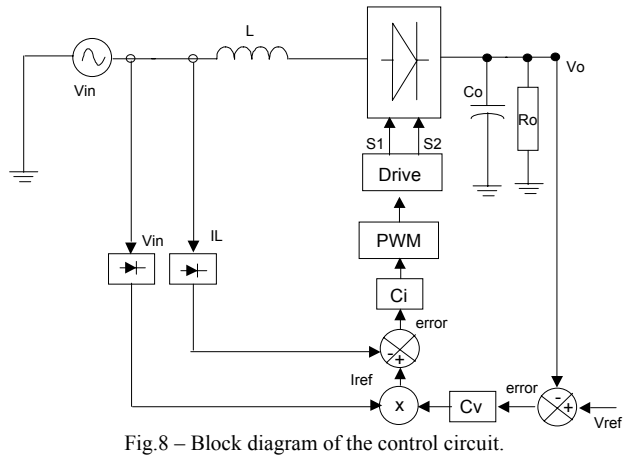

Fig.8 – Block diagram of the control circuit.

Cv - Voltage regulator. Block responsible by the converter output voltage regulation. The resultant control action in the exit of this regulator will contribute in the reference current composition (Iref), whose input is a resultant error signal of voltage sampling in the output voltage (Vo) of the converter and a reference voltage (Vref) pre-established in the design.

Ci - Current regulator. The reference of current is compared with a current sample in the inductor, producing an error signal that is applied to the regulator of current. The control action in the output of this block is applied to the PWM modulator (Pulse Width Modulation).

PWM - The control action in the output current regulator Ci is compared with a saw tooth signal in PWM block, resulting the PWM signal of switches command. This signal PWM is applied to both switches.

A. Converter model

It is necessary to know the converter model to design adequately the current and voltage regulators with the power factor correction goal, converter output voltage regulation and balance.

For the current loop the converter transfer function must take into consideration the input current *(IL)* related to control variable, in this case the duty cycle (6). A method for modeling using the model of PWM switch [4] proposed by [5] was used.

$$Gi(s) = \frac{IL(s)}{D(s)} \quad (6)$$

An option for the simplified model of the converter operating in continuous conduction mode (CCM) of current was made. This model considers the output voltage without ripple and the constant input voltage. Thus it arrives to the following transfer function of the converter, taking into consideration the input current and duty cycle.

$$Gi(s) = \frac{Vo}{S.L} \quad (7)$$

In the same way, to design the voltage regulator it is necessary to determine the transfer function that relates the output voltage to the current in the inductor (8):

$$Gv(s) = \frac{Vo(s)}{Il(s)} \quad (8)$$

Through the switch model PWM [5], the result is given by (9):

$$Gv(s) = (1 - D).\frac{Ro}{S.Co.Ro + 1} \quad (9)$$

Where:

Ro : Load resistance.

Co : Output capacitance.

The voltage and current regulators (Cv(z) and Ci(z)), employed in the converter control belong to the Proportional-Integral (PI) kind. The allocation criteria of the zero and of integrator gain adjustment of Ci(z) are based in [4], where integrator gain must be fitted to satisfy the gain crossing frequency criterion. It concisely has:

$$fc \leq fs/4 \quad (10)$$

$$\omega_z = \frac{2.\pi.fs}{20} \quad (11)$$

Where:

fc : Gain crossing frequency.

f_S : Switch frequency.

ω_Z : Zero frequency.

The voltage gain of the controller Cv(z) was determined through the direct design by the root locus method by the Z-plane [11].

The controllers were determined in the continuous time, and the discrete transfer function through the bilinear transformation, from the controller knowledge in the domain of Z. Applying the transformed Z^{-1} obtaining the controller under a difference equation form that will be implemented digitally [11].

The converter representation with the current and voltage, respective loops controls are shown by means of simplified blocks diagram in fig.9.

Each of the output voltages is sensed and regulated in the same designed voltage reference (Vref). The necessary corrections to maintain the output voltage in the specified reference are done through the converter power flow control for each of the output voltages.

The power flow control is represented through a switch that commutes to each half cycle of the AC-mains voltage period, fig.9.

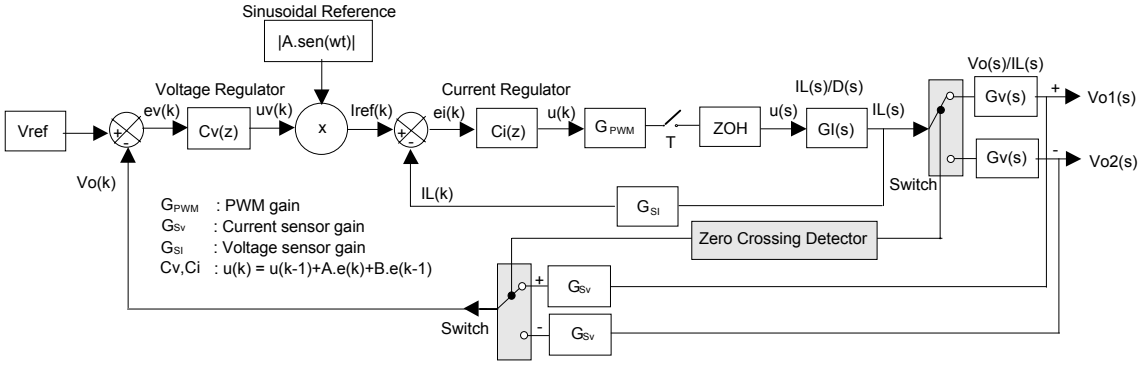

Fig. 9 – Block diagram of the converter control system.

IV. DIGITAL COMMAND AND CONTROL

The control technique is described in item III and was implemented using DSP ADMC331 of ANALOG DEVICES, whose main characteristic are:

- 26 MIPS Fixed-Point DSP core;
- Single cycle instruction execution (38.5 ns);
- Independent computational units: ALU, Barrel Shifter and Multiplier /Accumulator;
- Multifunction instruction;
- 2K x 24 bit – Program memory RAM;
- 2K x 24 bit - Program memory ROM;
- 1K x 16 bit - Data memory RAM;
- Three-Phase 16 bit PWM generator;
- Seven (7) analog input channel with 12 – bit resolution;
- 24 bits of digital I/O port;
- Two 8-bit auxiliary PWM;
- 16-bit Watchdog timer;
- Programmable 16–bit timer with prescaler;
- Two double buffered serial ports;
- ROM utilities.

Fig. 10 shows, using a block diagram, the digital control circuit used to command and control the rectifier. The execution implemented routines sequence blocks diagrams in ADMC331 are exhibited in fig.11.

The sampling frequency adopted in the voltage variable acquisition and current is 100 kHz, while the converter switching frequency is 50 kHz. The PWM controller of the ADMC331 is operating in double update mode; there is an additional PWMSYNC pulse produced at the midpoint of each PWM period. Consequently, it is possible to produce PWM switching patterns that are no longer symmetrical about de midpoint of the period (asymmetrical PWM patterns). With this sampling frequency of 100 kHz, a resolution of 8 bits Analog/Digital converter of the DSP was achieved. The effective ADC resolution is a function of the PWM switching frequency [1].

It was used one of the outputs of the three-phase PWM generator of ADMC331 for the activation of both switches, depending on the half-cycle of the AC-mains input voltage, one of the switches will conduct while the other will be blocked.

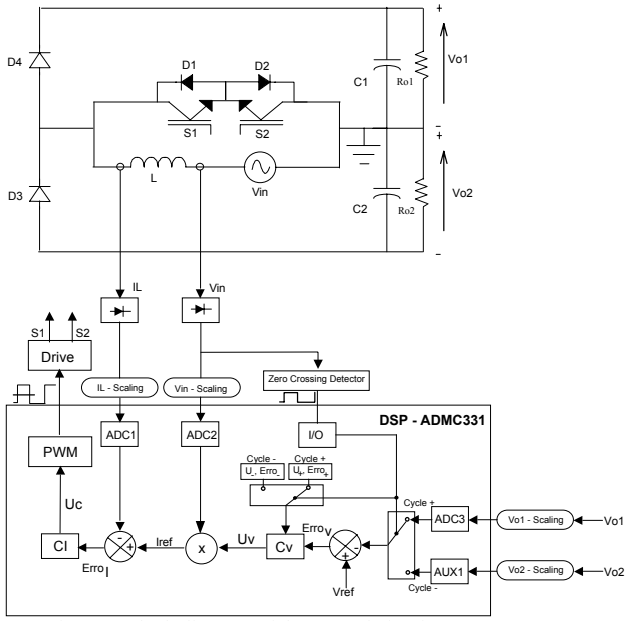

Fig. 10 –Block diagram of the control circuit.

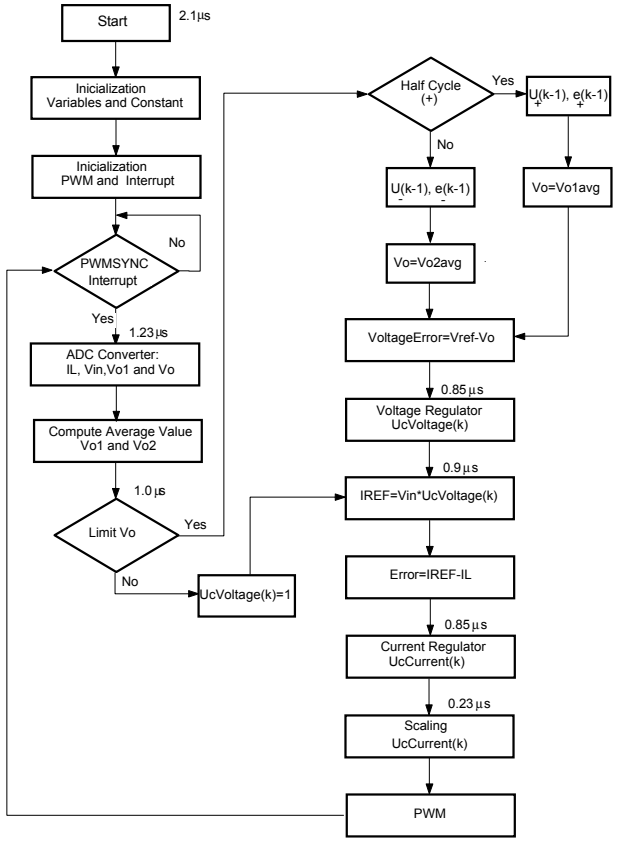

Fig. 11 – Program Blocks diagram.

At each PWM period beginning, the control unit of ADMC331 receives a synchronization pulse, change direction an interruption service routine, where the output voltages, the current in the inductor and the input voltage measures are made. From these values the controller calculations (PI) of voltages, whose output is compared with the input current sample generating an error that is applied to the controller (PI) of current. Once the controller control action of current is certain, this value is loaded in the three-phase PWM unit, which itself generates the PWM.

Fig.10 show that the AC-mains voltage signal sample (Vin) is carrying to zero crossing detector circuit. This output indicates to the DSP which half-cycle of the input voltage it operating the converter, that is, which of the output voltages (Vo1, Vo2) of the converter is susceptible to the control and regulation through the control voltage loops

V. Experimental Results

A prototype was planned and implemented using the specifications presented in table 2.

Table 2

Vin	Input rms voltage	127 V
Vo1,Vo2	Voltage at each output	250 V
Po	Total output power	1000 W
fs	Switching frequency	50 kHz
fr	AC line frequency	60 Hz

Fig.12 shows a converter photo and the environment of ADMC331.

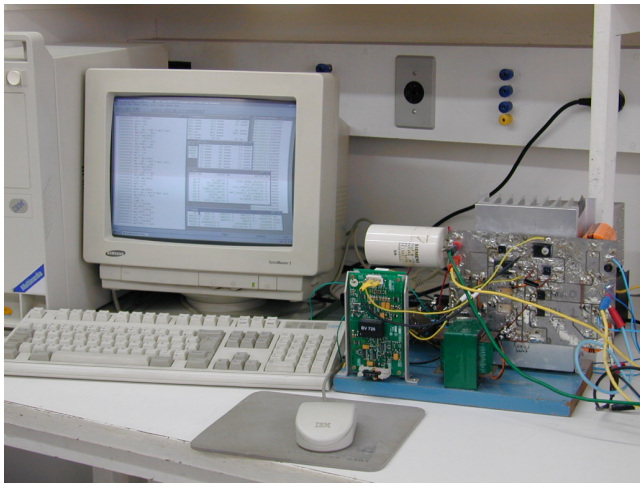

Fig.12 – Implemented prototype photo.

Fig.13 and Fig.14 shows de THD diagram of the input current and the THD diagram of the input voltage. The input current THD is 3.14% and the input voltage THD is 3.01 %. The Power Factor (PF) is 0.9985.

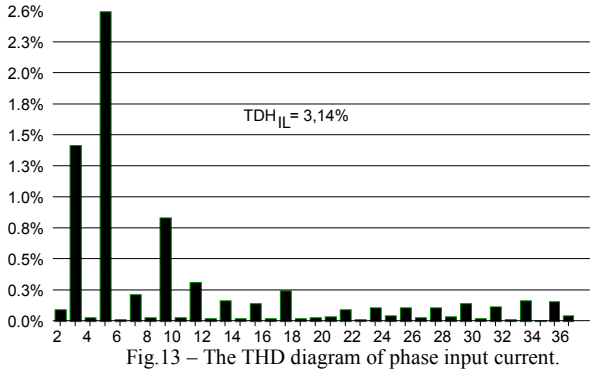

Fig.13 – The THD diagram of phase input current.

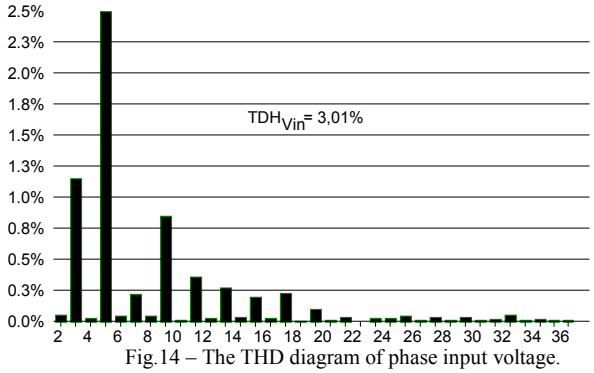

Fig.14 – The THD diagram of phase input voltage.

The following figures show the principal waveforms of the converter operating at rated power (1000 W). Fig. 15 shows the input voltage (Vin) and current (Iin) and output voltages (Vo1, Vo2).

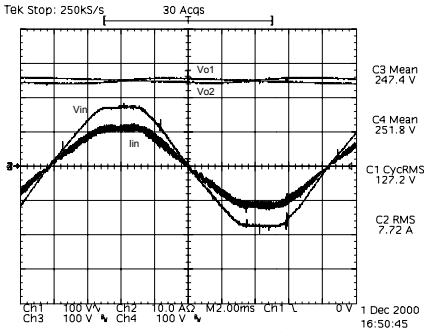

Fig. 15 – Input voltage (Vin) and current (Iin) and output voltages (Vo1, Vo2).

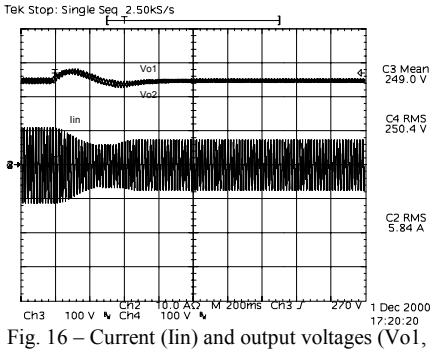

Fig. 16 – Current (Iin) and output voltages (Vo1, Vo2) with a 33% load disturbance.

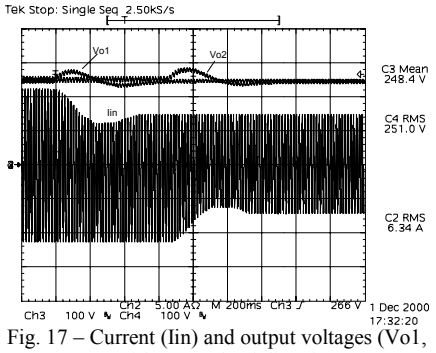

Fig. 17 – Current (Iin) and output voltages (Vo1, Vo2) with a 33% load disturbance.

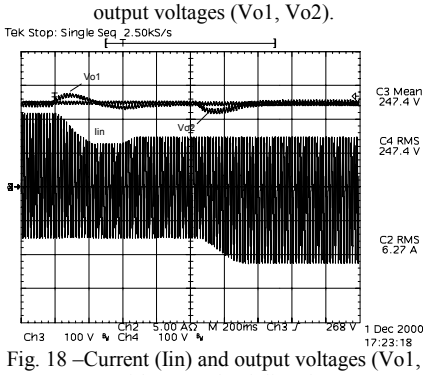

Fig. 18 –Current (Iin) and output voltages (Vo1, Vo2) with a 33% load disturbance.

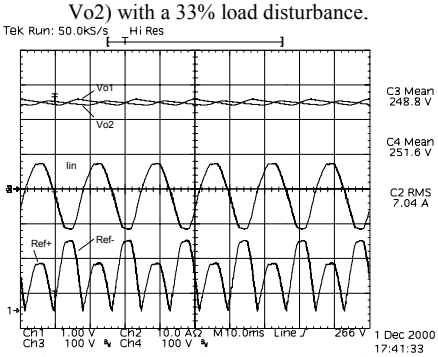

Fig. 19 – Output voltages (Vo1, Vo2), input current (Iin) and the reference signal (Ref+, Ref-) for unbalanced loads.

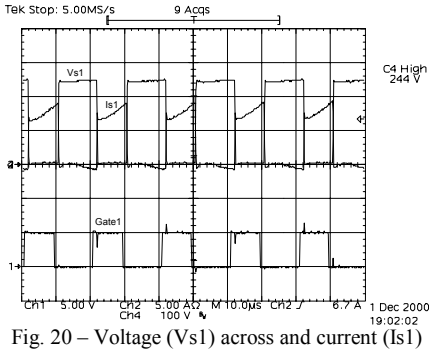

Fig. 20 – Voltage (Vs1) across and current (Is1) through the switch and the command signal (Gate1).

In the fig.16 both the converter output are perturbed at the same time. In the fig.17 it has a reduction of 33% of converter load, in different time. In the fig.18 withdraws the load (33%) of the output Vo1 and it afterwards adds in the output Vo2.

Fig.19 can be observed a converter operating with unbalanced load, it observes the unbalance provoked in the reference signal amplitude, similar of maintain the output voltages (Vo1 and Vo2) balanced.

VI. CONCLUSIONS

This paper has proposed the use of digital control for a voltage doubler rectifier by using a DSP, taking into consideration: The power factor correction and the regulation and balancing of the output voltages. Each of the output voltages is sensed and regulated in the same designed voltage reference (Vref) through the current reference amplitude variation of in each half cycle of the AC-mains voltage period.

Using digital techniques implemented by a DSP is possible to reduce the volume and cost of the command and control circuits. The reduction of volume is due to the fact that by using the ADMC331 most of the components responsible for implementing the control laws can be eliminated, since these laws are implemented by means of software. As for the cost, these components are becoming more and more accessible and diversified. The final result is high efficiency, high power factor converter with regulated and balanced output voltages.

The ADMC331 may also be used to perform more functions such as supervision and soft start.

VII. REFERENCES

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