# Dual-Bridge DC-DC Converter with Soft Switching in Full Load Range

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***Abstract - This paper presents a dual-bridge DC-DC converter with soft switching features from no-load to full-load range. To achieve ZVS commutation of the switches, asymmetrical PWM modulation and auxiliary circuits in each leg are applied to the converter. The proposed converter with input series connection is suitable for high voltage applications (>400V). Theoretical analysis and experimental results taken from a 3kW-laboratory prototype are presented.***

## I. INTRODUCTION

In high input voltage application (>400V), the conventional FB-ZVS-PWM converter is no suitable because the total input voltage is applied across its turned-off switches. To overcome such limitations must be applied some techniques capable to divide the input voltage across the switches of the converter. Switches series connections, converters based in multilevel inverter cells and converters based in converters series connections are among the possible solutions. In the switch series connection, the static and dynamic sharing of the voltage across the switches is very difficult to obtain and requires specific control circuits for compensate the voltage unbalance in each switch [1]. To minimize the static and dynamic voltage unbalance problems that occur in the conventional switches series connection, converters based in multilevel cells and converters series connection with magnetic coupling are an effective solution. In power electronic literature, converters with multilevel cells proposed in [1-4], and converters based on two full-bridge series connection proposed in [5,6] present maximum half input bus voltage across of the switches.

The dual-bridge DC-DC converter shown in Fig. 1 applying PWM phase-shift control was proposed in [8]. It is based on two forward converters connected in series and magnetically coupled by transformer. The maximum voltage across the switches is equal to half input voltage. Applying phase-shift control technique to the converter is necessary to add auxiliary circuits in each leg to achieve ZVS commutation of the switches in any load current. The addition of auxiliary circuits to the converter increases rms current through the components, and as consequence the conduction losses are also increased. On the other hand, a converter with full soft commutation of the switches presents reduced radio-frequency interference (RFI) and electromagnetic interference (EMI) problems. Also, snubber circuits across each switch to protect over voltages are avoided. Therefore, realizing a comparison between disadvantages and advantages, the converter with soft switching presents more advantages those disadvantages in the performance.

In this paper an asymmetrical PWM modulation is applied to the dual-bridge DC-DC converter shown in Fig. 1 [7]. Applying the indicated modulation, to get soft commutation of the switches in full load range operation, auxiliary circuits in each leg are necessary. The asymmetrical PWM modulation is other alternative capable of substitute the phase-shift control technique proposed in [8].

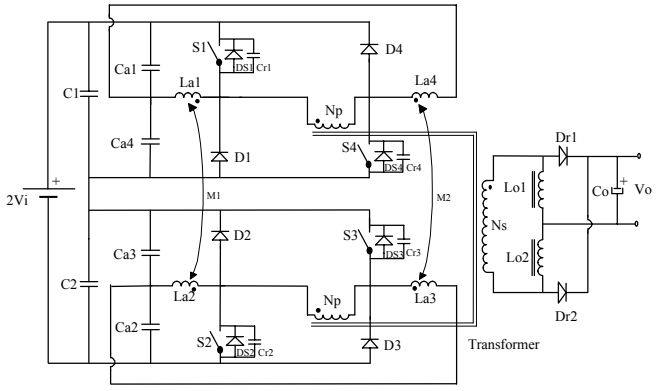



Fig. 1. Dual-bridge DC-DC converter with auxiliary circuits in each leg.

## II. PRINCIPLE OF OPERATION

### *A. Principle of Operation*

The converter operates in continuous conduction mode (CCM) and constant frequency.

The proposed modulation is shown in Fig. 3. It's given by four voltage pulses, where $V_{GS1}$ and $V_{GS3}$ are pulses with width lower than $T_s/2$, and $V_{GS2}$ and $V_{GS4}$ are pulses with width higher than $T_s/2$. The indicated pulses are complementary and easily obtained in laboratory using regulating pulse width modulator (SG3525) and hex inverting gates (MC14584) integrated circuits

In half period operation, the converter presents six stages, as is shown in Fig. 2. To simplify the stage descriptions, input capacitors $C_1$ and $C_2$ are substituted by voltage sources.

*First Stage ($t_o$, $t_1$):* During this stage, energy is transferred to the load from input source $V_1$ through

switches $S_1$ and $S_4$. In the secondary side of the transformer, the current flows through diode $D_{r1}$ and inductor filter $L_{o2}$. Switches $S_2$ and $S_3$ are turned off and the voltage across them is equal to $V_2$.

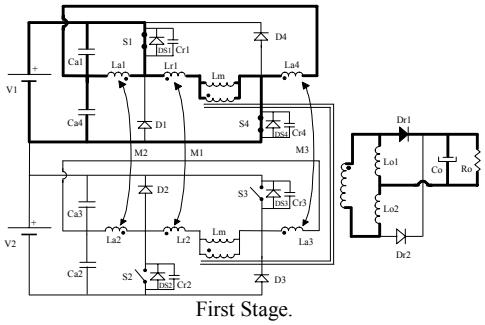
*Second Stage ($t_1$, $t_2$):* At $t=t_1$, switch $S_1$ is turned off under zero voltage and switch $S_4$ remain turned on. Capacitor $C_{r1}$, begins to charge linearly with a constant current. Also, energy is transferred from inductor $L_{a1}$ to $L_{a2}$ to discharge capacitor $C_{r2}$. This stage finishes when the voltage across $S_1$ is equal to $V_1$ and across $S_2$ is equal to zero.

*Third Stage ($t_2$, $t_3$):* At $t=t_2$, switch $S_2$ begins turned on under zero voltage, and diode $D_1$ is directly biased and conducts current through $L_{r1}$.The output inductors current starts freewheeling through $D_{r1}$ and $D_{r2}$. In this stage switch $S_4$ remain turned on.

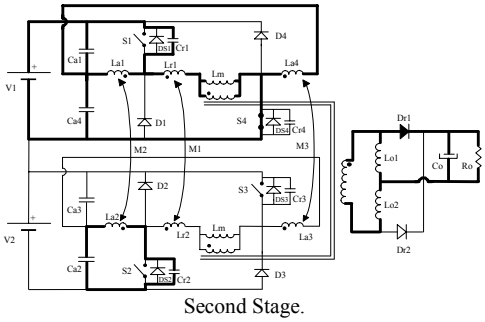
*Fourth Stage ($t_3$, $t_4$):* At $t=t_3$, switch $S_4$ is turned off under zero voltage. From inductor $L_{r1}$ energy is transferred to inductor $L_{r2}$ in flyback mode. Also, energy is transferred from inductor $L_{a4}$ to $L_{a3}$. These energies permit discharge of the capacitor $C_{r3}$. This stage finishes when the voltage across capacitor $C_{r3}$ is zero, and, the voltage across $C_{r4}$ is $V_1$.

*Fifth Stage ($t_4$, $t_5$):* At $t=t_4$, switch $S_3$ begins turned on and diode $D_4$ is directly biased and start conducting the current which decrease linearly through inductor $L_{r1}$. In this stage current through $L_{r2}$ also decrease linearly.

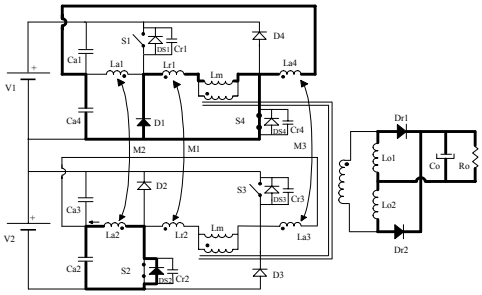
*Sixth Stage ($t_5$-$t_6$):* At $t=t_5$, switches $S_1$ and $S_4$ are turned off. The current through inductor $L_{r2}$ increases linearly from zero to $-nI_o/2$. During this stage, no energy transfer occurs from the input source $V_2$ to the load.



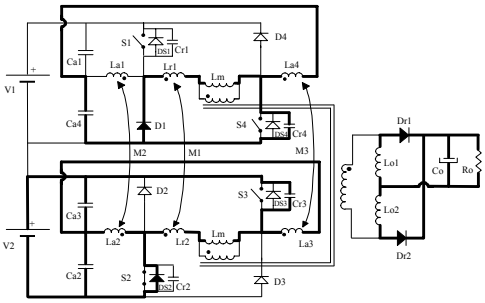
First Stage.



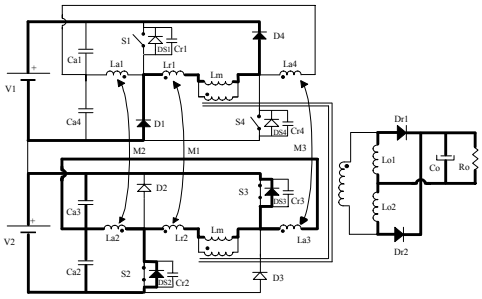
Second Stage.



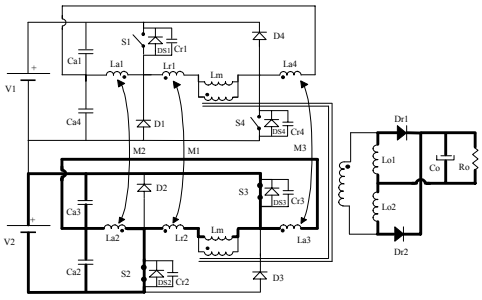
Third Stage.



Fourth Stage.



Fifth Stage.



Sixth Stage.

Fig. 2. Operation stages during half period.

## III. THEORETICAL ANALYSIS

### *A. Output Characteristic*

The output voltage $V_o$ as a function of the output current $I_o$, known as output characteristic, is defined by (1) [9,10],

$$V_o = n \cdot V_i \cdot \left[ \frac{D}{2} - \frac{f_s \cdot L_r \cdot n \cdot I_o}{V_i} \right]. \qquad (1)$$

In (1), $n=N_s/N_p$ is transformer turns ratio, $f_s$ is switching frequency, $L_r=L_{r1}=L_{r2}$ is inductance of the commutation inductors, and $D=2t_w/T_s$ is duty cycle.

Equation (1) is shown graphically in Fig. 14.

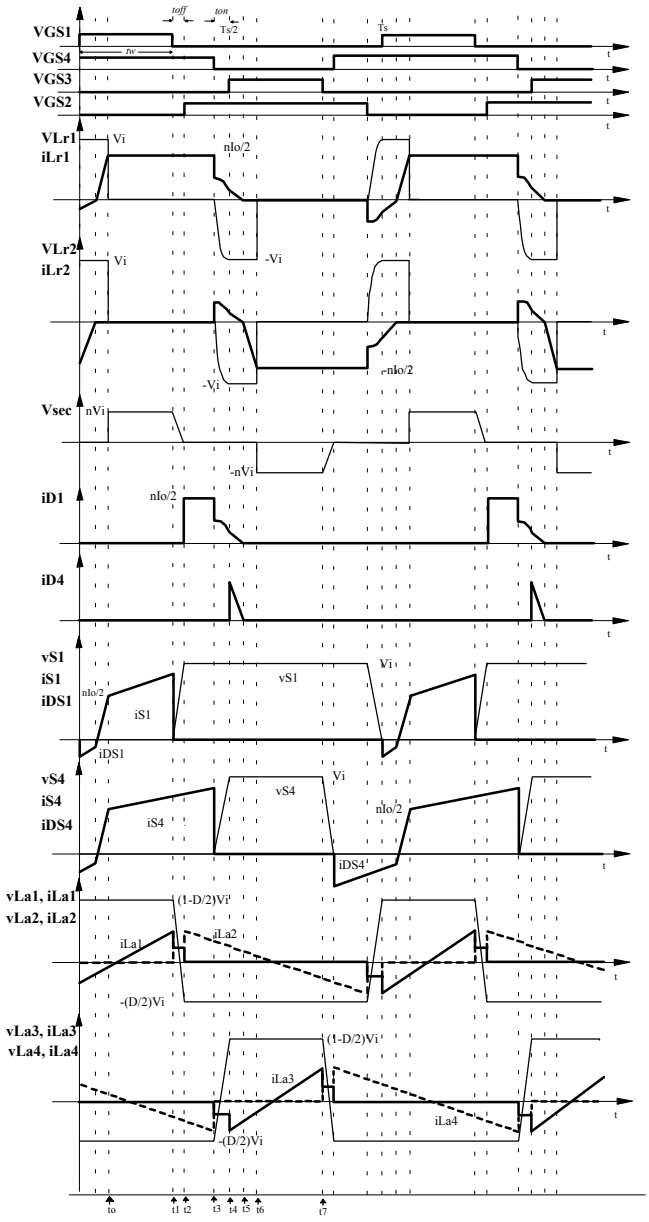



Fig. 3. Theoretical waveforms.

## B. Commutation Analysis

Commutation analysis is realized for critical situation that occurs when the load current is null ($I_o$=0). In the indicated condition the commutation auxiliary circuits must be capable of guarantee charge and discharge of the commutation capacitors in parallel with each switch.

In the critical condition, commutations of the left leg and of the right leg are similar. To follow commutation that occurs in the second stage is analyzed. The equivalent circuit of the second stage is shown in Fig. 4.

During this commutation the inductors of the auxiliary circuits are as current sources. In this way, the voltages across commutation capacitors change linearly.

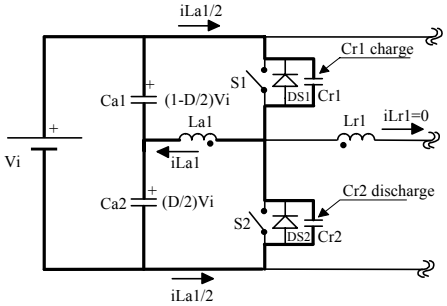



Fig. 4. Equivalent circuit during second stage.

The charge current of the capacitor $C_{r1}$ is given by (2),

$$i_{Cr1} = C_{r1} \cdot \frac{dv}{dt} . \quad (2)$$

During commutation the current that charge $C_{r1}$ is constant and equal to,

$$i_{Cr1} = \frac{I_{La1pk}}{2} . \quad (3)$$

Substituting (3) in (2) and realizing mathematical operations, voltage across capacitor $C_{r1}$ is given by (4),

$$v_{Cr1}(t) = \frac{1}{C_{r1}} \cdot \frac{I_{La1pk}}{2} \cdot t . \quad (4)$$

When capacitor $C_{r1}$ is charged in $t=t_{off}$ , the voltage across capacitor is equal to $v_{Cr1}(t_{off})=V_i$. Substituting this value in (4) is obtained (5),

$$V_i = \frac{1}{C_{r1}} \cdot \frac{I_{La1pk}}{2} \cdot t_{off} . \quad (5)$$

From (5) the capacitor $C_{r1}$ is equal to,

$$C_{r1} = \frac{I_{La1pk}}{2 \cdot V_i} \cdot t_{off} . \quad (6)$$

The commutation capacitors in parallel with each switches are equals ($C_{r1}=C_{r2}=C_{r3}=C_{r4}$). The commutation time interval ($t_{off}$) must be lower that the dead time assumed in the critical condition ($I_o$=0).

## C. Commutation Auxiliary Circuits in each Leg

Coupled inductors $L_{a1}$, $L_{a2}$, $L_{a3}$, and $L_{a4}$ and, capacitors $C_{a1}$, $C_{a2}$, $C_{a3}$ and $C_{a4}$ compose the auxiliary circuits placed in each leg. In this converter the inductors coupling is fundamental for the energy transfer process among inductors during commutation. To realize analysis the coupled inductors $L_{a1}$ and $L_{a2}$ are considered. The voltage and current waveforms across the inductors are shown in Fig. 5.

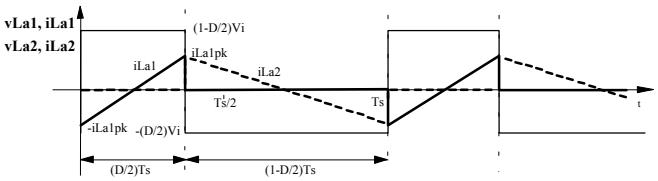



Fig. 5. Voltage and current waveforms in the inductors $L_{a1}$ and $L_{a2}$.

- *Auxiliary Inductors $L_{a1}$, $L_{a2}$, $L_{a3}$, $L_{a4}$*

The voltage across the inductor $L_{a1}$ is defined by (7),

$$v_{La1} = L_{a1} \cdot \frac{di}{dt} . \quad (7)$$

Resolving (7) the current through of the inductor $L_{a1}$ is given by (8),

$$i_{La1}(t) = -I_{La1pk} + \frac{v_{La1}}{L_{a1}} \cdot t \,. \qquad (8)$$

In $t=(D/2)T_s$ the current through of the inductor is equal to $i_{La1}((D/2)T_s)=I_{La1pk}$. Substituting this value in (8) is obtained (9),

$$I_{La1pk} = \frac{v_{La1}}{2 \cdot L_{a1}} \cdot \left( \frac{D}{2} \cdot T_s \right). \qquad (9)$$

The voltage across inductor $L_{a1}$ is equal to $v_{La1}=(1-D/2)V_i$. Substituting this value in (9) the inductance $L_{a1}$ is given by (10),

$$L_{a1} = \frac{D \cdot (2-D) \cdot V_i}{8 \cdot I_{La1pk} \cdot f_s} \,. \qquad (10)$$

Inductances of the auxiliary inductors are equals ($L_{a1}=L_{a2}=L_{a3}=L_{a4}$).

The rms currents through the inductors are:

$$I_{La1rms} = I_{La3rms} = I_{La1pk} \cdot \sqrt{\frac{D}{6}} \qquad (11)$$

$$I_{La2rms} = I_{La4rms} = I_{La1pk} \cdot \sqrt{\frac{(2-D)}{6}} \,. \qquad (12)$$

• *Auxiliary Capacitors $C_{a1}$, $C_{a2}$, $C_{a3}$, $C_{a4}$*

To determine capacitance of the capacitors, the resonance frequency between the capacitors and inductors of the auxiliary circuits is considered five times lower than commutation frequency $f_s$. Therefore,

$$f_{osc} = \frac{f_s}{5} \,. \qquad (13)$$

The resonance frequency is defined by (14),

$$f_{osc} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{a1} \cdot C_{a1}}} \,. \qquad (14)$$

Substituting (13) in (14) is obtained $C_{a1}$,

$$C_{a1} = \frac{6.25}{\pi^2 \cdot L_{a1} \cdot {f_s}^2} \,. \qquad (15)$$

Capacitance of the capacitors $C_{a2}$, $C_{a3}$ and $C_{a4}$, can be taken equal to $C_{a1}$ in the design.

## IV. SIMPLIFIED DESIGN EXAMPLE

A methodology and design procedure is presented in this section.

*A. Input Data*

$V_i$=200V: (input voltage)
$P_o$=3000W: (output power)
$V_o$=60V: (output voltage)
$I_o$=50A: (output current)

For full-load condition, a maximum duty cycle $D_{max}$=0.8, a maximum duty cycle reduction $\Delta D_{max}$=0.1, an output inductor filter current ripple $\Delta I_{Lo1}$=10A and switching frequency of $f_s$=25kHz are assumed. For no-load condition, a minimum duty cycle $D_{min}$=0.7 is considered.

The transformer turns ratio is equal to,

$$n = \frac{N_s}{N_p} = \frac{2}{(D_{max} - \Delta D_{max})} \cdot \frac{V_o}{V_i} = \frac{2}{(0.8-0.1)} \cdot \frac{60}{200} = 0.86 \cdot$$

*B. Commutation Coupled Inductors $L_{r1}$, $L_{r2}$*

Once the value of $\Delta D_{max}$ is known, the inductance can be calculated. Coefficient coupling of the commutation inductors is equal to K≅1 [9,10].

$$L_{r1} = L_{r2} = \frac{V_i \cdot \Delta D_{max}}{2 \cdot f_s \cdot n \cdot I_o} = \frac{200 \cdot 0.1}{2 \cdot 25 \cdot 10^3 \cdot 0.86 \cdot 50} = 9.3\mu H \,.$$

*C. Output Filter Inductors $L_{o1}$, $L_{o2}$*

The filter inductors are designed from the critical normalized current ripple $\overline{\Delta I_{Lo1}} = 0.25$ [10].

$$L_{o1} = L_{o2} = \frac{n \cdot V_i}{\Delta I_{Lo1} \cdot f_s} \cdot \overline{\Delta I_{Lo1}} = \frac{0.86 \cdot 200}{10 \cdot 25 \cdot 10^3} \cdot 0.25 = 172.0\mu H \,.$$

*D. Output Filter Capacitor $C_o$*

This capacitor is designed for a maximum voltage ripple $\Delta V_o = 0.48V$ (0.8% of $V_o$) across the output capacitor, $C_o$. The value is:

$$C_o = \frac{\Delta I_{Lo1}}{4 \cdot \pi \cdot f_s \cdot \Delta V_o} = \frac{10}{4 \cdot \pi \cdot 25 \cdot 10^3 \cdot 0.48} = 66.31\mu F \,.$$

The maximum allowable series resistance for the output capacitor is:

$$R_{SE} = \frac{2 \cdot \Delta V_o}{\Delta I_{Lo1}} = \frac{2 \cdot 0.48}{10} = 0.096\,\Omega \,.$$

*E. Input Capacitors $C_1$, $C_2$*

Capacitance of the input capacitor is calculated by:

$$C_1 = C_2 = \frac{5 \cdot n \cdot I_o}{V_i \cdot f_s} = \frac{5 \cdot 0.86 \cdot 50}{200 \cdot 25 \cdot 10^3} = 43\mu F \,.$$

*F. Commutation Capacitors $C_{r1}$, $C_{r2}$, $C_{r3}$, $C_{r4}$*

To calculate the commutation capacitors, the turned-off commutation time interval equal to 1% of Ts, and the peak current through auxiliary inductors equal to 20% of the transformer primary current in full load condition, are assumed. Therefore,

$$t_{off} = 0.01 \cdot 40 \cdot 10^{-6} = 400\ nsec$$

and,

$$I_{La1pk} = 0.2 \cdot \frac{0.86 \cdot 50}{2} = 4.3\ A.$$

From (6), capacitances of the commutation capacitors are calculated.

$$C_{r1} - C_{r4} = \frac{4.3 \cdot 400 \cdot 10^{-9}}{2 \cdot 200} = 4.3nF$$

*G. Auxiliary Inductors $L_{a1}$, $L_{a2}$, $L_{a3}$, $L_{a4}$.*

From (14), auxiliary inductors are calculated:

$$L_{a1} - L_{a4} = \frac{0.7 \cdot (2-0.7) \cdot 200}{8 \cdot 4.3 \cdot 25 \cdot 10^3} = 211.63\mu H \,.$$

*H. Auxiliary Capacitors $C_{a1}$, $C_{a2}$, $C_{a3}$, $C_{a4}$*

From (15), capacitances of the capacitors are calculated:

$$C_{a1} - C_{a4} = \frac{6.25}{\pi^2 \cdot 211.63 \cdot 10^{-6} \cdot \left(25 \cdot 10^3\right)^2} = 4.79\mu F \cdot$$

## V. EXPERIMENTAL RESULTS

To verify the practical aspects of the proposed converter, a prototype was built with the following components:

$S_1$-$S_4$: IRG4PC50W (IGBT)
$D_{r1}$, $D_{r2}$: HFA50PA60C (ultra-fast diodes)
$D_1$, $D_3$: MUR840 (ultra-fast diode)
$D_2$, $D_4$, $D_{S1}$-$D_{S4}$: MUR440 (ultra-fast diodes)
$C_1$, $C_2$: 60µF/250V (polypropylene capacitors
$C_{r1}$-$C_{r4}$: 3.9nF/400V (polypropylene capacitors)
$C_o$: 4x220µF/63V (electrolytic capacitor)
$T_r$: 3xE-76 (IP12); $N_p$=14 turns, $N_s$=12turns
$L_{o1}$, $L_{o2}$: E-65/26 (IP12); 172,0µH; $N_{Lo1}$=$N_{Lo2}$=26turns
$L_{r1}$, $L_{r2}$: E-42/20 (IP12); 7,5µH, $N_{Lr1}$=$N_{Lr2}$=6turns. ; K=1.
$L_{a1}$-$L_{a4}$: E-42/15 (IP12); 211.63µH, $N_{La1}$ - $N_{La4}$=55turns.
$C_{a1}$-$C_{a4}$: 5µF/250V (polypropylene capacitors).

The waveforms obtained for full load ($P_o$=3000W) are shown in Figs. 6, 7, 8, and 9; and for no-load condition is illustrated in Figs. 10 and 11. These results confirm the soft commutation of the switches in full load range operation.

Fig. 12 shows voltages across the input capacitors when inputs are connected in series. The theoretical value of these voltages is $V_i$=200V. In the prototype, a maximum unbalance of 1V is observed, which represents 0.5% of $V_i$. The voltage balancing is achieved coupling the converters with a single high-frequency power transformer.

Fig 13 shows rms currents through commutation inductors $L_{r1}$ and $L_{r2}$. It can be seen that the current unbalance through the circuits is negligible due to good voltage division across input capacitors.

Fig. 15 shows measured efficiency as a function of the output power.

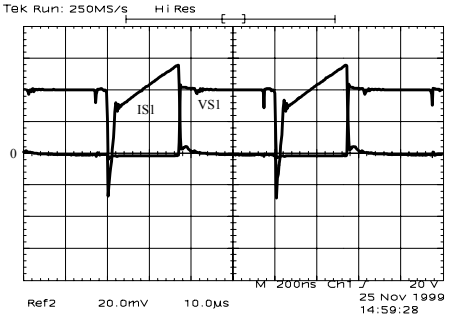


Fig. 6. Voltage and current in switch $S_1$.
(100V/div.; 10A/div.; 10us/div.)

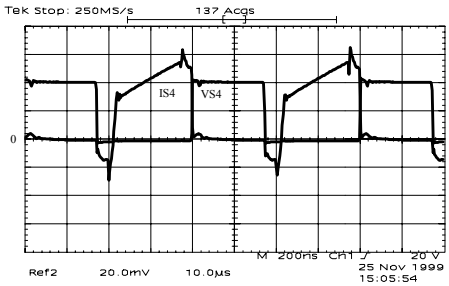


Fig. 7. Voltage and current in switch $S_4$.
(100V/div.; 10A/div.; 10us/div.)

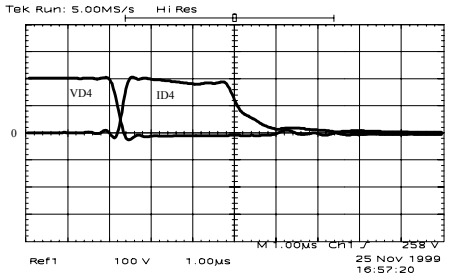


Fig. 8. Voltage and current in diode $D_4$.
(100V/div.; 10A/div.; 10us/div.)

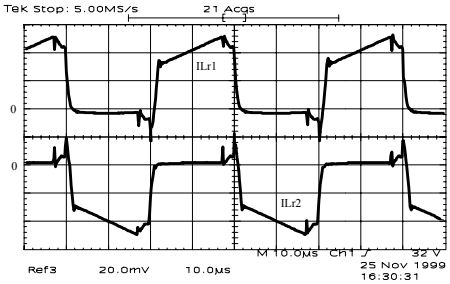


Fig. 9. Currents through inductors $L_{r1}$ and $L_{r2}$.
(10A/div.; 10us/div.)

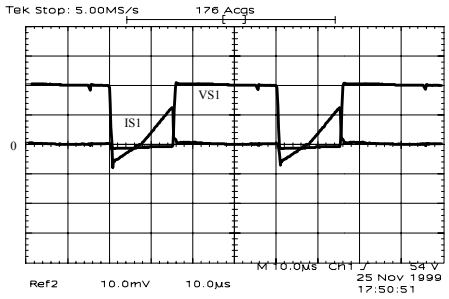


Fig. 10. Voltage and current in switch $S_1$.
(100V/div.; 10A/div.; 10us/div.)

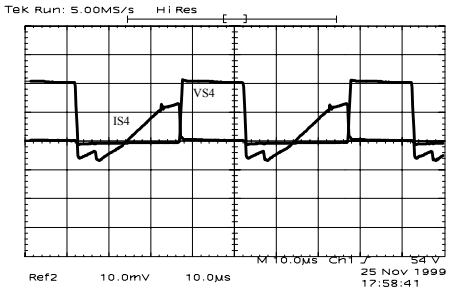


Fig. 11. Voltage and current in switch $S_4$.
(100V/div.; 10A/div.; 10us/div.)

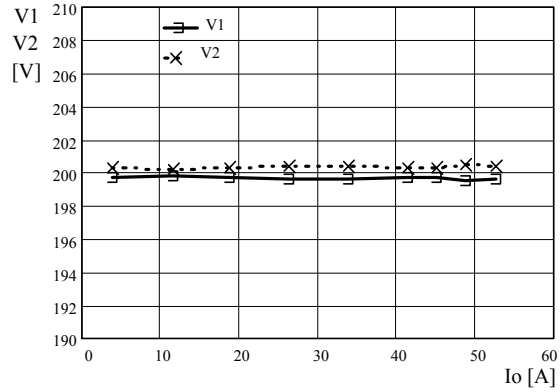



Fig. 12. Voltages across input capacitors $C_1$ and $C_2$.

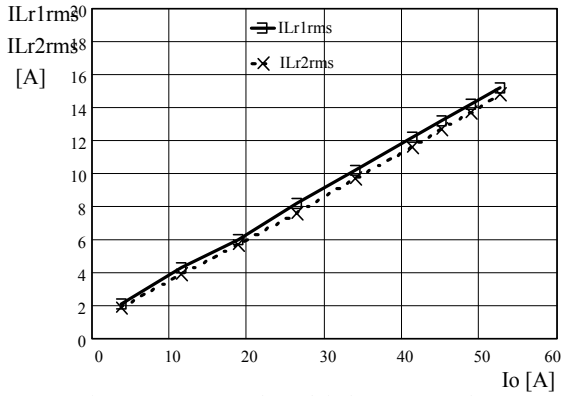



Fig. 13. rms current through inductors $L_{r1}$ and $L_{r2}$.

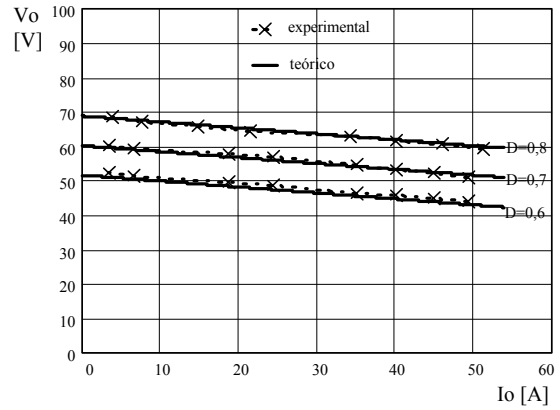



Fig. 14. Output characteristic of the converter.

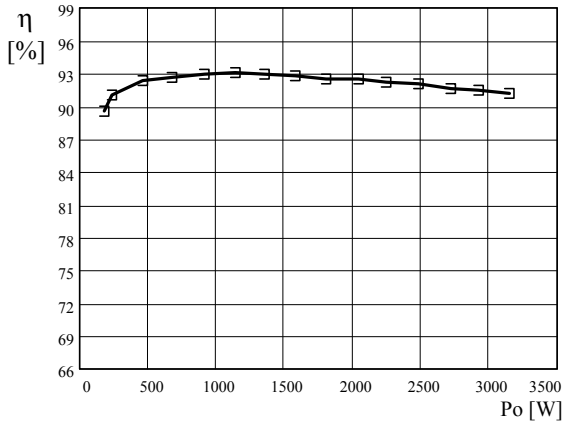



Fig. 15. Measured efficiency of the converter.

## VI. CONCLUSIONS

A dual-bridge DC-DC converter for high voltage applications with asymmetrical PWM modulation was studied in this paper. Analysis of the output characteristics and experimental results were presented.

Experimental results show that the converter presents the following features:

- Soft commutation of the switches in full load range.
- Voltage across the controlled switches is half of the input voltage.
- Frequency operation of the converter is constant.
- A good voltage division among the input capacitors is observed.
- A good distribution of currents through the coupled circuits is observed.
- The efficiency of the converter is 91.5%.

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