A Series Compensator for Voltage Sags

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***Abstract* – In this paper, a Dynamic Voltage Restorer (DVR) for voltage sag compensation is presented. The series PWM converter of the DVR is connected back-to-back with a shunt diode bridge through a common dc link. This configuration allows a reduction of the energy storage element installed in the dc link. The proposed system presents a simple design and a fast acting controller, based on the instantaneous active and reactive power Theory (p-q Theory). Simulation results show that it is able to compensate quickly for voltage sags or swells, improving the quality of the power supply.**

I. Introduction

A Power Electronics application that is receiving great effort relies on improvement of power quality delivered to customers. These customers should be supplied with constant, sinusoidal voltages. Active filtering has been used successfully to keep the supply voltage free of harmonics (sinusoidal). On the other hand, to keep constant the rms value of the supply voltage, some kind of compensation at the fundamental frequency is also required.

Nowadays, more and more critical loads are suffering due to temporary voltage drops, generally known as voltage sags. Distribution network suffers frequently voltage sags caused by remote faults. Very fast acting compensators are required to mitigate voltage sags, which is impossible to be reached by means of conventional techniques, such as transformers with on load tap change, or capacitor banks. Another common cause of voltage sags is the connection of large loads, such as the starting of large induction motor [1]. The diagram shown in Fig. 1 can represent this scenario. In this figure, the system bus IN is connected to a generator S through an equivalent inductance X_S. This bus supplies a critical load A and a purely inductive load B connected through the switch *SW1*, representing the start of a big induction motor. The switching of the load B causes temporary (or permanent) voltage sag at bus IN that should be compensated in order to supply the load A with constant voltage. The best way to solve this problem is to insert a series compensator between bus IN and load A. Such device is generally called as Dynamic Voltage Restorer, or simply DVR.

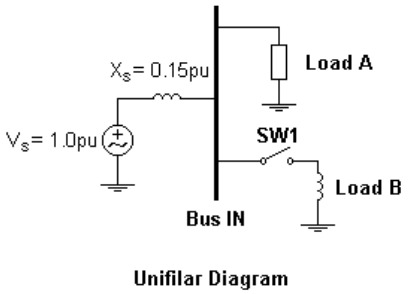

Fig. 1: Electric power system.

The aim of this paper is to present an alternative design of DVR for voltage sag compensation. This includes the principles of operation, details of the control scheme, and the power circuit configuration as well. A complete digital model is implemented and simulation results are presented to validate the proposed approach.

II. Power Circuit of the DVR

A three-phase PWM converter is used to synthesize compensating voltages v_{ca}, v_{cb}, v_{cc}, inserted in series between bus IN and bus OUT, as shown in Fig. 2. The series transformer is used to adequate the voltage and current levels of the power converter to the system ratings. Furthermore, it makes possible the series connection of the three-phase converter to the power line. In the present case, the turn ratios of the series transformers are equal to 1:1. The supply voltage at bus OUT is obtained by the sum of v_a at bus IN and v_{ca} of the DVR.

When voltage sags occurs, the DVR inserts v_{ca}, v_{cb}, v_{cc} to keep the voltage at bus OUT at the nominal value. Unfortunately, the compensating voltages v_{ca}, v_{cb}, v_{cc} produce with the load current, flowing through the series transformers, almost only active power (proportional to the power factor of load A). This means that the series PWM converter of the DVR should supply energy to the load. Therefore, to work properly, a large energy storage device such as batteries should be connected to the inverter dc link. An alternative solution is to provide a path of energy to flow through a shunt connected diode bridge, as shown in Fig. 2.

Despite its simplicity and robustness, diode bridge rectifiers draw high-distorted currents from the utility. This increases the distortion in the utility voltage waveform. To use this topology, simulation results reveled that the commutation inductors, represented by L_a, L_b and L_c in Fig. 2,

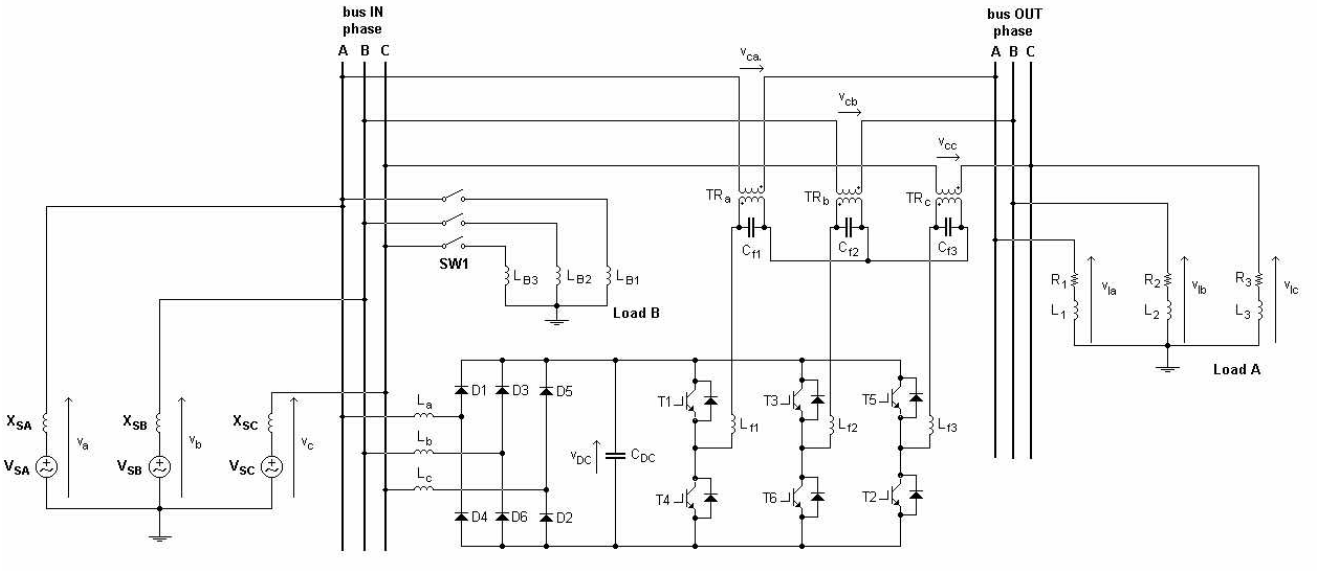

Fig. 2: Power Circuit Schematic.

should be at least three times greater than the equivalent impedance of the power supply (X_S).

Additionally, the high switching frequency of the IGBT's in the series PWM converter does itself produces harmonics that could not be neglected. The simplest solution to filter out the switching harmonics is the use of passive filters LC, formed by the pairs $L_{f1} - C_{f1}$, $L_{f2} - C_{f2}$ and $L_{f3} - C_{f3}$ in Fig. 2. If these inductances and capacitances are carefully adjusted, it is possible to attenuate the harmonic contents at a desirable level, in the power system [2].

III. Control Scheme of the DVR

A new control scheme is developed for the DVR. It is based on the instantaneous active and reactive power theory (*p-q Theory*) and on the concept of instantaneous aggregate voltage calculation. Fig. 3 shows the functional block diagram of the DVR Controller. Four blocks could be highlighted: 1) the positive sequence detector (v_{+1}); 2) the aggregate voltage (v_S) calculator; 3) the correction factor control block, and 4) the compensating voltage references. Next, these control blocks will be described.

Fig. 4 shows the complete functional control block diagram of the fundamental positive-sequence voltage detector. This detector, used here as part of the developed DVR controller, was proposed in [5], for applications in active filters and used successfully in other applications, like FACTS devices [6]. The Synchronizing Circuit (PLL Circuit) is responsible for determining the system frequency and the phase angle of the fundamental positive-sequence voltage of the ac bus IN. Fig. 5 shows the scheme of the used PLL circuit. This circuit has proved to be very effective, even under high-distorted system voltages.

The algorithm is based in the instantaneous active power expression:

$$p_{3f} = v_a.i_a + v_b.i_b + v_c.i_c = v_{ab}.i_a + v_{cb}.i_c \,. \quad (1)$$

Note that $i_a + i_b + i_c = 0$ is considered in (1). As no current is measured from the power circuit, one may find difficult to understand how the circuit works. Current feedback signals of Fig. 5 $i_a(w.t) = \sin(w.t)$ and $i_c(w.t) = \sin(w.t + 2.p/3)$ are built up by the PLL circuit, just using the output (ω) of the PI controller. The PLL reaches a stable operation point only if the input ($p_{3\phi}$) of the PI controller has a zero average value. This is found only if w equals the system frequency and the current $i_a(\omega t)$ becomes orthogonal to the phase voltage v_a of the power system. However, if the point where $i_a(\omega t)$ lags v_a by 90° is reached, this is still an unstable point of operation. At this point, a eventual disturbance that slightly increases the system frequency (v_{ab} and v_{cb} in Fig. 5) will

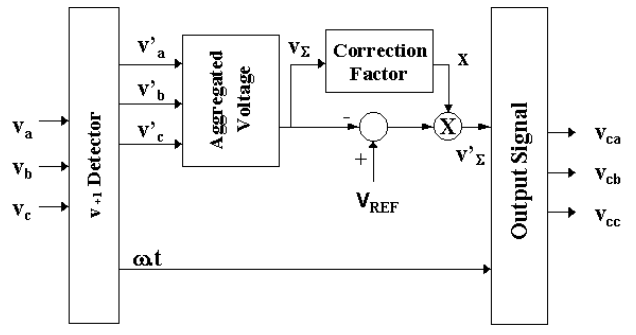

Fig. 3: Control Scheme.

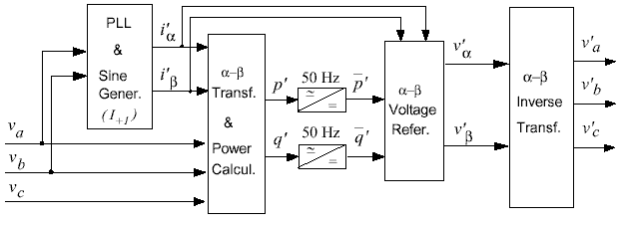

Fig. 4: Positive Sequence Detector.

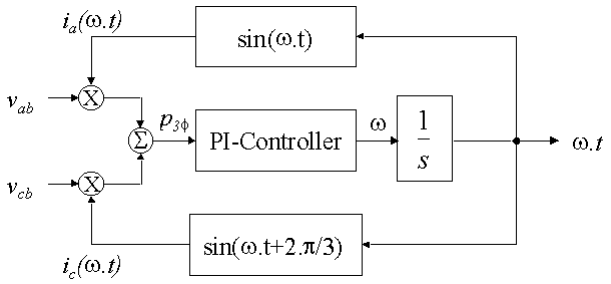

Fig. 5: Block Diagram of the PLL Circuit.

make the phase angle between v_a and $i_a(\omega t)$ become greater than 90°. This leads to a negative input ($p_{3\phi}$) and consequently to a decrease in the output ω, making this phase angle between v_a and $i_a(\omega t)$ even greater. This characterizes an unstable point of operation. Thus, the PLL has only one stable point of operation: $i_a(\omega t)$ leading 90° the phase voltage v_a. This fundamental characteristic of the PLL circuit can be exploited to compose the compensating voltage references for the PWM series converter, as will be shown later. First, the output ω.*t* of the PLL is used to compose auxiliary currents, in terms of αβ coordinates, given as

$$\begin{cases} i'_\alpha = sin(\omega t) \\ i'_\beta = -\cos(\omega t) \end{cases}, \tag{2}$$

that correspond to auxiliary currents composed only by the positive-sequence component at the fundamental frequency and are used in the next block in Fig. 4. In this control block, the voltages v_a, v_b and v_c are transformed into the α-β axis to give v_a and v_b, given as

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} . \tag{3}$$

They are used together with i'_a and i'_b, given by (2), for calculating the auxiliary power *p'* and *q'*, according to (4).

$$\begin{bmatrix} p' \\ q' \end{bmatrix} = \begin{bmatrix} v_a & v_b \\ v_b & -v_a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{4}$$

As mentioned, i'_a and i'_b contain only the fundamental positive-sequence current I'_{+1}. From the general equations of the real and imaginary powers [7], in terms of symmetrical components, given as

$$\bar{p}' = \sum_{n=1}^{\infty} 3V_{+n} I_{+n} \cos(f_{+\mathbf{n}} - d_{+\mathbf{n}}) + \\ + \sum_{n=1}^{\infty} 3V_{-n} I_{-n} \cos(f_{-\mathbf{n}} - d_{-\mathbf{n}}) \tag{5}$$

and

$$\bar{q}' = \sum_{n=1}^{\infty} -3V_{+n} I_{+n} \sin(f_{+n} - d_{+n}) + \\ + \sum_{n=1}^{\infty} 3V_{-n} I_{-n} \sin(f_{-n} - d_{-n}) \tag{6}$$

it is possible to conclude that the average real and imaginary powers, $\bar{p}'$ and $\bar{q}'$, will comprise only the positive-sequence component of the voltages, at the fundamental frequency, that is V_{+1}. The influence of the fundamental negative-sequence and the harmonics will appear only in the high frequency components of *p'* and *q'*. Two 5th order Butterworth low-pass filters are used for obtaining the average values of the real ($= \bar{p}'$) and imaginary ($= \bar{q}'$) powers.

Finally, the α-β voltage reference block of Fig. 4 calculates the voltages v'_a and v'_b, which correspond to the fundamental positive-sequence component (V_{+1}) of the system voltage transformed into the α-β axis, as follows:

$$\begin{bmatrix} v'_a \\ v'_b \end{bmatrix} = \frac{1}{i'^2_a + i'^2_b} \cdot \begin{bmatrix} i'_a & -i'_b \\ i'_b & i'_a \end{bmatrix} \begin{bmatrix} \bar{p}' \\ \bar{q}' \end{bmatrix} . \tag{7}$$

For several applications, the transformed voltages from (7) are useful, and may be directly used in the controller of the power electronics device. If necessary, the *abc*-phase voltages can be calculated applying the inverse transformation given by

$$\begin{bmatrix} v'_a \\ v'_b \\ v'_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v'_\alpha \\ v'_\beta \end{bmatrix} . \tag{8}$$

Experimental results have shown that the fundamental positive-sequence voltage detector presents a good dynamic and satisfactory accuracy, even under non-sinusoidal conditions. It can calculate accurately the amplitude, frequency and phase angle of V_{+1}, that are given in form of continuous time functions v'_a, v'_b and v'_c, or v'_α and v'_β.

Instead of calculating the rms value for each phase voltage, which requires storing past values, the aggregate voltage v_Σ, defined as follows, is used. The main advantage is that v_Σ requires only the present values.

$$\|v_\Sigma\| = \sqrt{v'^2_a + v'^2_b + v'^2_c} \tag{9}$$

For the output voltages v'_a, v'_b, v'_c, which comprise only positive-sequence components, v_Σ is equal to the rms line voltage, i. e.:

$$v_\Sigma = \sqrt{3}.V_k \quad , \tag{10}$$

where V_k, k = a, b or c, is the rms phase voltage.

As an example, suppose bus IN has a rms voltage equal to 0.85pu. It is desired that bus OUT, connected to bus IN through a DVR, presents constant voltage at 1.00 pu, which is supplied to load A. Then, the DVR should supply a voltage equal to 0.15pu and in phase with those in bus

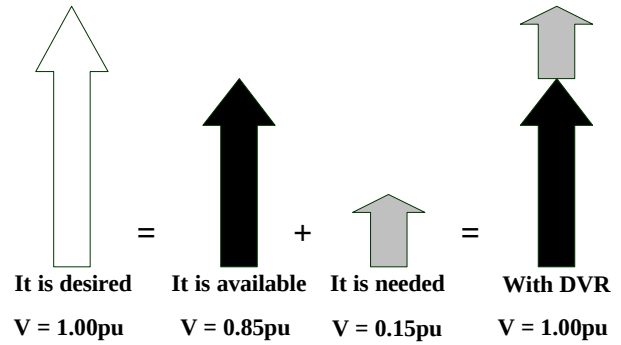

Fig. 6: How the voltage sag is compensated.

IN, as shown in Fig. 6. Therefore, the rms value of the voltages v_{ca}, v_{cb}, v_{cc}, needed to compensate the voltage sag, is given by the difference obtained comparing (9) against a reference V_{REF}. This reference value is equal to the desired rms line voltage at the controlled ac bus (terminals of load A).

The synthesis of v_{ca}, v_{cb}, v_{cc} is carried out by the inverter. Note that these voltages are in phase with v'_a, v'_b, v'_c [see (8)], respectively. However, the voltage sag at bus IN affects also the dc link voltage and the PWM controller of the series converter. Since a diode bridge is used, the dc link voltage is proportional to the line voltage at bus IN (V_{IN}), and is equal to

$$v_{DC}^{(const)} = 1.35 V_{IN} \quad . \tag{11}$$

The symbol $v_{DC}^{(const)}$ is used here to represent the nominal dc voltage (no-load ideal rectified voltage), when V_{IN} is equal to 1 pu.

If the dc voltage would be constant and equal to the nominal value, the ac output voltage of the series PWM converter is given by

$$V''_{LL} = 0.612.m_a.v_{DC}^{(const)} \quad , \tag{12}$$

where m_a corresponds to the amplitude modulation ratio of the PWM control, expressed by

$$m_a = \frac{\hat{v}_{control}}{\hat{v}_{tri}} \quad . \tag{13}$$

The triangular voltage amplitude used in the PWM switching strategy is represented by $\hat{v}_{tri}$. If v_{DC} is constant and equal to the nominal value $v_{DC}^{(const)}$, $\hat{v}_{control}$ corresponds to the amplitude of the compensating voltages v_{ca}, v_{cb} and v_{cc} that should be synthesized by the series PWM converter. Since v_{DC} varies together with V_{IN}, the amplitude modulation ratio m_a must varies inversely, in order to synthesize the desired compensating voltages v_{ca}, v_{cb} and v_{cc}.The correction factor x for m_a is given by

$$x = \frac{v_{DC}^{(const)}}{v_{DC}} \quad , \tag{14}$$

where $v_{DC}^{(const)}$ is determined in (11), considering V_{IN} equal to the nominal rms line voltage of bus IN and v_{DC} is the actual (measured) dc link voltage. Hence, the corrected amplitude modulation ratio m'_a given by

$$m'_a = x.m_a \tag{15}$$

must be used, in order to have the desired compensating voltages, when the dc link voltage varies. Therefore, in order to produce the desired compensating voltage V''_{LL} given in (12), under varying dc link voltage, the following expression should be considered.

$$V''_{LL} = 0.612.m_a.v_{DC}^{(const)} = 0.612.m'_a.v_{DC} \quad . \tag{16}$$

Equation (15) is realized by the multiplier represented in Fig. 3.

The rms value of the compensating phase voltage is determined as:

$$V''_{L0} = \frac{V''_{LL}}{\sqrt{3}} \quad . \tag{17}$$

By this way, the control scheme can compensate any voltage fluctuation in v_{DC} due to voltage sag in v'_a, v'_b, v'_c.

From (17) and from the phase angle $\omega.t$ given by the PLL circuit (Fig. 5), the compensating voltage references can be defined as

$$\begin{aligned} v_{ca} &= \sqrt{2}.V''_{L0}.sin(\omega t - \pi/2) \\ v_{cb} &= \sqrt{2}.V''_{L0}.sin(\omega t - \pi/2 - 2\pi/3) \\ v_{cc} &= \sqrt{2}.V''_{L0}.sin(\omega t - \pi/2 + 2\pi/3) \end{aligned} \quad . \tag{18}$$

The reason of the delay angle $\pi/2$ in (18) was explained before, as the fundamental characteristic of the used PLL circuit that has a unique stable operation point, where $\sin(\omega.t)$ leads $\pi/2$ the fundamental positive-sequence voltage (V_{+1}).

At this point, it should be highlighted that the proposed DVR topology, together with the developed control strategy, allowed a drastic reduction in the energy storage capacity inside the dc link of the DVR. The active power delivered by the series PWM converter, that is needed to compensate the voltage sag, is "instantaneously" drawn from the network by the shunt diode bridge. The greater the voltage sag, the more power is drained from bus IN. If bus IN, under faulty network conditions, has low short-circuit power related to the load A connected at the controlled ac bus, the increasing drain of power by the diode bridge can lead to voltage collapse. Therefore, the short-circuit power of bus IN should be rated as high as possible, or the amount of load connected after the DVR, at the controlled bus (bus OUT in Fig. 2), should be carefully limited.

IV. Test Case

Consider that the power system, shown in Fig. 7, is in steady state and *SW1* is open. During this period, the voltage applied at bus OUT differ from the AC voltage source V_S by the voltage drop in X_S, caused by the load current. When *SW1* is closed at the instant of time t_{close}, the steady state currents drained by loads A and B produce a voltage sag at bus *IN* due to a voltage drop at X_S greater than that

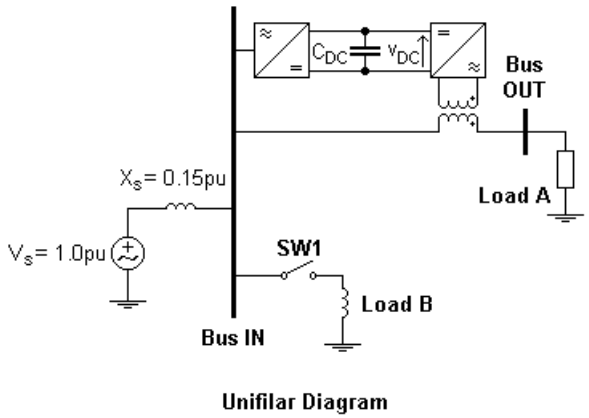

Fig. 7: Power system including DVR.

one before t_{close}. Should load A be a resistive or a RL load, the power flow decreases, as a consequence of the voltage sag, to a value that could be unacceptable for some applications that requires high quality standards.

Here, the proposed DVR offers an alternative solution with respect to that presented in [3], claiming the following objectives:

1. to provide bus OUT, connected at the DVR's output, sinusoidal voltage v_{la}, v_{lb}, v_{lc} regulated at 1,00 pu, for voltage sags in v_a, v_b, v_c up to 0.5 pu;
2. to be simple and efficient, lowering the cost and the complexity of the equipment;
3. to carry out the necessary compensation with very low harmonic generation.

The solution presented here consists of synthesizing three-phase sinusoidal voltage at fundamental frequency in phase with the voltages at bus IN, so that the following algebraic summation holds true:

$$\begin{aligned} v_{la} &= v'_a + v_{ca} = 1.00\,pu = cte \\ v_{lb} &= v'_b + v_{cb} = 1.00\,pu = cte \\ v_{lc} &= v'_c + v_{cc} = 1.00\,pu = cte \end{aligned} \quad (19)$$

To verify the performance of the proposed system, the complete system was simulated using the Saber™ Designer 5.1 software package. The pu base values used are as follows: voltage base = 13.8 $kV_{phase\text{-}phase}$, three-phase power base = 10.0 MVA. The major parameters used in the simulation are as follows:

- ✓ three-phase voltage source: V_S = 1.00pu, X_S = 0.15pu;
- ✓ Load A: RL series circuit per phase, Y connected, with R = 0.90pu, X_L = 0.15pu;
- ✓ Load B: there is an inductor in series with a switch per phase, Y connected. The t_{close} and t_{open} for each switch are as shown in TABLE 1. X_L = 0.67pu;
- ✓ Passive filters: $L_{f1} = L_{f2} = L_{f3}$ = 2mH and $C_{f1} = C_{f2} = C_{f3}$ = 47μH;
- ✓ Capacitor C_{DC}: 10μF;
- ✓ V_{REF} = 1.00pu;
- ✓ PWM inverter switching frequency: f_{sw} = 5.1 kHz.

TABLE 1

t_{close} and t_{open} for each phase of SW1

	Phase A	**Phase B**	**Phase C**
t_{close}	504.167 ms	509.722 ms	515.278 ms
t_{open}	804.167 ms	809.722 ms	815.278 ms

In the simulation, the DVR is blocked, by turning on T1, T3 and T5 and turning off T2, T4 and T6 (see Fig. 2), until the power system reaches the steady state at t(s) = 0.10s. After that, the DVR starts working, compensating any voltage sag at bus OUT. The whole system reaches steady state after 0.20s.

Fig. 8 shows the simulated results of the input and output voltages of the DVR. There are short transients around after the connection and disconnection of load B. After these transients, the *a*-phase voltage applied at load A (v_{la}) do not present any voltage sag. The rms voltage at the controlled ac bus (bus OUT) is kept constant, even during the period when load B is connected to bus IN. The rms voltage at bus OUT remains nearly equal to the nominal value, differing only 0.04 pu. It should be highlighted that the unit used to plot this graph is in pu. The voltage sag in v_a (bus IN) during the period of time t_{close} to t_{open}, is visible. The nominal amplitude is $\sqrt{2}$ (pu). The amplitude of the voltage at bus IN drops to 1.05pu during the connection of load B.

At steady state, the aggregate voltage for bus OUT ($v_{\Sigma A}$) is equal to 0.96pu, nearly equal to the reference value V_{REF}, as shown in Fig. 9. The absolute error between $v_{\Sigma A}$ and V_{REF} occurs mainly due to the use of dead time in the PWM switching control of the series converter. It should be highlighted that this absolute error is constant during the simulation, whatever load B is connected to bus IN or not. The transient periods take no more than 3 cycles, which is much shorter than those presented in [3]. The overshoots in the instantaneous aggregate voltage ($v_{\Sigma A}$) do not exceed 0,10pu and are mainly caused by the time differences in t_{close} and t_{open} of each single-phase switched of load B. All single-phase switches take up to 2/3 cycles to close or open completely. The relatively large commutation inductors of the diode bridge also contribute to increase the overshoots.

The difference between the aggregate value (v_{Σ}) at bus IN and the reference value (1 pu) is shown in Fig. 10. As

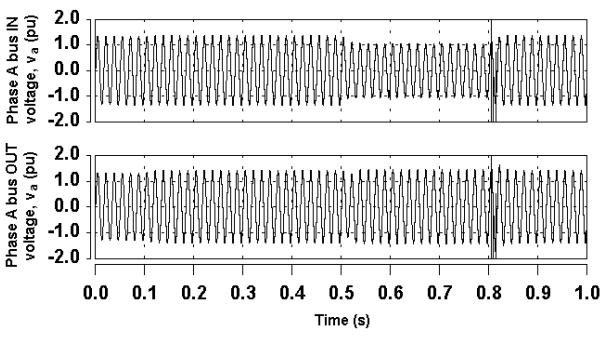

Fig. 8: DVR input and output voltages.

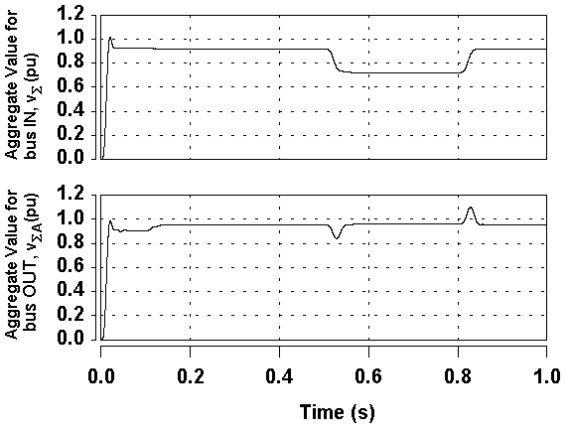

Fig. 9: Aggregate values at DVR's input and output.

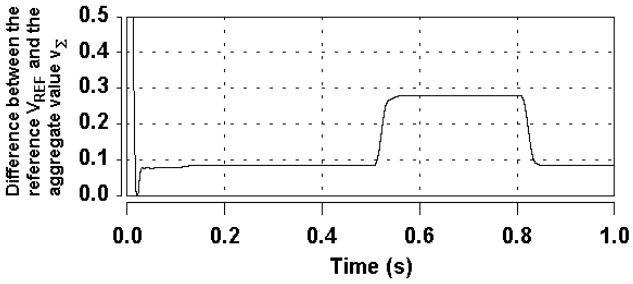

Fig. 10: Difference between v_Σ and V_{REF}.

expected, it is greater when load B is connected to bus IN.

As can be seen in Fig. 11, the *a*-phase voltage of bus OUT is nearly sinusoidal. The high frequency used in the PWM switching of the series converter is well filtered. However, it still presents some distortions at low frequencies due to the unavoidable high-distorted currents drained by the diode bridge. Nevertheless, the total harmonic distortion (THD) of the compensated voltages is still at acceptable level.

Finally, it should be noted that the proposed DVR is not able to compensate permanently voltage swells, because it would involve power flowing into the series converter. This flow of energy would cause overcharging of the dc capacitor voltage, since the diode bridge cannot regenerate energy.

V. Conclusions

In this paper, a three-phase DVR with the function of voltage sag compensation was explored. The operation of the proposed system configuration is verified by simulations. Optimization of the commutation inductances and

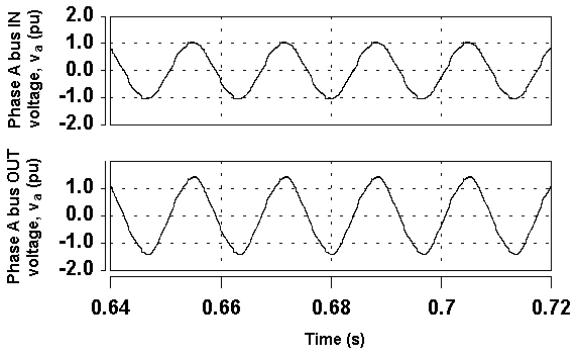

Fig. 11: Zooming the voltages v_a and v_L.

the use of proper passive filters allowed a reduction of harmonic pollution, to acceptable levels of THD in voltages and currents. The results show that the system is able to completely compensate voltage sags quickly, for long periods or even in steady state.

Presently, the authors are working in the implementation of a 2.0 kVA DVR laboratory prototype, using digital control (DSP) and in the investigation of incorporating active filtering functions, as well as compensation of voltage unbalances caused by the fundamental negative-sequence component.

VI. References

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