A Design Procedure for a Non-Dissipative Turn-on Turn-off Snubber Applied to the AC-DC Boost Converter

Anis C. Chehab and Ivo Barbi

Power Electronics Institute – INEP
Dept. of Electrical Engineering
Federal University of Santa Catarina – UFSC
P.O. Box 5119 – 88040-970 – Florianópolis – SC – Brazil
anis@inep.ufsc.br and ivobarbi@inep.ufsc.br

***Abstract* - The main goal of this paper is to present a design procedure for the correct choose of components for a non-dissipative turn on – turn off passive snubber applied to the power factor correction (PFC) boost converter. The snubber theoretical analysis and experimental results taken from a 1kW, 30kHz laboratory prototype are also presented.**

I. INTRODUCTION

Nowadays there are a lot of industrial applications that use switched converters, as: Inverters, UPS (Uninterrupted Power Supply), Ballast, Telecommunication's Power Supplies and so on. A very popular circuit used on most of these applications is the PFC based on the boost converter. The use of higher frequencies is a tendency when it is desirable to reduce volume and weight; as a consequence, the commutation losses increase a lot, becoming an important problem to be solved. A non-dissipative snubber has the purpose of taking advantage of the energy that would be lost during commutation, sending it to the source or to the load. The active snubbers are expensive and complex. So, the use of passive snubbers is becoming very common because they're cheap and reliable. During a brief review of what was done on this area ([1], [2], [3], [4], [5] and [6]), it was clear the importance of a reliable non-dissipative snubber's design procedure. The snubber presented on [1] and [5] was chosen to be deeply studied since it is a turn on - turn off snubber and presents few components.

II. THE SNUBBER PRESENTATION

The DC-DC boost converter with the chosen snubber is presented on Fig. 1. An inductor (L_s), two capacitors (C_s and C_a) and three diodes (D_{a1}, D_{a2} and D_{a3}) compose it. The inductor L_s limits the di/dt during the diode's (D_b) reverse recovery. The capacitor C_s limits the dv/dt across the boost switch (S_b) during its turn off. And the capacitor C_a is responsible to regenerate all the energy stored in the snubber components, sending it to the load through diodes D_{a1}, D_{a2} and D_{a3}.

III. PRINCIPLE OF OPERATION AND RESULTS FROM THE MATHEMATICAL ANALYSIS

In order to make easier the comprehension of the operation principle of the circuit from Fig. 1, some simplifications were done. It was considered that the current ripple through the boost inductor (L_b) and the voltage ripple across the output capacitor (C_o) are negligible, so the converter can be modeled as an input current source (I_1) and an output voltage source (V_o). This simplification also is valid if the converter is operating as a PFC stage, since the switching frequency is much bigger than the line frequency. Inductor L_s reduces a lot the reverse recovery's peak current, so this phenomena can also be neglected. All the components are ideal. Only the main equations used to find the proposed design procedure will be presented. The converter topological state during each snubber operational stage and the main waveforms are shown from Fig. 3 to Fig. 11 and Fig. 2 respectively, and described as follows:

1st stage ($t_0 – t_1$): Diode D_b conducts the input current, transferring energy from the source to the load. The capacitor C_s is charged with the output voltage V_o and the capacitor C_a is discharged. This stage ends at instant t_1 when the control circuit turns on the switch S_b.

2nd stage ($t_1 – t_2$): This stage begins at instant t_1 when the switch S_b is turned on. The current through diode D_b decreases following a rate given by $-V_o/L_s$, and the current through switch S_b increases following the same rate. This stage ends at instant t_2 when the current through diode D_b reaches zero and it is turned off. The time interval of this stage is given by (1).

$$\Delta t_2 = \left(L_S \cdot I_1\right)/V_o \qquad (1)$$

3rd stage ($t_2 – t_3$): This stage begins at instant t_2 when the capacitor C_s begins to discharge through diode D_{a2}, transferring its energy to the inductor L_s and to the capacitor C_a, in a resonant way. This stage ends at instant t_3 when the capacitor C_s is completely discharged, directly polarizing diode D_{a1}. The time duration of this stage is given by (2), where $\omega = \sqrt{\left(C_S + C_a\right)/L_S \cdot C_S \cdot C_a}$ and $\omega_S = \sqrt{1/L_S \cdot C_S}$.

$$\Delta t_3 = \left(\text{acos}(1-\omega^2/\omega_s^2)\right)/\omega \qquad (2)$$

4th stage ($t_3 – t_4$): This stage begins at instant t_3 when diode D_{a1} starts to conduct and the inductor L_s transfers its energy to the capacitor C_a in a resonant way. This stage ends at instant t_4 when the current through inductor L_s reaches zero and diodes D_{a1} and D_{a2} are turned off. The

time interval of this stage is given by (3) where $\omega_a = \sqrt{1/L_s \cdot C_a}$.

$$\Delta t_4 = \left(\text{atan}\left(\left(\sqrt{2\cdot\omega_s^2 - \omega^2}\right)/\omega_a\right)\right)/\omega_a \quad (3)$$

5th stage ($t_4 - t_5$): This stage begins at instant t_4. The switch S_b conducts the input current until the moment t_5 when the control circuit turns it off.

6th stage ($t_5 - t_6$): This stage begins at instant t_5 when the switch S_b is turned off and the input current is quickly deviated, through diode D_{a1}, to the capacitor C_s, charging it. This stage ends at instant t_6 when the voltage across capacitor C_s added to the voltage across capacitor C_a reaches the output voltage, directly polarizing diode D_{a3}. The time interval of this stage is given by (4).

$$\Delta t_6 = \left(\left(V_o \cdot C_s\right)/I_1\right)\cdot\left(1-\omega_a/\omega_s\right) \quad (4)$$

7th stage ($t_6 - t_7$): This stage begins at instant t_6 when the capacitor C_a begins to discharge. The capacitor C_s is still charging. This stage ends at instant t_7 when the voltage across capacitor C_s reaches the output voltage V_o, directly polarizing diode D_{a2}. (5), (6), (7) and (8) give the time interval and the main equations that describe this stage, where $x = C_s/C_a$, $Z_s = \sqrt{L_s/C_s}$ and

$$A = -\sqrt{8\cdot(1+x)}\cdot\cos\left(\text{acos}\left(\left(3\cdot V_o\cdot\sqrt{x}\right)/\left(\sqrt{8}\cdot I_1\cdot Z_s\right)\right)+4\cdot\pi\right)/3) .$$

$$\Delta t_7 = A/\omega \quad (5)$$

$$I_{Ls}(t) = I_1\cdot\left(C/C_s\right)\cdot\left(1-\cos(\omega\cdot t)\right) \quad (6)$$

$$I_{Ls}(t_7) = \left(I_1/(x+1)\right)\cdot\left(1-\cos(A)\right) \quad (7)$$

$$V_{Ca}(t_7) = \frac{I_1\cdot Z_s\cdot x}{\sqrt{(x+1)^3}}\cdot\left(\text{sen}(A)-A\right)+V_o\cdot\sqrt{x} \quad (8)$$

8th stage ($t_7 - t_8$): This stage begins at instant t_7. The current through inductor L_s continues to increase and, at the same time, the capacitor C_a keeps discharging. This stage ends at instant t_8 when the current through L_s reaches the input current and diodes D_{a1} and D_{a2} turn off. (9), (10) and (11) give the time interval and the main equations that describe this stage, where $Z_a = \sqrt{L_s/C_a}$ and $B = I_{Ls}(t_7)^2 + \left(V_{Ca}(t_7)^2/Z_a^2\right)$.

$$\Delta t_8 = \left|\text{asen}\left(\left(\left(2\cdot V_{Ca}(t_7)\cdot I_1/Z_a\right)-2\cdot I_{Ls}(t_7)\cdot\sqrt{B-I_1^2}\right)/2\cdot(B)\right)\right|/\omega_a \quad (9)$$

$$V_{Ca}(t_8) = -Z_a\cdot I_{Ls}(t_7)\cdot\text{sen}(\omega_a\cdot\Delta t_8)+V_{Ca}(t_7)\cdot\cos(\omega_a\cdot\Delta t_8) \quad (10)$$

$$V_{Ca}(t) = -I_{Ls}(t_7)\cdot Z_a\cdot\text{sen}(\omega_a\cdot t)+V_{Ca}(t_7)\cdot\cos(\omega_a\cdot t) \quad (11)$$

9th stage ($t_8 - t_9$): This stage begins at instant t_8 when the current through inductor L_s reaches the input current. The capacitor C_a continues to discharge, but now in a linear way. This stage ends at the instant t_9 when the voltage across capacitor C_a reaches zero and the input current is assumed by the boost diode, coming back to the first stage. Its time interval is given by (12).

$$\Delta t_9 = C_a\cdot V_{Ca}(t_8)/I_1 \quad (12)$$

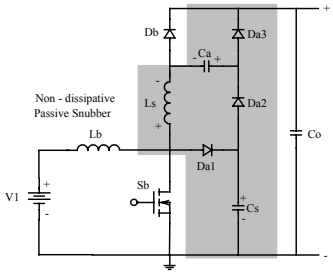


Fig. 1 - DC-DC boost converter with snubber.

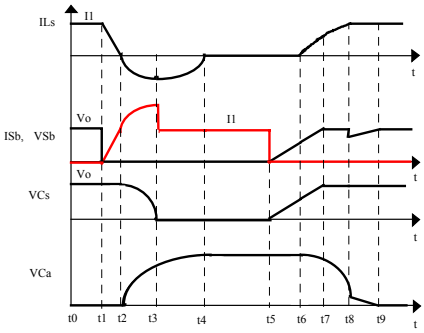


Fig. 2 - Main illustrative waveforms.

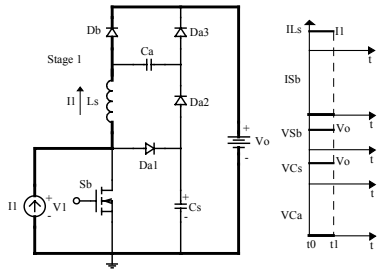


Fig. 3 – 1st operational stage.

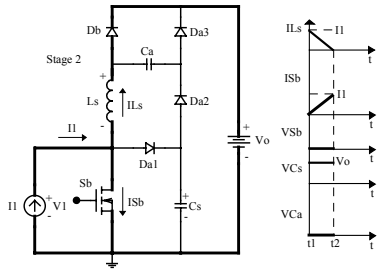


Fig. 4 – 2nd operational stage.

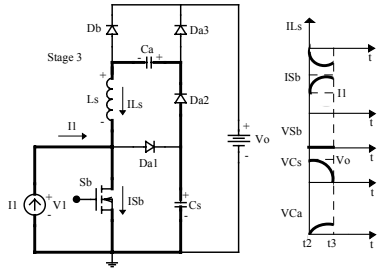


Fig. 5 – 3rd operational stage.

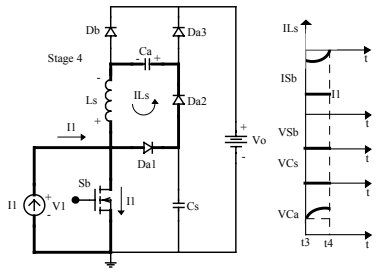


Fig. 6 – 4th operational stage.

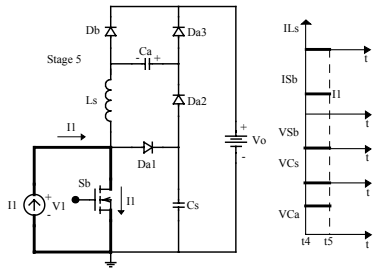


Fig. 7 – 5th operational stage.

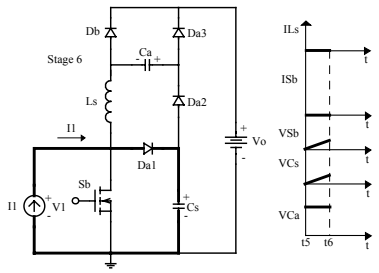


Fig. 8 – 6th operational stage.

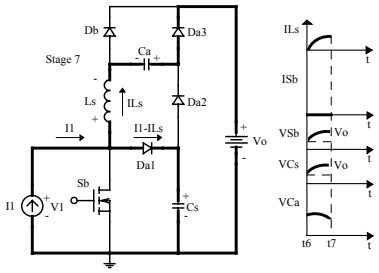


Fig. 9 – 7th operational stage.

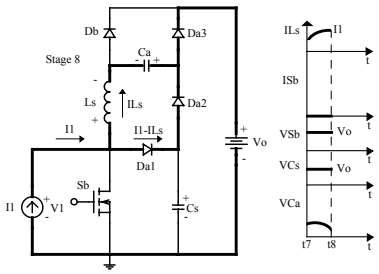


Fig. 10 – 8th operational stage.

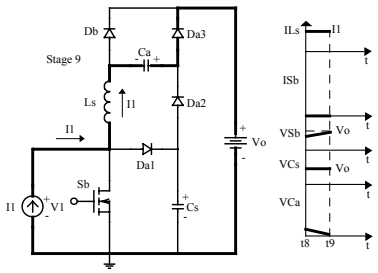


Fig. 11 – 9th operational stage.

IV. OPERATIONAL RESTRICTIONS AND MAIN ABACUS FOR THE DESIGN PROCEDURE

Four operational restrictions must be obeyed to have the snubber operating in its correct way, as discussed before:

- The first one is related to the seventh stage. In this stage, the voltage across capacitor C_s must reach the output voltage V_o before or at the same time that the current through L_s reaches the input current. Otherwise, the circuit goes to the topological state showed in Fig. 12. The worst case happens when $I_1=I_{1min}$, the instant in which the snubber must start to work correctly, considering that the converter is being used as a PFC stage.
- The second one is related to the eighth stage. In this stage, the current through inductor L_s must reach the input current before or at the same time that the voltage across capacitor C_a reaches zero. Otherwise, the circuit also goes to the topological state showed in Fig. 12. The worst case happens when $I_1=I_{1max}$, when the input current crosses its peak value.
- The snubber operational stages 2nd, 3rd and 4th referred to the switch turn on, must happen in a time interval smaller, or at least equal, to the smallest time interval the switch remains conducting, which happens when $I_1=I_{1max}$.
- The snubber operational stages 6th, 7th, 8th and 9th referred to the switch turn off, must happen in a time interval smaller, or at least equal, to the smallest time interval the switch remains turned off, which happens when $I_1=I_{1min}$.

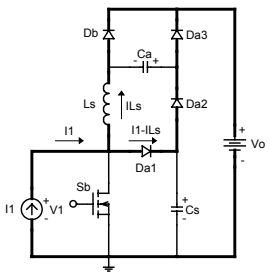


Fig. 12 – Prohibit topological stage inside the desirable range of operation.

Making a brief analysis of the topological state presented in Fig. 12, it can be concluded that: The voltage across inductor L_s is zero and the current through it remains constant until the moment the switch is turned on.

At this moment, the amount of current through diodes D_{a1}, D_{a2} and D_{a3} is quickly deviated to the switch (with an increasing rate only limited by the loop impedance, which is almost null). Depending on this amount of current, it can increase a lot the commutation losses across the switch S_b.

After a hard mathematical analysis of these restrictions, it were found four abacus that are very useful for choosing correctly the snubber components, given a converter specification. These curves are shown in Fig. 13, Fig. 14, Fig. 15 and Fig. 16. Equations (13), (14) and (15) define mathematically the abacus shown in Fig. 14, Fig. 15 and Fig. 16, respectively. V_{1peak} is the input voltage peak value, f_s is the switching frequency and ΔI_1 is the current ripple through the boost inductor.

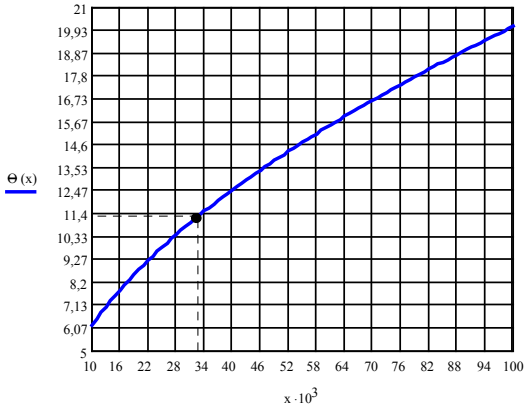


Fig. 13 – Electrical instant (degrees) of I_{1min} as a function of 'x'.

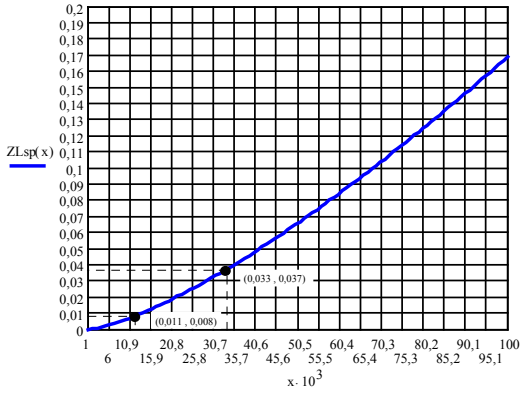


Fig. 14 – Normalized inductive impedance of L_s as a function of 'x'.

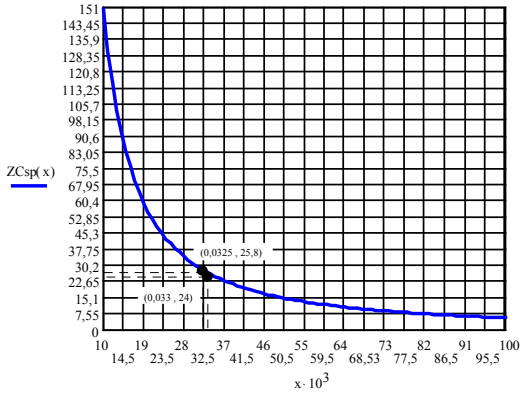


Fig. 15 – Normalized capacitive impedance of C_s as a function of 'x'.

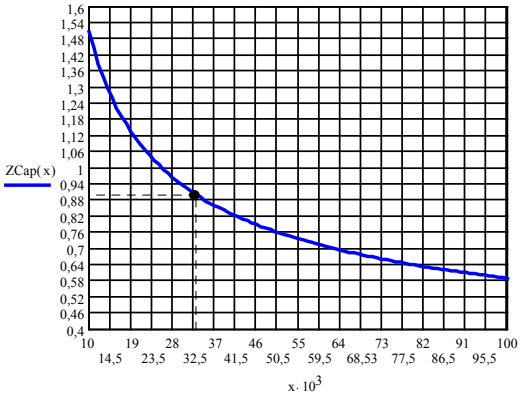


Fig. 16 – Normalized capacitive impedance of C_a as a function of 'x'.

$$ZL_{sp}(x) = \frac{\left(I_{1max} + \Delta I_1/2\right) \cdot 2 \cdot \pi \cdot f_s \cdot L_s}{V_{1peak}} \quad (13)$$

$$ZC_{sp}(x) = \frac{\left(I_{1max} + \Delta I_1/2\right) \cdot V_{1peak}}{2 \cdot \pi \cdot f_s \cdot C_s \cdot V_o^2} \quad (14)$$

$$ZC_{ap}(x) = ZC_{sp}(x) \cdot x = \frac{\left(I_{1max} + \Delta I_1/2\right) \cdot V_{1peak}}{2 \cdot \pi \cdot f_s \cdot C_a \cdot V_o^2} \quad (15)$$

It can be verified that the current ripple through the boost inductor appeared in equations (13), (14) and (15) since, depending on the converter specifications, this value can be relevant. The following considerations must be taking account to choose the parameter 'x':

- The minimum value of $ZL_{sp}(x)$ is related to the maximum di/dt desirable through the boost diode during its reverse recovery;
- The maximum value of $ZC_{sp}(x)$ is related to the maximum dv/dt desirable across switch S_b and capacitor C_s;
- These considerations give a minimum value for the parameter 'x'. From Fig. 13, as greater is the value of 'x', smaller is the correct operational range of the snubber, so it's desirable to choose the smallest value of 'x' allowed.

V. A DESIGN PROCEDURE EXAMPLE AND EXPERIMENTAL RESULTS

In order to validate the abacus obtained, it was implemented a PFC boost converter with the snubber presented. The specifications are shown in Table 1. The design procedure to find the values of L_s, C_s and C_a is presented below:

First of all, it must be found the values of 'x' corresponding to the minimum value of ZL_{sp} and the maximum value of ZC_{sp}.

$$ZL_{sp_{min}} = \frac{(I_{1max} + \Delta I_1/2) \cdot 2 \cdot \pi \cdot f_s \cdot V_o}{V_{1peak} \cdot (di/dt)_{max}} \quad (16)$$

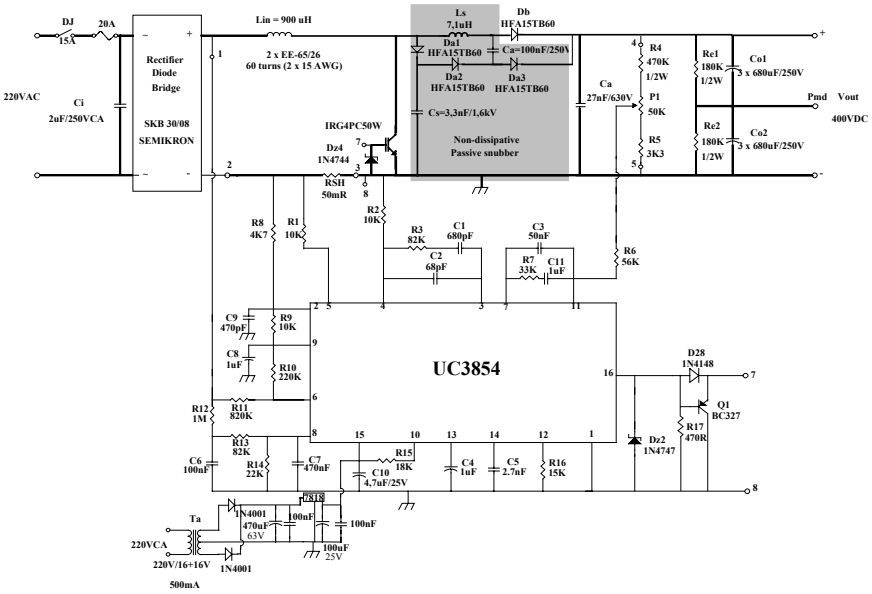


Fig. 17 – Electrical diagram of the circuit implemented in the laboratory.

$$ZL_{sp_{min}} = \frac{(6,76+1,845)\cdot 2\cdot\pi\cdot 30k\cdot 400\cdot 10^{-6}}{311\cdot 250} = 0,00834$$

From Fig. 14: $ZL_{sp_{min}} = 0,00834 \rightarrow x_{min(1)} = 0,011$

$$ZC_{sp_{max}} = \frac{(I_{1max} + \Delta I_1/2)\cdot V_{1peak}\cdot (dv/dt)_{max}}{2\cdot\pi\cdot f_s\cdot (I_{1max}+\Delta I_1/2)\cdot V_o^2} \qquad (17)$$

$$ZC_{sp_{max}} = \frac{(6,76+1,845)\cdot 311\cdot 2500}{2\cdot\pi\cdot 30k\cdot (6,76+1,845)\cdot 10^{-6}\cdot 400^2} = 25,79$$

From Fig. 15: $ZC_{sp_{max}} = 25,79 \rightarrow x_{min(2)} = 0,0325$

Considering the values of 'x' found above and having in mind that this parameter must be smaller as possible, it is chosen x=0,033. So, replacing this value on the equations (13) and (14), it is obtained:

$$L_s(0,033) = \frac{ZL_{sp}(0,033)\cdot V_{1peak}}{2\cdot\pi\cdot f_s\cdot (I_{1max}+\Delta I_1/2)}$$

$$L_s(0,033) = \frac{0,037\cdot 311}{2\cdot\pi\cdot 30k\cdot (6,76+1,845)} = 7,1\mu H$$

$$\boxed{L_s = 7,1\mu H}$$

$$C_s(0,033) = \frac{(I_{1max}+\Delta I_1/2)\cdot V_{1peak}}{ZC_{sp}(0,033)\cdot 2\cdot\pi\cdot f_s\cdot V_o^2}$$

$$C_s(0,033) = \frac{(6,76+1,845)\cdot 311}{24\cdot 2\cdot\pi\cdot 30k\cdot 400^2} = 3,6nF$$

→ Commercial value: C_s=3,3nF

$$\boxed{C_s = 3,3nF}$$

$$C_a(0,033) = C_s(0,033)/x = 3,3\cdot 10^{-9}/0,033 = 100nF$$

$$\boxed{C_a = 100nF}$$

The electrical diagram of the circuit implemented in the laboratory is shown on Fig. 17.

Table 1 – Converter specifications.

V_l=220Vac$_{rms}$	(Line voltage)
P_o=1kW	(Output power)
V_o=400Vdc	(Output voltage)
f_s =30kHz	(Switching frequency)
$(di/dt)_{max}$=250A/us	(Maximum di/dt desirable)
$(dv/dt)_{max}$=2500V/us	(Maximum dv/dt desirable)
L_b=900uH	(Boost inductor)
DI_l=3,69A	(Current ripple)
0,95	(Expected efficiency)

The input current and voltage with the snubber included are shown in Fig. 18. In Fig. 19 to Fig. 22 are shown the switch and boost diode (turn-on and turn-off) commutations with the snubber. In Fig. 23 to Fig. 26 are presented the same waveforms without the snubber.

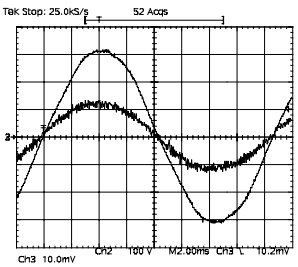


Fig. 18 – Input current and voltage with snubber. (5A/div. and 100V/div.)

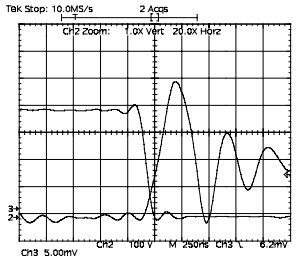


Fig. 19 - Switch turn-on with snubber. (2,5A/div and 100V/div.)

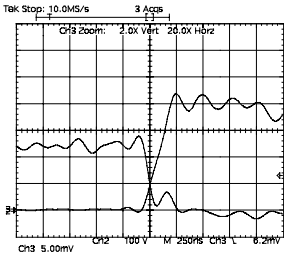


Fig. 20 – Switch turn-off with snubber. (2,5A/div. and 100V/div.)

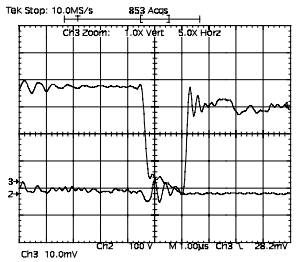


Fig. 21 – Diode D_b turn-on with snubber. (2,5A/div. and 100V/div.)

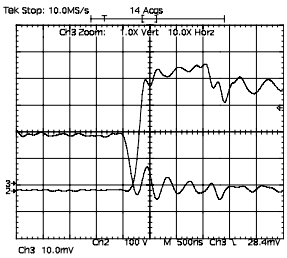


Fig. 22 – Diode D_b turn-off with snubber. (2,5A/div. and 100V/div.)

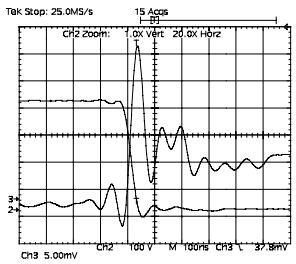


Fig. 23 – Switch turn-on without snubber. (2,5A/div. and 100V/div.)

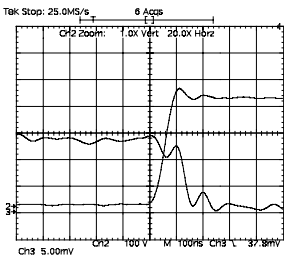


Fig. 24 – Switch turn-off without snubber. (2,5A/div. and 100V/div.)

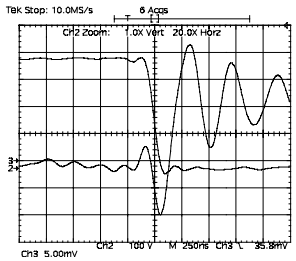


Fig. 25 – Diode D_b turn-on without snubber. (2,5A/div. and 100V/div.)

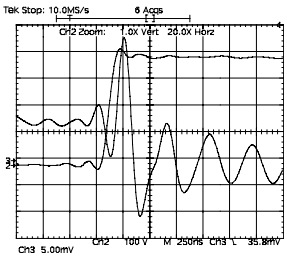
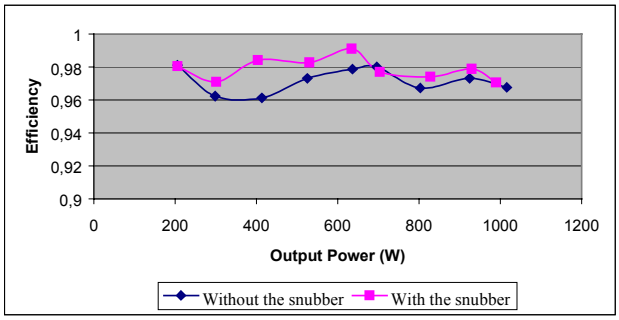


Fig. 26 – Diode D_b turn-off without snubber. (2,5A/div. and 100V/div.)

It was verified in the laboratory that the snubber does not affect the quality of the input current. Due to the snubber, the commutation is with almost null current during the switch turn-on and almost null voltage during the switch turn-off. Due the insertion of the inductor L_s, the reverse recovery peak current is almost neglected and di/dt is controlled. The insertion of the capacitor C_s makes the dv/dt also controlled. Those characteristics reduce a lot the EMI interference and increases the efficiency of the converter. An efficiency comparison of the PFC tested in laboratory with and without snubber is showed in Table 2. Depending on the load, the efficiency difference reached almost 3%. The efficiency without the snubber is also very good since the switching frequency and output power processed are low.

Table 2 - Efficiency comparison with and without the snubber.



VI. CONCLUSION

From this study, some conclusions can be drawn:

- The mathematical analysis to develop the curves presented in Fig. 13 to Fig. 16 is very hard, but the results obtained are very good since it makes possible the correct choice of the snubber components without having to adjust those parameters by simulation;
- The commutation losses are very small and di/dt and dv/dt are controlled which decreases the EMI interference;
- Even neglecting the boost diode reverse recovery peak current, the switch peak current is more than twice its nominal current. This is an disadvantage of this snubber;
- The efficiency comparison showed that with the snubber, the efficiency of the converter was improved. Even without the snubber, it efficiency was very good since the chosen switching frequency was small. It can be concluded that this kind of snubber is more recommended to be applied when it is working with a frequency greater than 30kHz and an output greater than 1kW.

VII. REFERENCES

[1] Nasser H. Kutkut, "Investigation of Soft Switched IGBT Based Boost Converters for High Power Applications*",in 32nd IEEE Industry Applications Society Annual Meeting*, Vol.2, 1997, pp. 1616-1623.

[2] K. Mark Smith Jr and K. M. Smedley, "Engineering Design of Lossless Passive Soft Switching Methods for PWM Converters. I. With Minimum Voltage Stress Circuit Cells", *in 13th Annual Applied Power Electronics Conference and Exposition*, Vol.2, 1998, pp. 1055-1062.

[3] Ching-Jung Tseng and Chern-Lin Chen, "Passive Lossless Snubbers for DC/DC Converters", *in 13th Annual Applied Power Electronics Conference and Exposition*, Vol.2, 1998, pp. 1049-1054.

[4] Hanan Levy, Isaac Zafrany, Gregory Ivensky and Sam Ben-Yaakov, "Analysis and Evaluation of a Lossless Turn-on Snubber", *Proceedings APEC'97*, pp. 757-763.

[5] S. Ben-Yaakov and G. Ivensky, " Passive Lossless Snubbers for High Frequency PWM Converters", *Proceedings PESC'97*.

[6] Cícero Marcos Taváres Cruz, "*Estudo de retificadores monofásicos e trifásicos não reversíveis de três níveis, operando com fator de potência unitário: comutação, modulação e controle*" (in Portuguese), Qualification Exam, UFSC (Federal University of Santa Catarina)-INEP (Power Electronic Institute), Brazil, 1999.