Analysis, Design And Experimentation Of A Snubber For The Three-Level Neutral Clamped Inverter

Yales Rômulo de Novaes and Ivo Barbi

INEP - Power Electronics Institute
UFSC - Federal University of Santa Catarina
P.O. Box: 5119 - fax: +55-48-234-5422
88040-970 – Florianópolis – SC – Brazil
www.inep.ufsc.br – yales@inep.ufsc.br

***Abstract* – The study of a totally passive snubber applied to the Three-Level Neutral Clamped Inverter is presented in this paper. The snubber circuit aids all commutations in all the switches. The voltage across the switches is clamped close to half of the input voltage, and the snubber does not excessively increase current stresses. The description of the operation, theoretical analysis and experimental results are presented in this paper, for a 10 kW prototype.**

I. INTRODUCTION

During the commutations, the simultaneous presence of voltage and current in the power switches causes denominated commutation losses. Being the commutations hard, the losses in a switch become directly proportional to the commutation frequency, limiting for instance, the frequency increase and the possibility of reduction of the output filter volume. The hard switching also can impair the efficiency of a certain structure, as well as increase the necessary heatsink volume of the semiconductors. This work will present a passive snubber circuit without direct regeneration of energy, applicable to the Three-Level Neutral Clamped Inverter also known by the acronym NPC. The presented snubber is derived from the Undeland Snubber [1], usually employed in half-bridge inverters and full bridge inverters, including the contribution published by Péres [2].

II. DESCRIPTION OF THE CIRCUIT AND OPERATION PRINCIPLES

Fig. 1 shows the passive snubber circuit, together with the three-level inverter. Switches S1, S2, S3, S4, diodes Dg1, Dg2, D1, D2 and D4 form the inverter circuit. The principal characteristic of this inverter is that the applied voltage on the switches is half of the input voltage, and the output voltage has three levels [3, 4]. The other components (Ds1, Ds2, Ds3, Ds4, Cs1, Cs2, Cg1, Cg2, Rg1 and Rg2) compose the snubber circuit. Inductors Ls1 and Ls2 propitiate the soft commutation of the switches during turn-on and capacitors Cs1 and Cs2 accomplish the soft commutation turn-off. Capacitors Cg1 and Cg2 are of high value and they will be represented here as ideal voltage sources, that are responsible for storing the energy originated from structure's operation stages. Resistors Rg1 and Rg2 have the function of dissipating this energy.

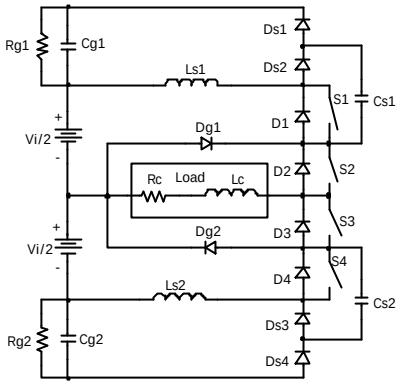

Fig. 1– Three Level Inverter with the snubber circuit.

In this work the three levels modulation with fourth wave symmetry [5] was used, because it presents better results in relation to the total harmonic distortion when compared to other modulation types [6]. However, the analysis can be easily extended for other modulation types.

A. Topological Stages For No-load Operation

First of all, it will be demonstrated that in no-load operation, some energy is dissipated in the snubber circuit. Due to operation symmetry, only the topological stages regarding the positive semi-cycle output voltage will be shown (see Fig. 2).

During the no-load operation of the inverter, the average current that flows through source Vg and the power dissipated by resistor Rg, are represented in (1) and (2), respectively.

Fig. 3 shows the power dissipated by resistor Rg in function of voltage Vg and using the relationship between frequencies as a parameter.

$$\overline{IVg_{AVG}} = \frac{\mu o(1+q)}{4.\pi.q} \qquad (1)$$

$$\overline{PVg} = \frac{1}{4\pi}\mu o(1+q) \qquad (2)$$

where:

$$\overline{IVg_{AVG}} = IVg_{AVG}.\frac{Vin}{2}.\sqrt{\frac{Ls}{Cs}} \qquad (3)$$

IVg_{AVG} - Average current of resistor Rg.

μo - Relationship between the resonant frequency of the snubber (Ls and Cs) and the commutation frequency.

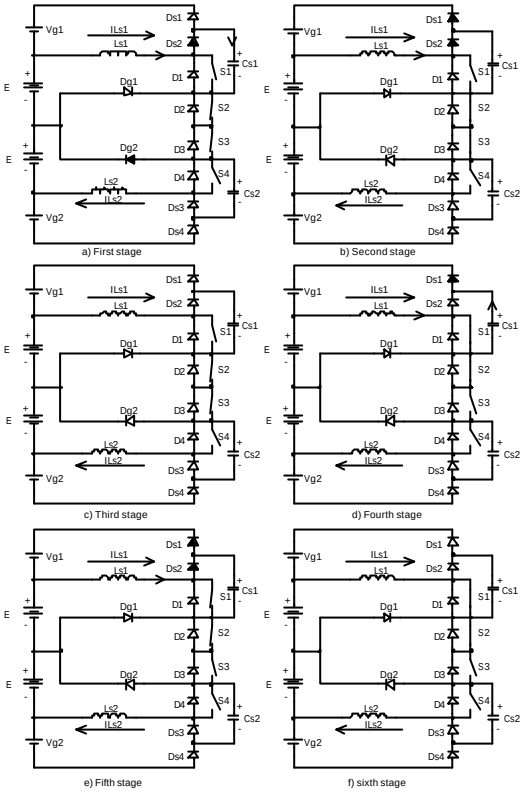

Fig. 2 – Topological stages for the Three-Level Inverter.

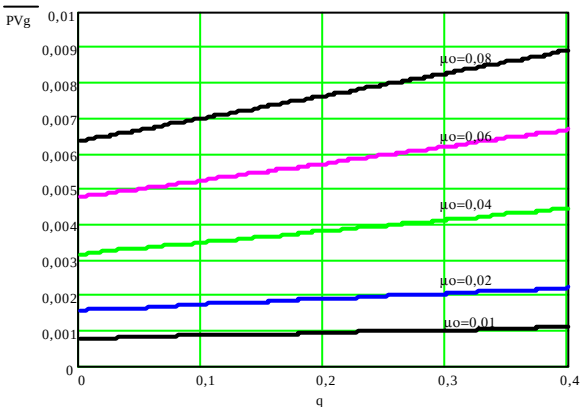

Fig. 3 – Power dissipated by source Vg in no-load operation.

q – Relationship between the clamping voltage and half of the input voltage.

PVg – Power dissipated by resistor Rg.

Icp – Load's peak current.

B. *Topological stages for load operation*

Analyzing the operation of the inverter operating with a load, we can determine its stages of operation, as represented in Fig. 4. This mode of operation presents seven topological stages, explained as follows:

First stage (t_0, t_1)

In this stage, switches S1 and S2 conduct the load current, Ic(t), and the current through inductor Ls is equal to the load current. The voltage across capacitor Cs is equal to zero and the output voltage is equal to E. During this stage, the energy is transferred to the load.

Second stage (t_1, t_2)

At instant t1, switch S1 is turned-off, consequently, diode Ds2 conducts the load current through capacitor Cs. The voltage across this capacitor changes from zero to E+Vg.

Third stage (t_2,t_3)

At instant t2, the voltage across capacitor Cs is equal to Vg+E and diode Ds1 starts to conduct current ILs, demagnetizing inductor Ls. During this stage, the energy stored in inductor Ls is transferred to source Vg. Diode Dg turns-on at instant t2 and the load current circulates in free-wheeling.

Fourth stage (t_3, t_4)

At instant t3, the current that circulates through inductor Ls becomes null, blocking diodes Ds1 and Ds2. The load current circulates through diode Dg. The duration of this stage is defined by the command of switch S1.

Fifth stage (t_4, t_5)

At instant t4, switch S1 is gated-on and the turn-on commutation is soft due to inductor Ls. The current that circulates through the clamping diode, Dg, is gradually transferred to switch S1 and the current through inductor Ls increases linearly up to the load current, Ic(t).

Sixth stage (t_5, t_6)

At instant t5, diode Dg is blocked and diode Ds1 starts to conduct. The current that circulates through Ls and the voltage in capacitor Cs change in a sinusoidal form until capacitor Cs is fully discharged.

Seventh stage (t_6, t_7)

At instant t_6, the voltage across capacitor Cs remains null and diode Ds2 is turned-on, conducting the excessive current due to the resonant stage. The end of this stage occurs when currents ILs(t) and Ic(t) become equal, blocking diodes Ds1 and Ds2, concluding one cycle of operation.

C. *Simulation Results*

Fig. 5 shows the main waveforms of the inverter, obtained from simulation results, using ideal model components. As can be observed in this figure, the commutation of the switches becomes quite attractive when using the snubber.

D. *Quantitative analysis*

By the mathematical analysis of each topological state, considering ideal conditions, we can develop some important equations to design this snubber.

Equations (4), (5), (6) and (7) represent the average current for a commutation and a modulation period.

$$\overline{IVg_{AVGI}} = \frac{1}{Tc}\left(\int_0^{\Delta t32} \overline{Ic(t)} - q.wo.tdt + \int_0^{\Delta t65} sen(wot)dt + \int_0^{\Delta t76} \overline{I1} - q.wo.tdt\right) \quad (4)$$

$$\overline{IVg_{AVGI}} = \frac{mo}{4pq}\left(\overline{Ic(t)}^2 + (q+1)^2\right) \quad (5)$$

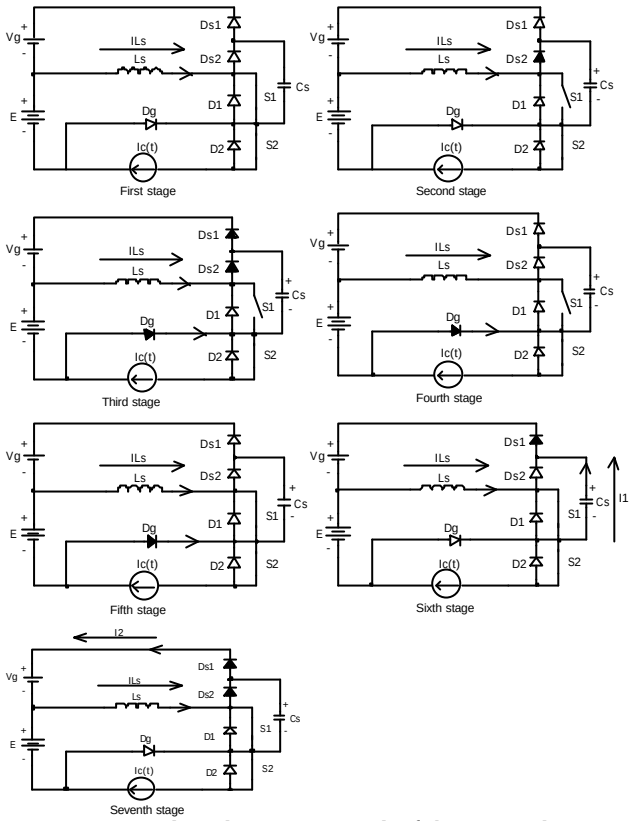

Fig. 4 – Topological stages in one cycle of the output voltage.

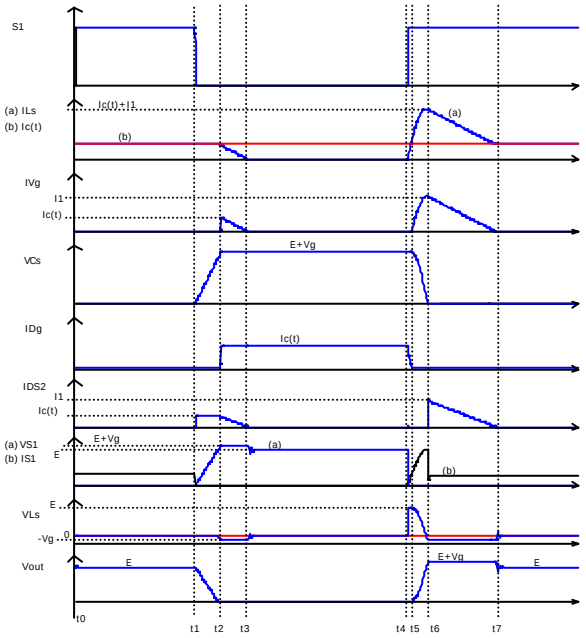

Fig. 5 – Main waveforms.

$$\overline{IVg_{AVG}} = \frac{1}{2\pi}\left(\int_0^{\pi} \frac{m\pi}{4\pi q}\left(\overline{Icp}^2.sen^2(\omega t) + (q+1)^2\right) d\omega t\right) \quad (6)$$

$$\overline{IVg_{AVG}} = \frac{m\pi}{8\pi q}\left(\frac{1}{2}\overline{Icp}^2 + (q+1)^2\right) \quad (6)$$

In the same manner, we will determine the power dissipated by resistor Rg and current stresses in the components of the snubber, as follows:

$$\overline{PVg} = \frac{m\pi}{8\pi}.\left[\frac{1}{2}\overline{Icp}^2 + (q+1)^2\right] \quad (7)$$

- Average current in diodes Ds1 and Ds2: the average current in diode Ds1 has the same value as IVgmed.

$$\overline{IDs2_{AVG}} = \frac{m\pi}{8\pi q}\left((1+q)^2 + \frac{1}{2}.\overline{Icp}^2\right) \quad (8)$$

- Peak current through the semiconductors:

$$\overline{IS1,2,3,4_{peak}} = 1 + \overline{Icp} \quad (9)$$

$$\overline{IDg1,2_{peak}} = \overline{Icp} \quad (10)$$

$$\overline{IDs1,2,3,4_{peak}} = \overline{Icp} \quad (11)$$

or

$$\overline{IDs1,2,3,4_{peak}} = 1 \quad (12)$$

With the purpose of facilitating the calculation of the RMS current that circulates through clamping capacitor Cg, it is determined through (14) RMS current that flows through source Vg for one commutation period.

$$\overline{IVg_{RMS}} = \sqrt{\frac{mo}{4\pi}\left[\frac{4}{9}.\frac{\overline{Icp}}{q\pi} + \frac{1}{2}\left(q.\sqrt{1-q^2} + \arccos(-q) + \frac{1}{3}\left(1-q^2\right)^{3/2}\right)\right]} \quad (13)$$

The capacitor current is represented by (15).

$$\overline{ICg_{RMS}} = \sqrt{\overline{IVg_{ef}}^2 - \overline{IVg_{med}}^2} \quad (14)$$

The resonant inductor's RMS current is defined by (16).

$$\overline{ILs_{RMS}} = \sqrt{\frac{1}{2\pi}\left[\frac{2mo}{3\pi}Icp^3\left(\frac{1}{3.q}-1\right) + \frac{4}{3}Icp^2.Mi + Icp.\frac{mo}{\pi}\left(3(q+1) + \frac{(1-q)^2}{q}\right) + \right.} \quad (15)$$
$$\left. + mo\left[\frac{1}{6q}\left(1-q^2\right)^{\frac{3}{2}} + \frac{1}{4}\left(q\sqrt{1-q^2} + \arccos(-q)\right)\right]\right]$$

During the project of this snubber it should be taken into consideration the maximum value of the inverter index modulation, determining the values of the passive components, as demonstrated by (17).

$$Mi = 1 - \frac{m\pi}{2\pi}\left[\frac{1+q}{\overline{Icp}} + \frac{\overline{Icp}}{q}\right] \quad (16)$$

III. Design Example and Experimental Results

A 10 kW inverter was designed and implemented with the following specifications:

A. *Specifications*

- Input voltage: Vi = 800 V
- RMS output voltage: Vo = 220 V
- Switching frequency: fc = 20 kHz
- Output voltage frequency: f = 60 Hz
- Output power: S = 10 kVA
- Clamping voltages: Vg = 70 V
- Clamping voltages variation: ΔVg = 5 V

B. *Snubber Design*

The components of the snubber are defined as follows: inductor Ls needs to be as small as possible, and can be determined by the reverse recovery characteristics of the diode, as shown in (18).

$$Ls = \frac{E}{IRRM}.trr_{Dg} = \frac{400\times140\times10^{-9}}{16} = 3.5\,mH \qquad (17)$$

The peak current due to the resonant stage defines the value of capacitor Cs:

$$Cs = \left(\frac{Icp\times zn}{E}\right)^2 \times Ls = \left(\frac{64{,}3\times0{,}65}{400}\right)^2 \times 4\times10^{-6} = 43.7\ nF$$

Capacitor Cs → 47 nF

where zn can be obtained from the abacus shown in Fig. 6.

G → Relationship between the maximum currents through inductor Ls.

zn → Relationship between the inverter's impedance and the snubber's impedance currents through inductor Ls.

$$zn = \frac{Vi}{2.Icp}.\sqrt{\frac{Cs}{Ls}} \qquad (18)$$

r → Relationship between the reverse recovery of the diodes and the load's current peak (Icp).

The power that will be dissipated by resistor Rg is determined by (20).

$$PVg = \overline{PVg}\times\frac{E^2}{z} = \frac{0{,}0054\times400^2}{9{,}2} = 93\,W \qquad (19)$$

The minimum capacitance required for capacitor Cg is 2.2µF, shown by (21).

$$Cg = \frac{PVg}{2.f.Vg.\Delta Vg} = \frac{93}{2\times60\times70\times5} = 2.22\,10^{-3}\ F \qquad (20)$$

Due to technological limitations, the RMS current of the capacitor is an important parameter, determined by (22).

$$ICg_{RMS} = \overline{ICg_{RMS}}x\frac{E}{z} = 0.15x\frac{400}{9.2} = 6.5A \qquad (21)$$

Adopted practical values:

Inductors Ls1 and Ls2 → 4.5 µH

Capacitors Cs1 and Cs2 → 47 nF

Capacitors Cg1 and Cg2 → 2200 µF

Resistors Rg1 and Rg2 → 50 Ω

Output filter inductor: 500µH

Output filter capacitor: 22 µF

The experimental results of the implemented prototype are presented as follows. In Fig. 7, the output current and voltage of the inverter operating with a 0.88 power factor load are shown. In Fig. 8, the commutations of all the switches of the inverter are shown. These acquisitions were accomplished for 50% of the nominal output power, due to

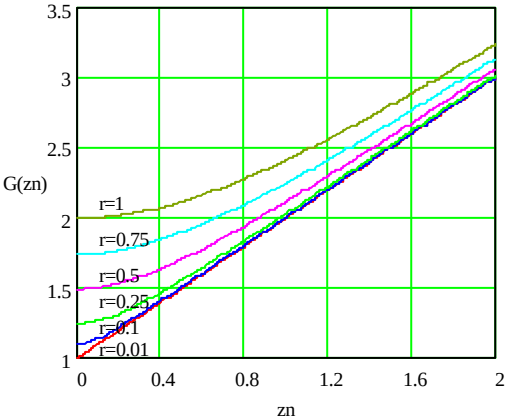

Fig. 6 – Peak current through inductor Ls.

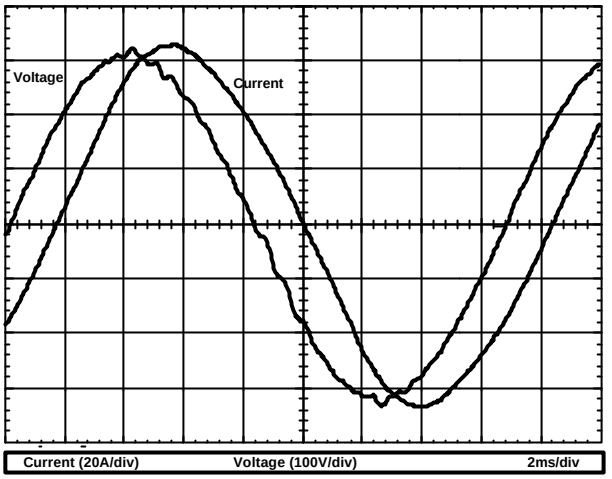

Fig. 7 – Output voltage and current.

the presence of the measurement elements, which cause an undesirable increment of parasitic inductances. It can be observed in this illustration, that the commutations of switches S2 and S3 are relative to the stage in that the load, being inductive, returns energy to the input source. The acquisitions shown in Fig. 9 are relative to the no-load operation of the inverter.

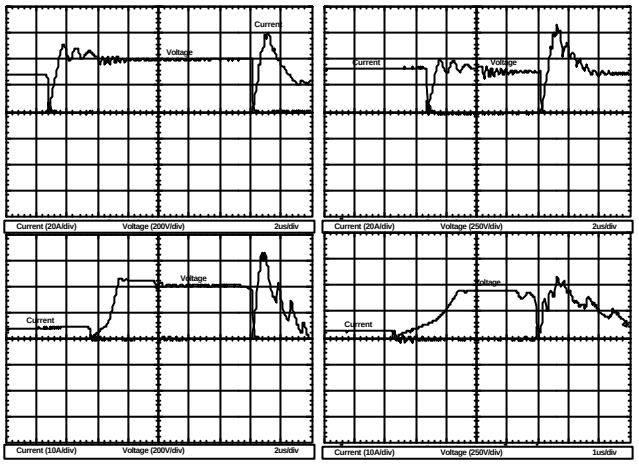

Fig. 8 – Commutations in the switches at 50 % of the output power.

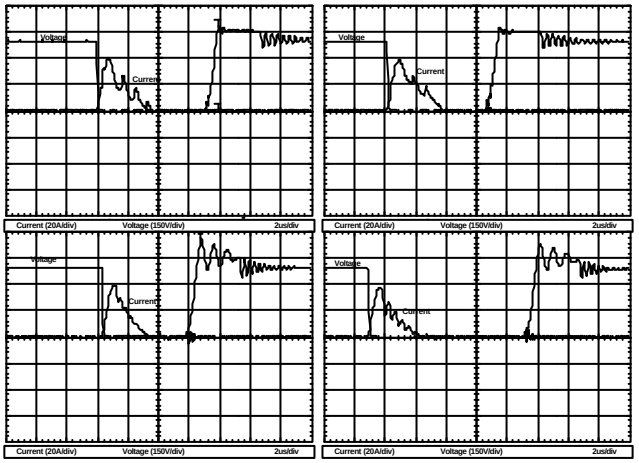

Fig. 9 – Commutations in the switches without a load.

The clamping voltages, during the no-load operation of the inverter, are shown in Fig. 10a and, during the operation with a reduced load (300 W), the clamping voltage is presented in Fig. 10b. It can be observed that the power dissipated by resistor Rg, which is directly proportional to voltage Vg, can be smaller during the operation with small loads than during the no-load operation, due to the different topological states already presented.

The energy dissipated by the clamping resistor could be regenerated easily, simply by using auxiliary low power converters. To accomplish this, the use of a Flyback converter is recommended, due to the difference between the input voltage and the clamping voltage, which can be very high, increasing the effort of the control loops. The efficiency at nominal power was 92 % without energy regeneration and including the output filter losses. Considering a possible regeneration of the energy dissipated by the resistors, of about 80%, the efficiency would be about 94% (Fig. 11). Without the use of the snubber, the efficiency of the inverter decreases to 86%.

IV. CONCLUSIONS

In this work the results obtained using a fully passive snubber for the three-level inverter were presented. Its operation was confirmed by experimentation, which propitiates soft commutations in all switches. We could observe that utilizing the snubber, the output voltage harmonic distortion is not deteriorated. The possibility of regeneration of the energy sent to the clamping capacitor is evident and it can be achieved by a cheaper investment than if this energy was simply dissipated.

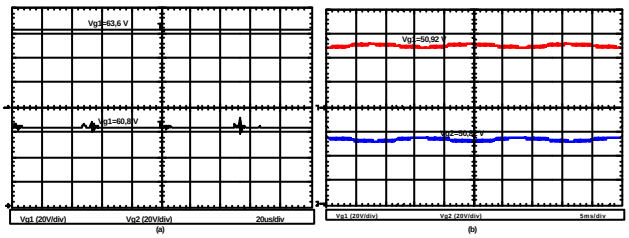

Fig. 10 – Voltage across the clamping capacitors: (a) unload operation; (b) 300 W load.

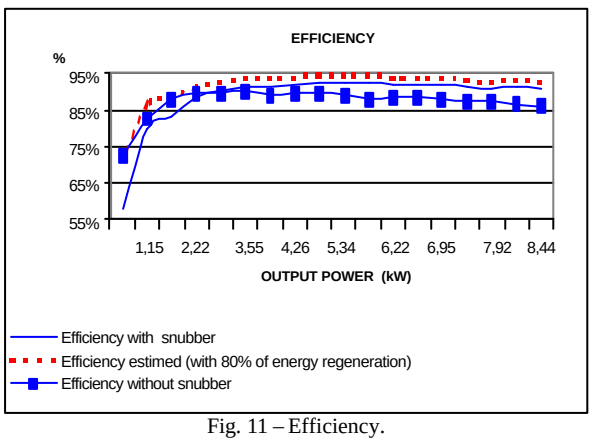

Fig. 11 – Efficiency.

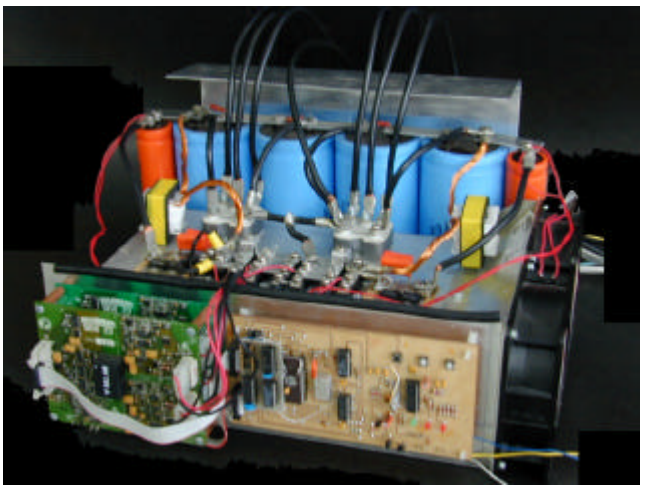

Fig. 12 - Picture of the implemented prototype.

The global efficiency structure was of 92%, being 1.8% relative to the output filter. The main advantage of this topology is that the simple implementation becomes very attractive for industrial applications, and its operation is not dependent of the technological development (reverse current of the clamping diodes).

V. REFERENCES

[1] UNDELAND, T.M.; et alli. "A Snubber Configuration for Both Power and GTO PWM Inverters". Anais do IEEE PESC, p. 42-53, 1984.

[2] PÉRES, A. "Uma Nova Família de Inversores com Comutação Suave Empregando a Técnica de Grampeamento Ativo". Tese de doutorado, INEP/UFSC, 2000.

[3] NABAE, A.; TAKAHASHI, I.; AKAGI, H. (1981). "A New Neutral-Point-Clamped PWM Inverter". *IEEE Transactions on Industry Applications*, Vol. IA-17, No. 5, September/October 1981.

[4] BACKER, R. H.; BEDFORD, M. "Bridge Converter Circuit" *United States Patent*, 4270163, 1979.

[5] MARUYAMA, T.; KUMANO, M.. "New PWM Control Method for a Three-Level Inverter", *IEEE, IPEC'91 Proceedings*, vol. 2 pp. 870-877, 1991.

[6] PERIN, A. J. "Modulação PWM". *Relatório Interno* – INEP/UFSC, 1998.

[7] DESCHAMPS, E. "Conversores CC-CC Isolados de Alta Tensão de Entrada". *Tese de Doutorado*, PPGEEL-INEP/UFSC, 1999.

[8] STEIMER, P.; GRUNING, H.; WERNINGER, J.; *et alli*. "Series Connection of GTO Thyristors for High Power Static Frequency Converters", *ABB Review*, No. 5, pp 14-20, 1996

[9] SCHAUDER, C.; GERNHARDT, M.; STACEY, E.; *et alli*. "Development of a 100 MVAR Static Condenser for Voltage Control of Transmission Systems", *IEEE Trans. On Power Delivey*, Vol. 10, No 3, pp 1486-1496, July 1995.

[10] YUAN, X. "Soft Switching Techniques for Multilevel Inverters". *Tese de Doutorado*, PPGEEL-INEP/UFSC, 1998.

[11] BLABJERG, F. "Snubbers in PWM-VSI-Inverter" Anais do IEEE PESC 1991, pp. 104-111.

[12] PINHEIRO, J. R. "Conversores CC-CC Três Níveis com Comutação Sob Tensão Nula" *Tese de Doutorado*, PPGEEL-INEP/UFSC, 1994.

[13] NASCIMENTO, C. B. "Estudo dos Inversores de Tensão Multiníveis com Modulação por Largura de Pulso". Dissertação de Mestrado, PPGEEL-INEP/UFSC, 1996.

[14] .ANDERSEN, M. A. E. "Comparison of Three IGBT-Inverters, One Hard-Switched and Two With Snubber Circuits Using a Minimum Number of Componentes". EPE - European Power Electronics Congress. pgs 306-311, 1983.

[15] BRAGA, H. C. "Conversores Estáticos Multiníveis – Uma Revisão" , *Anais do XII Congresso Brasileiro de Automática – CBA*, vol II, pp 683-688, 1998.

[16] MEYNARD, T. A.; FOCH, H. "Multilevel Conversion: High-Voltage Choppers and Voltage-Source Inverters", PESC'92 – Power Electronics Conference Records, pp. 397-403, 1992.

[17] NOVAES, Y. R.; "Estudo de um *snubber* para o Inversor de Três Níveis com Neutro Grampeado", *Dissertação de Mestrado*, PPGEEL-INEP/UFSC, 2000.