Novel Quasi-Square-Wave DC-Link Converters

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Abstract - **This paper compares two Quasi-Square-Wave DC Link (QSWDCL) converters, which improve existing topologies. For reducing switching losses in both topologies the current in the DC switch is restricted to the value of the load current. Both proposed circuits provide zero-DC-link voltage notches, during which the inverter switching is effected, and impose a minimum DC bus voltage stress to the PWM inverter. Simple design conditions are offered. Simulated and experimental results demonstrate the validity of the proposed topologies.**

I. Introduction

In Pulsed DC-Link Voltage (PDCLV) inverters an auxiliary circuit - mainly composed of switches, capacitors, and inductors - introduces zero voltage notches in the DC-link. The bridge switches are then turned on and off under a Zero-Voltage-Transition (ZVT) condition [1, 2, 3, 4, 5]. Among the PDCLV converters, the Quasi-Square-Wave with Resonant Transition (QSWRT) converter, also known as quasi-resonant converter, is an attractive topology since it transfers more power with its switches rated lower than those in the basic resonant DC-Link converter [1]. In QSWRT inverters the DC link is isolated from DC voltage source by a here named *DC switch*. Also, individual capacitors are connected across each switch in the inverter bridge. An alternative is to connect an equivalent resonant capacitor in parallel with the bridge input either to replace the individual capacitors or to simplify the circuit analysis. Such capacitor will be here named *input capacitor*. The ZVT condition for the bridge switches is only achieved if the input capacitor is completely discharged. Also, for ZVT turn on of the DC switch the input capacitor must be charged to the value of the input voltage source.

In general, the QSWRT inverters suffer from one of the following disadvantages:

· The auxiliary switches are hard-switched [5];
· Voltage stresses applied to the switches [1];
· More than one inductor in the auxiliary circuit [6];
· Need of an initial current in the resonant inductor [4, 7, 8]; if the inductor charge occurs via the DC switch, its turn off losses increase;
· Free-wheeling current in the inductors of the auxiliary circuit during the notch interval and/or the on period, causing a decrease in the circuit efficiency;
· Two resonant capacitors operate simultaneously, thus increasing the complexity of the control for the energy balance in the auxiliary circuit;

As an example, the inverter introduced in [5] is free from almost all such disadvantages but one of its auxiliary switches (other than the DC switch) is hard-switched. Instead the inverter introduced in [9] has a very good performance.

This paper first proposes a Quasi-Square-Wave DC Link (QSWDCL) inverter that is a modification of the topology presented in Wang [5], of which the hard-switched auxiliary switch is replaced by a soft-switching one (zero-voltage condition). Next, the paper proposes a second QSWDCL inverter which is an improvement of the inverter in [9]. Both circuits provide zero-DC-link voltage notches, during which the inverter switching is effected. Also, the voltage stress that they suffer is restricted to the DC bus value. Besides that the losses produced by the proposed topologies are compared to their hard-switched counterpart. Experimental prototypes of the equivalent ZVT single-phase PWM inverters were used to confirm the analytical studies.

II. Topology I

Figure 1(a) introduces the first three-phase QSWRT inverter proposed . Its simplified equivalent circuit is shown in Fig. 1(b), in which the input capacitor is in parallel with the equivalent inverter switch. The equivalent circuits for each interval of operation are shown in Fig. 2 while its main operation waveforms are presented in Fig. 3. Consider for analysis that all switches are ideal and that the load current is maintained constant and equal to I_0 in the simplified circuit. Also, consider that for $t < 0$ the switch S_a is conducting an increasing linear current. The difference between this current and the load current is flowing through the diode D_i so that the voltage across the input capacitor, C_i, is zero. With reference to Figs. 1, 2, and 3, a cycle of operation will be described in sequence.

A. Intervals of operation

Interval I $[0, t_1)$,Fig.2(a)]: This interval starts when the value of the current in S_a reaches I_0 and

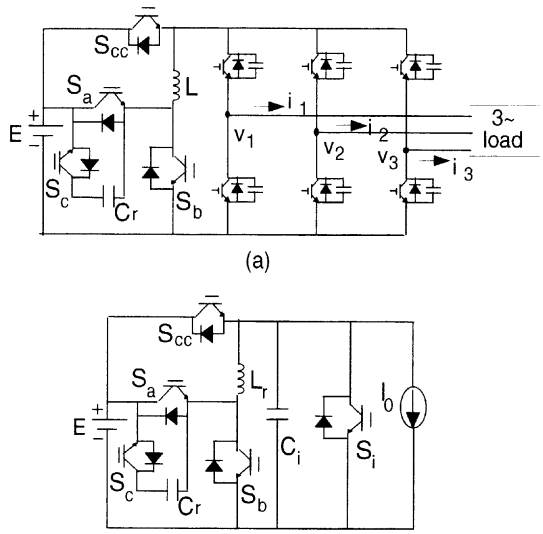

Fig. 1 Proposed quasi-square-wave inverter.

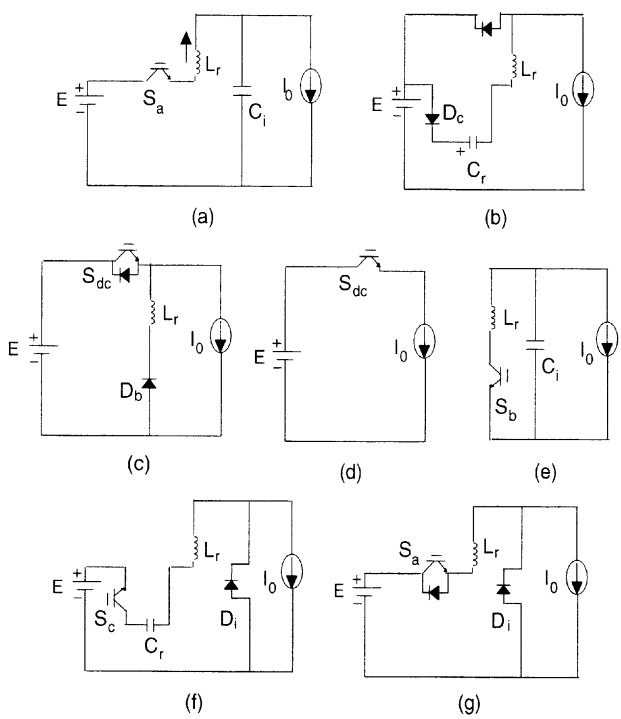

Fig. 2 Equivalent circuits for each interval of operation

the diode D_i blocks. An oscillation with a resonant frequency $\omega_i = \frac{1}{\sqrt{L_r C_i}}$ starts between L_r and C_i, which has to be charged to the source voltage E.

Interval II $[(t_1, t_2)$,Fig.2(b)]: After the input capacitor voltage reaches E, diode D_{dc} starts conducting and the auxiliary switch S_a is turned-off under ZVT. Then the inductor current starts decreasing due to the resonance between C_r and L_r. A trigger signal is applied to the switch S_{dc} gate while D_{dc} is conducting to allow its ZVT turning on. For an adequate circuit operation the voltage across C_r must increase till the source value so that D_b starts conducting. The equations for the interval, in which $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ and $t' = t - t_1$, are:

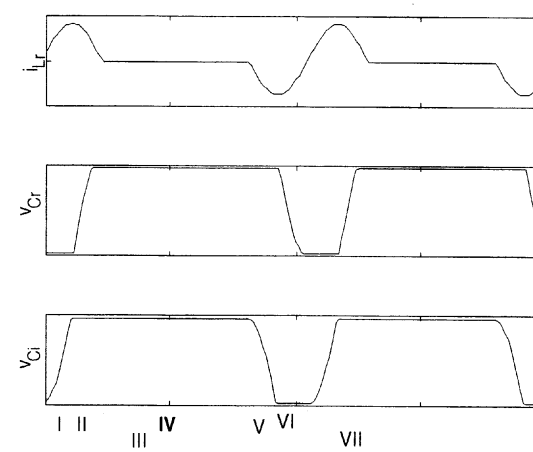

Fig. 3 Main waveforms for the simplified circuit

$$\begin{aligned} i_{Lr} &= \left(\sqrt{\frac{C_i}{L_r}}E + I_0\right)\cos(\omega_r t') \\ v_{Cr} &= \left(\sqrt{\frac{C_i}{C_r}}E + \sqrt{\frac{L_r}{C_r}}I_0\right) sin(\omega_r t') \\ v_{\mathrm{Ci}} &= E \end{aligned} \quad (1)$$

Interval III $[(t_2, t_3)$,Fig.2(c)]: With the conduction of D_b, the inductor current is forced to decrease by the voltage source. When this current is less than I_0, then the diode D_{dc} blocks and the switch S_{dc} starts conducting under ZVZCT, due to L_r.

Interval IV $[(t_3, t_4)$,Fig.2(d)]: In this interval the load current flows through S_{dc}, of which the turning off can be synchronized to an external PWM signal. During this interval, $i_{Lr} = 0$, $v_{Cr} = E$, and $v_{\mathrm{Ci}} = E$.

Interval V $[(t_4, t_5)$,Fig.2(e)]: When desired S_{dc} is turned off under ZVT. At same time S_b is turned on under ZVZCT. A new resonance starts between C_i and L_r discharging the capacitor to zero. The interval ends when D_i starts conducting. In this interval, $t'' = t - t_4$

$$\begin{aligned} i_{Lr} &= -\sqrt{\frac{C_i}{L_r}}E\,sin(\omega_i t'') - I_0\cos(\omega_i t'') + I_0 \\ v_{Cr} &= E \\ v_{\mathrm{Ci}} &= E\cos(\omega_i t'') - \sqrt{\frac{L_r}{C_i}}I_0\,sin(\omega_i t'') \end{aligned} \quad (2)$$

So, the load current helps C_i to discharge, except for $I_0 = 0$.

Interval VI $[(t_5, t_6)$,Fig.2(f)]: The interval starts with turn on of S_b and turn off of S_c, both under

ZVT. The energy stored in L_r is then transferred to C_r. The interval ends when the voltage across C_r becomes null and the diode D_a turns on, clamping the input capacitor and S_a voltages to zero. Here, $t''' = t - t_5$

$$\begin{aligned} i_{Lr} &= i_{Lr}(t_5)\cos(\omega_r t''') \\ v_{Cr} &= E + \sqrt{\frac{L_r}{C_r}} i_{Lr}(t_5)\, sin\,(\omega_r t''') \\ v_{Ci} &= 0 \end{aligned} \quad (3)$$

Interval VII $[(t_6, t_7)$,Fig.2(g)]: The conduction of D_a forces the linear decrease of the negative current in L_r. During the conduction of D_a, gate signals are applied to S_a with the purpose of having a ZVZCT condition at the instant the inductor current reverses its direction. When that current reaches I_0, the diode D_i blocks and a new cycle of operation starts.

During intervals VI and VII, the conduction of D_i produces a zero voltage notch at the inverter input, which allows its switches to commutate under ZVT. A delay in the S_a gate signal results in a variable notch width.

B. Design Consideration

The condition for the capacitor C_i voltage reaching E at the end of interval I is $\sqrt{C_i/C_r}E + \sqrt{L_r/C_r}I_0 > E$, obtained from equation (1). It can be seen that the interval operation can become independent of the load if $C_i > C_r$. On the other hand, at the end of interval V, the capacitor voltage must become null and for that, from equation 5, $|i_{Lr}(t_5)| > E\sqrt{C_r/L_r}$.

C. Analysis During the Negative Load Current

This case, in which $I_0 < 0$, corresponds to the regeneration mode of a motor. The equivalent circuits for analysis are shown in Fig. 4. Only one interval will be explained since the others are almost similar to the previous ones.

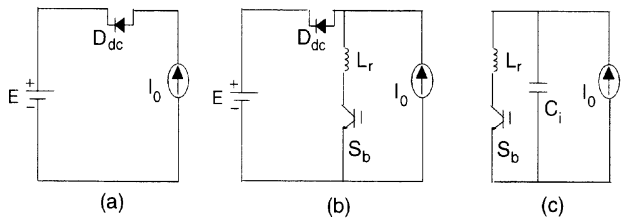

Fig. 4 Equivalent circuits for the negative load current

Charge Interval [Fig.4(b)]: Since $i_{dc} = I_0$ is negative, i_{dc} flows at initial instant through the anti-parallel diode D_{dc}. Then, the current through D_{dc} decreases and i_{Lr} increases steadily from zero to I_0 with the slope E/L_r. When the i_{Lr} reaches I_0, a resonance occurs.

III. Topology II

The second three-phase QSWRT inverter proposed is an improvement of the topology introduced in [9] and its simplified equivalent circuit is presented in Fig.5. The equivalent circuits for each interval of operation are shown in Fig. 6 while its main operation waveforms are presented in Fig. 7. Consider that for $t < 0$ diode D_a is conducting an increasing linear current due to the voltage $E/2$ applied across L_r. The difference between such current and the load current is flowing through the diode D_i so that the voltage across the input capacitor, C_i, is zero.

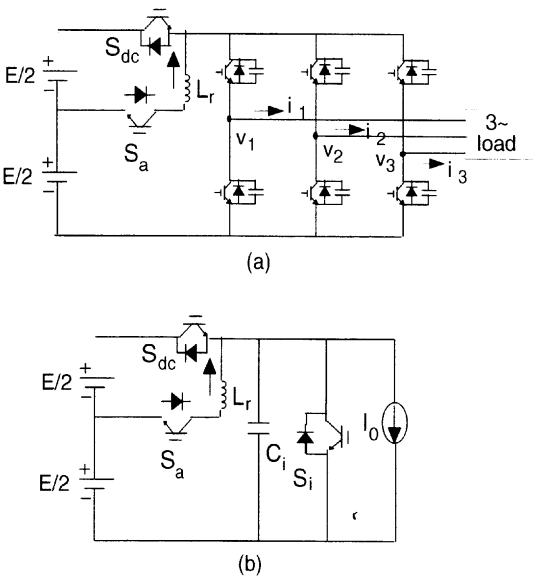

Fig. 5 Proposed quasi-square-wave inverter.

A. Intervals of operation

Interval I $[(0, t_1)$,Fig.6(a)]: This interval starts when the value of the current in D_a reaches I_0 and the diode D_i is turned off softly. An oscillation between L_r and $C_i$with a resonant frequency $\omega_i = \frac{1}{\sqrt{L_r C_i}}$ starts naturally, without the need to setup the initial current of i_{Lr}. This is an important feature of the proposed inverter. The equations for the interval are:

$$\begin{aligned} i_{Lr} &= I_o + \frac{E}{2}\sqrt{\frac{C_i}{L_r}}\sin(\omega_i t) \\ v_{Cr} &= \frac{E}{2}[1 - \cos(\omega_i t)] \end{aligned} \quad (4)$$

During this resonance interval, the voltage over C_i increases to E, reaching this value after a half of

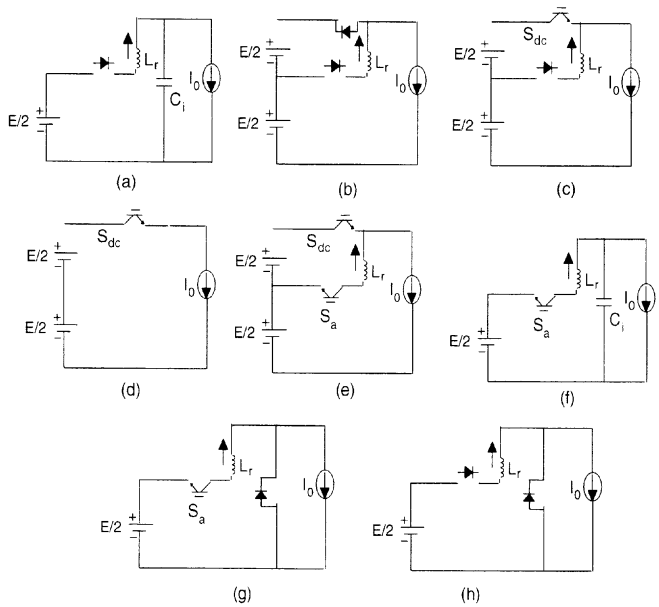

Fig. 6 Equivalent circuits for each interval of operation

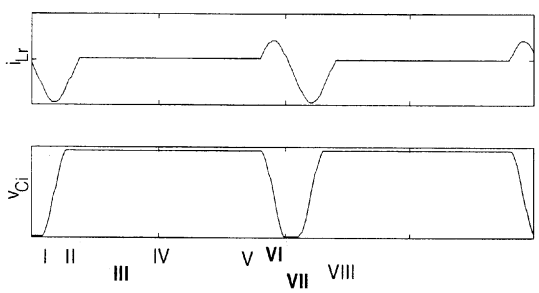

Fig. 7 Main waveforms for the simplified circuit

the resonant period, that is, $\pi\sqrt{L_r C_i}$. At this time switch S_{dc} is turned on under zero voltage condition. Note that $i_{Lr\max} = \frac{E}{2}\sqrt{\frac{C_i}{L_r}}$.

Interval II $[(t_1, t_2)$,Fig.6(b)]: After the input capacitor voltage reaches E, diode D_{dc} starts conducting and the remnant current in L_r decays quickly during the time $\Delta T_d = 2L_r I_o/E$ due to the voltage $-E/2$ applied over it. A trigger signal is applied to the gate while D_{dc} is conducting to allow its later turning on.

Interval III $[(t_2, t_3)$,Fig.6(c)]: When the current i_{Lr} reaches I_0 again, diode D_{dc} blocks and switch S_{dc} starts conducting under simultaneous zero current and zero voltage condition. The current in L_r continue to decay linearly and the interval ends when it reaches zero.

Interval IV $[(t_3, t_4)$,Fig.6(d)]: During this interval the load current flows through S_{dc}, of which the turning off can be synchronized to an external PWM signal.

Interval V $[(t_4, t_5)$,Fig.6(e)]: Before the instant S_{dc} is desired to turn off , S_a is turned on forcing an increase of the current in L_r in the negative direction due to the voltage $E/2$ applied over it. The interval ends when the current in L_r reaches a predefined value, $-I_b$. This current will become the initial current of the resonant inductor that guarantees the change of the DC bus from E to zero using the resonant discharge of the input capacitor C_i in the case of low values of the load current.

Interval VI $[(t_5, t_6)$,Fig.6(f)]: A new resonance starts between C_i and L_r discharging the capacitor to zero. With the initial conditions $i_{Lr}(0) = -I_b$, $v_{Cr}(0) = E$, and $i_{Cr}(0) = -I_o$,

$$i_{Lr} = I_o + \sqrt{\frac{E^2 C_i}{4L_r} + (I_b + I_o)^2}\, sin(\omega_i t' + \phi) \quad (5)$$

$$v_{Ci} = \frac{E}{2} + \sqrt{\frac{E^2 C_i}{4} + \frac{(I_b + I_o)^2 L_r}{C_r}}\, \cos(\omega_i t' + \phi)$$

where $\mathrm{tg}\phi = \frac{2(I_b+I_o)}{E}\sqrt{L_r/C_r}$ and $t' = t - t_5$. Note that v_{Cr} cannot be negative due to diode D_i. The interval ends when D_i starts conducting.

Interval VII $[(t_7, t_8)$,Fig.6(g)]: The conduction of D_a forces the linear decrease of the negative current in L_r.

Interval VIII$[(t_8, t_9)$,Fig.6(h)]: After the current in L_r reaches zero, it starts increasing in the positive direction due to the voltage $E/2$.The difference between such current and the load current flows through diode D_i and a new cycle of operation starts.

During intervals VII and VIII, the conduction of D_i produces a zero voltage notch at the inverter input, during which its switches can be commutated under ZVT.

B. Design Consideration

Equation 5 indicates that the condition $I_b + I_o > 0$ to complete discharge C_i. Then an initial current of the resonant inductor is not necessary (Interval V) when the load current is large enough to guarantee the change of the DC bus from E to zero. Instead it is needed for low values of load current. Also the maximum current rating is dependent on $\frac{E}{2}\sqrt{\frac{C_r}{L_r}}$ and I_o. As a guideline, L_r and L_r can be selected such that $i_{Lr\max} = \frac{E}{2}\sqrt{\frac{C_i}{L_r}} \leq 2I_o$ and $\Delta T_d = 2L_r I_o/E < 0.5\sqrt{L_r C_r}$. This means

$$\frac{4I_o}{\pi E} \leq \sqrt{\frac{C_i}{L_r}} \leq \frac{2I_o}{E} \quad (6)$$

IV. Losses Comparison

In QSWRT inverters, specific constraint is imposed to the PWM patterns to be used [3]. In the modulating process used here, the auxiliary circuit is used just once during each modulation interval.

Each modulation interval starts with a notch in the DC bus. Inside the modulation interval, commutation occurs naturally. Note that this case is only possible when the resonant capacitors are placed across each switch of the bridge and the relation between voltage and current sectors is taken into account as well.

Taking into account the different aspects mentioned and considering the IGBT type IRGPC50F of the International Rectifier, the power conduction losses and switching losses have been modeled for a comparative study on losses. As in [10] the conduction loss for an IGBT or a diode have been calculated by the well known approximation [11]

$$P_{con,x} = \frac{1}{T}\int_0^T \left(U_{o,x} + r_{o,x}\, i(t)^{B_{con,x}}\right) i(t)\, dt \quad (7)$$

Switching losses for turn on and turn off of IGBTs as well for diodes have been calculated by [10]

$$E_{sw,x} = A_{sw,x}\, i(t)^{B_{sw,x}} \quad (8)$$

In these equations:
$U_{o,x}$ = bias voltage for device x
$r_{o,x}$ = dynamic resistance for device x
A_x, B_x = curve fitting constants for device x
A voltage source of $500V$ and frequencies and currents in the range of $10 - 50kHz$ and $10 - 70A$, respectively have been considered.

Results in Fig. 8 compare the total losses of the proposed topologies as referred to their hard-switched counterpart. The losses have been calculated for constant zero-voltage interval operation although it can be made adjustable for Topology I . The results in the Fig. 8 show that the fact of introducing soft-switching is not sufficient to compensate the losses introduced by DC and auxiliary switches. Instead, Topology II shows to be competitive with the hard-switched inverter version. This happens above 20 kHz. It should be noticed that in the topology the IGBT used loss calculation has considered to be the same for both the main and auxiliary switches of the circuit. Also, losses in Topology I can be reduced if a MOSFET of lower rating replaces the auxiliary IGBT.

V. Experimental Results

To confirm the theoretical analysis for both topologies, an experimental prototype of their equivalent ZVT single-phase PWM inverter using the IGBT FUJI 2MBI25-120 (Fig. 1) were implemented and tested for $E = 100V$ e $I_0 = 10A$. The auxiliary circuit parameters used for Topology I are $C_r = 230nF$, $C_i = 360nF$ and $L_r = 47\mu H$ and for Topology II are $C_i = 230nF$ and $L_r = 47\mu H$. In both topologies, voltage detectors for each capacitor command the circuit switches via a microcomputer.

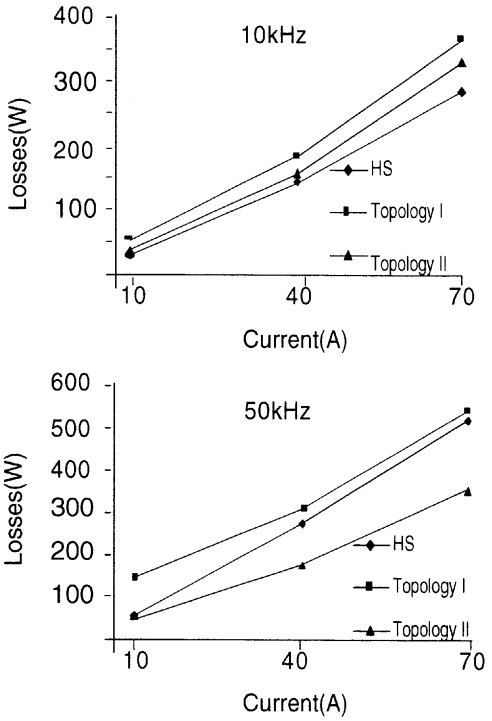

Fig. 8 Power efficiency of three-phase inverter

The results in figures 9 and 10 have been obtained for $I_0 = 0$, which is an bad condition for the input capacitor discharging. This condition is also and is useful to show that in Topology I there is no excess of current in S_{dc} during its turning off, since this value is zero at the interval. The voltages across capacitors C_i e C_r and the inductor current are shown for Topology I to confirm that the two resonant capacitors never operate at same time, guaranteeing the simplicity of the circuit design. Finally, it can be seen that voltages across the capacitors and switches can be limited to value of the source voltage with an adequate choice of semiconductors and circuit layout.

VI. Conclusion

This paper has examined two new quasi-square-wave with soft transition inverters. In both topologies (a) all switches are soft-switched, (b) no current flows in the inductor neither during the notch nor during the link voltage pulse, (c) the capacitor charge with the source voltage value is guaranteed without loss increase, and (d) the current value in the DC switch is limited to that of the load. Also the voltage stress that the switches suffer is restricted to the source value. In Topology I there is no need of storing any energy in the resonant inductor for helping the discharge of C_i, even for zero load current condition, and the design conditions are simple. However, this topology has a large the number of switches (three besides S_{dc}). When com-

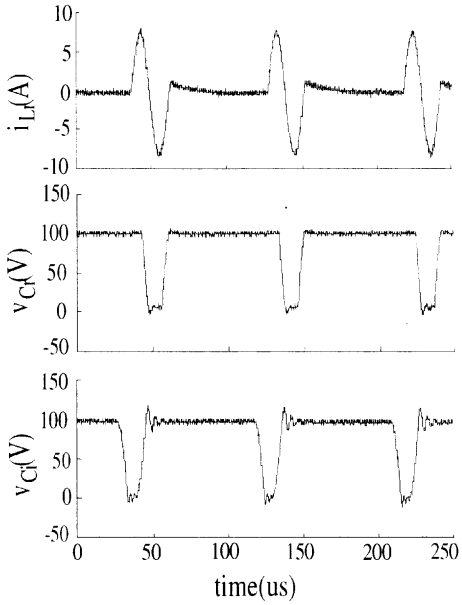

Fig. 9 Experimental results for the proposed circuit

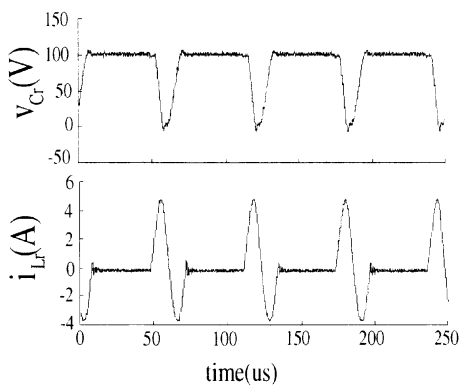

Fig. 10 Experimental results for the proposed circuit

pared to its hard-switched counterpart, the study of losses produced indicates that the simple introduction of soft switches is not sufficient to justify the use of quasi-square-wave with soft transition converters. However, these losses can be reduced with use of MOSFETs as auxiliary switches with smaller ratings than those used in the examined conditions. On the other hand, Topology II is competitive with the hard-switched version and offers simple design conditions.

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