SINGLE STAGE SELF-OSCILLATING HPF ELECTRONIC BALLAST

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Abstract - This paper presents a single stage self-oscillating high power factor (HPF) electronic ballast more suitable for both low power levels (because it operates in discontinuous conduction mode) and low AC mains applications (since it employs an input doubler rectifier). The electronic ballast is based on a high frequency dither signal, which shapes the input current in a sinusoidal waveform. In order to reduce the electronic ballast components the self-oscillation technique has been employed. An electronic ballast prototype operating at 25kHz has been implemented to drive two 40W straight-type fluorescent lamps from a 127V utility line. High power factor is achieved even though the electronic ballast drives just one fluorescent lamp. The experimental results demonstrated the electronic ballast operation.

I. INTRODUCTION

A HPF electronic ballast can be implemented by using two power processing stages. The input one, called pre-regulator stage, is used to obtain HPF maintaining the DC bus voltage constant. The output stage, which is an inverter, produces a high frequency voltage to drive the fluorescent lamps.

However, two power processing stages demand more components, that increase the overall cost and reduces the electronic ballast reliability [1,2, 3]

A simple electronic ballast can be obtained combining both stages, forming a single power processing stage [1, 2, 3, 4, 5, 6]. Therefore, the resulting ballast must be able to ensure at the same time a low-distortion current through the lamps (in order to increase their lifetime) and into the AC mains. Furthermore, the single stage topologies yield high switching current stress compared with two stage topologies. This drawback reduces its application at low power levels.

Several single stage topologies employing a great number of components have been proposed on the technical literature [1, 2, 4, 6, 7, 8, 9]. A simple HPF electronic ballast has been proposed in [5, 10], which is based on a high frequency dither signal.

This paper presents a self-oscillating single stage electronic ballast based on a dither signal suitable for both low power levels (because it operates in discontinuous conduction mode) and low AC utility voltage (due to an input doubler rectifier).

Usually, a self-oscillating electronic ballast presents fixed duty cycle of 0.5. However, by using bipolar transistors as power switches, the duty cycle becomes variable, modulated by the input voltage. At high values of the input voltage, the duty cycle reduces, reaching values around 0.25. This characteristic allows the electronic ballast to operate in discontinuous conduction mode with low DC bus voltage. Even though one fluorescent lamp is removed or failed, the increasing of the DC bus voltage is maintained in accepted levels.

II. PRINCIPLE OF OPERATION OF THE PRE-REGULATOR STAGE

The conventional rectifier diodes conduct during a short time interval $|\Delta t|$. This fact takes place due to the DC bus voltage V_b becomes greater than the AC input voltage almost all the time, as shown in Fig. 1(a).

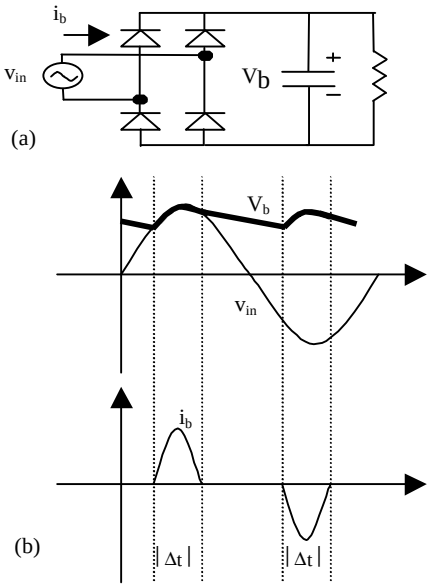

Fig. 1. (a) Conventional Rectifier and (b) waveforms.

HPF can be obtained when the rectifier diodes conduct in larger $|\Delta t|$ interval. It can be accomplished by adding a high frequency voltage source v_d in series with an inductor L_b, as shown in Fig. 2(a). When v_d is added to the input voltage V_{in}, the resulting voltage is larger than the DC bus voltage V_b. In this case, there is current circulation through the circuit, which is limited by the inductance L_b. At the moment v_d changes its polarity, the resulting voltage becomes lower than V_{in}. During this time interval the inductor current reduces until it reaches zero, maintaining in this value up to a new cycle starts. Consequently, the operation in the discontinuous current conduction is assured. The HPF rectifier waveforms can be seen in Fig. 2(b), where i_{b1} represents the i_b fundamental component.

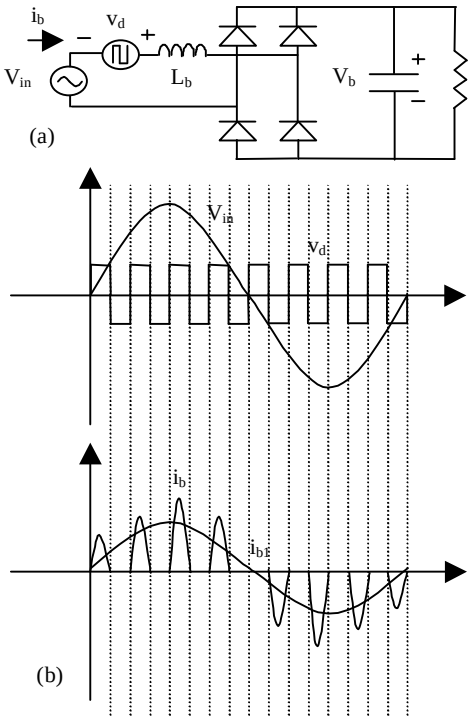

Fig. 2. (a) HPF rectifier and (b) waveforms.

A simple way to produce a high frequency voltage v_d from a single stage converter is to employ the own inverter stage, interconnecting it with the mains line and with the inductor L_b, as proposed by [5,10] and shown in Fig. 3.

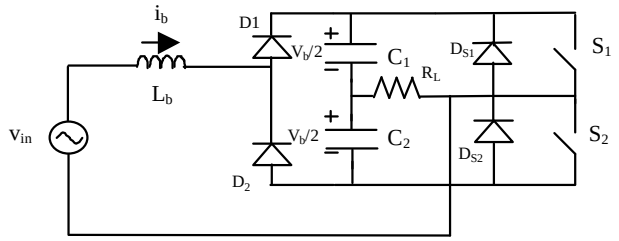

Fig. 3. HPF single stage converter.

By considering the positive half cycle of the AC mains, the pre-regulator operation, in a switching period T_S, can be described by two stages, as follows:

1st stage: This stage begins when switch S_1 is turned on, which maintain the current i_b flowing through V_{in}, L_b, D_1 and S_1. During this stage the line voltage is maintained across the inductor L_b, increasing i_b linearly according to the following equation:

$$i_b = \frac{V_{in}}{L_b} t \tag{1}$$

This stage ends at instant t_1 when S_1 is turned off. The maximum value of the current i_b in each period is given by:

$$i_{b\max} = \frac{V_{in}}{L_b} \Delta t_1 \tag{2}$$

2nd Stage: This stage starts when S_1 is turned off. After this moment, D_{s2} starts to conduct. Thus, S_2 is turned on under zero voltage switching. The current i_b keeps flowing through V_{in}, L_b, D_1, C_1, C_2 and by the intrinsic diode D_{s2}. The pre-regulator stage function as a boost converter, thus, the voltage V_b must be greater than V_{in}. However, the voltage across L_b maintains i_b decreasing linearly according to the following equation:

$$i_b = \frac{V_{in} - V_b}{L_b}(t - t_1) + i_{b\max} \tag{3}$$

This stage ends at instant t_2 when i_b becomes zero and the diode D_1 is turned off. The current i_b is maintained equals to zero until the instant when S_1 is turned on again. The Fig. 4 shows the waveforms of two stages of operation.

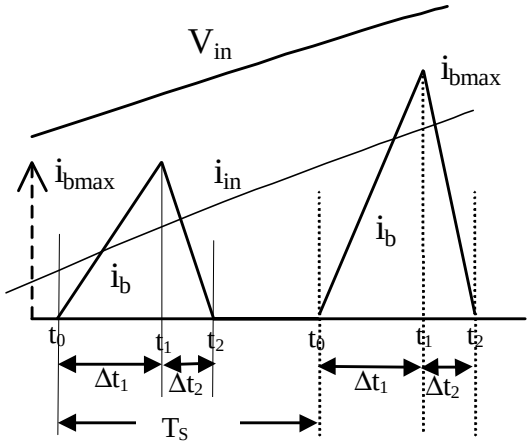

Fig. 4. Waveforms of the stages of operation.

By assuming the discontinuous conduction mode operation, with:

$$V_{in} = V_{pk} \operatorname{sen} \omega t \tag{3}$$

The Δt_2 can be obtained as:

$$\Delta t_2 = \frac{\alpha \operatorname{sen} \omega t}{1 - \alpha \operatorname{sen} \omega t} \Delta t_1 \tag{4}$$

Where:

$$\alpha = \frac{V_{pk}}{V_b} \tag{5}$$

The maximum value of Δt_2 occurs when the conduction becomes critical, which results:

$$\Delta t_{2\max} = (1 - D) T_s \tag{6}$$

Where D is the duty cycle, defined by:

$$D = \frac{\Delta t_1}{T_s} \tag{7}$$

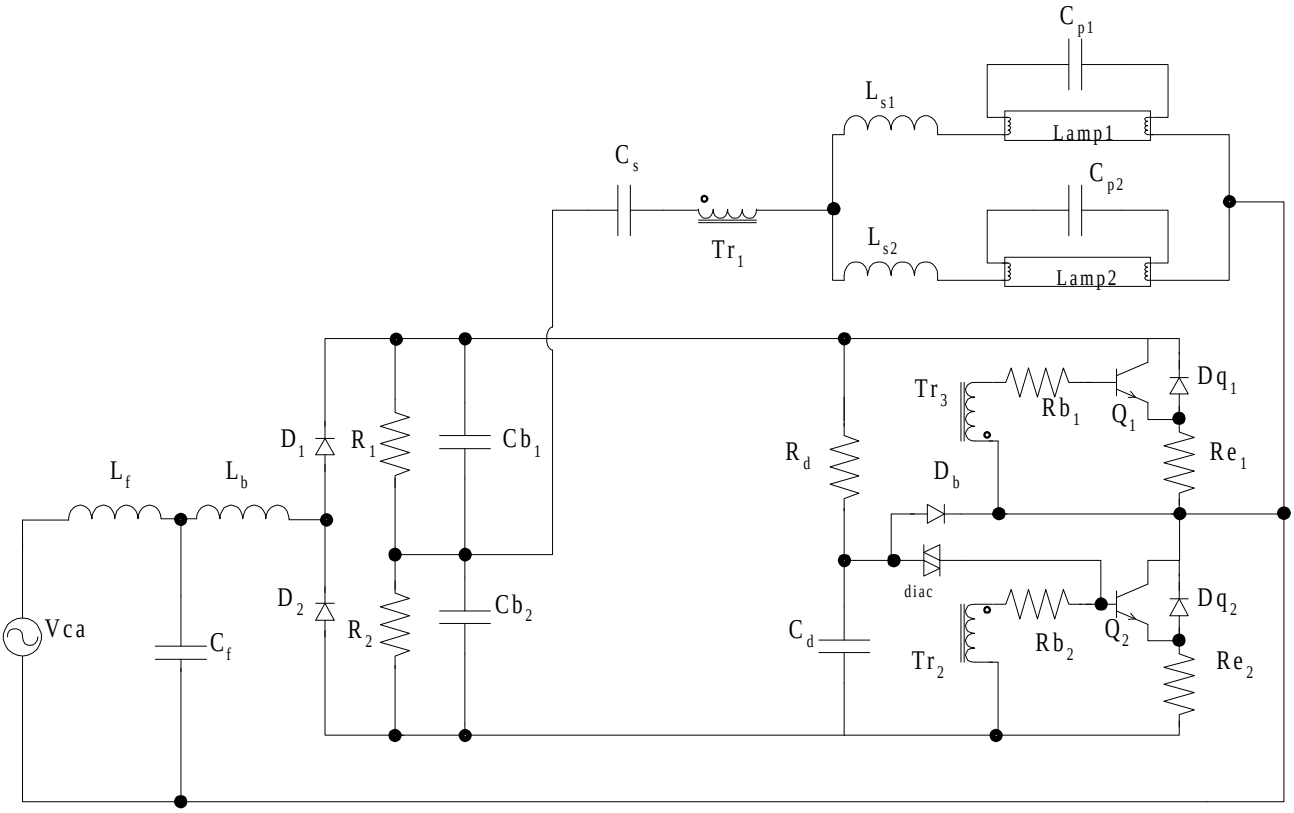

Fig. 5. The proposed electronic ballast diagram.

The maximum value of i_b occurs in the input peak voltage, when Δt_2 reaches its maximum value. By considering critical conduction operation at this moment, and assuming $\text{sen}\,\omega t = 1$ in (4), when comparing with (2.6), results:

$$\alpha_{\max} = 1 - D \tag{8}$$

Where $\alpha_{\max}$ is the maximum admissible value of α which assures the discontinuous conduction mode of the current in the pre-regulator stage.

III. ELECTRONIC BALLAST TOPOLOGY

The electronic ballast diagram is shown in Fig. 5. As can be seen, this ballast compared with other single stage topologies uses few components, as described: two rectifier diodes (D_1, D_2), two electrolytic DC link capacitors (C_{b1}, C_{b2}), two bipolar transistors (Q_1, Q_2), one boost inductor (L_b), parallel resonant circuits formed by: two inductors (L_{s1}, L_{s2}) and two capacitors (C_{p1}, C_{p2}), a blocking capacitor (C_s), a high frequency input filter: inductor (L_f) and capacitor (C_f). Further components are used in the startup circuit (R_d, C_d, diac, and D_b) and in the self-oscillating circuit (pulse transformer T_{r1}:T_{r2}:T_{r3}, and resistors R_{b1}, R_{b2}, R_{e1}, R_{e2}).

The boost inductance value is defined in order to maintain the pre-regulator stage operation in discontinuous conduction mode, which naturally provides HPF to the utility line.

The resonant circuit formed by L_s e C_p functions as a parallel resonant converter, operating above the resonant frequency due to the self-oscillating gate-drive technique, which ensures Zero Voltage Switching (ZVS). The self-oscillating design and operation are demonstrated in [2].

IV. DUTY CYCLE

The operation of this self-oscillating electronic ballast occurs with variable duty cycle, modulated by the input voltage. The duty cycle is maintained in 0.5 solely when the input voltage presents values close to zero. However, its value reduces reaching 0.25 at the peak of input voltage value. This characteristic takes place due to different currents through the bipolar transistors during a switching cycle, as shown in Fig. 6.

For the positive cycle of the input voltage, the bipolar transistor Q_1 conducts current values (boost inductor plus resonant circuit) larger than Q_2 (resonant circuit), mainly due to discontinuous current in the boost inductor. Transistor Q_1 requires larger base current values to maintain its conduction. However, the base current presents oscillating characteristics and when its value becomes lower than a threshold level, Q_1 turns off, as

shown in Fig. 6. Consequently, transistor Q_1 will conduct during small time interval, reducing the electronic ballast duty cycle. This effect is more meaningful for larger values of the boost inductor current.

As can be seen in Fig. 6, in order to drive a transistor with the current $I_c^{`}$ a minimum base current equals $I_b^{`}$ is required, which results in the conduction time interval $\Delta t^{`}$. A greater minimum base current value $I_b^{``}$ is necessary to maintain the transistor conduction with $I_c^{``}$, which reduces the conduction time interval to $\Delta t^{``}$.

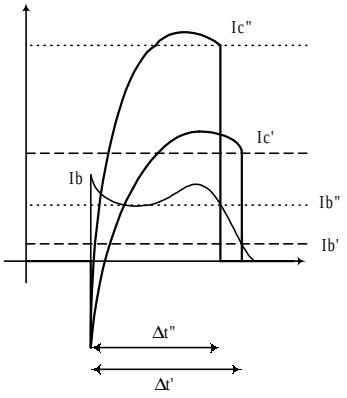

Fig. 6. Transistor currents.

Thus, the electronic ballast duty cycle reduces while the input voltage increases. This interesting feature allows low electronic ballast DC link voltage operation in discontinuous conduction mode. Even though one lamp is removed or failed, the DC link voltage is maintained in acceptable levels. Besides that, the DC link voltage does not achieve excessive levels in case of AC line overvoltage.

V. BOOST INDUCTANCE

Due to the high frequency input filter, the AC line current is given by the instantaneous mean value of the boost inductor current, according to the following:

$$i_{in} = \frac{(\Delta t_1 + \Delta t_2)}{2T_s} i_{b\max} \tag{9}$$

Substituting (2) and (6) into (9) results:

$$i_{in} = \frac{V_{pk}}{2 f_s L_b}\left(\frac{\Delta t_1}{T_s}\right)^2 \frac{\operatorname{sen}\omega t}{1-\alpha \operatorname{sen}\omega t} \tag{10}$$

Based on experimental results and in the previously mentioned analysis, it has been verified that the duty cycle variation can be approximated as a quadratic function of the input sinusoidal waveform, given by:

$$d(\omega t) = \frac{\Delta t_1}{T_s} = 0.5 - k \cdot \operatorname{sen}^2(\omega t) \tag{11}$$

Where k is the maximum duty cycle variation, which occurs at the input peak voltage. At this moment, the duty cycle reaches its minimum value, given by:

$$D_{\min} = 0.5 - k \tag{12}$$

The input power can be obtained by the following equation:

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} V_{in}.i_{in}\, d(\omega t) \tag{13}$$

By considering that the output power is given by $P_o = \eta P_{in}$, where η is the estimate electronic ballast efficiency, and substituting (10) and (11) into (13) results in:

$$\frac{L_b}{K_b} = \frac{1}{\pi}\int_0^{\pi} \frac{(0.5 - k\operatorname{sen}^2\omega t)^2 \operatorname{sen}^2\omega t}{1-\alpha \operatorname{sen}\omega t} \cdot d(\omega t) \tag{14}$$

Where:

$$K_b = \frac{\eta V_{pk}^2}{2 f_s P_o} \tag{15}$$

The normalized boost inductance, as a function of α and with D_{min} as a parameter, can be obtained from Fig. 7.

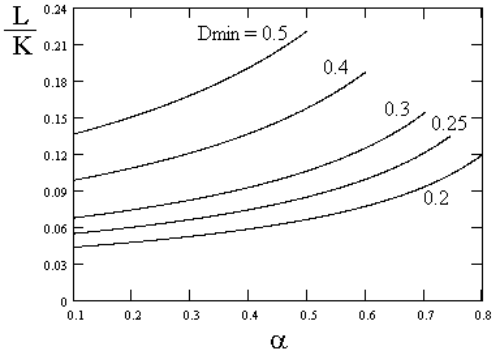

Fig. 7. Normalized boost inductance.

V. EXPERIMENTAL RESULTS

An electronic ballast prototype was built to meet the following specifications:

- rms AC mains voltage: V_{in} = 127V $\pm$ 10%, 60Hz;
- output power: P_o = 68W (15% lower than the basic power);
- switching frequency: f_s = 25kHz;
- steady state fluorescent lamps voltage: V_{op} = 110V;
- fluorescent lamps rated current: I_{op} = 0.3A;
- estimate efficiency: η = 90%.

Based on the experimental results it has been verified that $D_{min} = 0.25$. Thus, from (5) and (8) one can obtain that the DC bus voltage is equal to 240V, which assures the discontinuous conduction mode. The normalized boost inductance equal to 0.137 can be obtained from Fig. 7, with $D_{min} = 0.25$ and $\alpha = 0.75$. By using $V_{pk} = 180V$, $f_s = 25$ kHz, $P_o = 68$ W and $\eta = 0,9$ into (15), K_b is obtained, from which results $L_b = 1.16$mH.

The electronic ballast parameters and components are the following:

- L_f = 3.5mH, 260 turns of 28AWG wire on core C15, IP6 – Thornton.
- L_b = 1.25mH, 200 turns of 25AWG wire on core C20, IP6 - Thornton;
- $L_{s1} = L_{s2}$ = 2.3mH, 200 turns of 28AWG wire on core C15, IP6 - Thornton;
- C_f = 330nF/250V, $C_{p1} = C_{p2}$ = 15nF/400V, C_s = 0.33μF/400V (polypropylene);
- C_{b1}, C_{b2} = 68μF/250 V (electrolytic);
- Pulse transformer: T_{r1}-T_{r2}-T_{r3}: 3/7/7 turns on toroidal core NT7/5, IP6 - Thornton;
- Rectifier diodes: D_1, D_2: MUR140 (Motorola);
- BJT transistors: Q_1, Q_2: BUL38D (International Rectifier);
- Startup circuit: R_d = 470kΩ, C_d = 22nF/250V, diac - DB3, D_b -1N 4004;
- Gate-drive circuit: R_1,R_2= 470kΩ, R_{b1},R_{b2} = 15Ω, R_{e1},R_{e2} = 1.2Ω.

The AC input voltage and current, which show the HPF of this electronic ballast can be seen in Fig. 8.

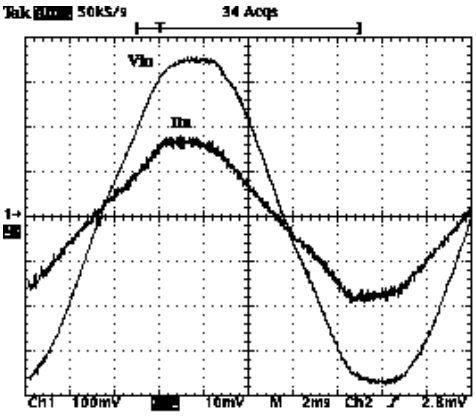

Fig. 8. Input voltage (50V/div) and input current (0.5A/div); time scale: 2ms/div.

The boost inductor current and the utility line voltage are shown in Fig. 9.

The bipolar transistor Q_1 and Q_2 commutations can be seen in Fig. 10 and Fig. 11, respectively, which show the turn-on at ZVS.

The high frequency fluorescent lamp current and voltage are shown in Fig. 12.

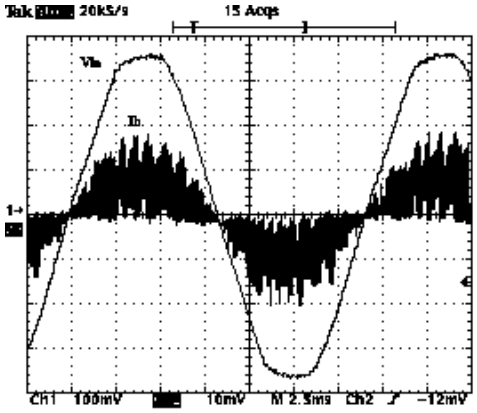

Fig. 9. Mains line voltage (50V/div) and boost inductor current (1A/div); time scale: 2.5ms/div.

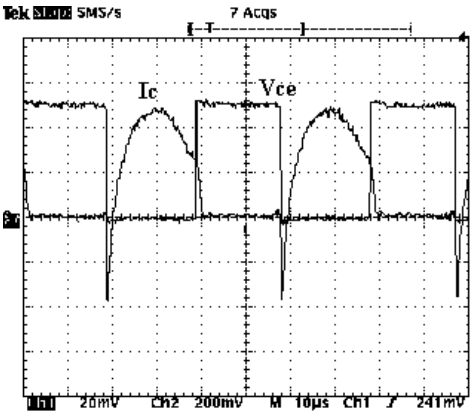

Fig. 10. Transistor Q_1 voltage V_{CE} (100V/div) and current (1A/div); time scale: 10μs/div

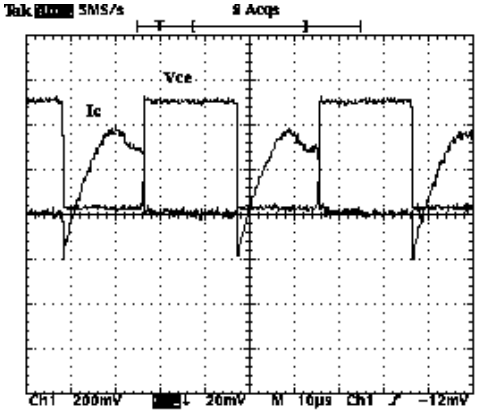

Fig. 11. Transistor Q_2 voltage V_{CE} (100V/div) and current (1A/div); time scale: 10μs/div

The DC link voltage and the utility line voltage are shown in Fig. 13, when the ballast is driving two fluorescent lamps. Fig. 14 shows these waveforms when the ballast is driving just one fluorescent lamp. In this case the DC link voltage reaches 380V.

Fig. 15 shows the Q_1 voltage for the peak value of the input voltage. At this point, the duty cycle decreases to 0.25.

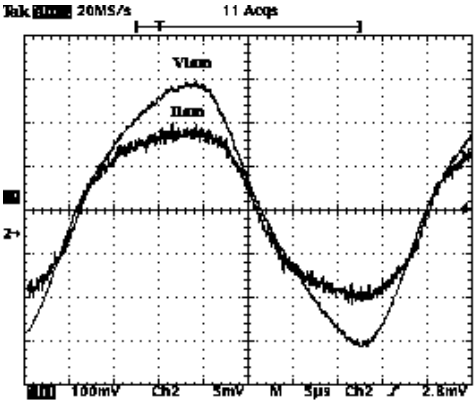

Fig. 12 High frequency fluorescent lamp voltage V_{lamp} (50V/div) and current I_{lamp} (250mA/div); time scale: 5µs/div

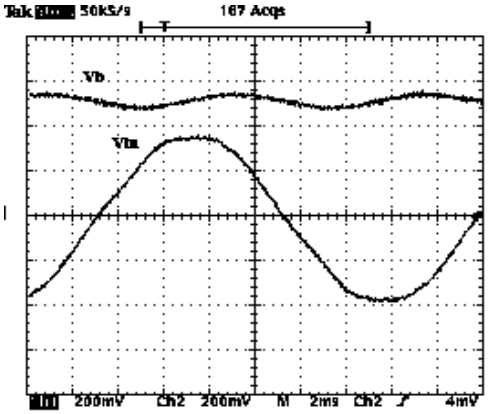

Fig. 13. DC lik voltage (100V/div) and input voltage (100V/div) for two fluorescent lamps, time scale: 2ms/div.

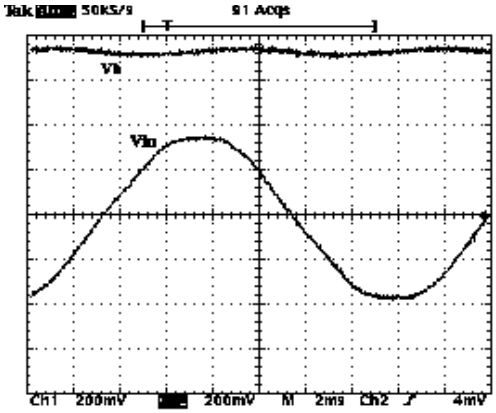

Fig. 14. DC lik voltage (100V/div) and input voltage (100V/div) for one fluorescent lamp; time scale: 2ms/div.

The experimentally obtained characteristics were: η = 85%, PF = 0.99, crest factor, F_c = 1,53 and THD = 8% (two lamps) and 12% (one lamp).

VI. CONCLUSIONS

This paper has presented a single stage electronic ballast based on a high frequency dither signal in order to obtain HPF. The ballast is more appropriate for low power

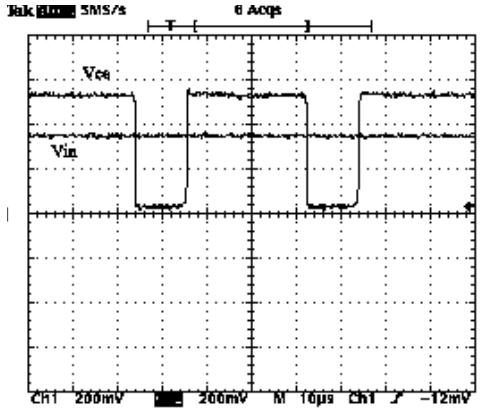

Fig. 15. Q_1 voltage v_{CE} (100V/div) and the input voltage (100V/div); time scale: 10µs/div.

levels and low AC rms levels because it employs an input doubler rectifier and operates in discontinuous conduction mode. By using bipolar transistor, the self-oscillating electronic ballast operates with variable duty cycle, modulated by the input voltage. Increasing the input voltage results in a reduction of electronic ballast duty cycle, which allows low electronic ballast DC link voltage operation in discontinuous conduction mode. Even though one lamp was removed the DC link voltage is maintained in acceptable levels. A laboratory prototype operating at 25kHz has been built in order to drive two 40W fluorescent lamps from 127 rms line voltage. The experimental results have demonstrates the HPF of this electronic ballast, with low THD and low crest factor.

VII. REFERENCES

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