# Improved Crest Factor Valley Fill Filters Applied to Low Power and Low Cost Electronic Ballasts


Rodrigo Nascimento Marques and Henrique A. C. Braga

Núcleo de Automação e Eletrônica de Potência- NAEP
Universidade Federal de Juiz de Fora- UFJF
Caixa Postal 422 - 36.001-970 - Juiz de Fora – MG - Brazil
hbraga@engelet.ufjf.br - rmarques@eletrica.ufjf.br



*Abstract* - **This paper presents a discussion about power factor correction techniques based on passive networks, known as valley fill filters, applied to low power electronic ballasts for fluorescent lamps. Since the conventional valley fill topologies have as side effect a very high crest factor (CF) of the lamp current, it is of significant interest to propose suitable modifications to minimize or solve this problem. The paper describes in depth a recently introduced simple CF correction (CFC) valley fill filter, reorganizing its main equations and design procedure. Auxiliary curves are plotted and experimental waveforms are presented for a commercial low power electronic ballast (inverter/lamp stage) being fed by the proposed CFC filter. Another simpler structure (employing just three components) is introduced here. In this circuit a diode of the original topology has been suppressed, but practically the same good performance has been observed, as proved by digital simulation. The simulated circuit has been built of a double arrangement of the proposed CFC filter, in order to provide a structure capable to operate under 127V or 220V utility. Both structures proposed here have shown a CF between 1.6 and 1.7 while featuring a PF between 0.8 and 0.9.**


## I. Introduction

Tubular and compact fluorescent lamps are attracting the industry and consumer attention in an increasing rate due to either the natural limitation of energy resources or due to economic issues, since these lamps have a higher luminous efficacy as compared to incandescent ones. These low pressure discharge devices need special circuits, designed to provide a proper high ignition voltage and to limit the lamp current, called ballasts. Electronic ballasts have conquered the consumer preference in the recent years, since they are lightweight, flicker free, compact and specially, because they are becoming cheaper. As for a magnetic conventional ballast, an electronic ballast is mainly evaluated according to its power factor (PF), line current total harmonic distortion (THD) and current crest factor (CF) imposed to the lamp. Depending on the manufacturer design, an electronic ballast may perform either as a high power factor, low THD device (e.g. 0.98 and 20% or better, respectively) or a low power factor, high THD device (e.g. 0.50 and 170%, respectively). In any case, the lamp crest factor may vary from 1.5 to 2.3, although lamp makers and standards require a CF lower than 1.7, to preserve the lamp lifetime. National and international regulation standards determine the harmonic limits for the ballast input current, but those limits must be observed only for products that drive a minimum power from the utility. For the European Community the limits are set by the EN 61000-3-2. In this standard, Class C devices (lighting equipment) must observe the limits if their input power is above 25W [1]. On the other hand, the Brazilian ABNT standard, NBR 14418 – Annex E, which is going to be effective in 2002, determines harmonic restrictions for lighting devices above 60W [2].

As can be seen, no regulation is set for the low power mass market fluorescent electronic ballasts. However, these devices can be widely spread over domestic and commercial sites, resulting in electromagnetic pollution problems and low power factor consumers (on a higher net power, by a cascade effect). Federal agencies and programs, however, are recursively stimulating efficient, high power quality and economic devices, which should naturally present a high power factor [3], [4].

There are two basic categories of power factor improvement circuits namely active and passive. A typical active PFC circuit supplies a regulated DC bus at a higher voltage than the maximum peak voltage of the AC supply and uses a simple boost topology [5]. The high PF boost solution operates at a high frequency in a continuous or critical conduction current mode. Otherwise, passive solutions operate at line frequency (50 or 60 Hz) employing capacitor and inductor filters.

Active solutions employ a more complex strategy and circuitry and are normally avoided for low power electronic ballasts, which are expected to be sold for a low price.

A very interesting passive alternative is named valley fill filter, which can feature a high power factor and a low THD (> 0.91 and < 47%, respectively) [6]. The basic valley fill filter topology is depicted in Fig. 1 and its typical waveforms are shown in Fig. 2. In Fig. 1, *Ro*, represents the equivalent impedance of the inverter stage of the ballast along with the fluorescent lamp and ac filter elements.

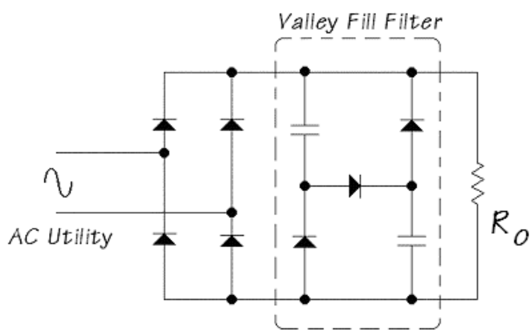



Fig. 1. Basic valley fill filter arrangement.

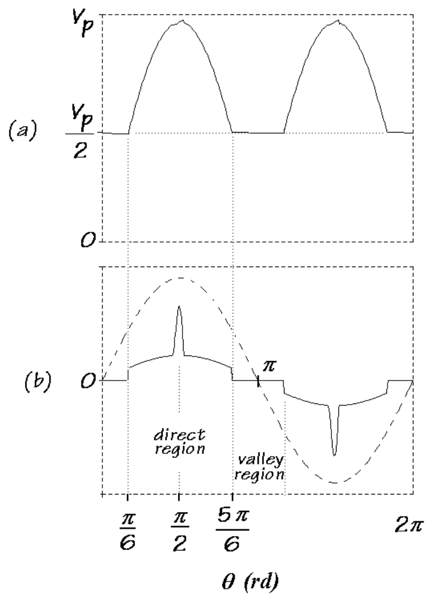



Fig. 2. Typical valley fill filter waveforms.
(a) DC bus voltage; (b) line voltage (dashed) and current.

The conventional valley fill topology of Fig. 1 should be modified to draw a less pronounced spike in the line current (as depicted in Fig. 2b). This can be accomplished by means of a resistor placed in series with the diode that connects the two capacitor/diode legs (see Fig. 1). By this way, the structure PF can reach 0.98 with a THD of 21%. Unfortunately the dc bus voltage ripple increases slightly, deteriorating the crest factor.

Valley fill filters are used in some low power electronic ballasts nowadays [6], because of their low cost, reduced number of components and their good performance from the utility viewpoint. However, as crest factor is as higher as 2.3, the use of these filters may reduce the lamp lifetime, and should be avoided by serious designers unless the lamp technology can be improved to deal with such a high crest factor mark.

Many papers have recently proposed modified valley fill topologies, that keep the good behavior of line current while improving the CF of the lamp current [5], [8] and [9]. Although these new alternatives do accomplish what they promise the cost of the additional circuitry is often unacceptable in many low cost mass market ballast applications.

In this paper a very simple valley fill filter is revised and a derived even simpler topology is introduced. The structures can present a crest factor lower than 1.7 and a power factor close to 0.9, which is significantly higher than the one obtained with a single capacitor filter, which is used in many low cost electronic ballasts nowadays. The circuits are so intended to provide a reliable and high efficiency front-end dc bus filter, that could be used by manufacturers without the need of changing the inverter stage design of a well established electronic ballast.

## II. An Improved Crest Factor Valley Fill Filter

Fig. 3 shows a crest factor correction - CFC - valley fill filter, which has been presented first in [6]. A more detailed characterization of this circuit will be made in this paper, since it is the base for the next section.

Typical waveforms for the structure of Fig. 3 are shown in Fig. 4. The better crest factor feature is attained by means of a greater "valley" dc bus voltage. In fact, different from the 50% valley dc bus voltage of Fig. 2a, the correspondent voltage in Fig. 4a presents a lower ripple and, consequently, a lower crest factor of the lamp current can be expected.

Comparing to Fig. 1, it can be noticed that the filter of Fig. 3 employs less two components (disregarding the filter resistor, which is important to reduce the line current peak): a diode and a capacitor.

The ideal waveforms of Fig. 4 have been sketched considering a fixed capacitor voltage, $V_f$, with no discharge effect. As can be proved by simulation and experimental data, this approximation leads to a negligible overall error. Another result of this simplified approach is that all the waveforms are symmetrical for a sine wave half cycle. Therefore, angle $\theta_2$ can be expressed as $\pi - \theta_1$. It can also be noticed from Fig. 4c that the charging stage of capacitor $C_V$, which lasts from $\theta_1$ to $\theta_2$, follows a sinusoidal curve, with a peak value, $I_{CP}$, of $(V_p-V_f)/R_V$.

By observing Fig.4a one can easy obtain:

$$\theta_1 = \arcsen(a)\,. \tag{1}$$

Where the normalized capacitor voltage, a, is defined as:

$$a \equiv \frac{V_f}{V_p}\,. \tag{2}$$

Another useful parameter is the average dc bus voltage, $V_o$, which can be derived by means of:

$$V_o = \frac{1}{\pi}\left(\int_0^{2\theta_1} V_f\, d\theta + \int_{\theta_1}^{\pi-\theta_1} Vp\,\mathrm{sen}(\theta)\,d\theta\right). \tag{3}$$

The solution of (4) can be better stated referring to the normalized dc bus voltage ($V_o/V_p$), $b$:

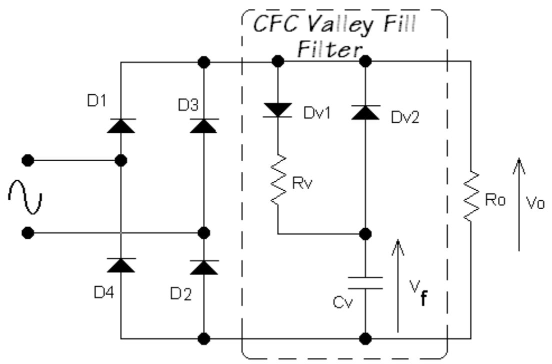



Fig. 3 . CFC valley-fill filter.

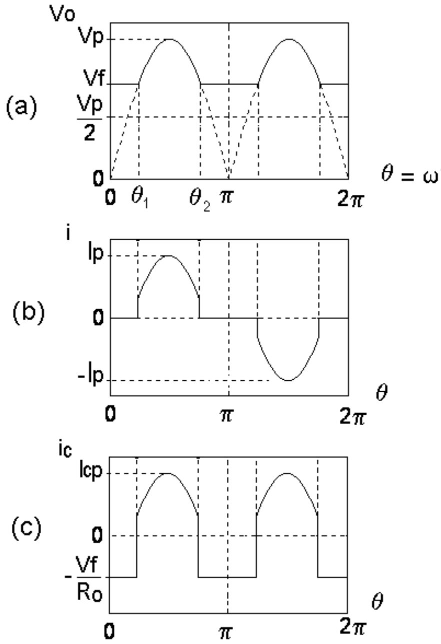



Fig. 4. Typical theoretical waveforms for the CFC valley fill filter. (a) dc bus voltage; (b) line current; (c) capacitor ,$C_V$, current.

$$b = \frac{2[a\theta_1 + \cos(\theta_1)]}{\pi}. \tag{4}$$

Another important equation can be obtained considering that the capacitor current (Fig. 4b) has a null average value. In the form of equation:

$$I_C = \frac{1}{\pi}\cdot\left(\begin{array}{l}\int_0^{2\theta_1}\left(-\frac{V_f}{R_o}\right)d\theta + \\ + \int_{\theta_1}^{\pi-\theta_1}\left(\frac{V_p\cdot \operatorname{sen}(\theta) - V_f}{R_V}\right)d\theta\end{array}\right) = 0. \tag{5}$$

By solving and manipulating equation (1) it is possible to obtain the normalized filter resistance *($R_V/R_o$)*, $\rho$:

$$\rho = 1 + \frac{\cos(\theta_1)}{a\,\theta_1} - \frac{\pi}{2\theta_1}. \tag{6}$$

Fig. 5 shows a graphical representation of equation (5), where one can see an almost linear relationship between the normalized voltage parameters.

On the other hand, equation (7) is graphically represented in Fig. 6. It is not difficult to conclude that a higher valley voltage, $V_f$, is associated to a lower filter resistance value, $R_v$. It must be pointed that, for simplicity, the impedance representing the inverter and lamp, $R_o$, has be considered a constant parameter.

A proper calculation, based on the waveform of Fig. 4b, can lead to the *PF* and *THD* behaviors for the structure under consideration. These important figures, as functions of the normalized capacitor voltage, are plotted both in Fig.7. In addition, it is possible to roughly predict the crest factor of the lamp current by assuming this parameter has an envelope uniquely determined by the waveform of the dc bus voltage (Fig. 4a). Doing so, one can obtain the curve of Fig. 8.

## III. A Modified CFC Valley Fill Filter

If in the circuit of Fig. 3 diode $D_{v1}$ is suppressed, the structure becomes as shown in Fig. 9. The presence of $D_{v1}$ was originally justified to avoid additional power losses in $R_{v1}$ during the capacitor discharge stage (valley region). However, since conduction of $D_5$ is almost ideal (short circuit) that loss can be disregarded. By this way, the modified topology presents a reduced number of components becoming cheaper and more compact. This is even more evident when considering the 127V/220V double structure, shown in Fig. 10. By using this topology the final product could be either connected to a 127V or a 220V utility, what is a very useful property in some countries and is called a "bivolt" feature.

It is not difficult to understand that the same equations and theoretical approach made in the last section are valid for the structure of Fig. 9. This statement will be proven in the next items through the procedures of theoretical design, computational simulation and experimental results

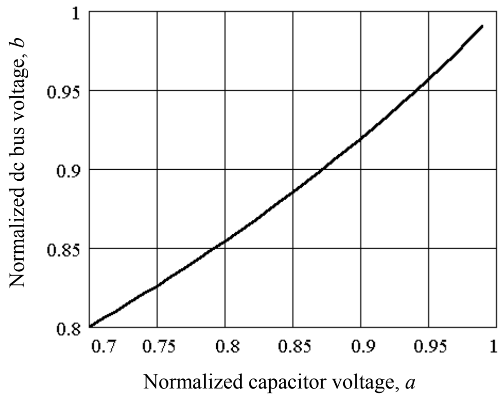



Fig. 5. Relationship between normalized voltages.

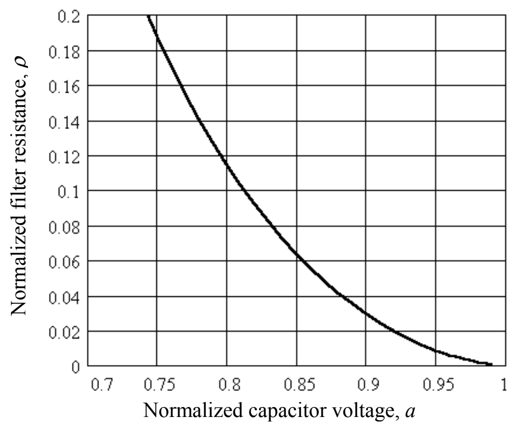
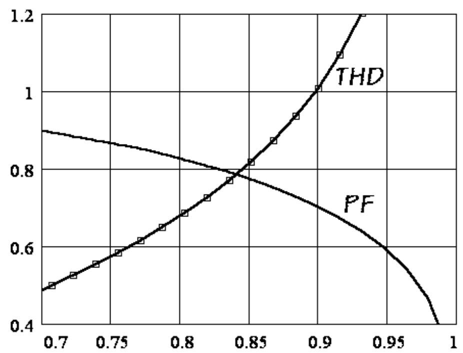
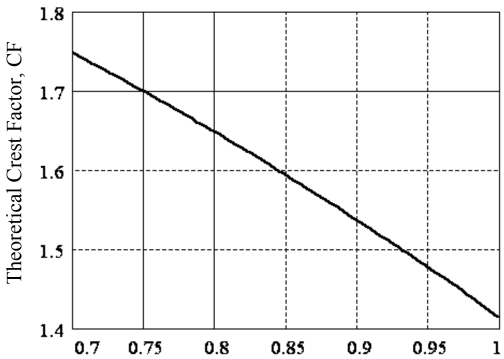



Fig. 6. Normalized filter resistance as a function of the normalized capacitor voltage




Normalized capacitor voltage, *a*

Fig. 7. PF and THD behavior as functions of the normalized capacitor voltage.




Normalized capacitor voltage, *a*

Fig. 8. Crest Factor as a function of the normalized capacitor voltage.

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*A. Prototype Design*

To design a CFC filter prototype it will be chosen an output power of 32W a PF greater than 0.8 and a CF lower than 1.7.

Using information from Fig. 5, 6, 7 and 8 one can find the design parameters of Table 1.

With the Table 2 parameters one can calculate other quantities to design the filter, which are shown in equations (7) to (9).

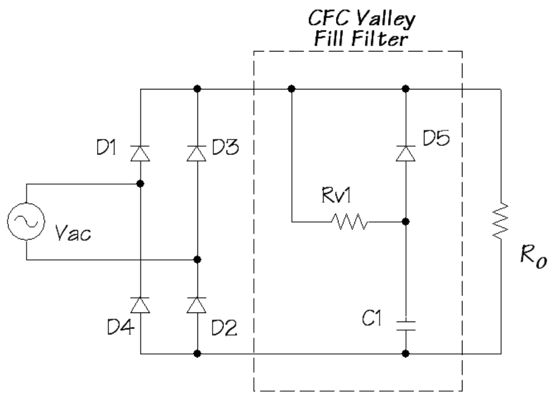


Fig. 9. Modified CFC valley fill filter.

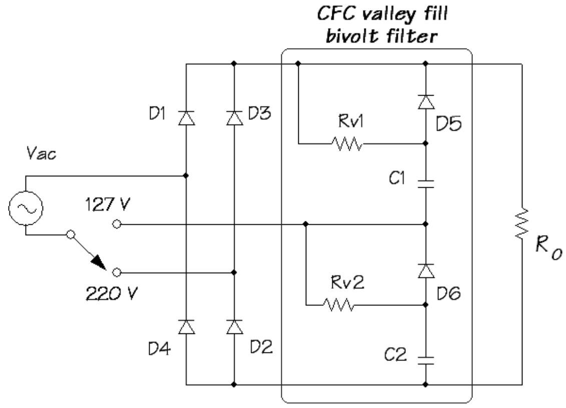


Fig. 10. “Bivolt” CFC valley fill filter.

$$V_o = b \cdot V_p = 0.9 \cdot 311 = 279.9\Omega\,. \qquad (7)$$

$$R_o = \frac{V_o^2}{P_o} = \frac{279.9^2}{32} = 2448.25\Omega\,. \qquad (8)$$

$$R_v = \rho \cdot R_o = 0.038 \cdot 2448.25 = 93.09\Omega\,. \qquad (9)$$

*B. Computer Simulation Results*

Fig. 11 and Fig. 12 show the Pspice simulated waveforms for the structure of Fig. 12, which are useful to check the filter behavior under the two voltage possibilities (selected manually by the bipolar switch shown in Fig. 12). In this simulation $R_{v1}$ = $R_{v2}$ = 90Ω, $R_o$ = 2350Ω and $C_1 = C_2 = 47\mu F$.

It can be observed that the average dc bus voltage is essentially the same for the two cases (127V and 220V utilities), although a slightly different line current harmonic behavior has been obtained. In fact, a better harmonic performance occurred for the circuit supplied by a 127V utility, as can be verified from Table 2. However, in this case, the power loss in the two filter resistors is more than two times the one computed for the 220V case.

TABLE 1 . DESIGN PARAMETERS.

| | |
|---|---|
| $\rho$ | 0.038 |
| $b$ | 0.9 |
| $a$ | 0.87 |

TABLE 2 . SIMULATED PARAMETERS FOR THE “BIVOLT” CFC FILTER. OUTPUT POWER ≈ 32W

| | | |
|---|---|---|
| Line Voltage [V rms] | 127 | 220 |
| THD [%] | 54.8 | 73.9 |
| PF | 0.87 | 0.80 |
| Filter resistor loss [W] | 6.6 | 2.7 |

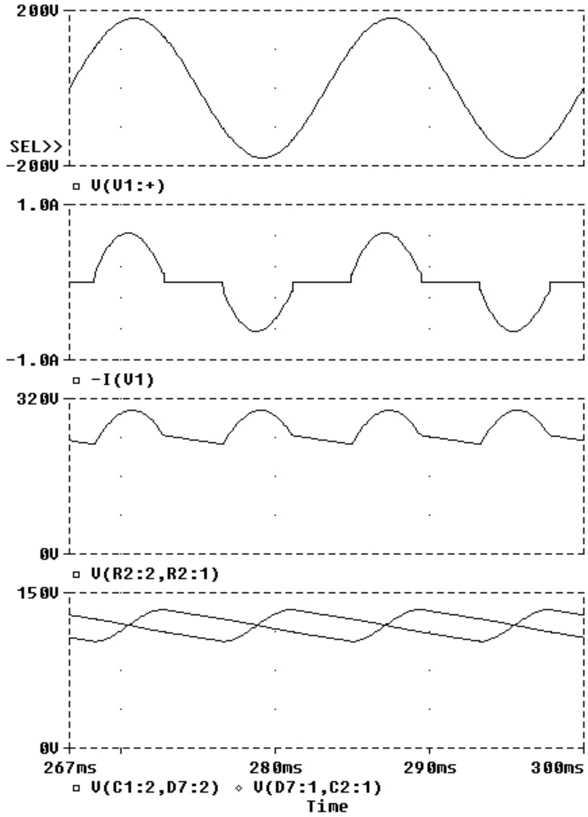


Fig. 11 . Bivolt CFC filter waveforms (127V).
From top to bottom: line voltage; input current;
dc bus voltage and capacitor voltages.

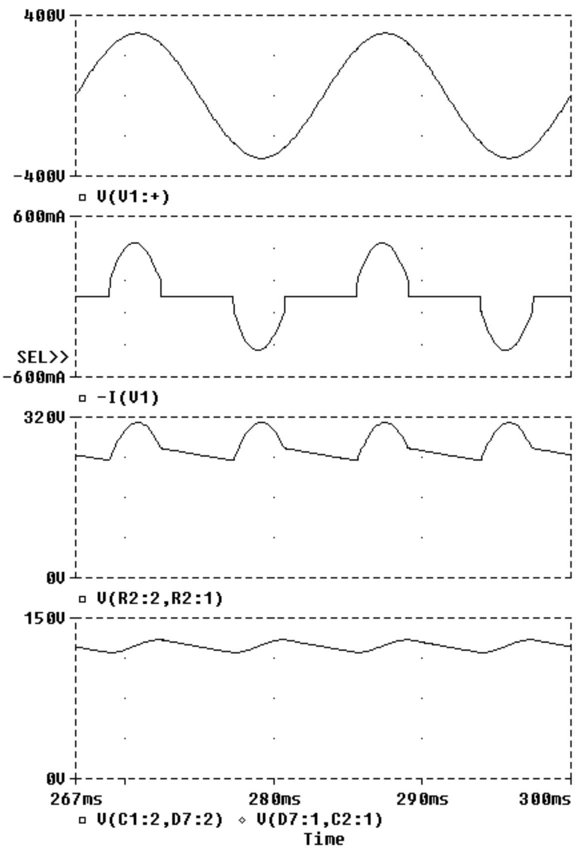


Fig. 12 . – Bivolt CFC filter waveforms (220V).
From top to bottom: line voltage; input current;
dc bus voltage and capacitor voltages (coincidents)

*C. Experimental Results*

The filter was also implemented in laboratory in order to verify the theoretical and simulation approaches. The filter stage has been connected to a commercial electronic ballast inverter stage, used to power up a single 40W fluorescent lamp. The original ballast, filtered by a single capacitor, presented a power factor below 0.5, a THD above 180% and a CF around 1.5.

Fig. 13 shows the line voltage and input current waveforms when the circuit is fed by a 127V utility. Fig. 14 shows the DC bus voltage and the current through the lamp using the same line voltage.

Similar waveforms have been shown in Fig. 15 and Fig. 16, by feeding the circuit with a 220V utility voltage.

The current lamp crest factor for both cases became very close to 1.65, being below the recommended maximum value of 1.7.

Table 3 summarizes the main parameters for the bivolt CFC circuit. It can be observed a good agreement with Table 2 simulated parameters.

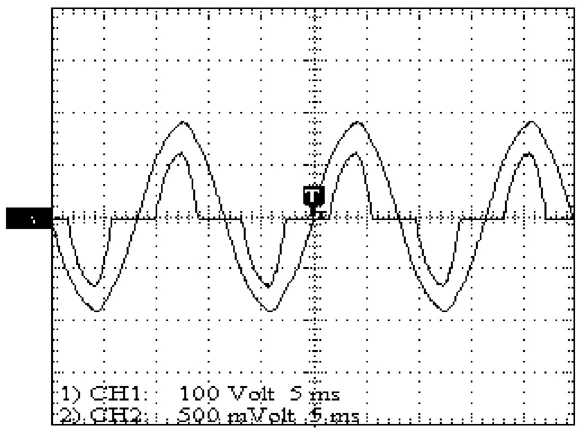


Fig. 93. Line voltage and input current (100V/div and 0.5A/div).
Line voltage: 127V.

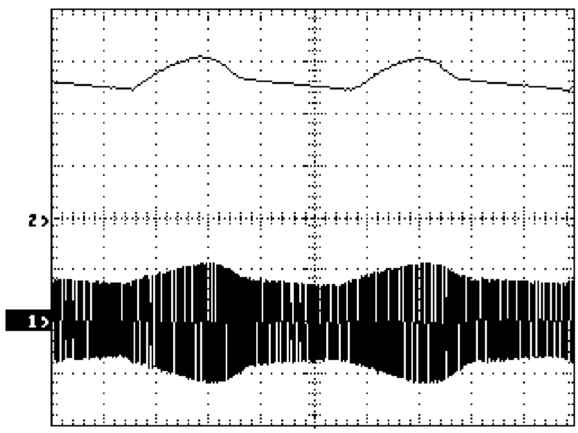


Fig. 14 . Upper trace: DC bus voltage (100V/div);
Lower trace: Lamp current (300mA/div).
(Line voltage: 127V)

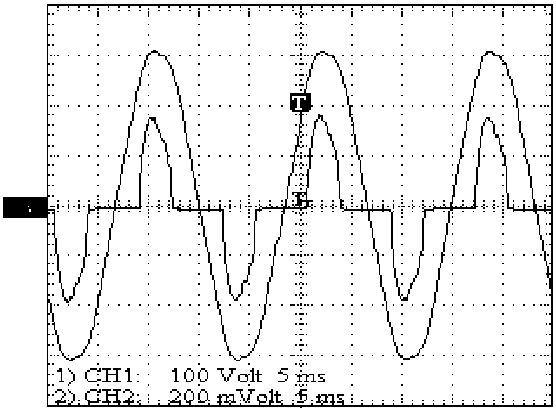


Fig. 15. Line voltage (220V) and current.

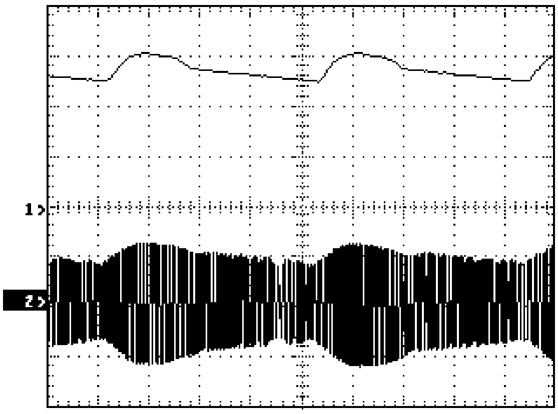

Fig. 16 . Upper trace: DC bus voltage (100V/div);
Lower trace: Lamp Current (300mA/div).
(Line voltage: 220V)

TABLE 3. EXPERIMENTAL RESULTS FOR THE "BIVOLT" CFC FILTER. OUTPUT POWER ≈ 32W

| Line Voltage [V rms] | 127 | 220 |
|---|---|---|
| THD [%] | 58.85 | 73.33 |
| PF | 0.852 | 0.809 |
| Filter resistor loss [W] | 5.92 | 2.44 |

The structure of Fig. 10 can be considered a good alternative to implement commercial electronic ballast products for the low power mass market case. Compared with the conventional single capacitor filter it presents a much better harmonic behavior (good PF and THD) and a significant lower apparent power, while preserves a safe crest factor value. These are important features when the energy efficiency is a crucial matter. On the other hand, comparing with other valley fill structures, it employs a smaller number of components and does not present a crest factor greater than 2.0, as expected when the valley fill filter is employed. These comments are organized in Table 4, where an output power of 32 W has been considered for all cases.

TABLE 4 – FILTER COMPARISON

| Filter Type* | PF | THD (%) | # comp. | CF | $P_i$ (W) | N (VA) | $P_{Rv}$ (W) |
|---|---|---|---|---|---|---|---|
| 1 | 0.45 | 200 | 1 | 1.5 | 32.4 | 70.0 | - |
| 2 | 0.91 | 44 | 5 | 2.1 | 32.3 | 36.8 | - |
| 3 | 0.94 | 34 | 6 | 2.3 | 32.3 | 34.4 | 0.43 |
| 4 | 0.80 | 74 | 3 | 1.6 | 35.4 | 44.2 | 2.41 |

*Where:
type 1: single capacitor filter
type 2: conventional valley fill filter
type 3: modified valley fill filter
type 4: CFC valley fill filter (220V)

## IV. CONCLUSION

This paper described some valley fill filter topologies, with a main focus on low power fluorescent electronic ballasts. A review of the basic valley fill filter has been presented along with the more important parameters from the viewpoint of harmonic behavior and lamp current crest factor. Although conventional valley fill filters feature a good harmonic performance the resultant crest factor (> 2.0) becomes prohibitive if an electronic ballast product intends to preserve the expected lamp lifetime and observe worldwide standards. If the fluorescent lamp technology changes in the future (in order to accept a greater CF), basic valley fill filters would be a good option again.

The paper also revised a recently introduced crest factor correction (CFC) valley fill filter based on the conventional idea, but presenting a more simple network. The main equations and merit figures have been described in order to prove the structure is able to provide a recommended CF mark and also present a good harmonic behavior. Those features ensure an improved front-end alternative comparing to the simple capacitor filter rectifier, used in many mass market low power electronic ballast nowadays. Another simpler valley fill structure has been introduced here, based on the CFC original one, which also presented a good performance. The main proposal has been adapted to be used when supplied either by a 127V or a 220V utility, which is a very useful technique in some countries.

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