The 6th Brazilian Power Electronics Conference
November 11-14, 2001
Florianópolis, SC - Brazil

Power Electronics Research - A Paradigm Shift

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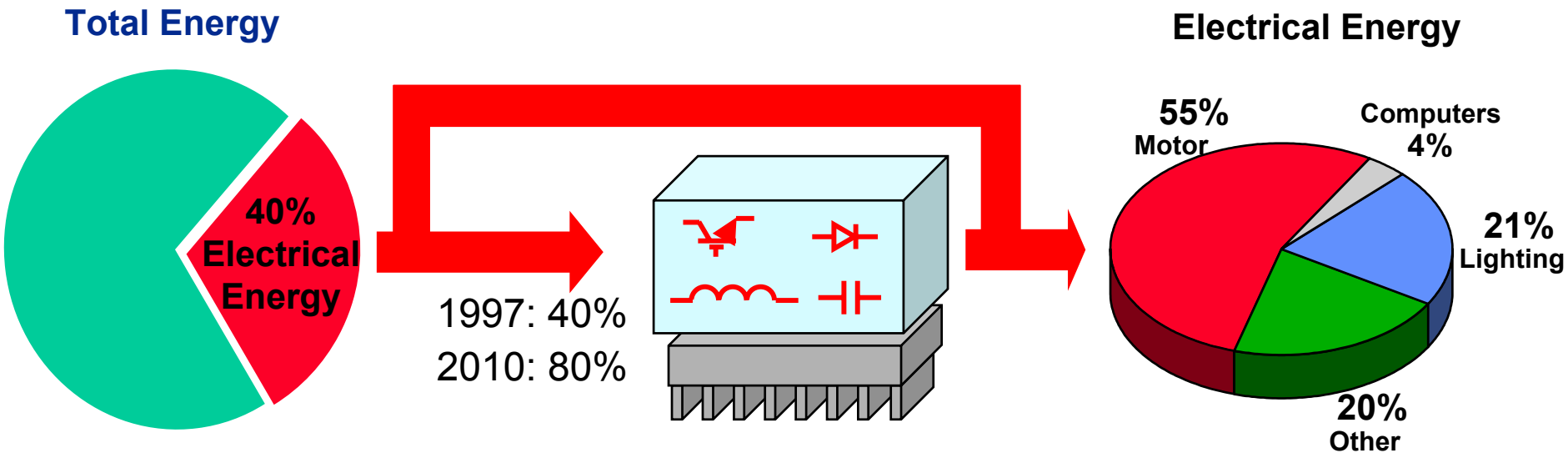
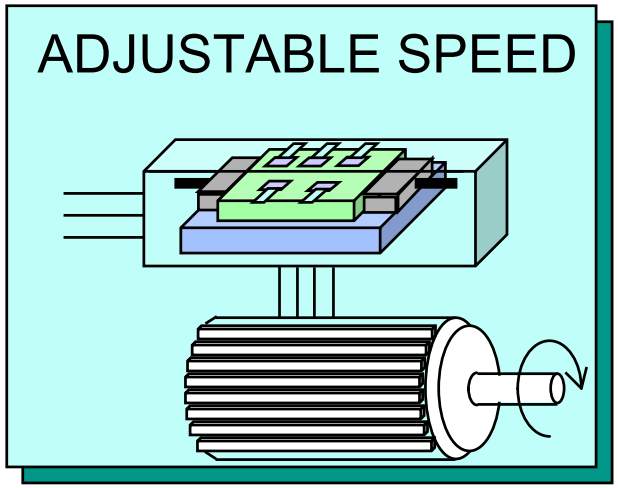
Virginia Tech, University of Wisconsin - Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, University of Puerto Rico - Mayaguez

Energy and Power Electronics

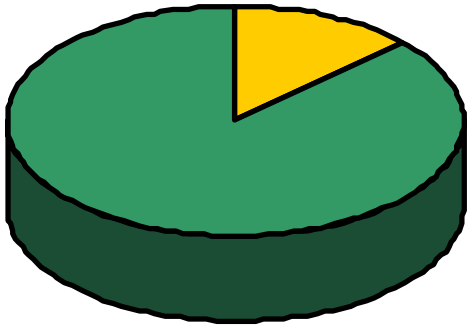


* *EPRI*



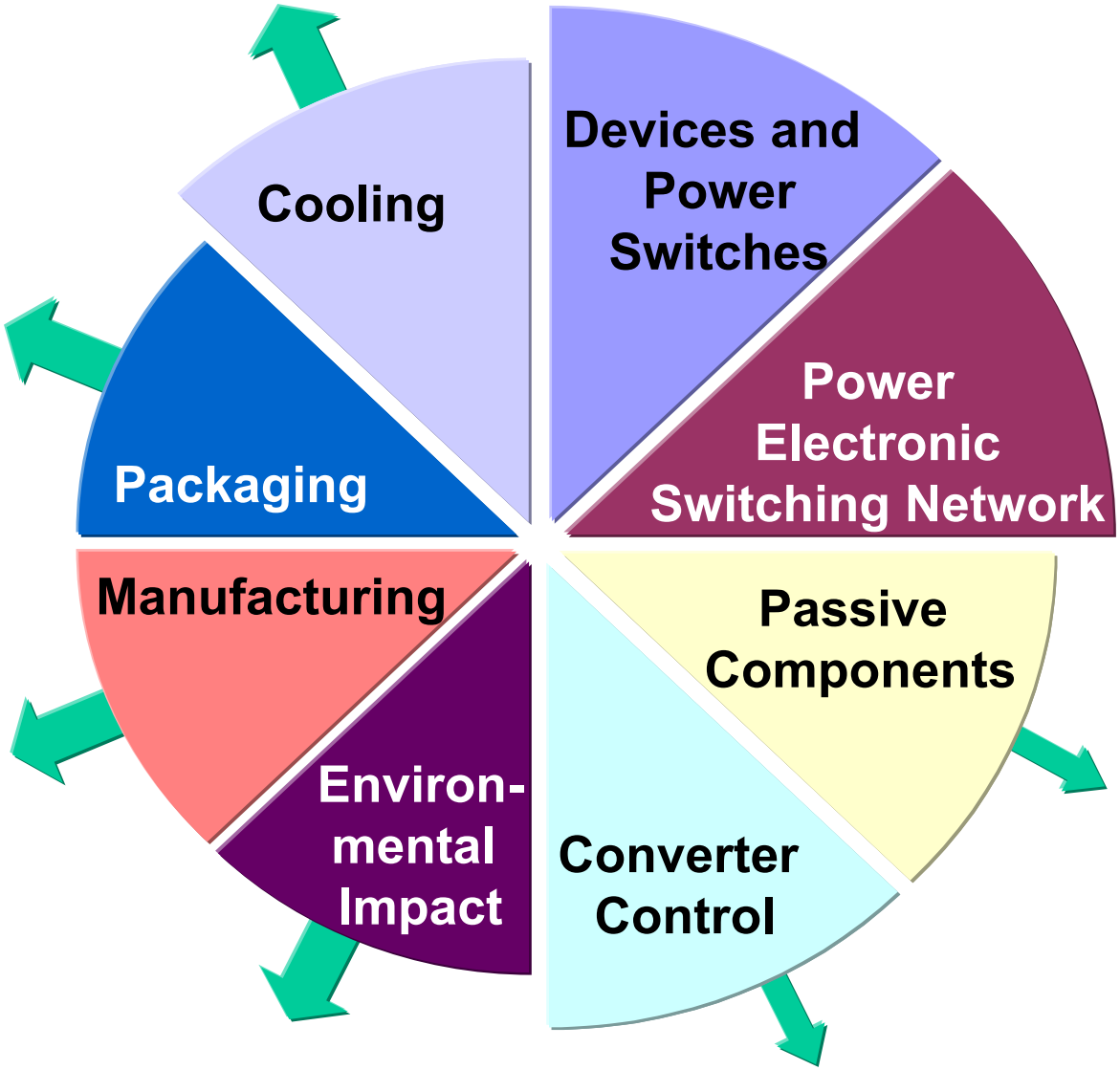
35% Efficiency Gain

Internet* **13%** 2001

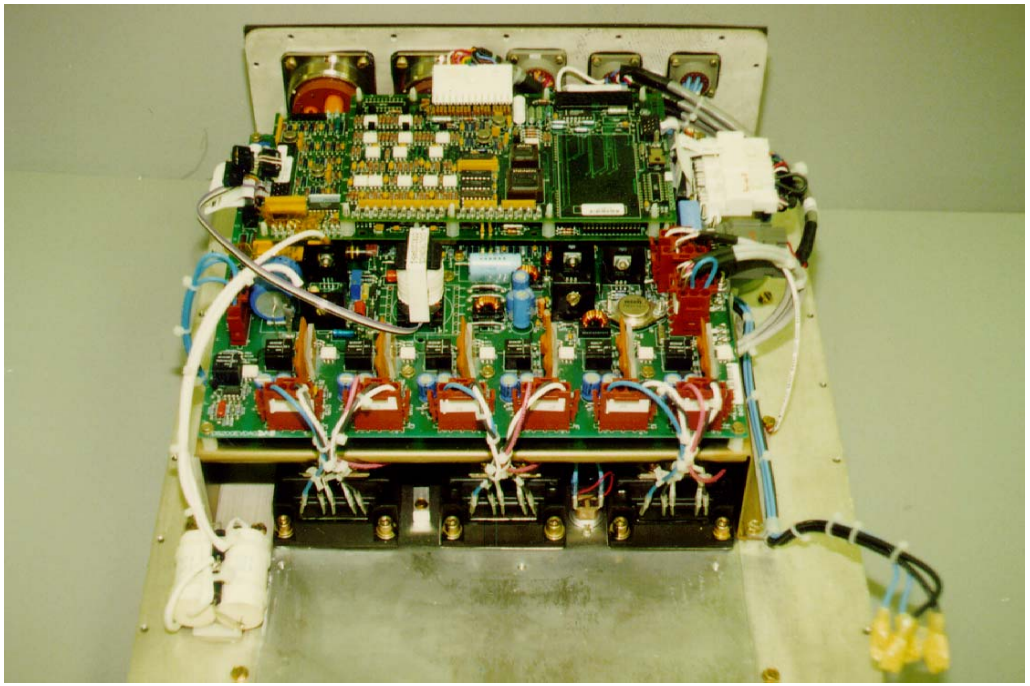


**K Azar*

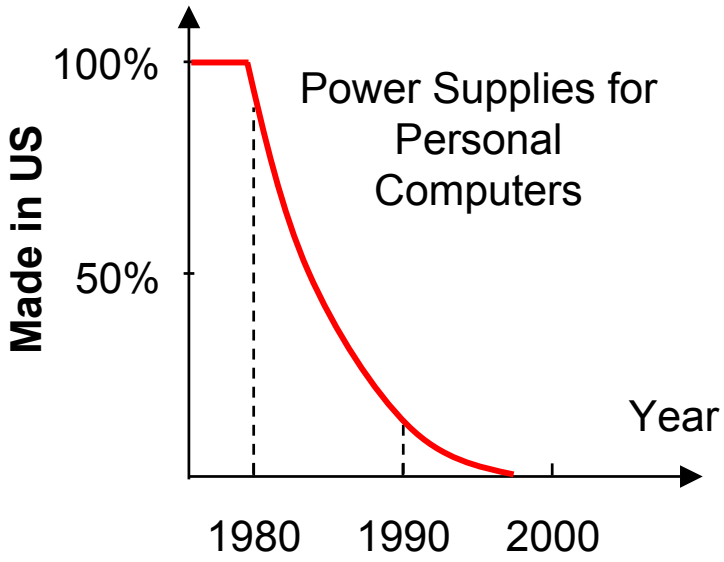
State-of-the-Art Power Electronics

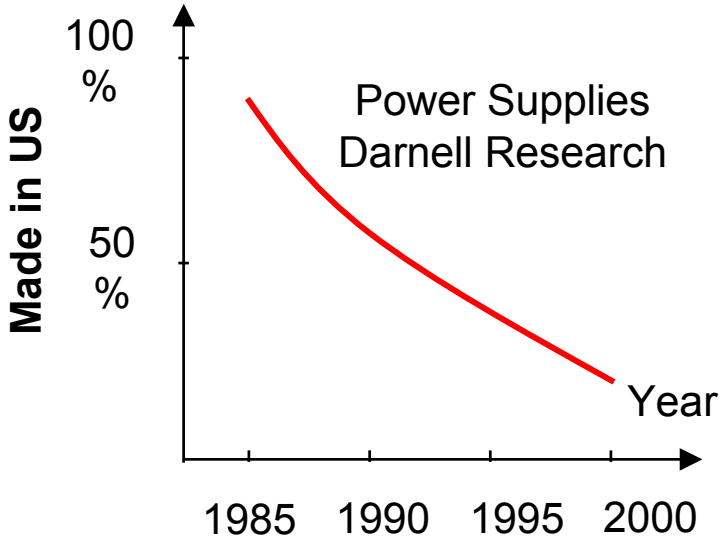


State-of-the-Art of Power Electronics Technology



Losing Manufacture Base



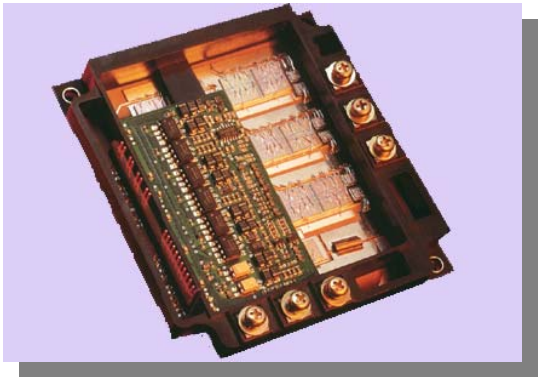


Issues

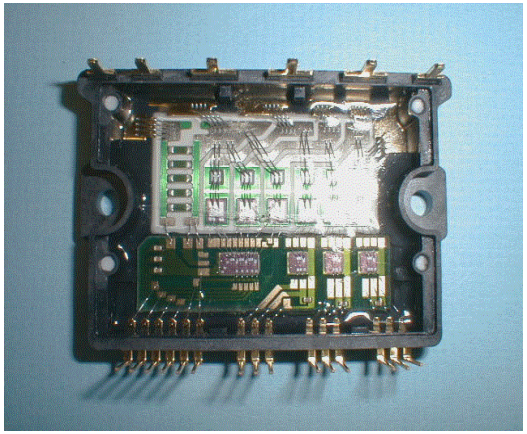
- **Long design cycle**
- **Non standard circuits and parts**
- **High labor content**
- **Poor reliability**
- **High cost**

Industry Trends
Intelligent Power Modules (IPM)

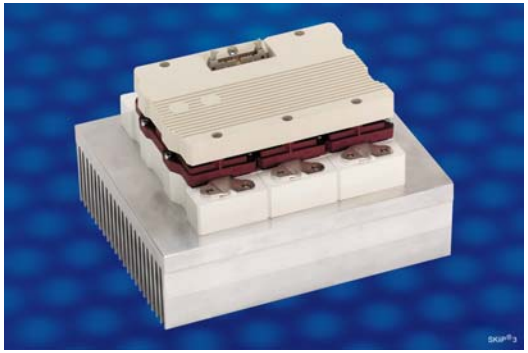
Toshiba



Fuji

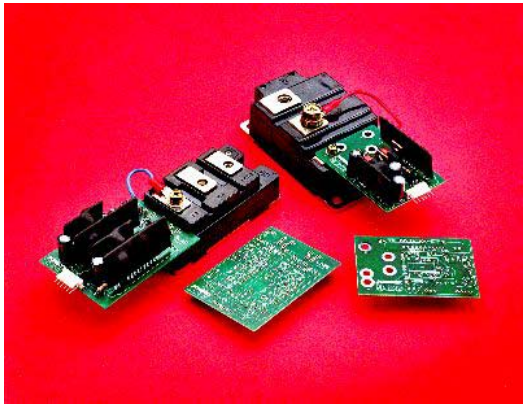


Semikron



- Standard modules
- Low labor content
- Improved reliability
- Reduced cost

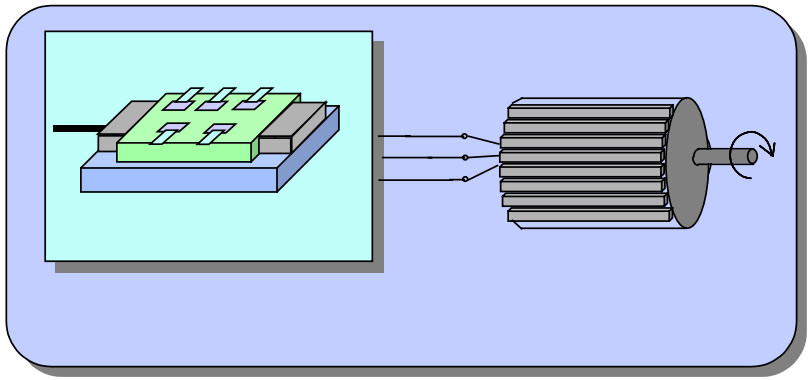
Powerex



Eupec/Infineon

System Integration via IPEM

Motor Drives

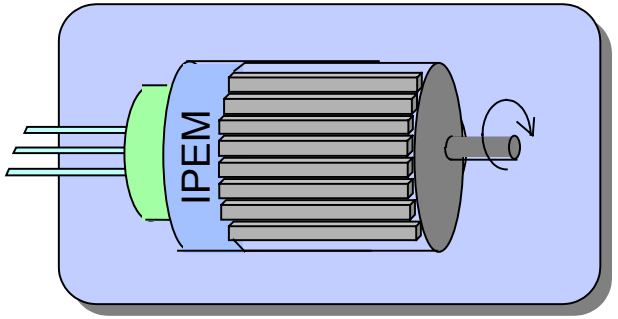


Improve reliability

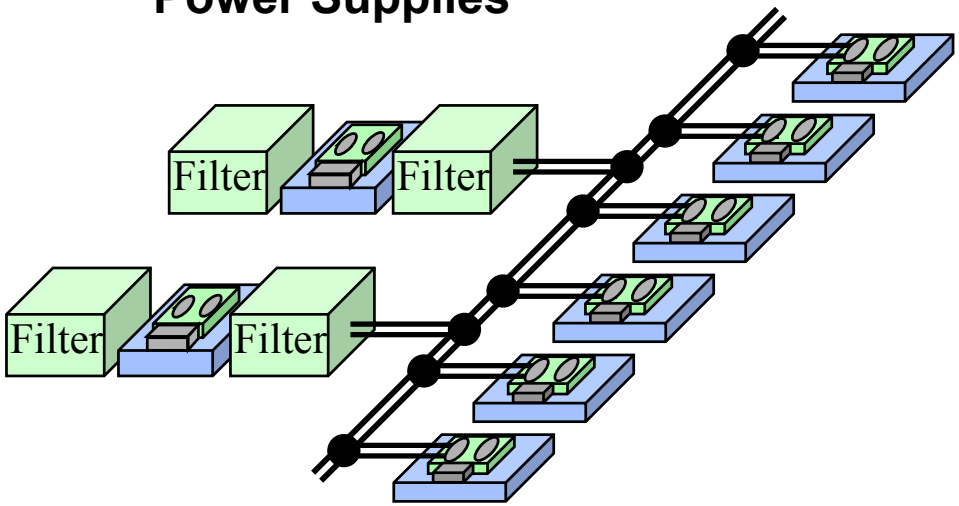
Challenge

Reduce cost

More integration



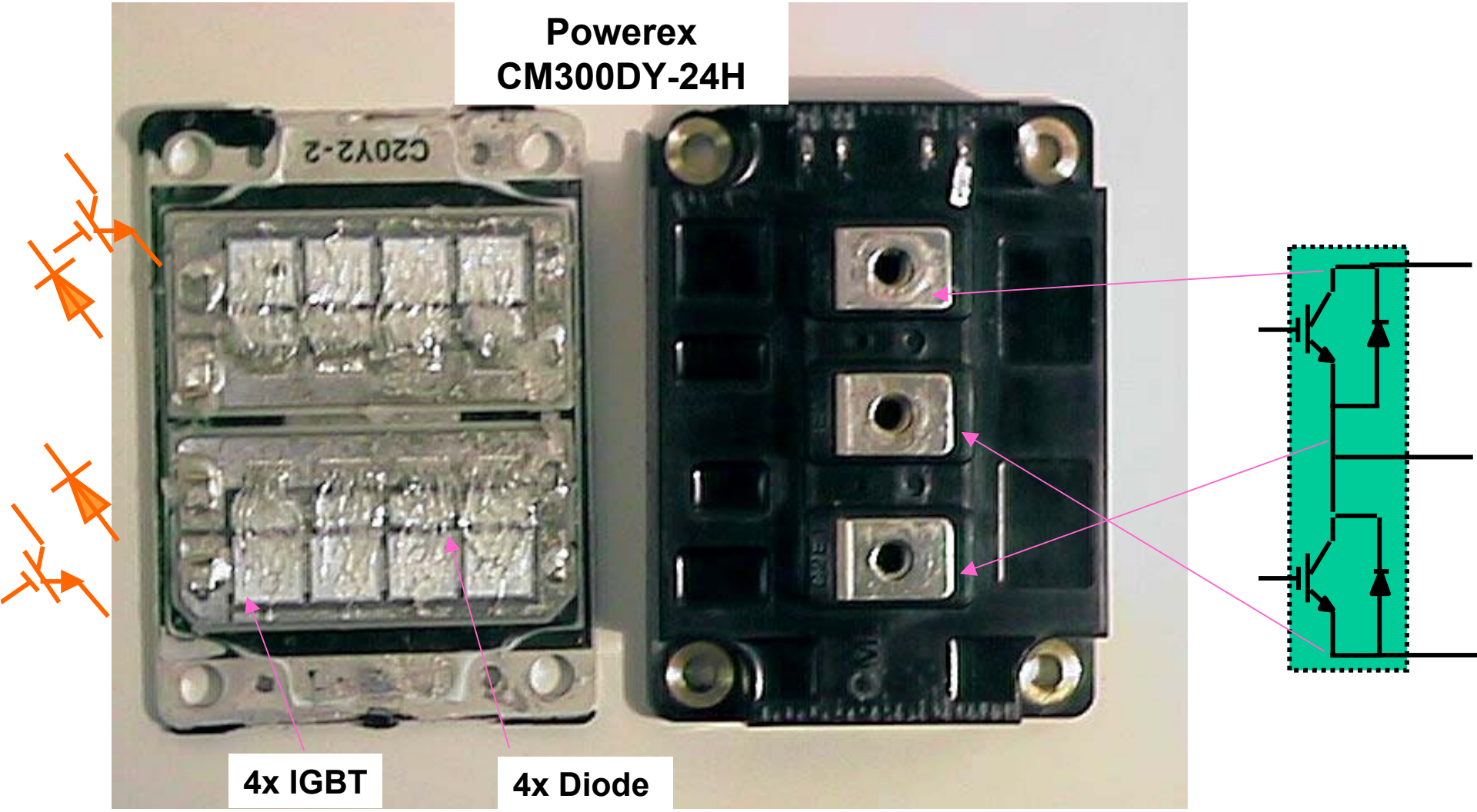
Power Supplies



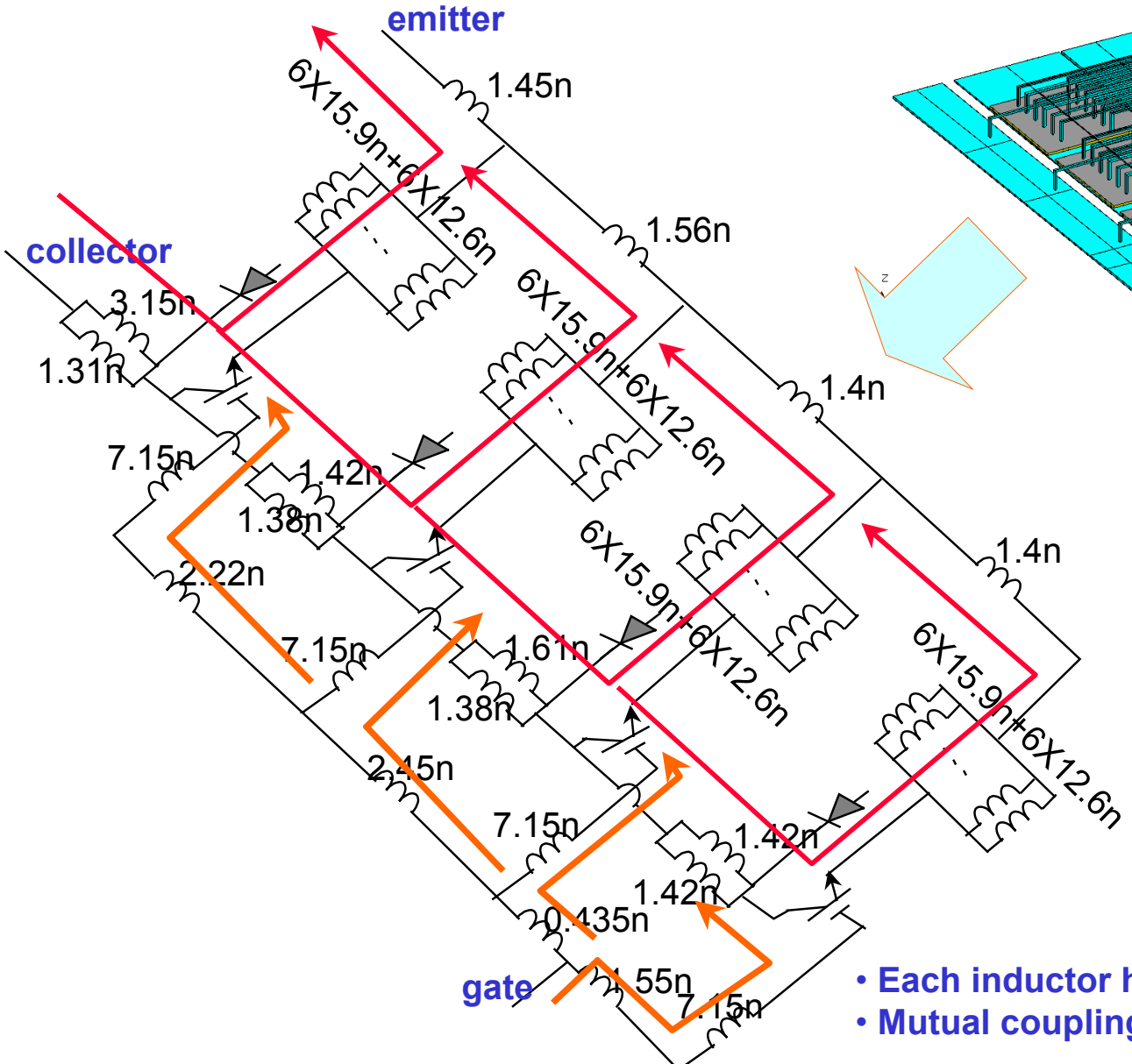
Challenges:

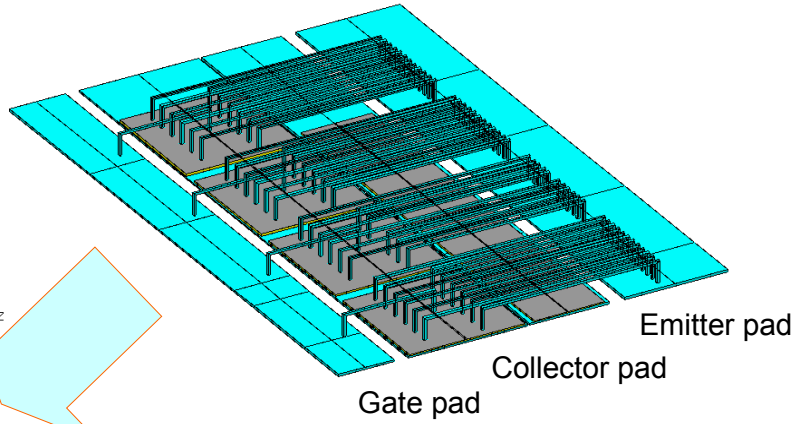
- Standardized IPEMs
- Application specific IPEMs
- Improved power density
- Reduce cost

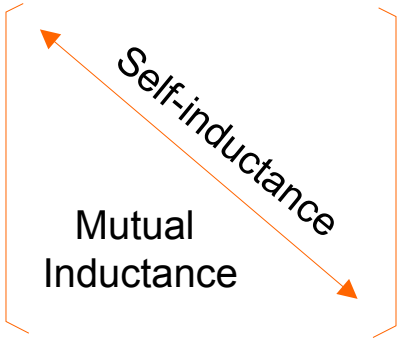
Layout of A High Power IGBT Module



Mappings Between Module Layout and Parasitics





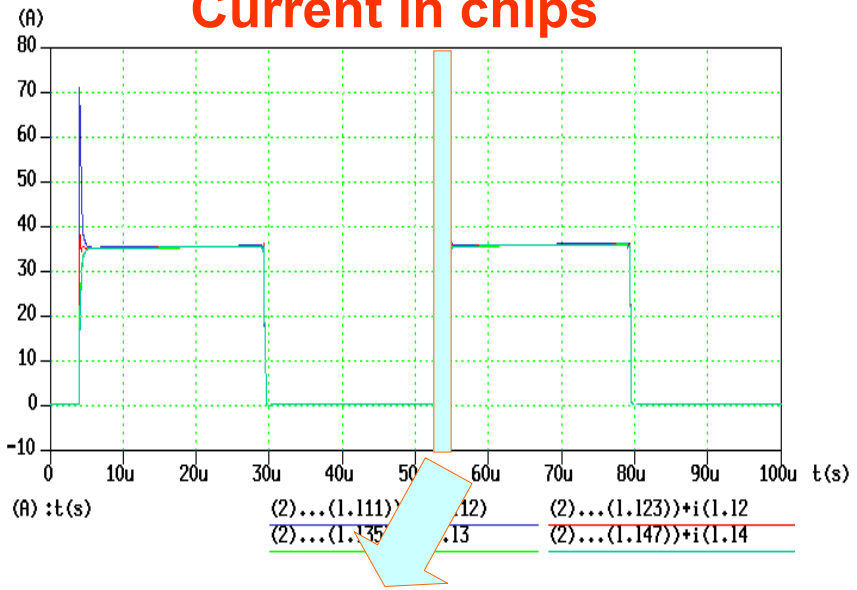


60x60 elements

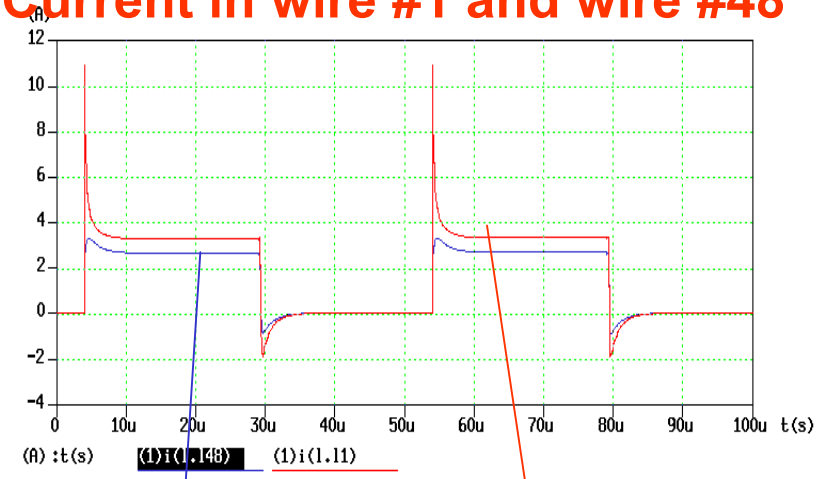
- **Each inductor has resistance associated**
- **Mutual coupling is not indicated**

Current Distribution Between Paralleled Chips

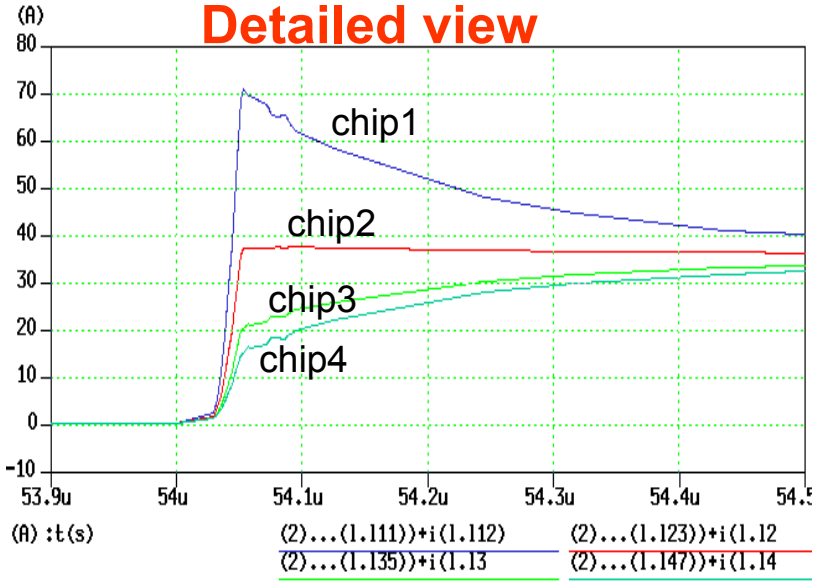
Current in chips

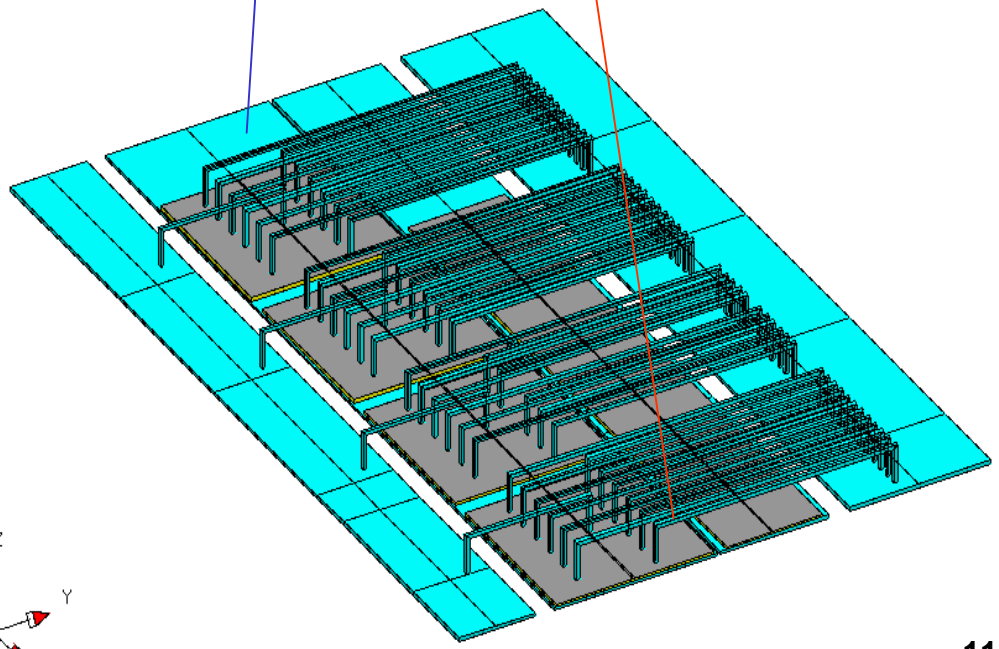


Current in wire #1 and wire #48

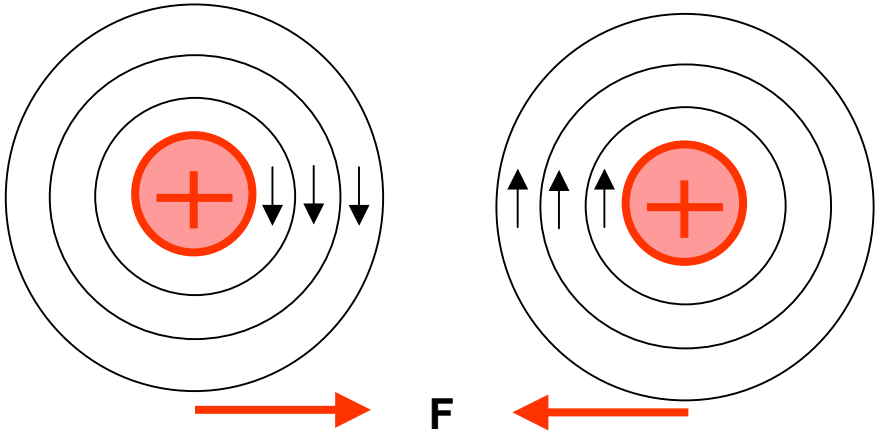


Detailed view

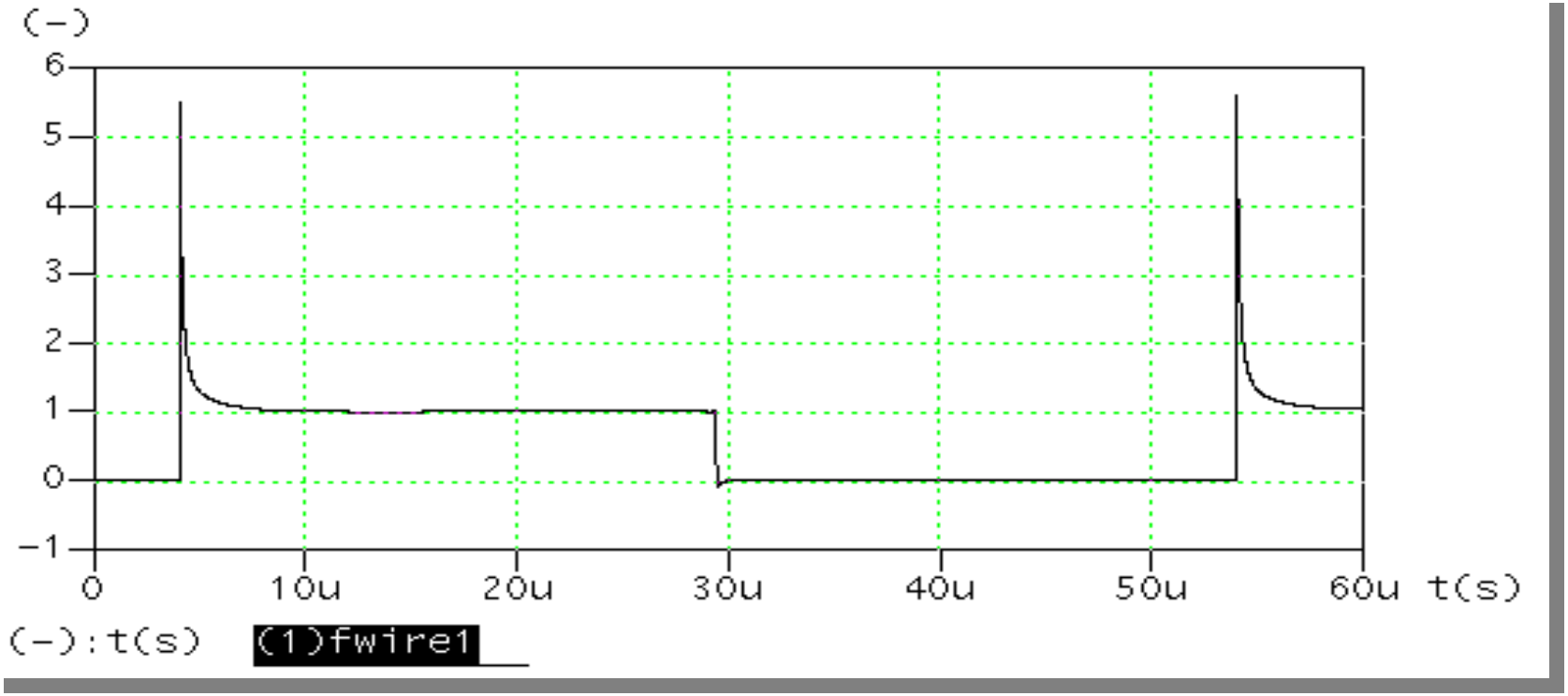




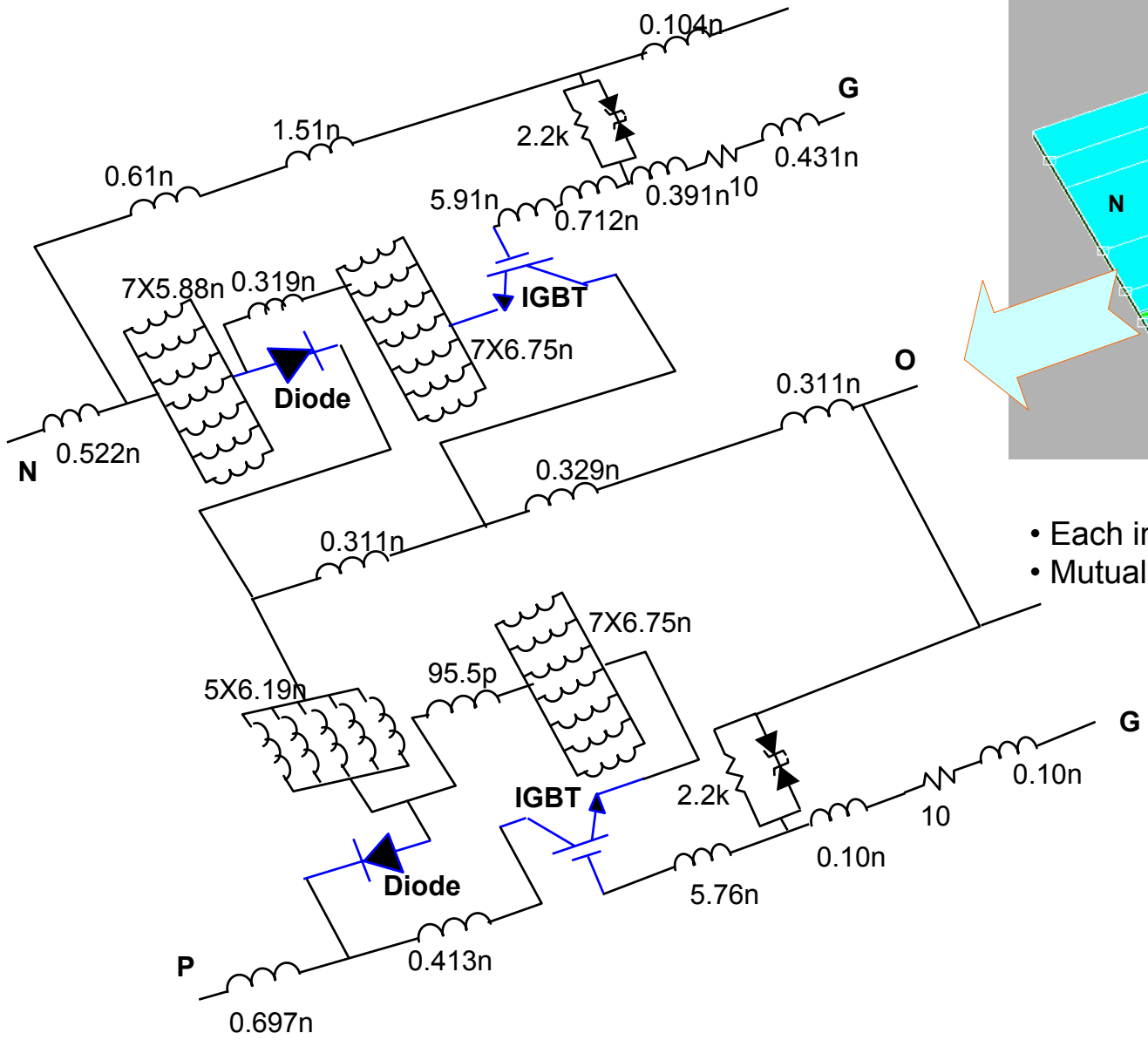
Mechanical Force Generated on Wire #1

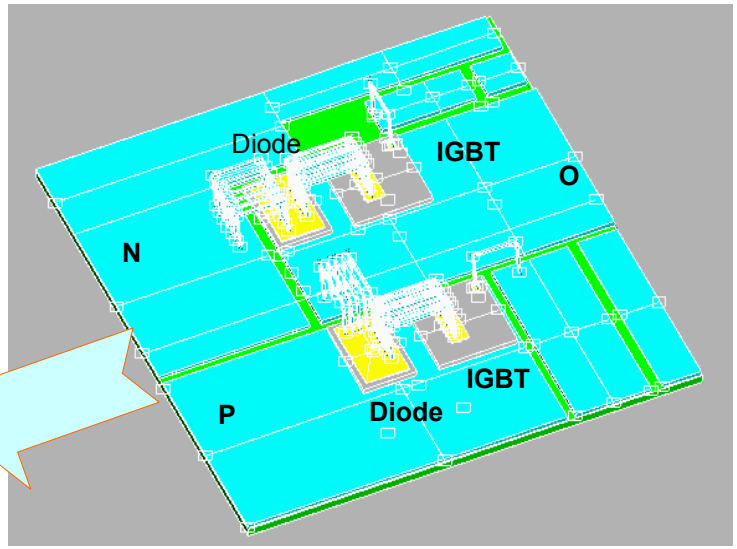


Gram



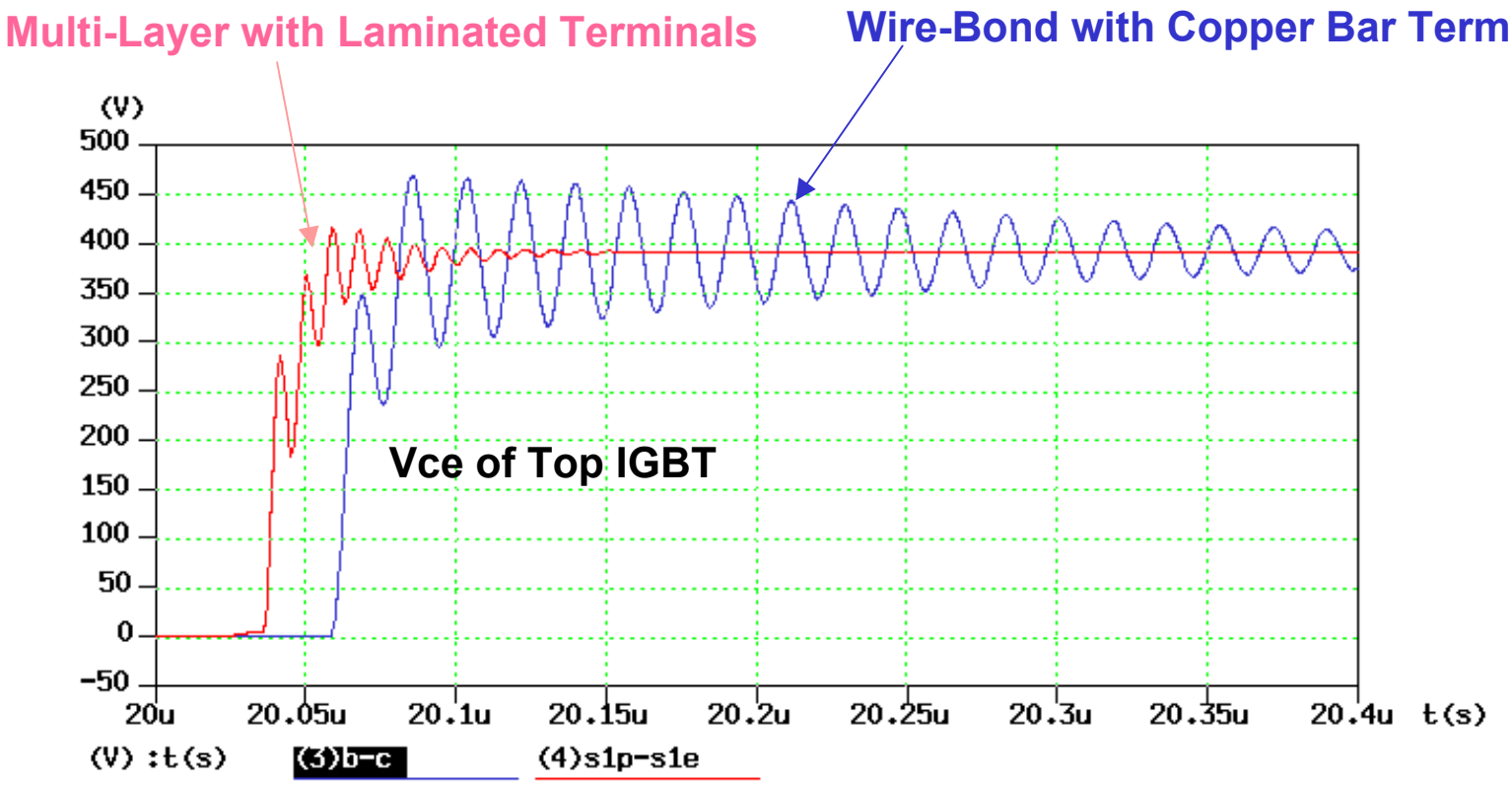
Mapping between The Module Layout and Its Equivalent Parasitic Inductance





- Each inductor has a resistance associated
- Mutual coupling effect

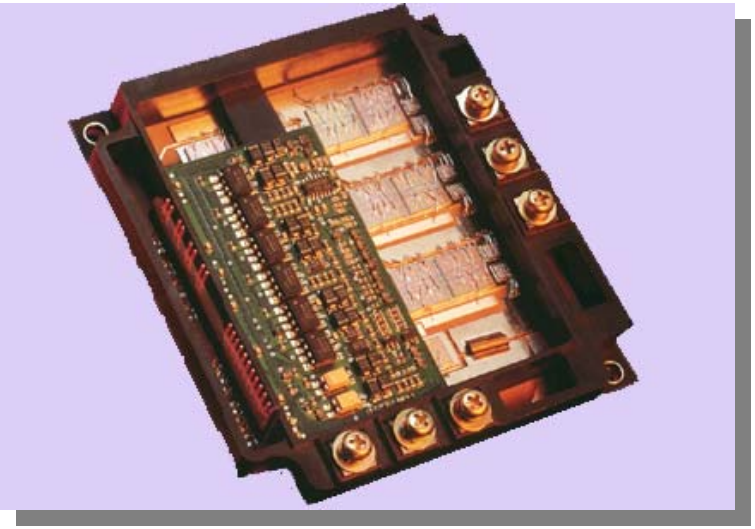
A Comparison of Voltage Stress With Different Packaging Designs



Simulation Condition:

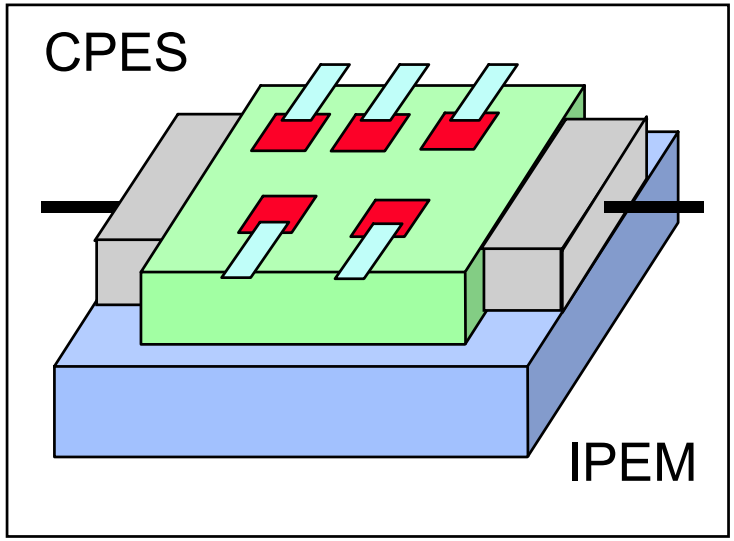
- Ideal DC Bus 400V, inductive load, load current 40 A
- Wire-bond and multi-layer layout for PEBB packaging
- Rg=12 Ohm
- Terminal Inductance 30nH and 8nH respectively
- No snubber caps are used

CPES Approach via IPEM



More

Integration



Limitations:
- Wire bond
- Thermal management
- Low power applications

- Eliminate wire bond
- 3-D thermal management
- Low-medium power applications

Research Goal: Improve the quality, reliability and cost effectiveness of power electronics systems

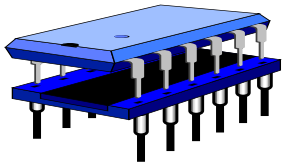
IPEM Follows VLSI

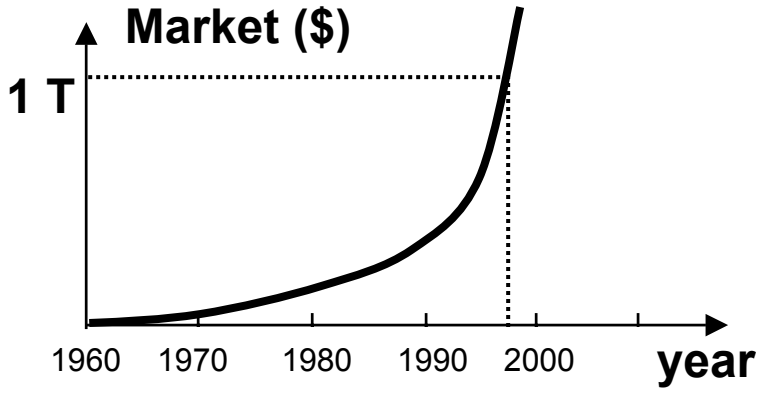
Moore's Law Prevails

- Standardization
- Manufacturability
- Volume Production
- Cost Reduction

Signal Processing

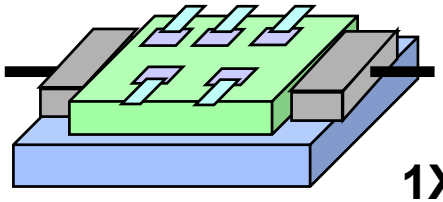
IC

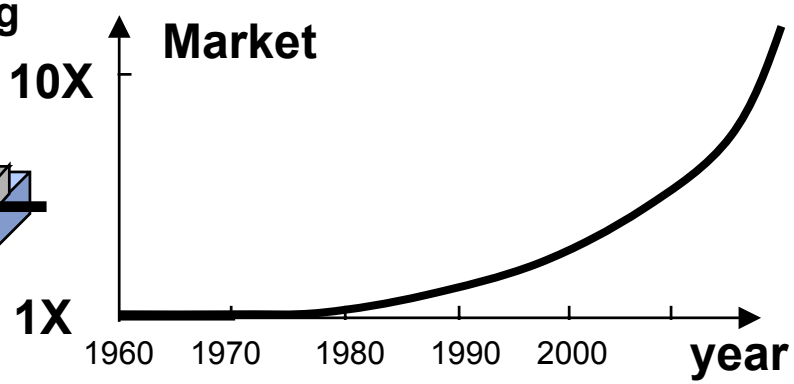




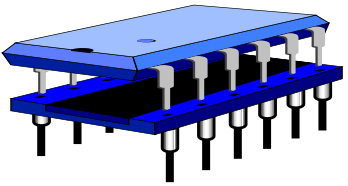
Power Processing

IPEM



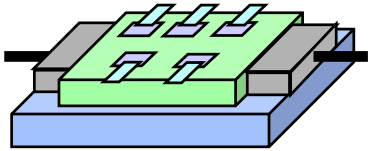


Major Challenges for IPEMs



Short term

- Integration of passives
- Thermal management
- Minimization of parasitics



Medium term

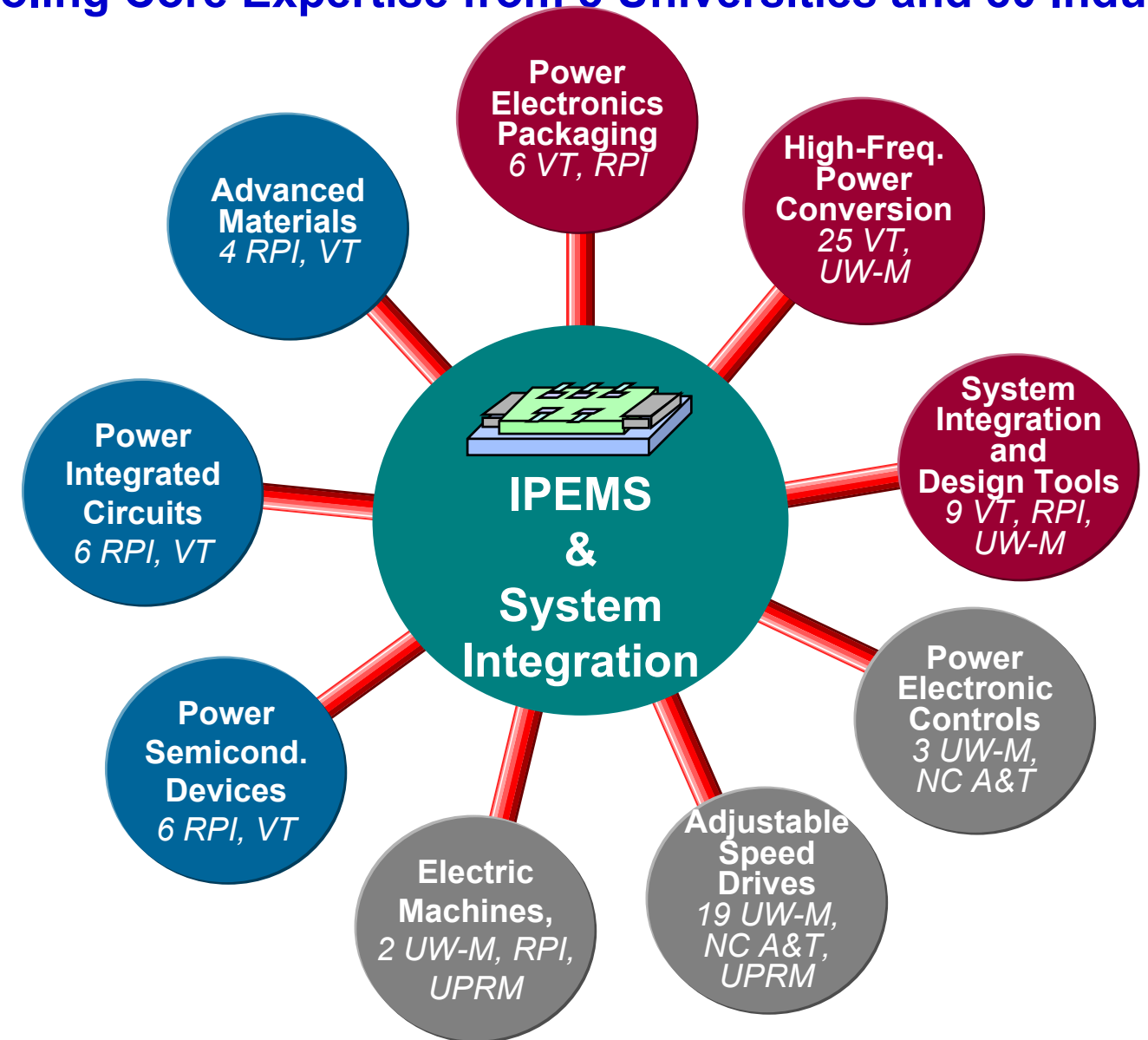
- 3-D packaging
- Integration of power devices and ICs
- Integration of controls and sensors
- Integrated design methodology
- Integrated CAD tools / models

Long term

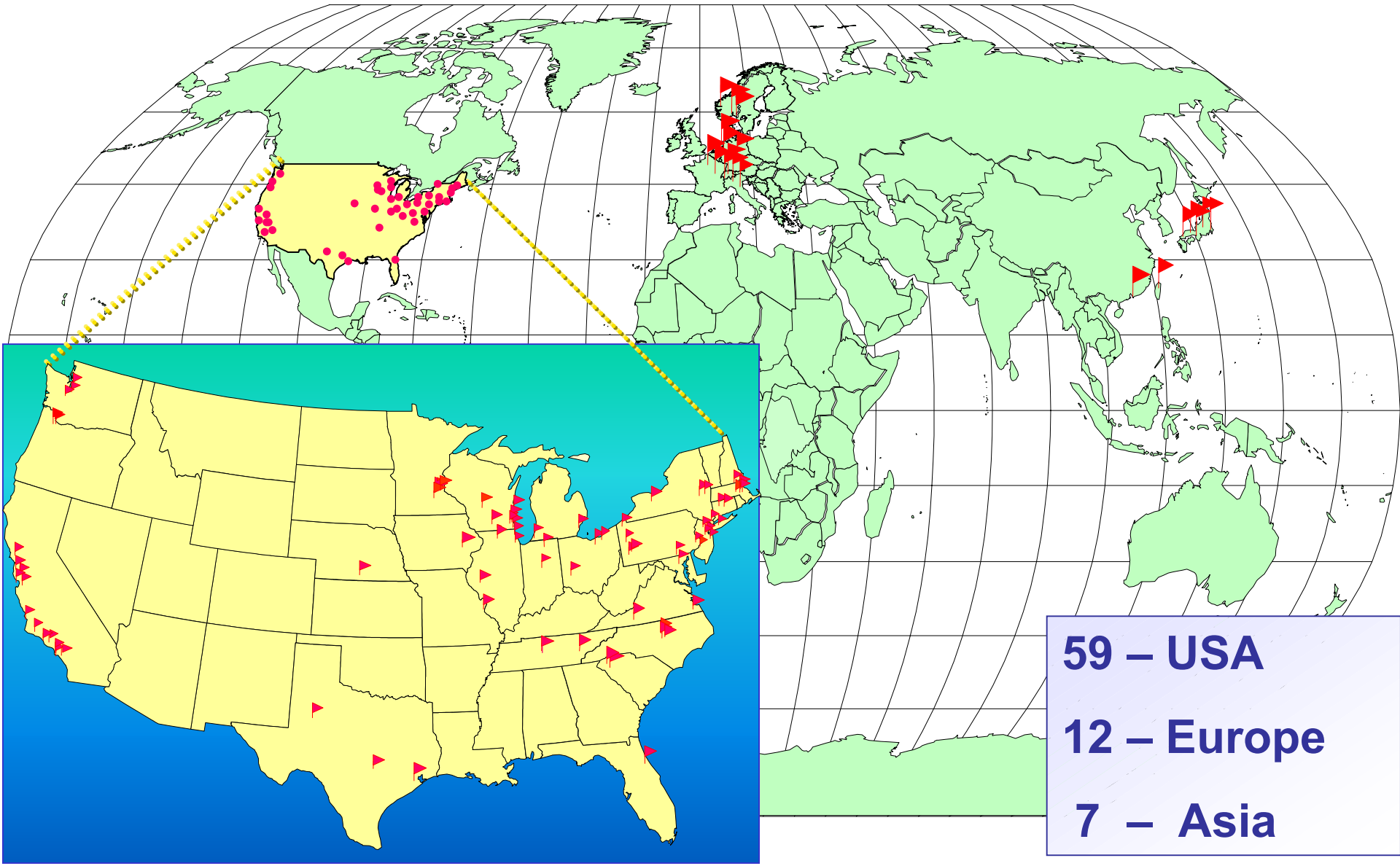
- Novel power devices / materials
- Standardization of IPEMs
- Reliability
- Cost reduction

CPES Approach - Industry/University Partnership

Pooling Core Expertise from 5 Universities and 80 Industries



CPES
Industry Partners Worldwide

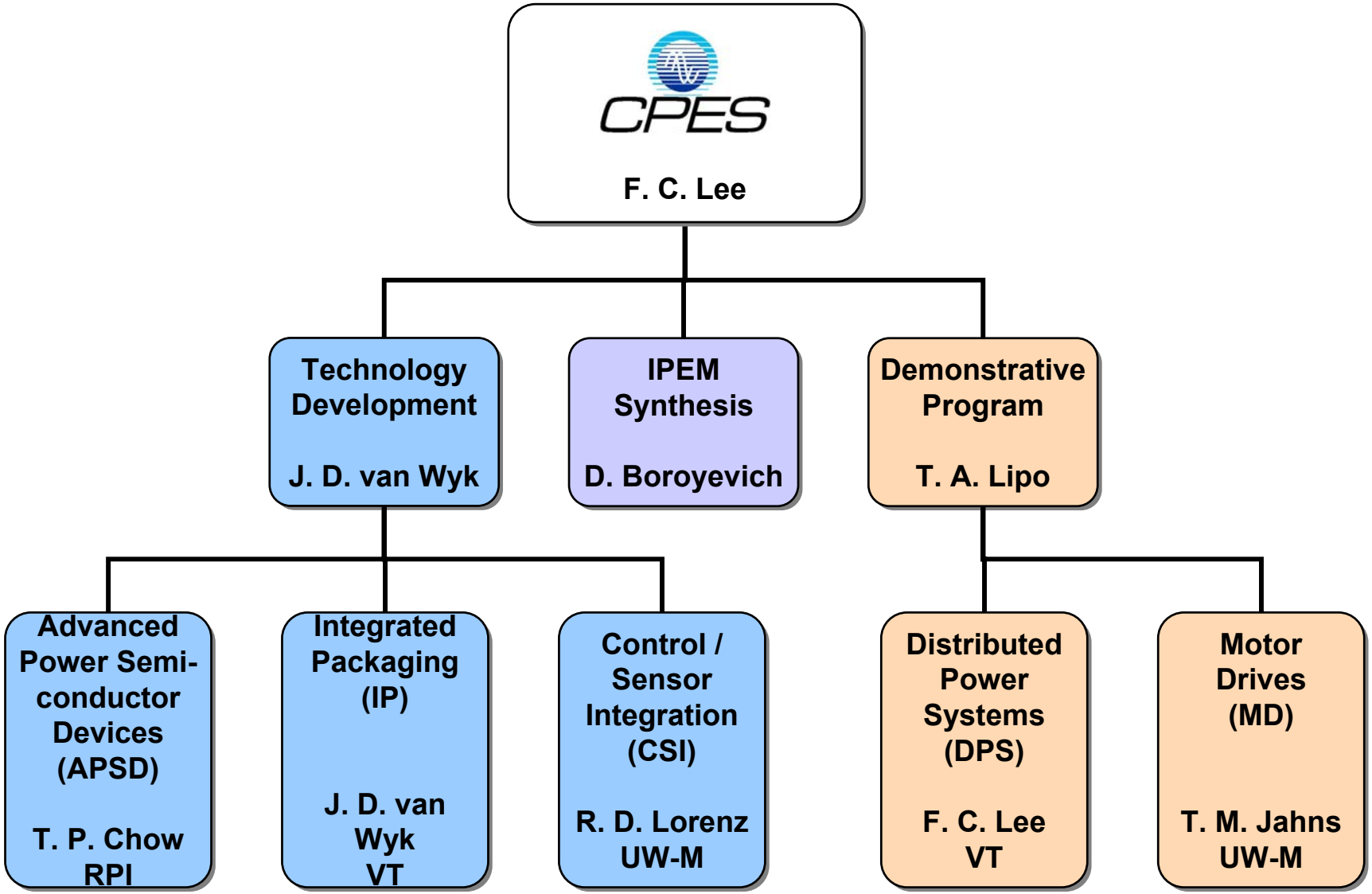


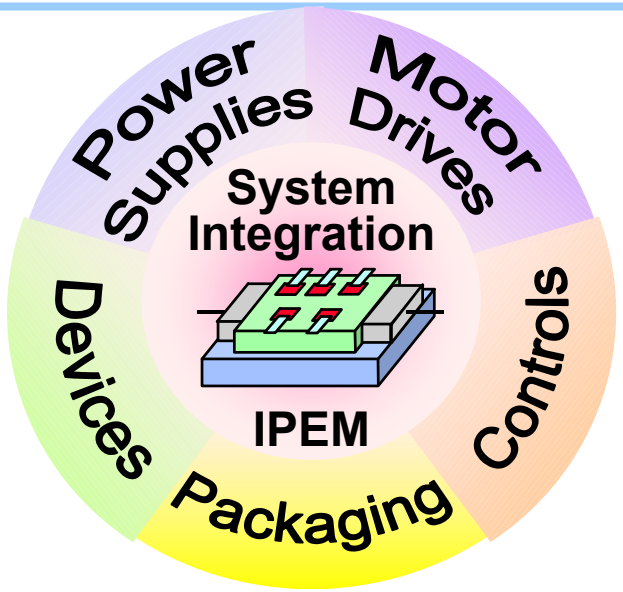
59 – USA

12 – Europe

7 – Asia

CPES Research Programs



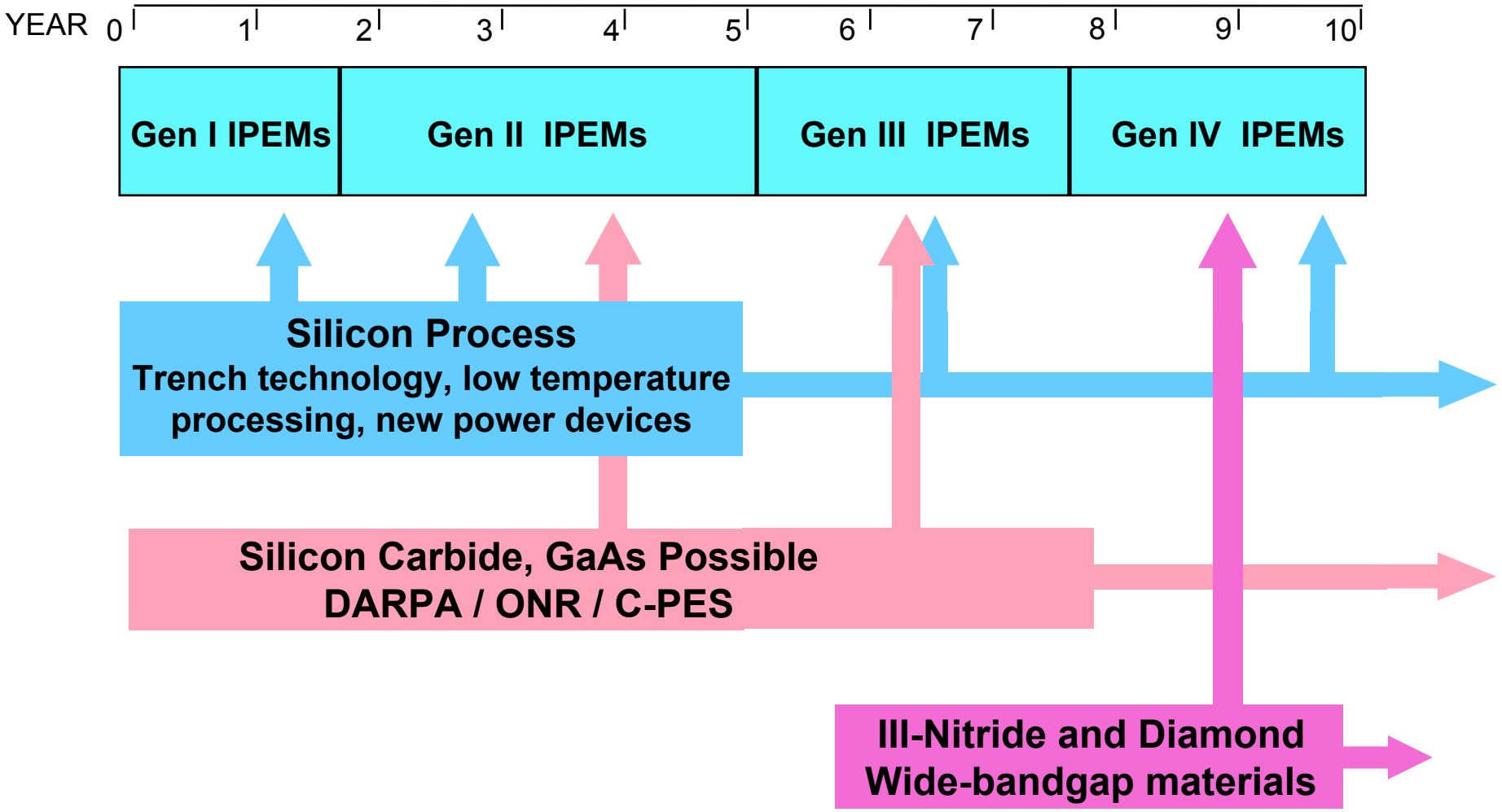


Advanced Power Semiconductor Devices (APSD)

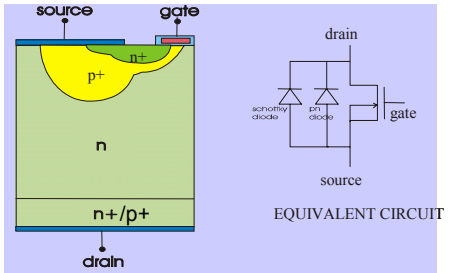
Paul Chow

Rensselaer Polytechnic Institute
APSD Leader

Advanced Power Devices Needed for Next Generation Testbeds

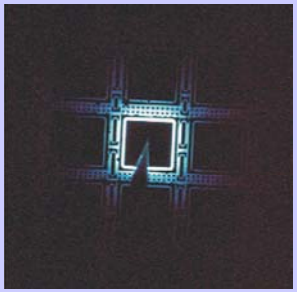


APSD Impact on Motor Drive Testbed



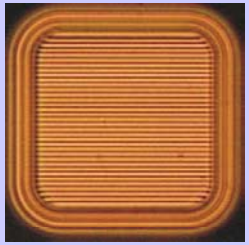
DMOS-FET/IGBT with Fast Diode

or

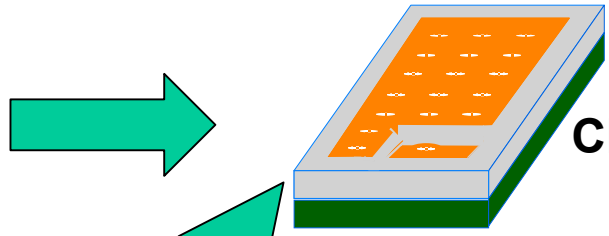


SiC Rectifier

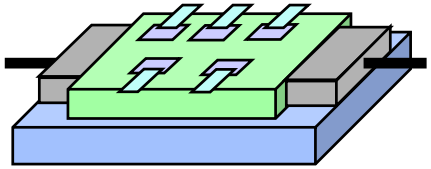
or



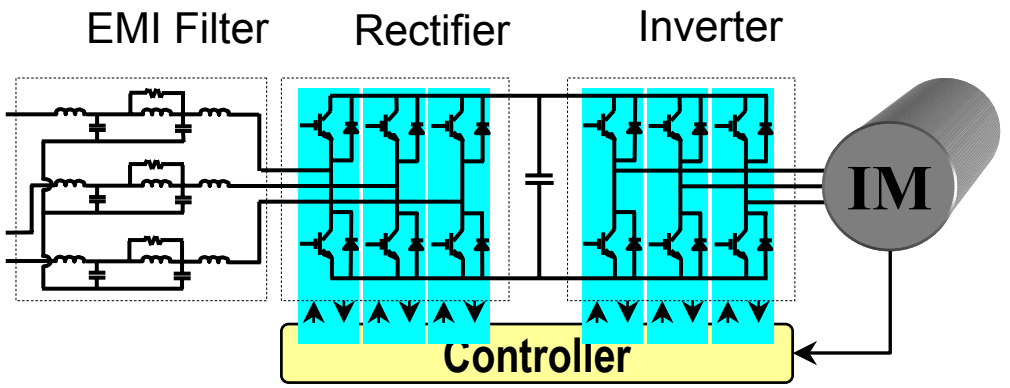
Si Trench Rectifier



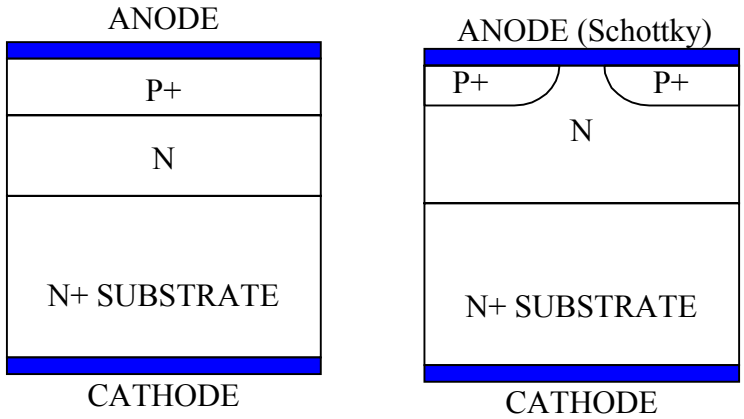
Chip-Scale Package



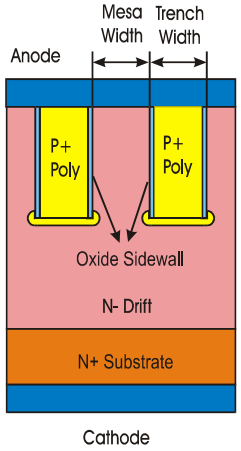
IPEM



Conventional vs Trench Rectifier

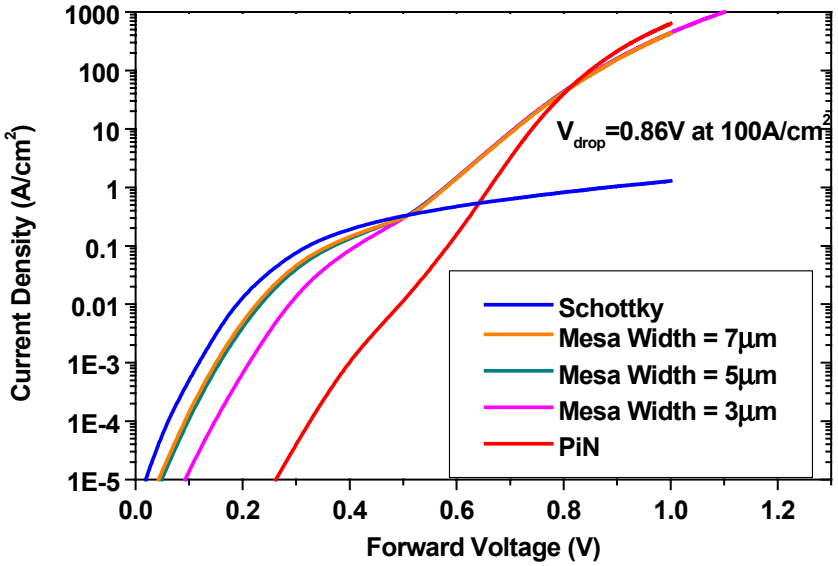


Conventional PiN and MPS Rectifiers Cross-Sections

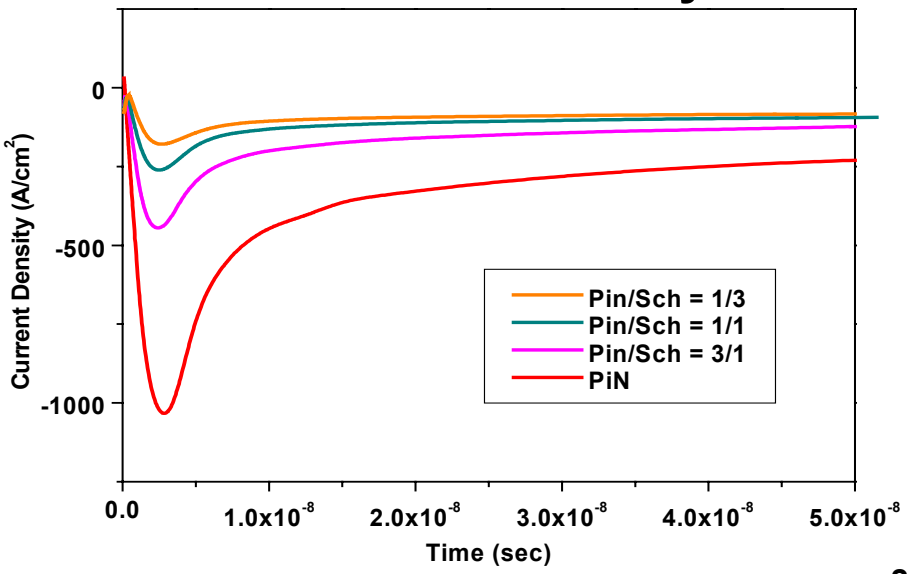


Trench MPS Rectifier Cross-Section

Forward I-V

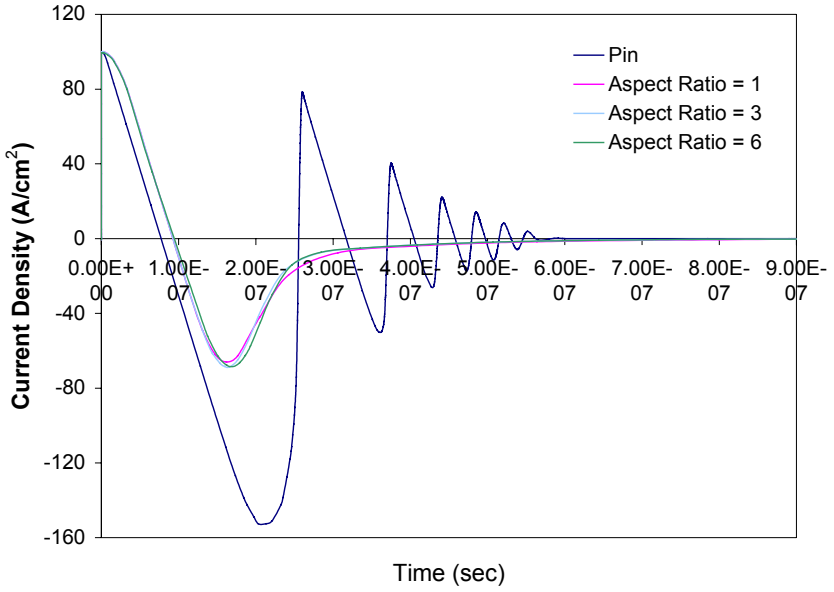


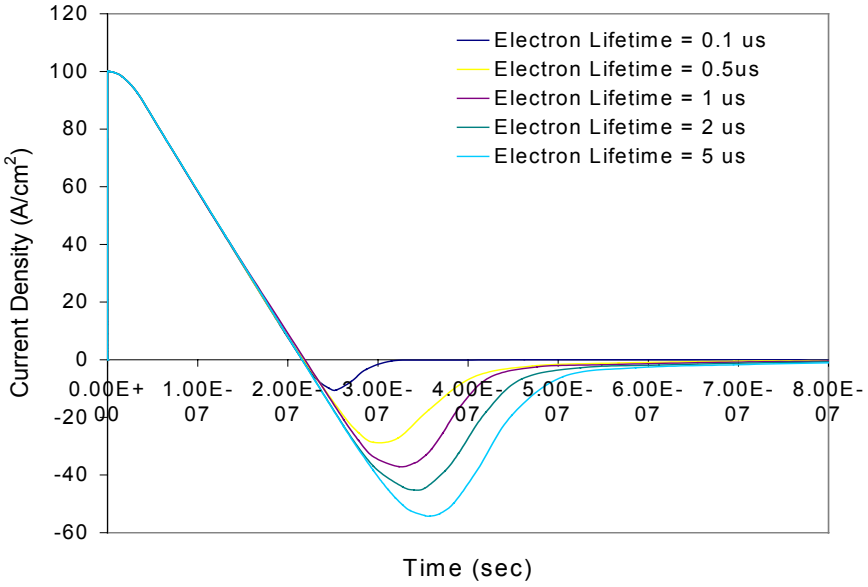
Reverse Recovery



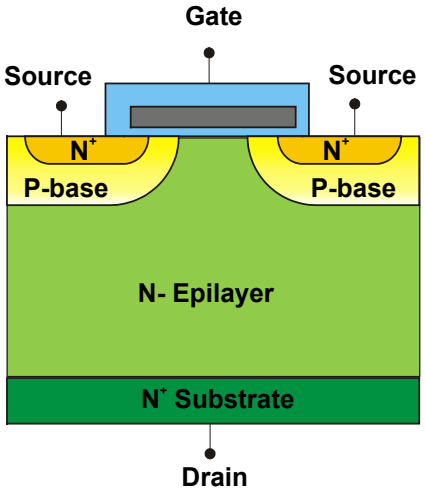
High-Voltage Si Trench MPS Rectifier

600 V Device Reverse Recovery Characteristics

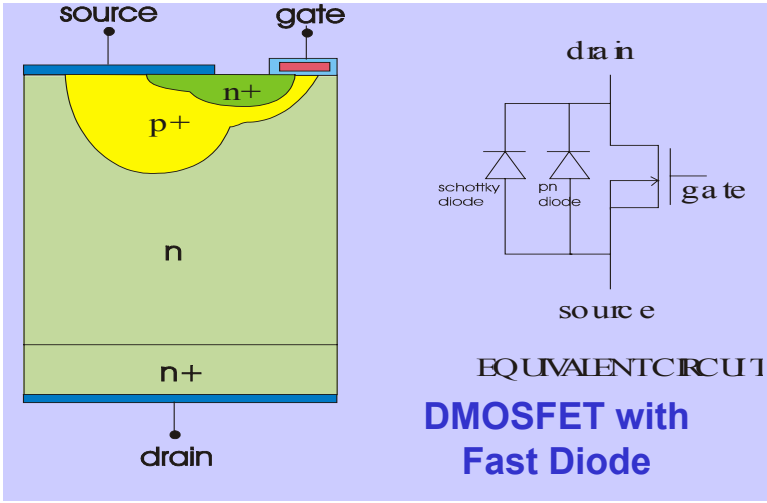




Integrated Si DMOSFET/MPS Rectifier Device



Conventional DMOSFET with Integral PiN Rectifier



Drawbacks:

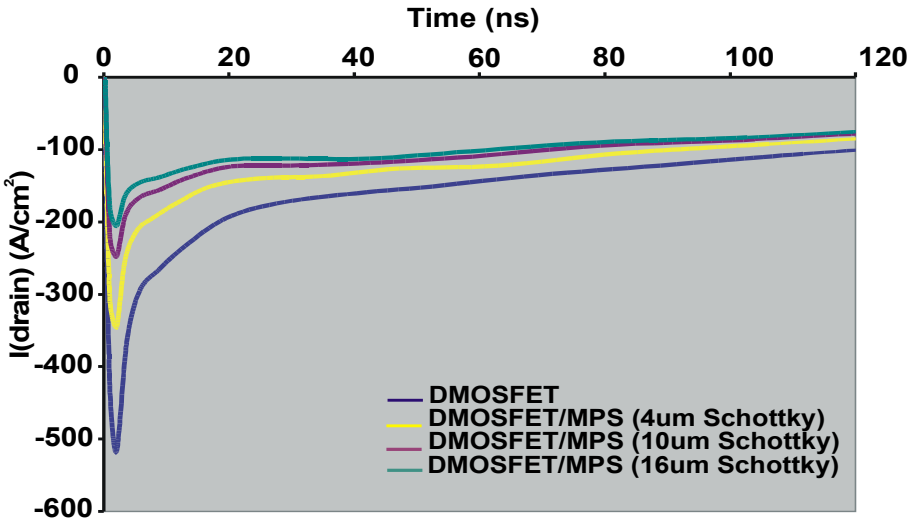
- Slower switching response
- Less ruggedness
- Large reverse peak current of integral PiN rectifier

Advantages:

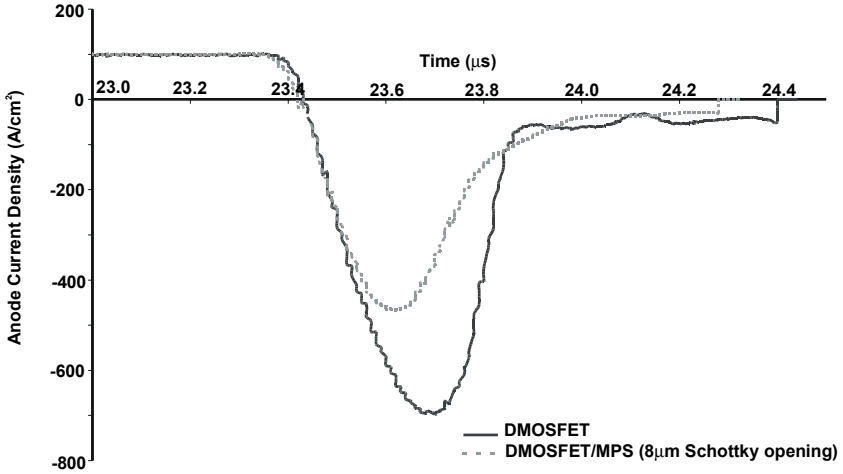
- Faster integral rectifier
- No change in fabrication process
- No degradation in forward conduction or switching characteristics
- Improved ruggedness

Integrated Si DMOSFET/MPS Rectifier Device

Reverse Recovery characteristics



Experimental Reverse Recovery Results



100°C

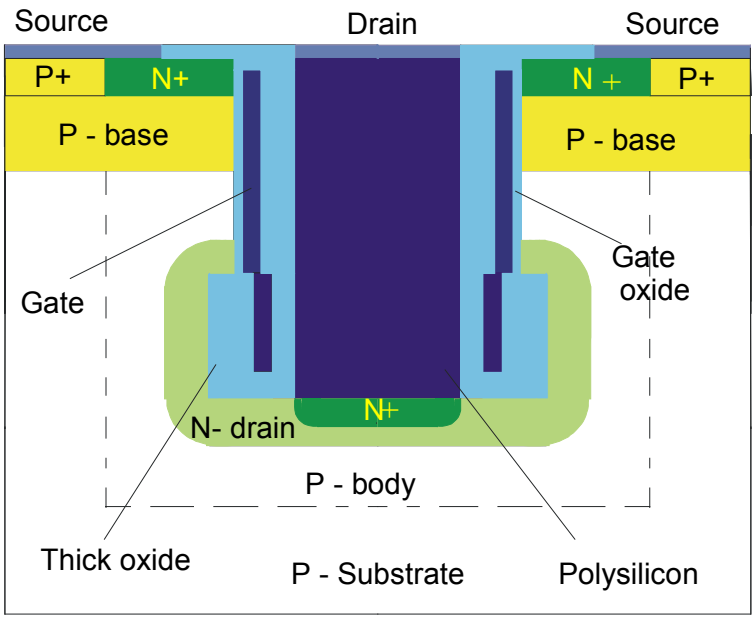
Future Work:

- Complete detailed device characterization
- Deliver large-area functional chips to IPEM packaging

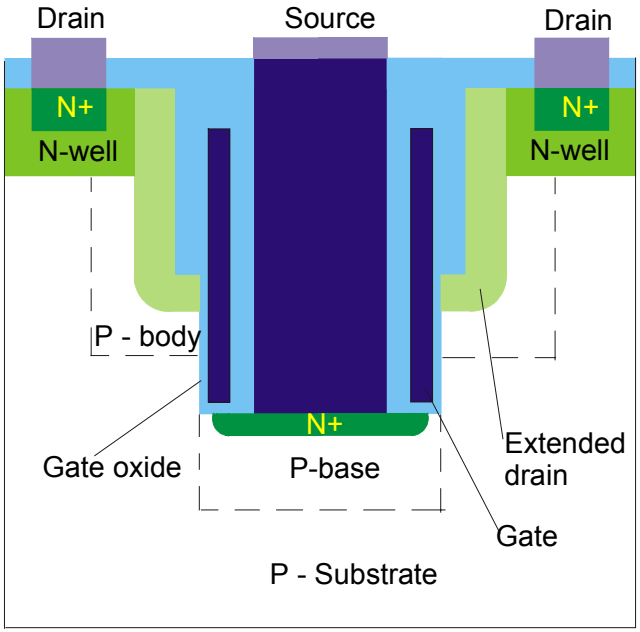
Lateral Trench MOSFETs for 48V VRM

Device Cross-Sections

Bottom Drain Contact

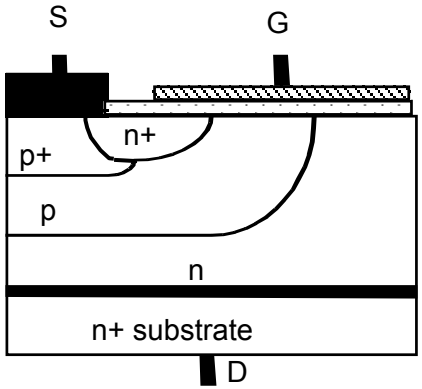


Bottom Source Contact

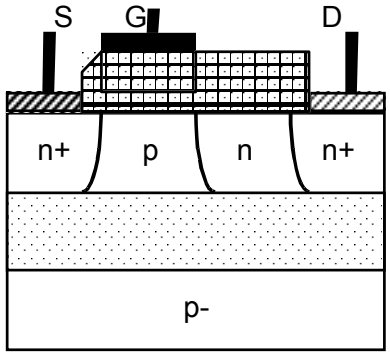


- Small cell size
- Channel length not limited by lithographic capabilities
- Reduced Miller Capacitance

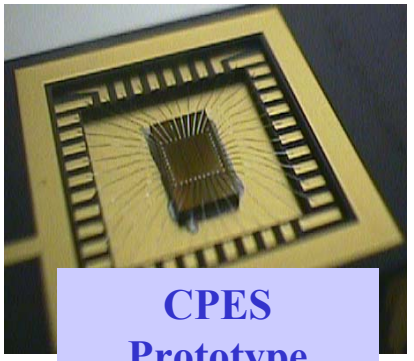
Lateral Power MOSFETs for High Frequency Operation



Today's Device VDMOS

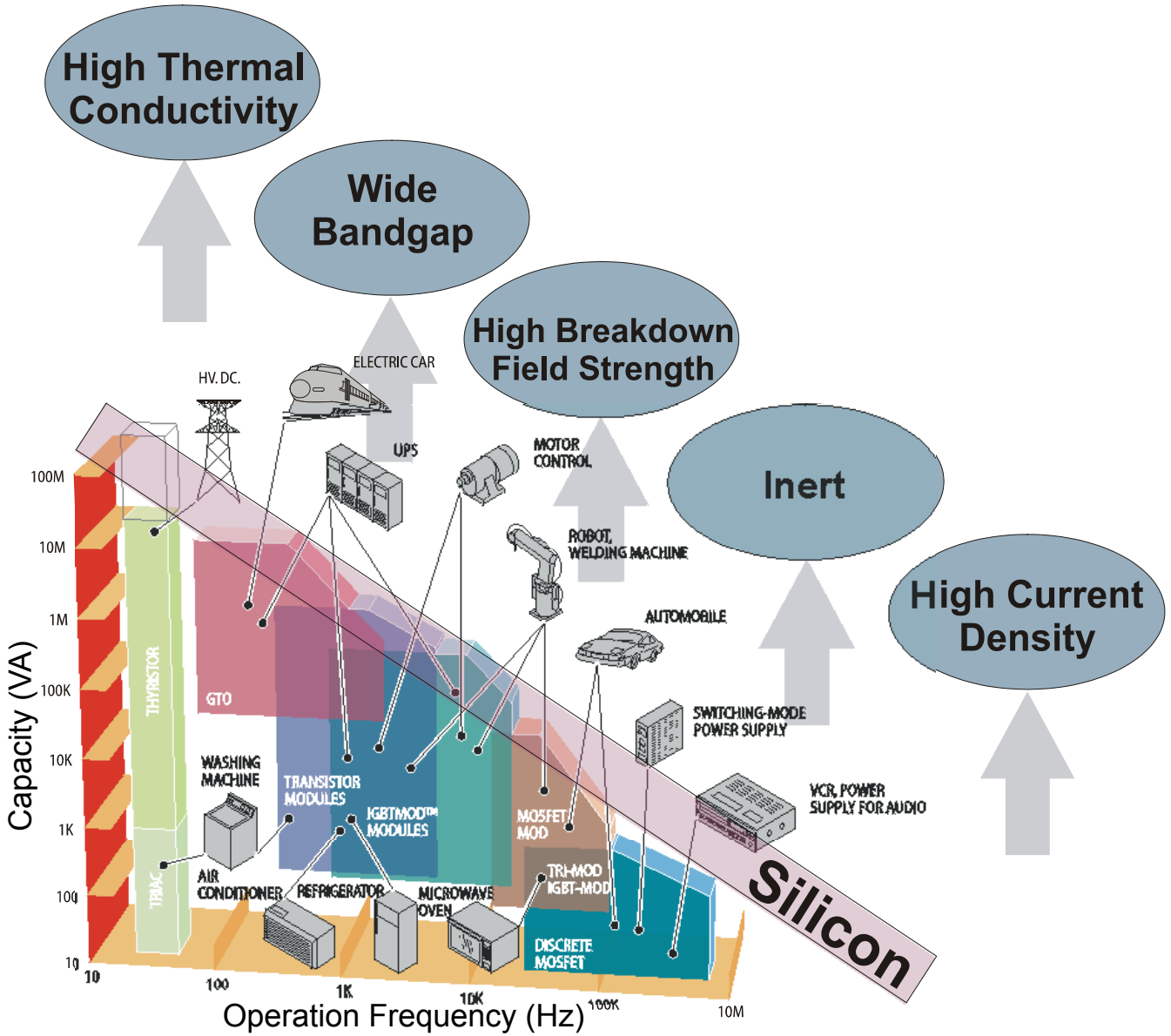


Future Device LDDMOS


CPES Prototype

	CPES Prototype Lateral MOS	Si4410 Trench MOS	IRF7805 VDMOS
Ron (mOhm)	6	16.5	10
Qg (nC)	3.2	25	29
FOM (mohm*nC)	24.5	566	389

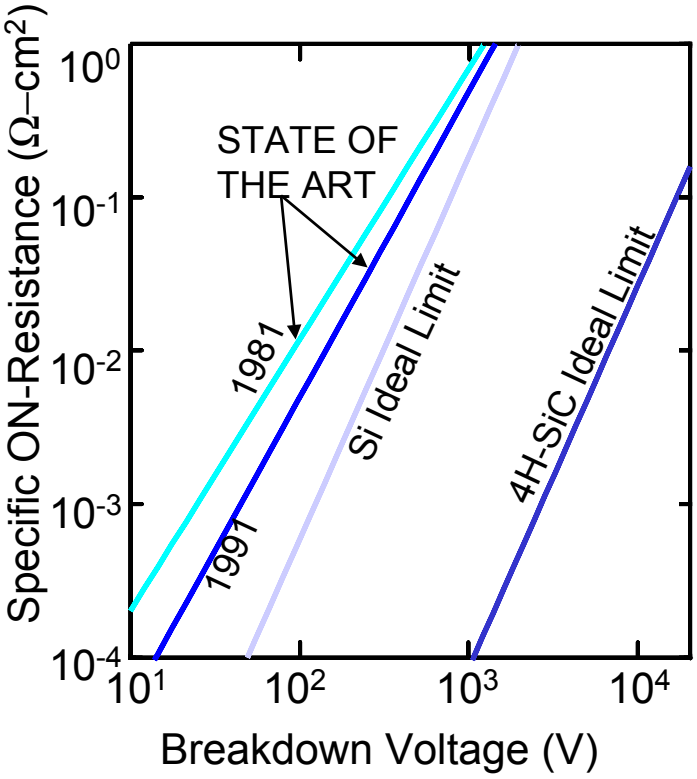
Why SiC?



Modified from an Application Note of Powerex, Inc. Youngwood, PA.

Motivations

Silicon high-voltage power devices are approaching theoretical performance limits imposed by material properties



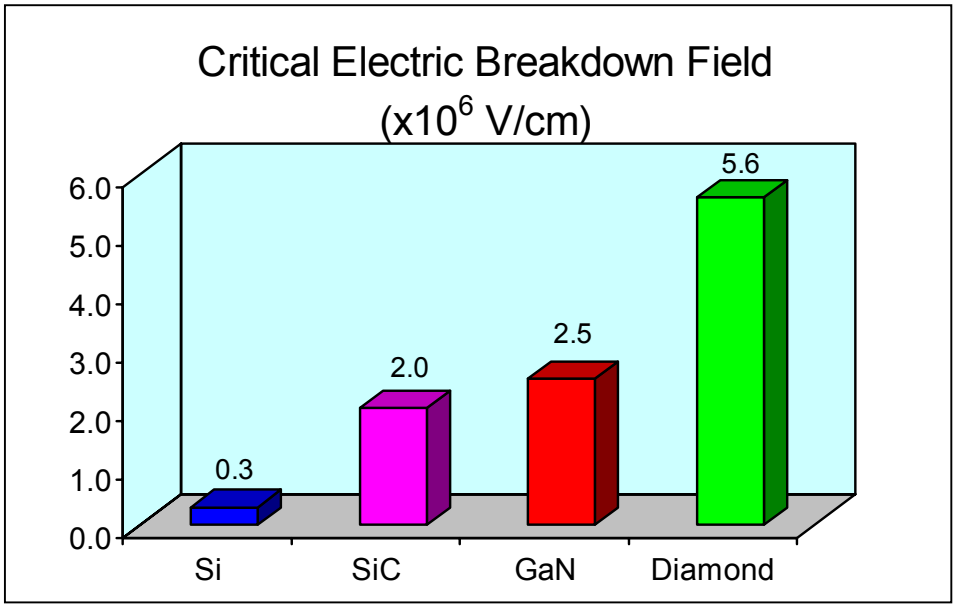
Power MOSFET

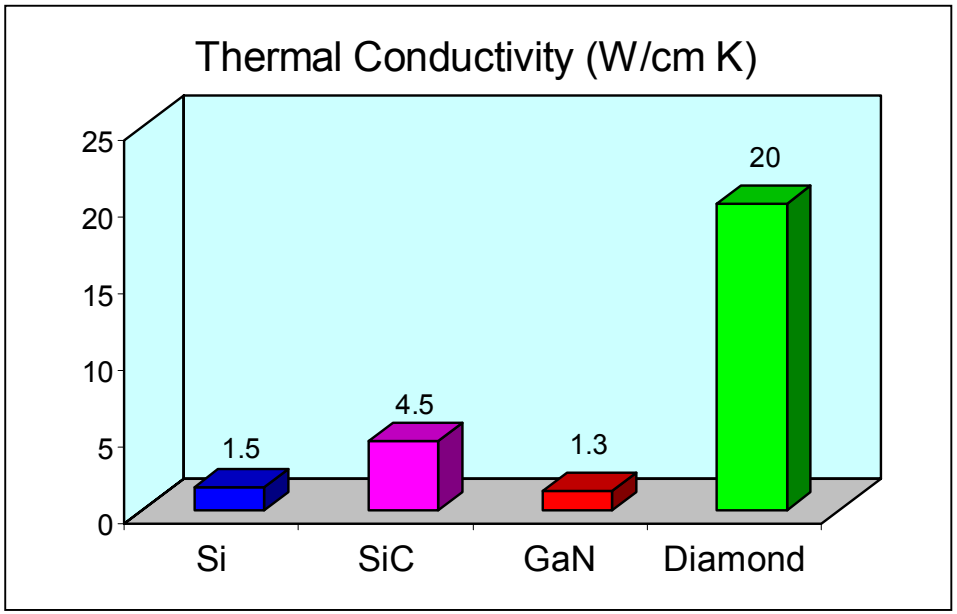
Example: 1000 V MOSFET

$$R_{on,sp}(\mathrm{Si}) = 5.93\times10^{-9}\,(BV)^{2.5}$$
$$= 187\ \mathrm{m\Omega\cdot cm^2}$$

$$R_{on,sp}(\mathrm{4H\text{-}SiC}) = 2.78\times10^{-12}\,(BV)^{2.5}$$
$$= 0.09\ \mathrm{m\Omega\cdot cm^2}$$

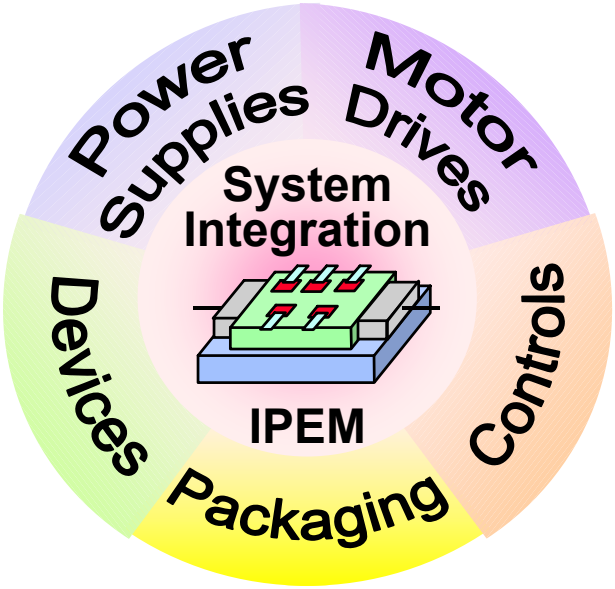
Material Properties





- High Critical Electric Field
  - **High blocking voltage capability**
  - **Low ON-Resistance**
  - **High power density**

- High Thermal Conductivity
  - **High power density**
  - **High integration density**

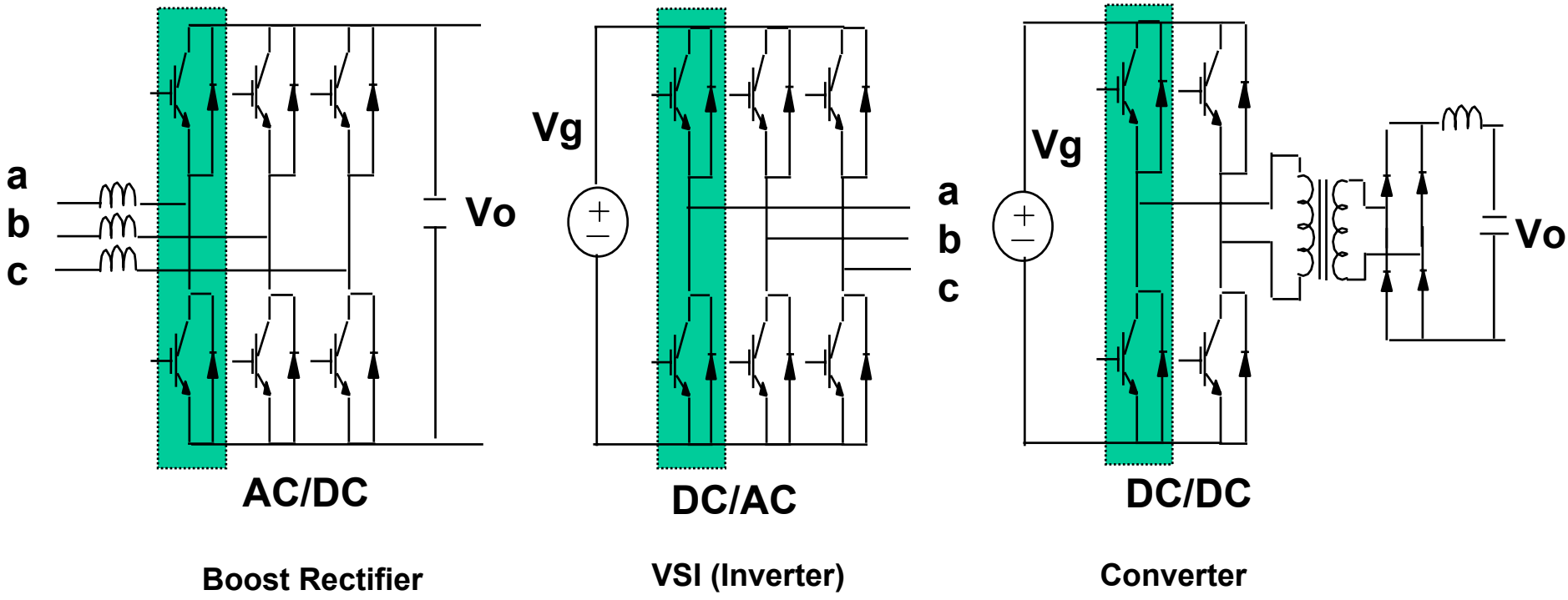


Integrated Packaging

Daan van Wyk

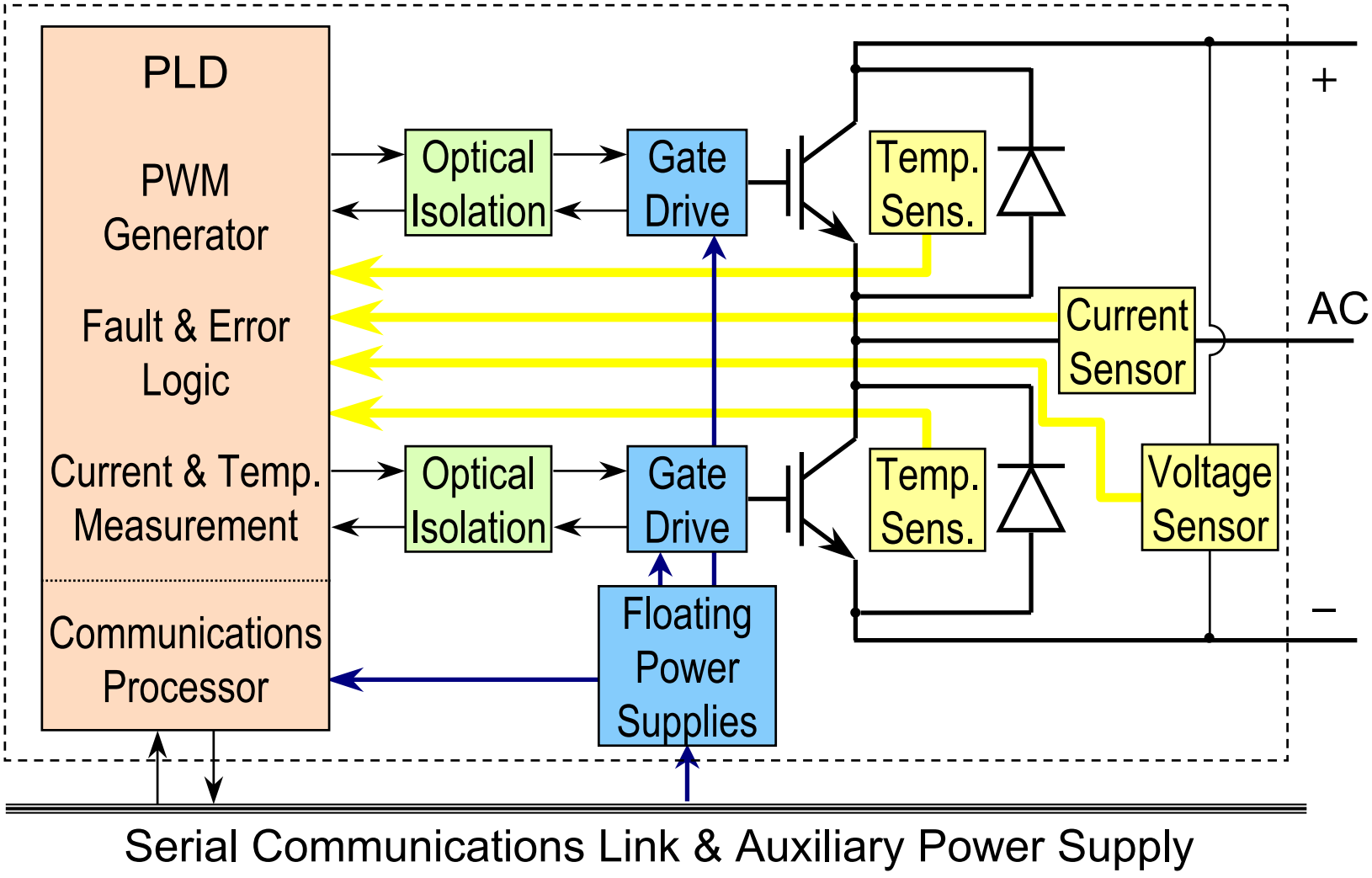
Virginia Tec
IP Leader

Common Switching Cells for Power Converters



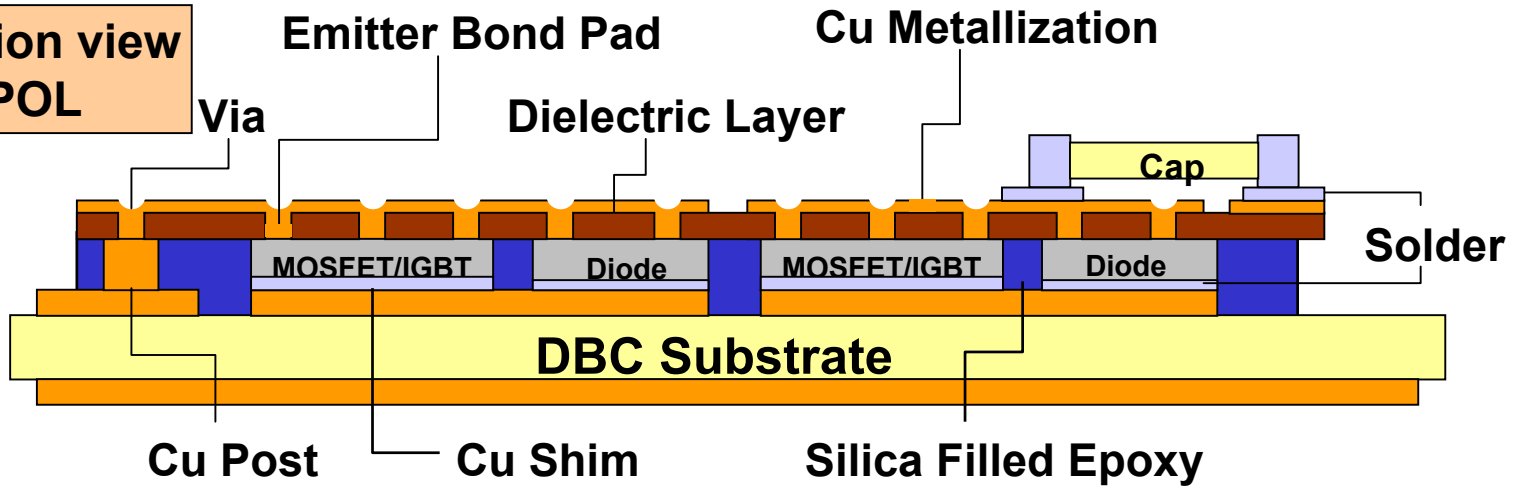
One phase leg - a common switching cell applicable to a wide range of applications

“Intelligent” Half-Bridge IPEM

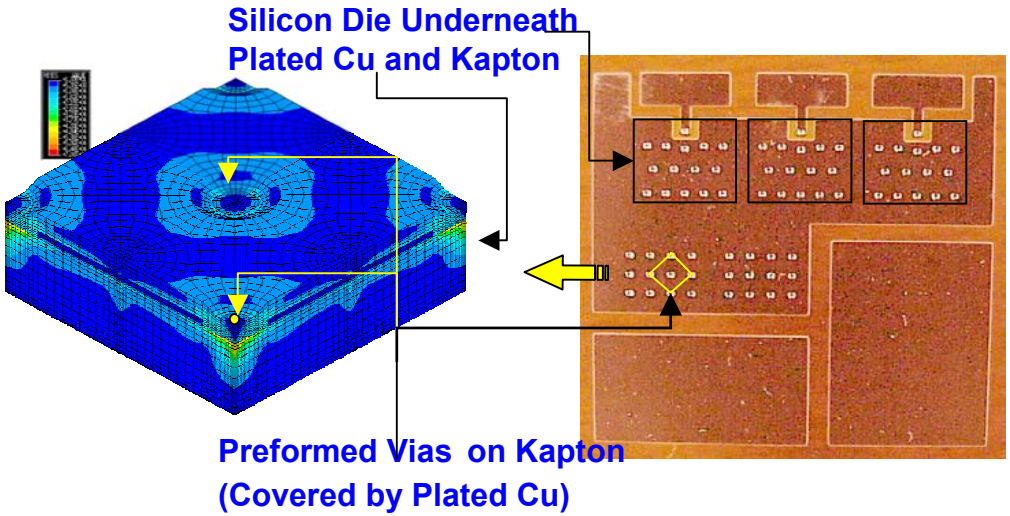


Transfer of GE POL Technology to CPES

Cross-section view of GE POL



Modeling of Thermo-mechanical Stresses at Vias

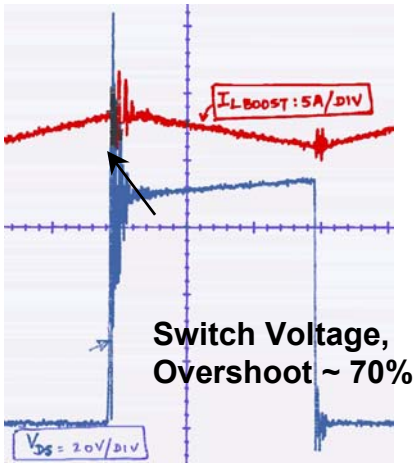


Module Fabrication

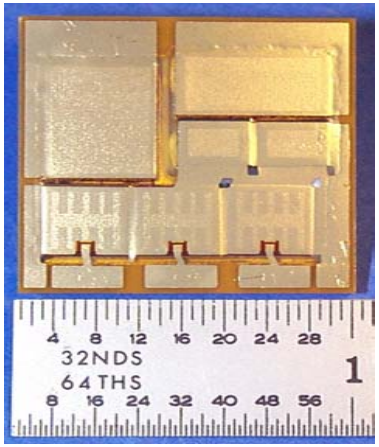
Demonstration of Power Overlay Packaging Technology

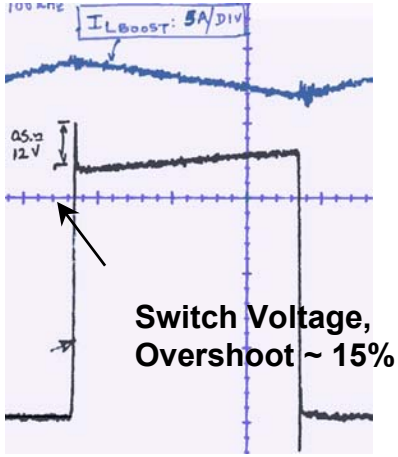
GE Corporate R&D

Baseline Power Module
Rating : 200V, 150A; Size : 2" * 2" * 0.3"



Power Overlay Module
Rating : 200V, 150A; Size : 1" * 1" * 0.1"

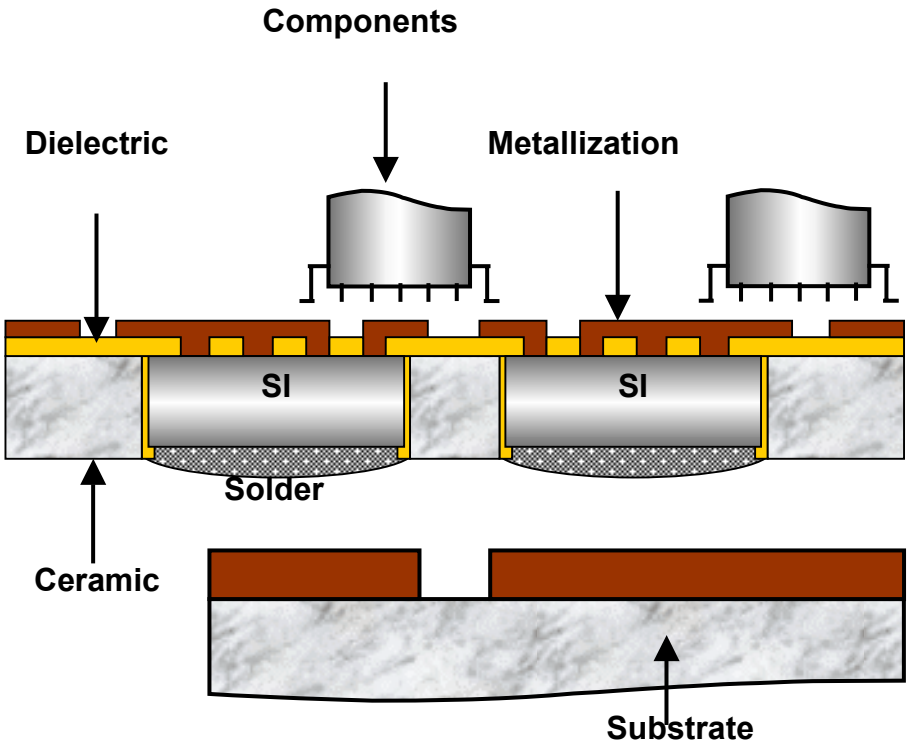


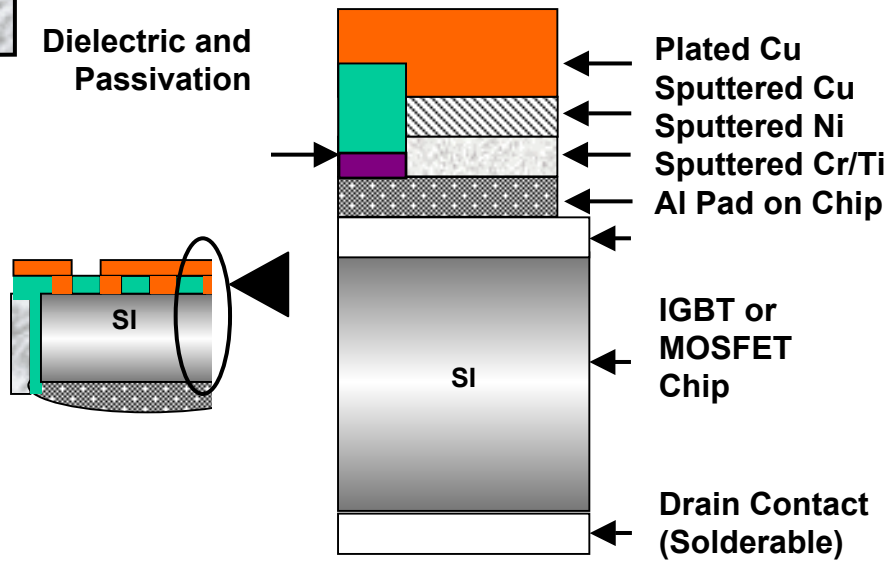


Aerospace Application : Battery Power Converter

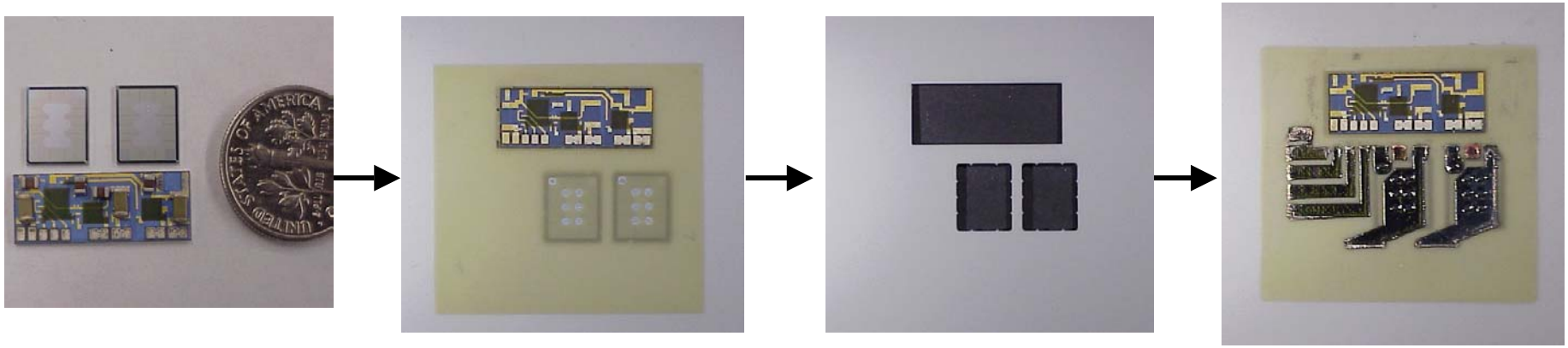
- Power Levels tested to 1500W
- Module Power Density Increased by at least 3x
- Improved Electrical switching performance
  - No wire bonds
  - Substantially reduced overshoots, no ringing
  - No R-C snubbers required
  - Reduced switching losses
- Improved thermal performance
  - Fewer thermal interfaces

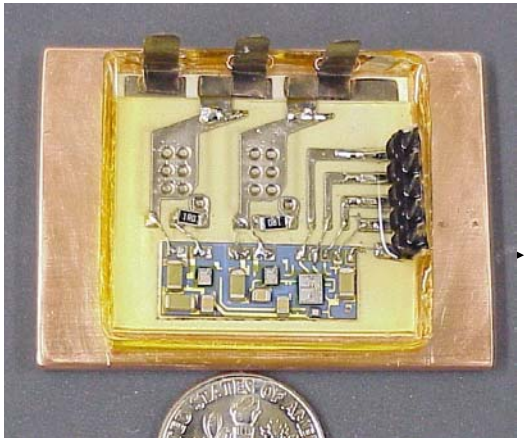
Embedded Power – Structure, Contacts, and Isolation

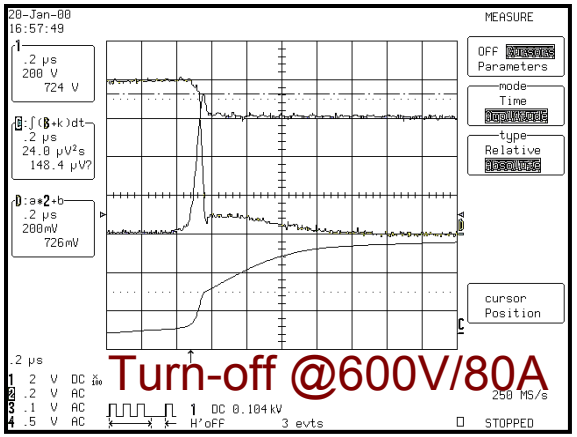




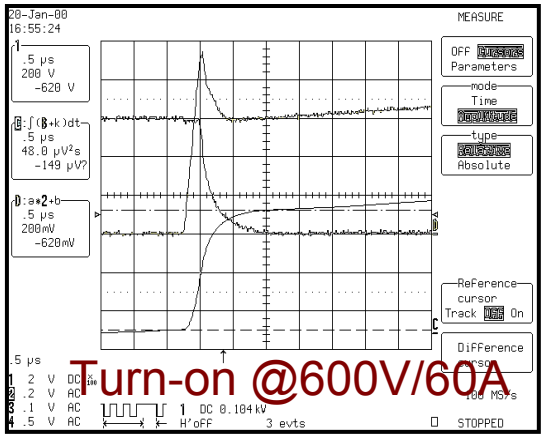
Embedded Power – Prototype Fabrication and Test Results







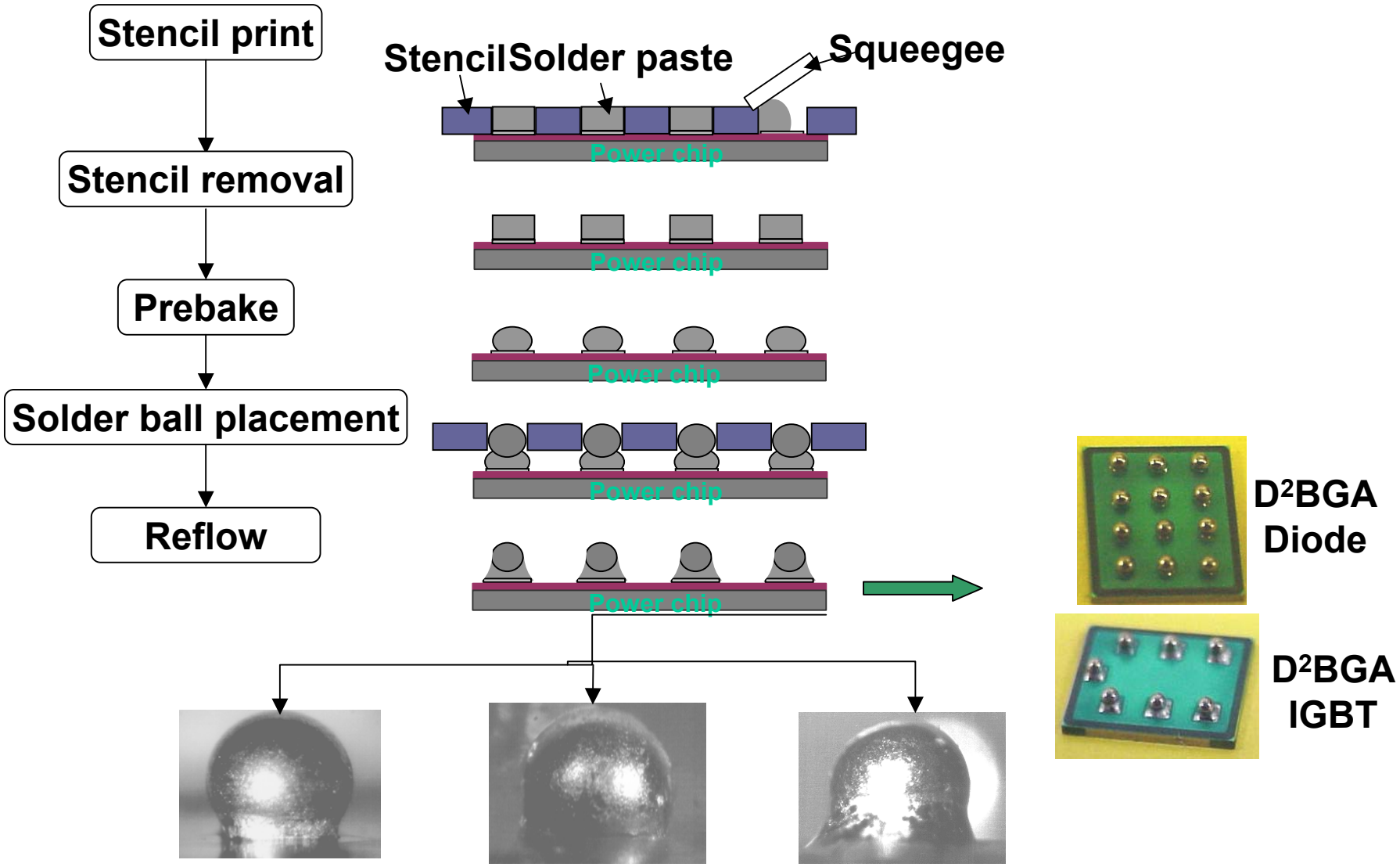
Turn-off @600V/80A



Turn-on @600V/60A

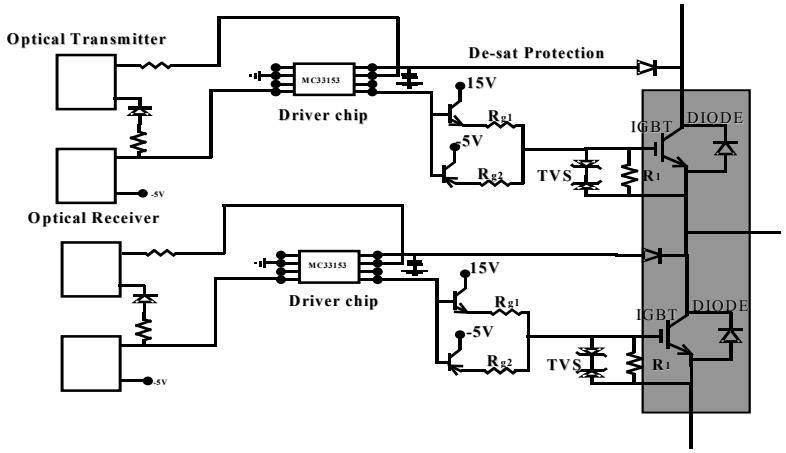
Power switching characteristics of prototype module

Die-Dimensional Ball-Grid-Array (D2BGA) Packaging of Power Devices



Assembly of D2BGA Devices in Power Modules (Flip-Chip on Flex Modules)

+



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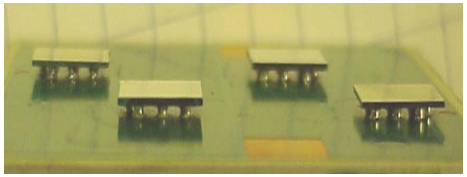

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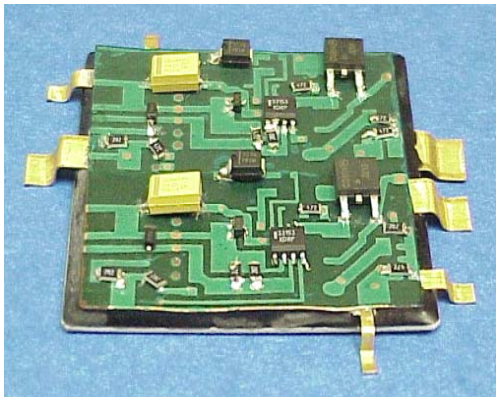
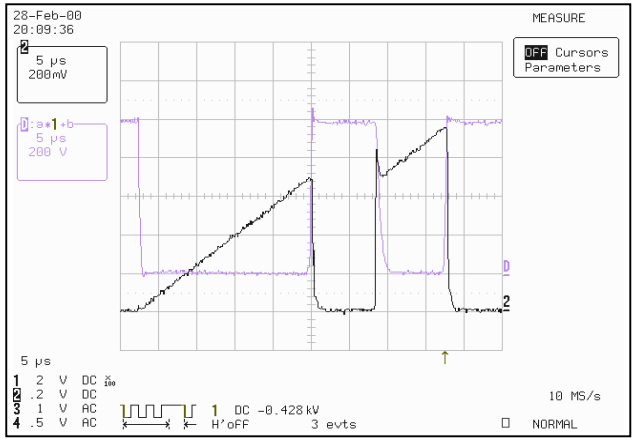
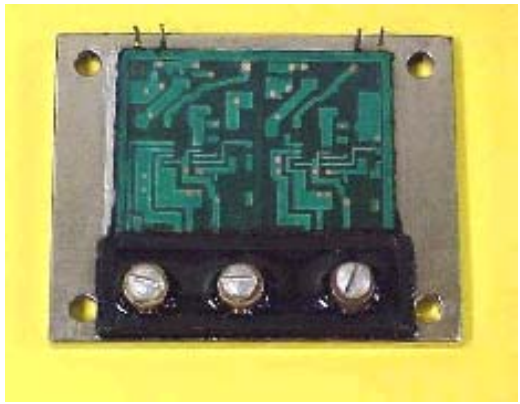
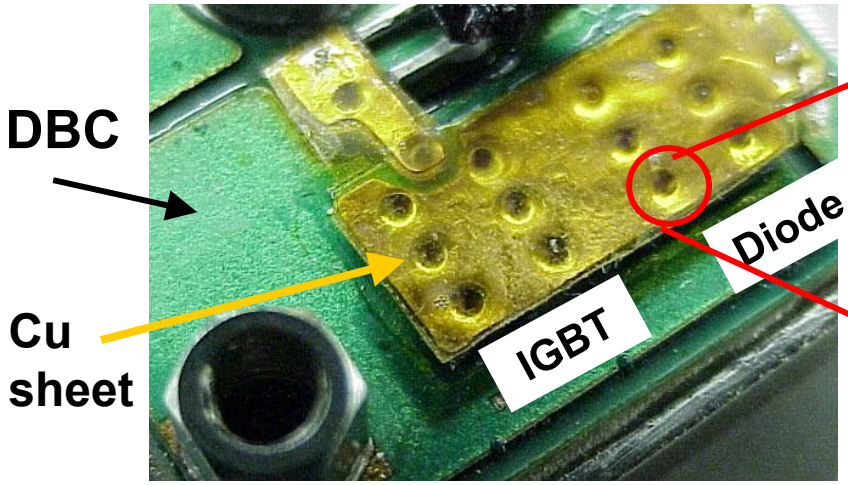


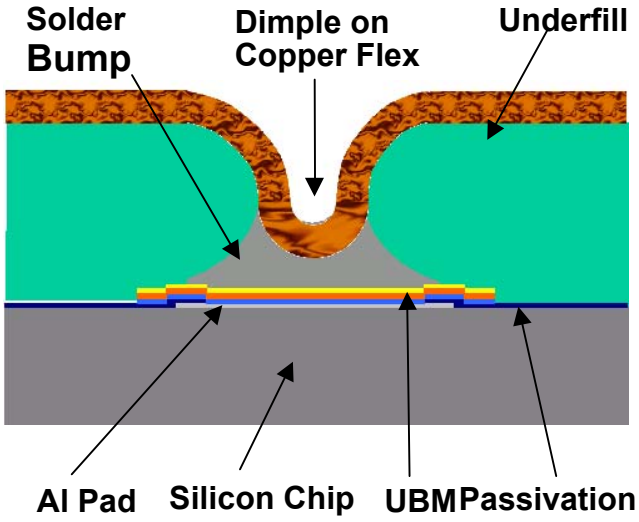


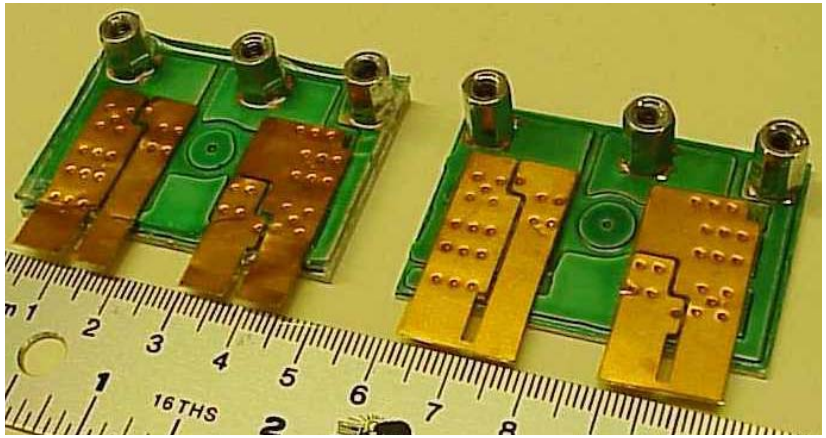


Switching waveforms Tested up to 800V/90A

Dimple-Array Interconnected Power Modules

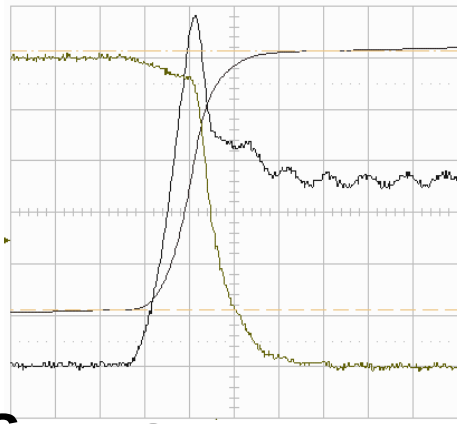




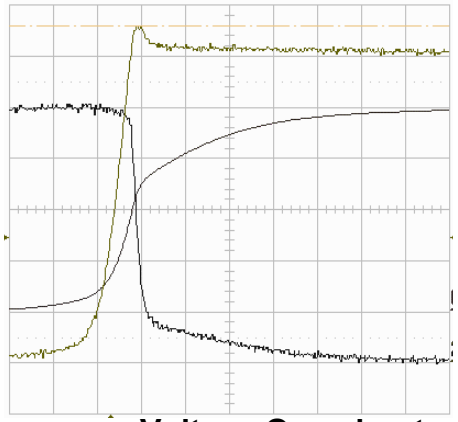


Power Switching Modules

Turn-on I-V curve



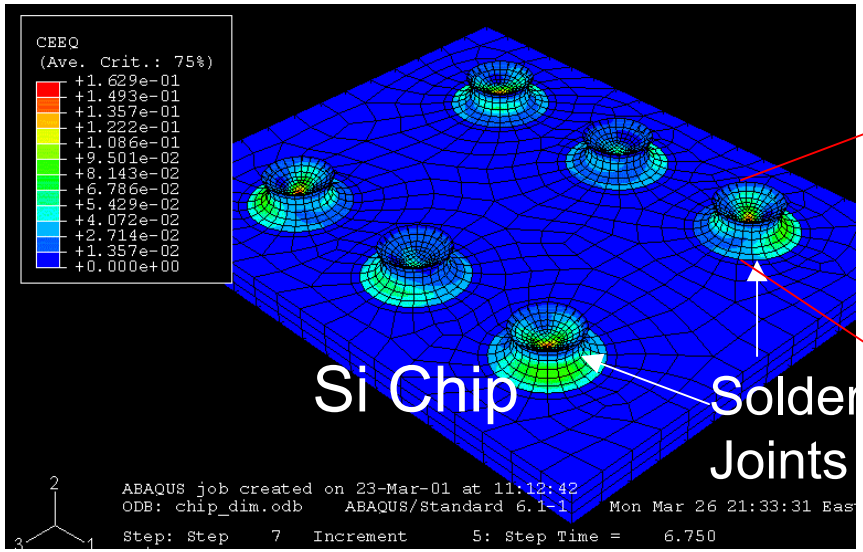
Turn-off I-V curve

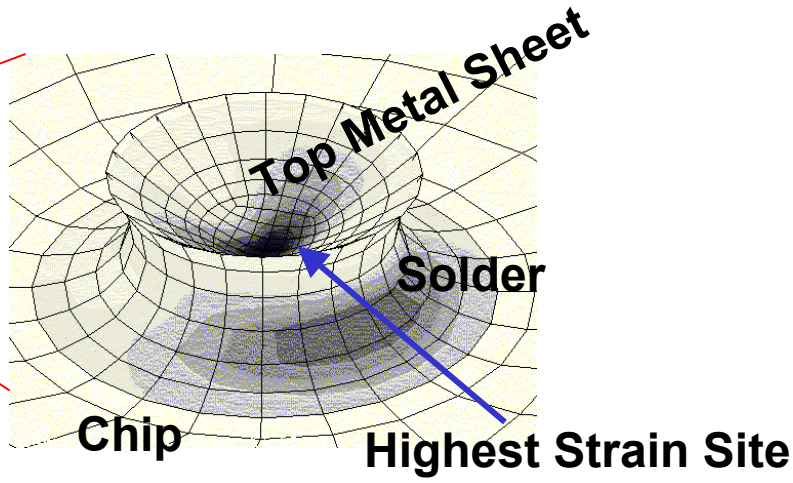


@ 600V, 50A

Voltage Overshoot ~ 50-60V

Modeling of Thermo-Mechanical Stresses of Dimple-Array Interconnection



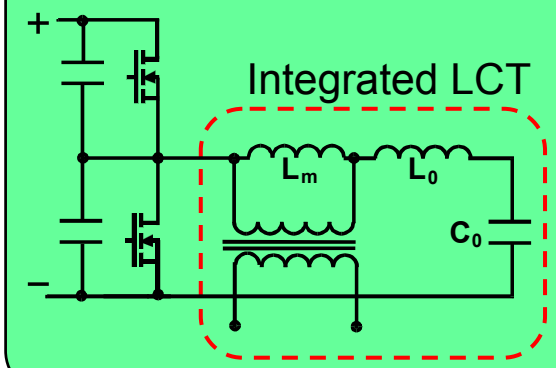


Comparing with a conventional solder joint of the same volume, potential advantages of dimpled solder joints are:

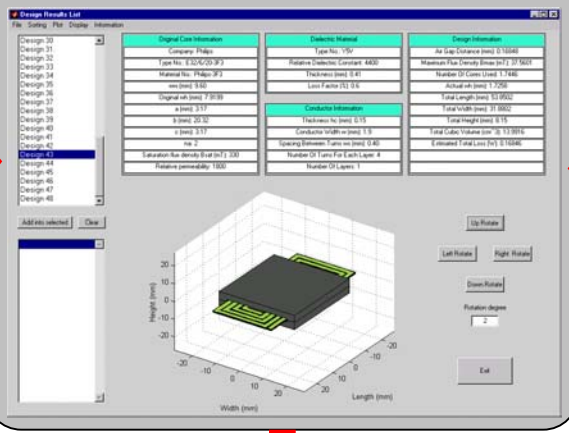
- **Lower overall inelastic strains (by a factor of 2);**
- **Relocation of the highest strain site away from the chip-to-solder interface;**
- **Better thermal performance from shortened heat path in the center.**

Integration of Power Passives

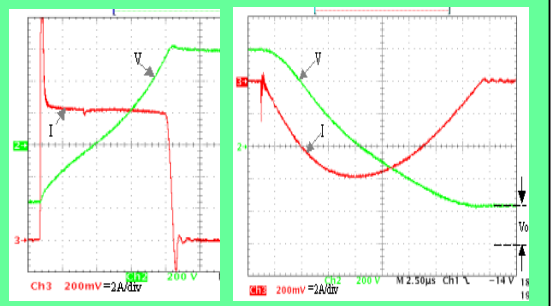
Circuit



EM/Thermal Design

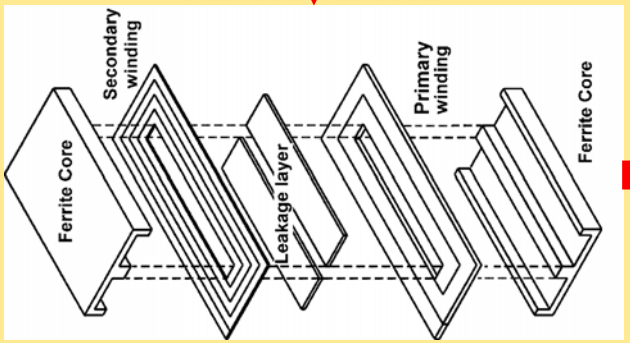


Materials



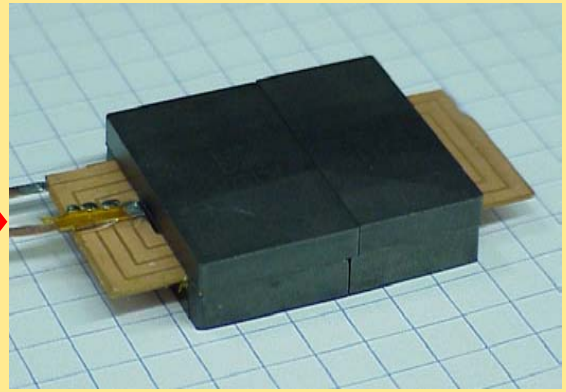
Characterization

Current Construction Processes



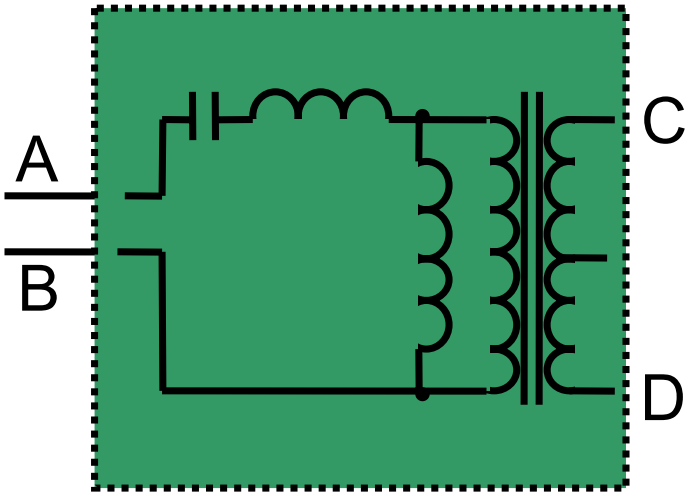
Integrated LCT

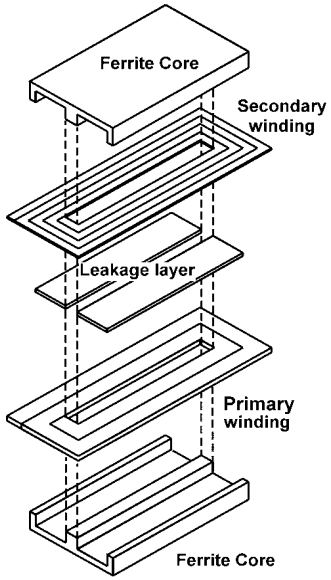
- Materials Deposition
- Photo Lithography
- Wet Chemistry
- Encapsulation
- Laser Machining

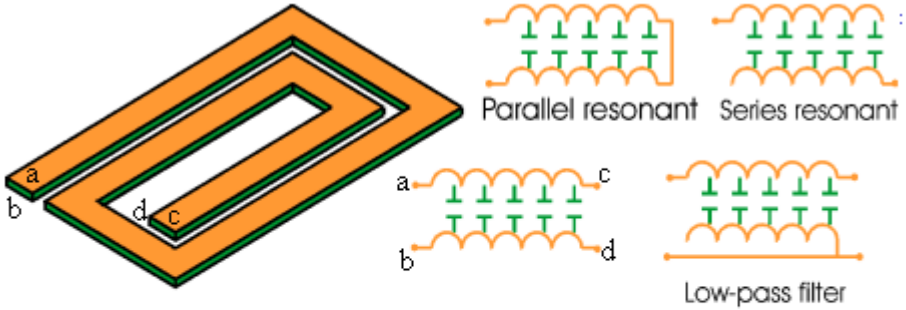


Integrated LC

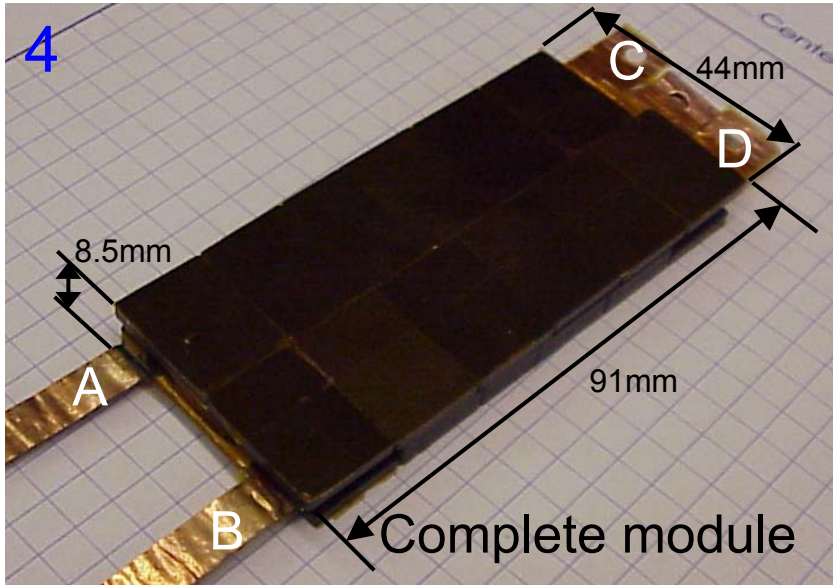
Integration of Power Passives: Generic Structure for L+C+T





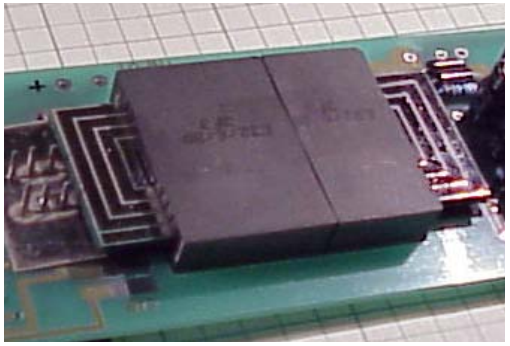


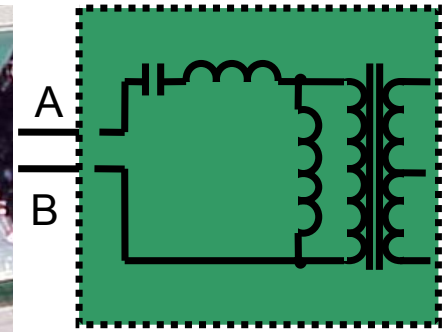
- Consists of a number of layers
- Planar LC resonant structure
  - Two planar windings separated by dielectric material
  - Transmission-line structure - multiple resonance points
  - Terminal characteristics changeable

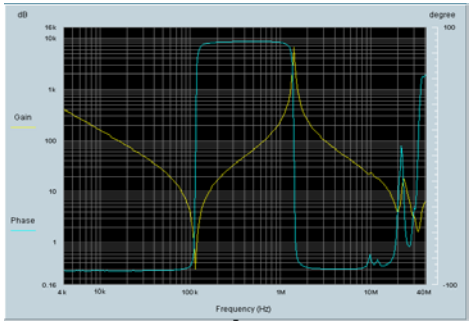


Examples of Integrated Power Passives

120 W Half Bridge LLC Resonant Converter





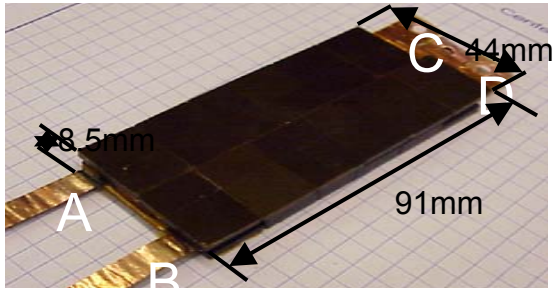


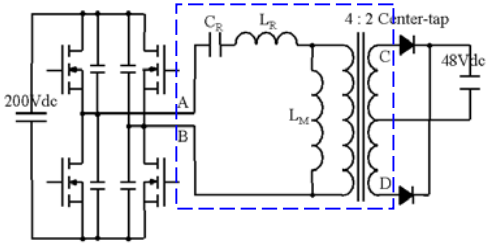
f_0=330 kHz

Po=120 W

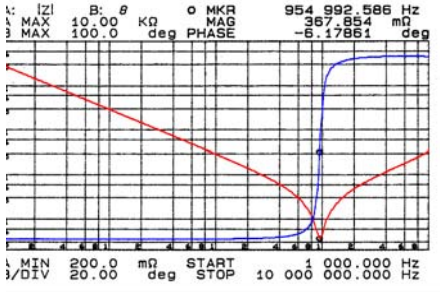
108 W/in^3

500 W Full Bridge LLC Resonant Converter





Full bridge series resonant with no-load ZVS (using magnetizing current)

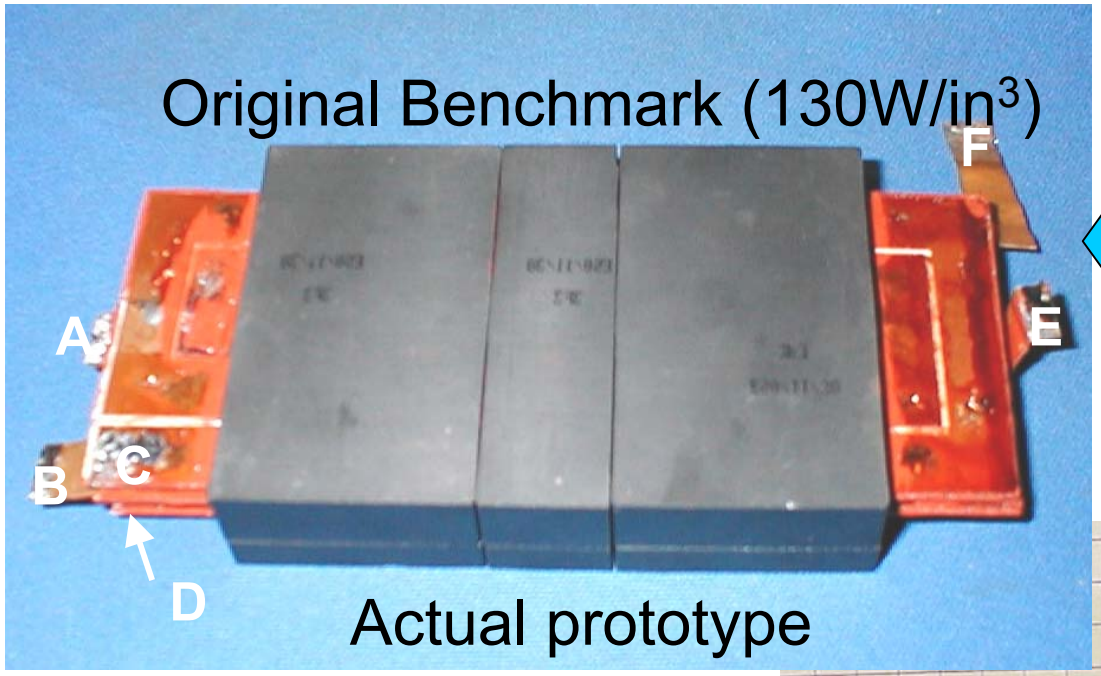


f_0=1 MHz

Po=500 W

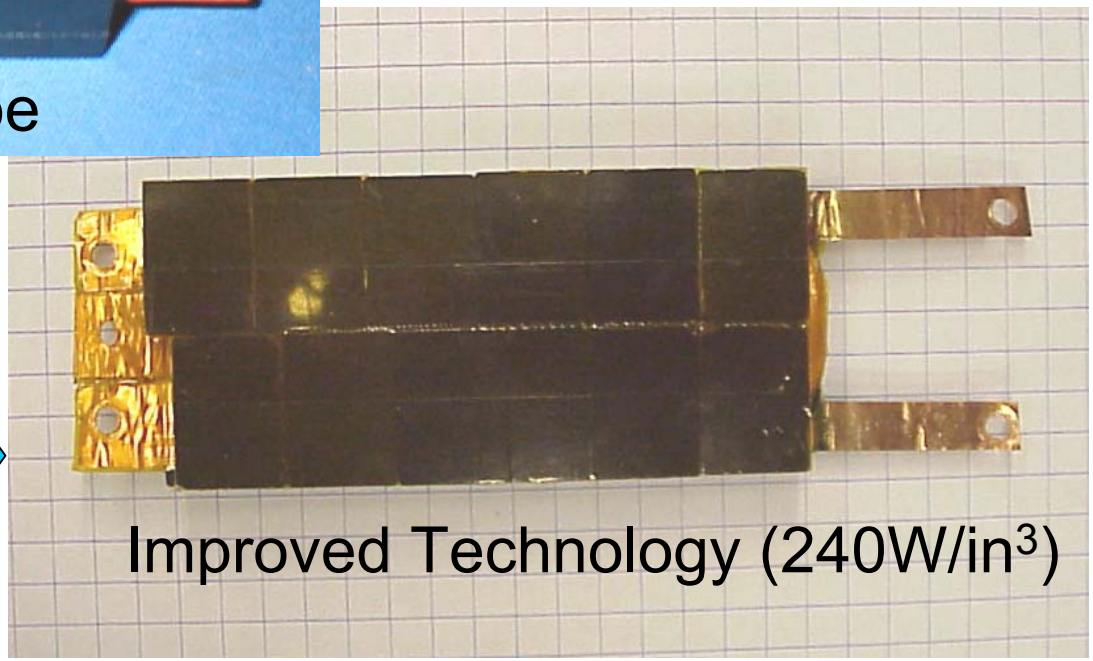
240 W/in^3

Example Prototypes

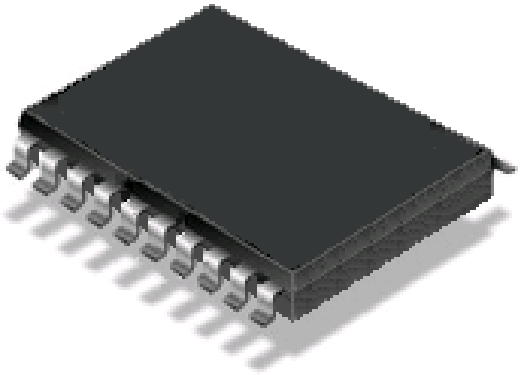


First presented:
IAS ’99
1kW, 1MHz

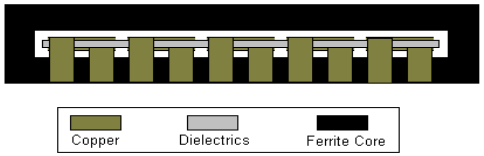
First presented:
APEC ’01
500W, 1MHz



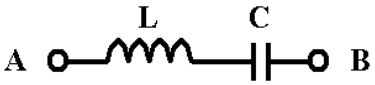
In Line Passive Packaging: Concept and Different Possibilities

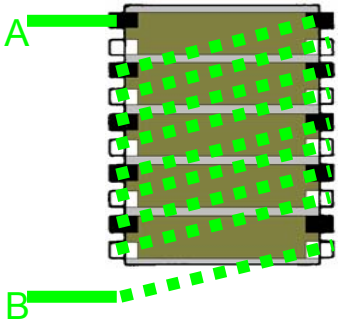


(a) Outlook

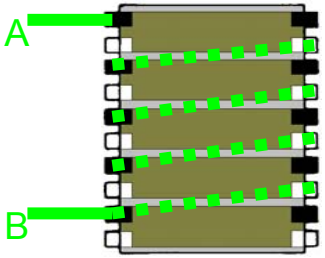


(b) Front view

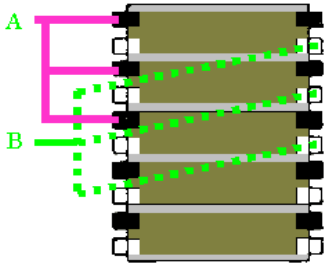




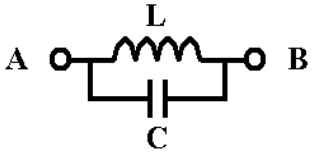
$$L = N^2 L_{unit}$$
$$C = NC_{unit}$$

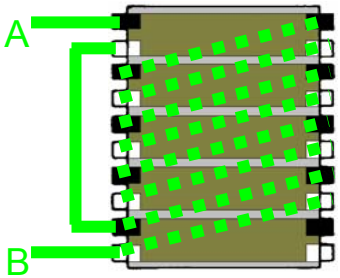


$$L = N^2 L_{unit}$$
$$C = C_{unit} / N$$

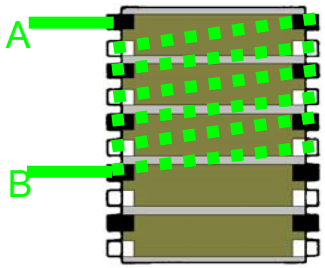


$$L = L_{unit} / N$$
$$C = NC_{unit}$$

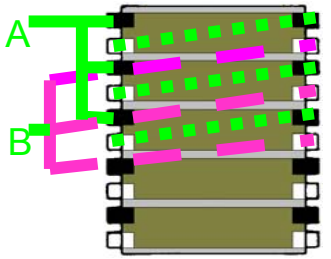




$$L = (2N)^2 L_{unit}$$
$$C = NC_{unit} / 4$$

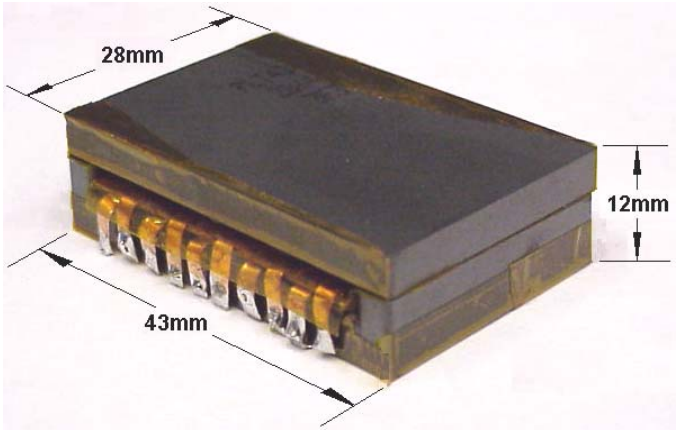


$$L = (2N)^2 L_{unit}$$
$$C = C_{unit} / 4N$$

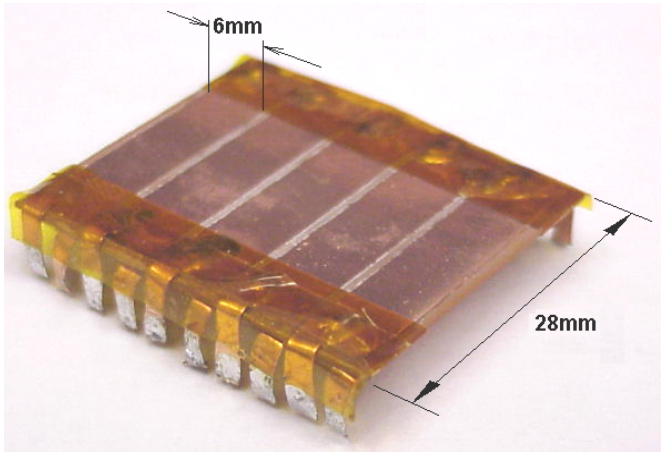


$$L = L_{unit} / N$$
$$C = NC_{unit} / 4$$

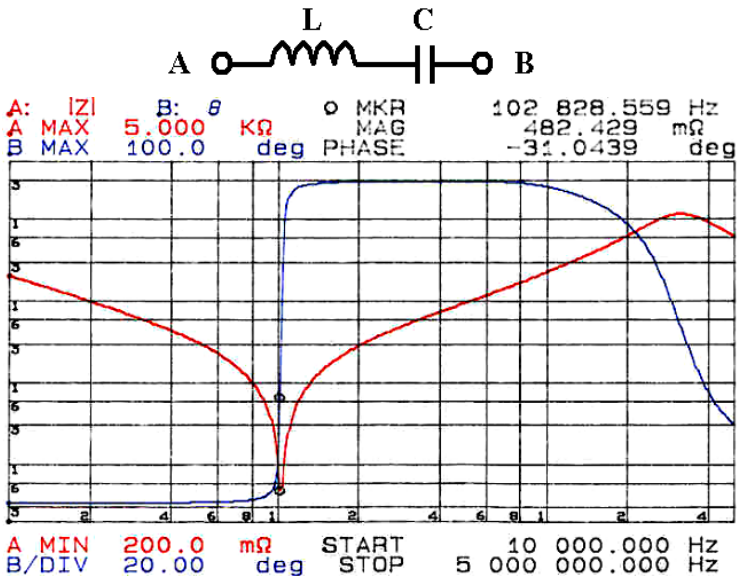
In Line Passive Packaging: Prototype and Z(f)

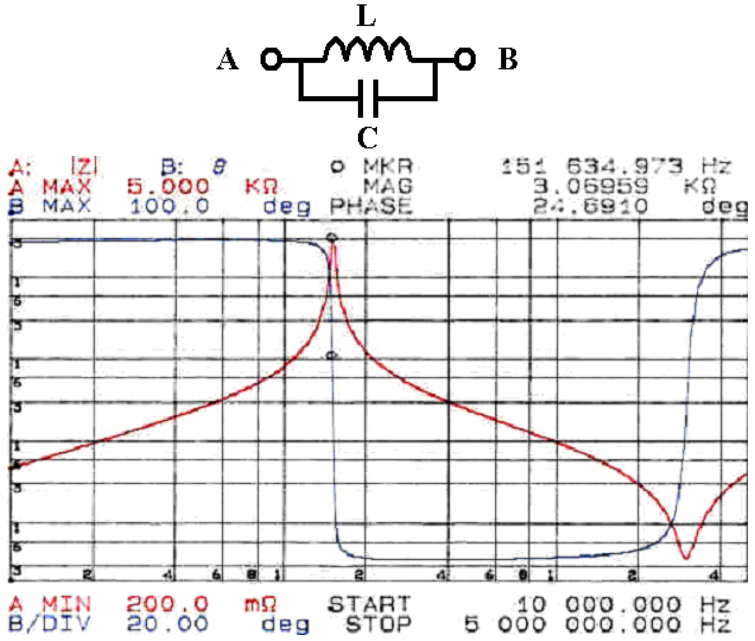


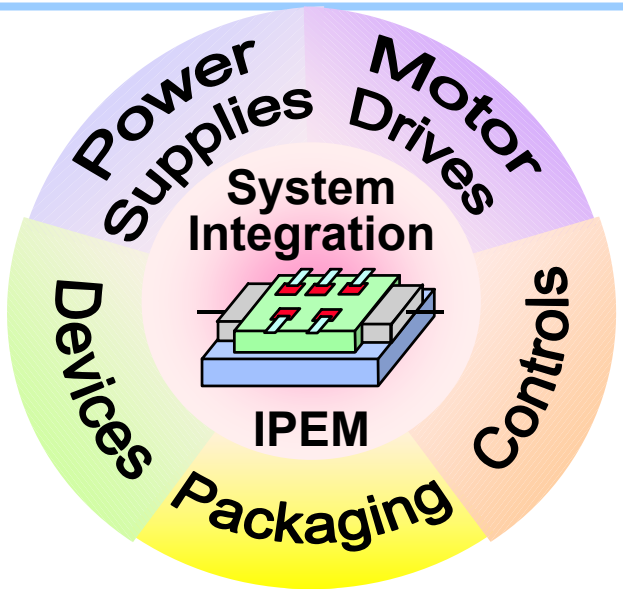
(a) Overview



(b) Inside view





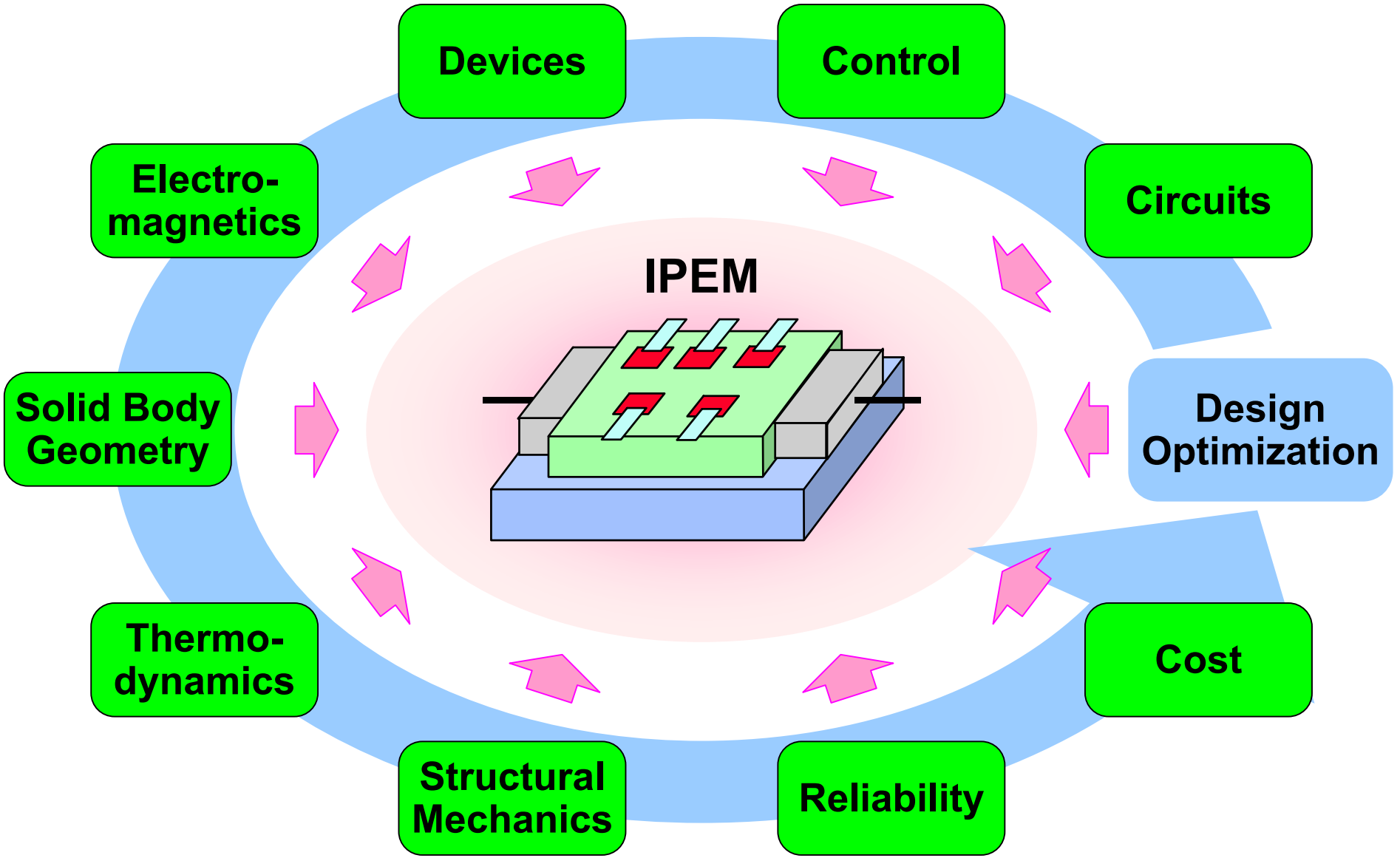


Integrated Power Electronics Module Synthesis (IPEMS)

Dushan Boroyevich

Virginia Tech
IPEMS Leader

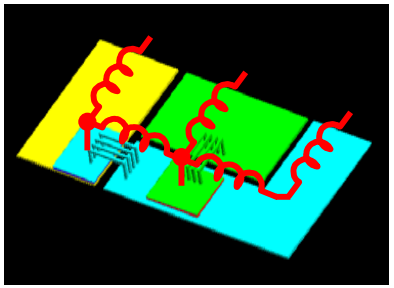
IPEM Synthesis



3D Solid Body Geometry Electrical and Thermal Modeling

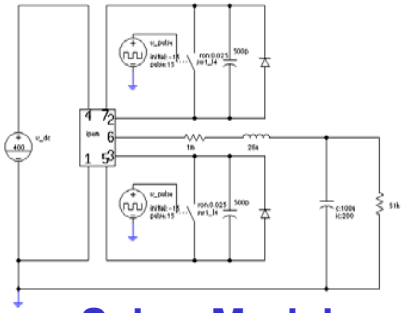
Goal: Develop 3D solid-body geometry-based thermal and electrical models of IPEMs to enable integrated analysis

Parasitic Extraction



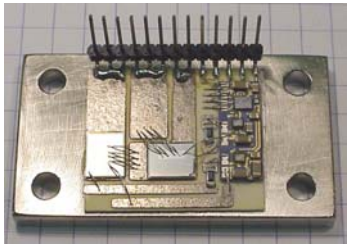
Maxwell Q3D Model

Electrical Simulation



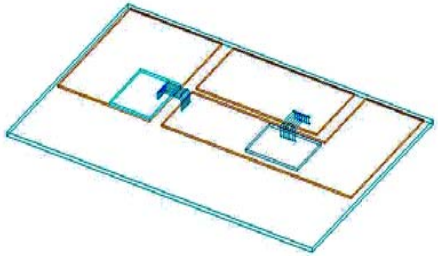
Saber Model

Experiment



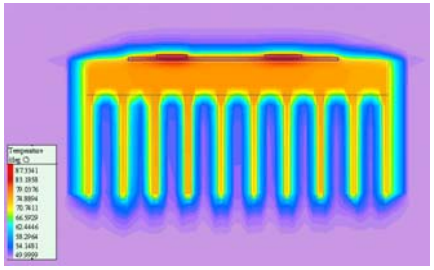
1st Gen. DPS IPEM

Mechanical Layout

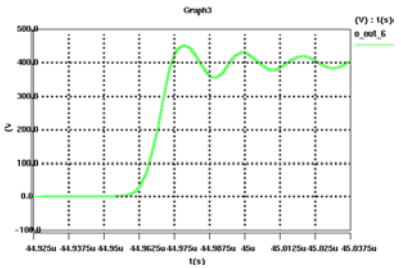


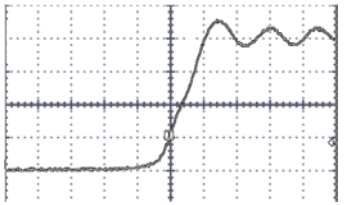
I-DEAS Model

Thermal Analysis



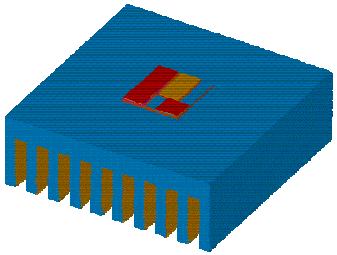
FLOTHERM Model

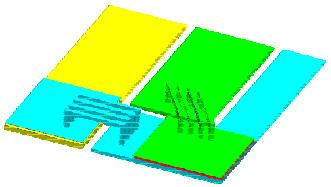


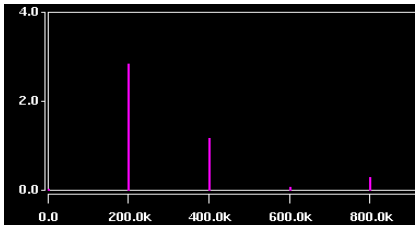


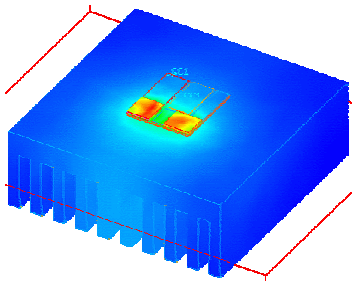
Voltage waveform of the bottom switch at turn off

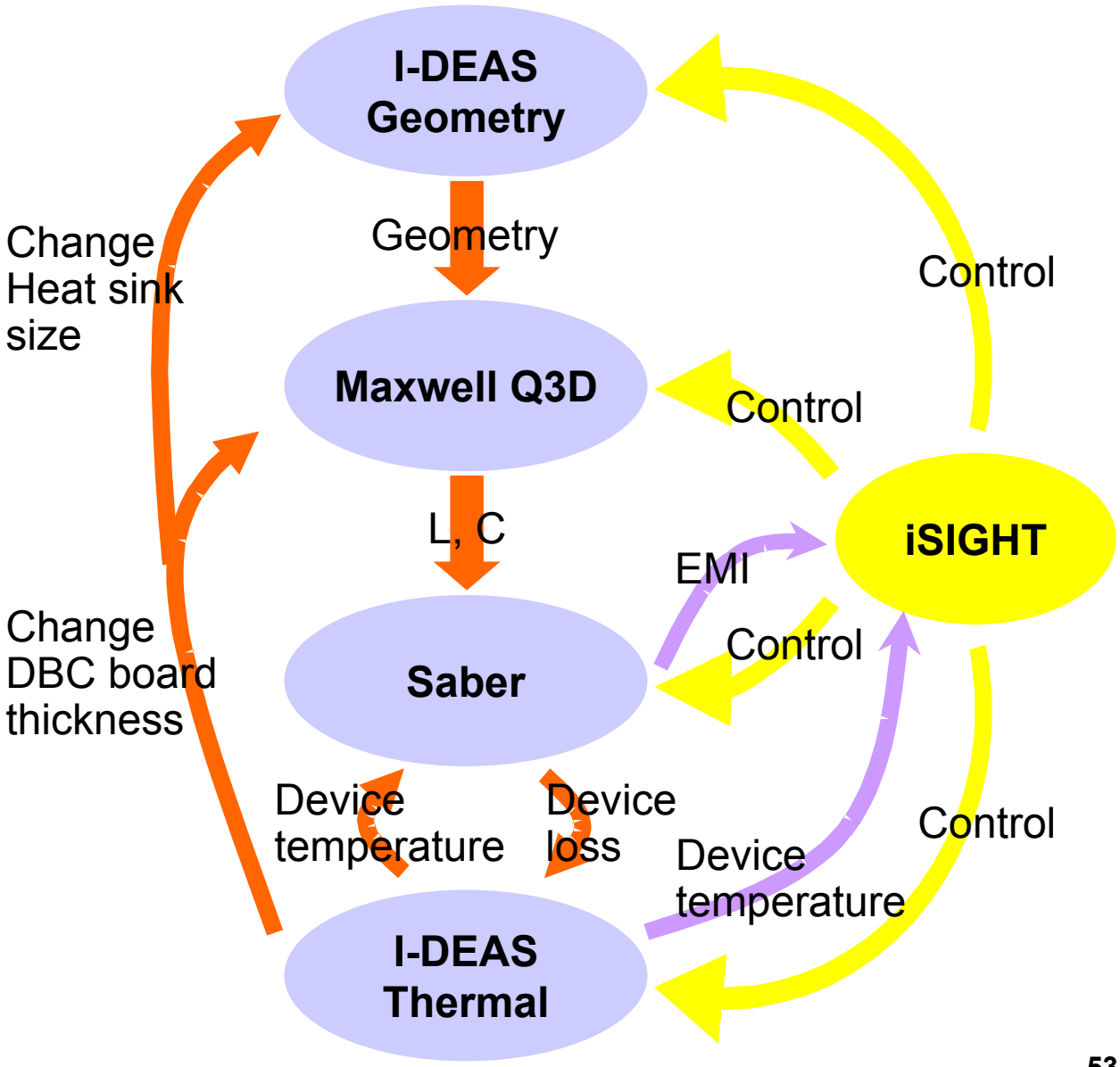
Design Process Control





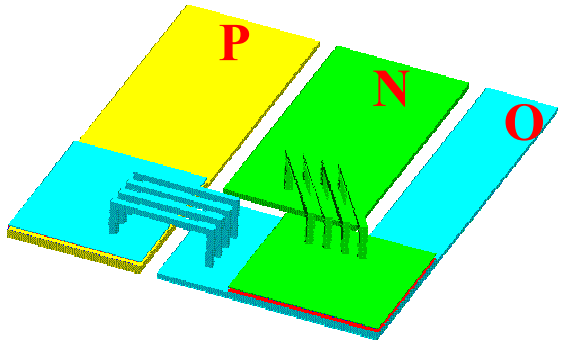






Electrical Lumped Parameter
Extraction and Electrical Circuit Modeling

IPEM Model in MAXWELL Q3D

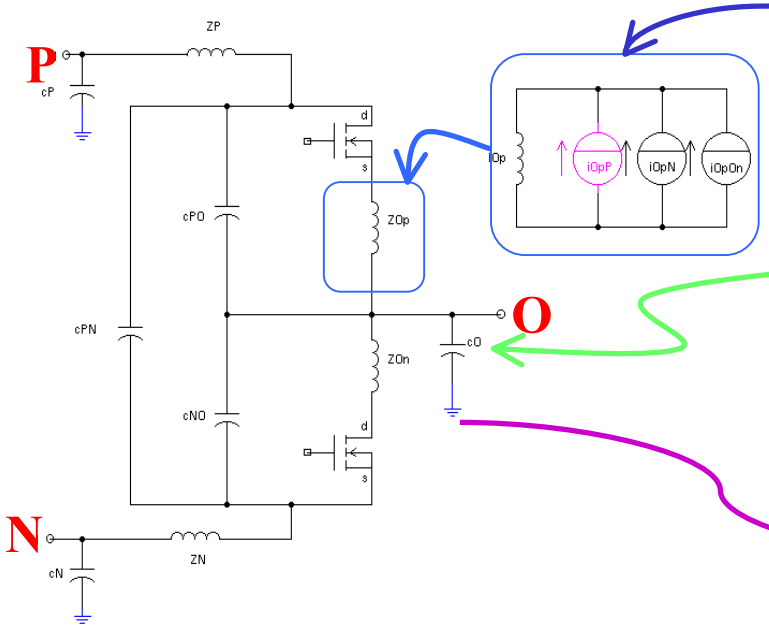


Parasitic Inductance Matrix

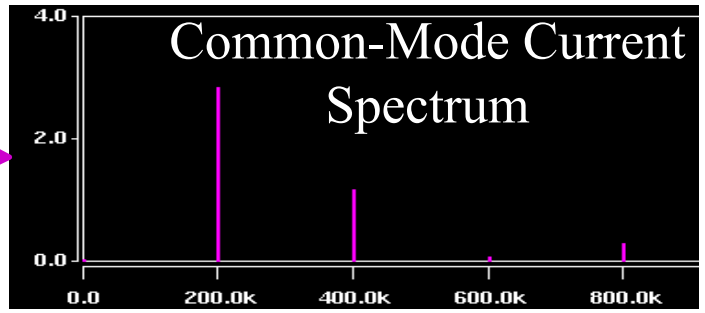
(nH)	P	N	O_P	O_N
P	5.7	2.6	-1.4	-1.4
N	2.6	8.9	-3.1	-3.5
O_P	-1.4	-3.1	11.8	8.1
O_N	-1.4	-3.5	8.1	8.0

Parasitic Capacitance Matrix

(pF)	P	N	O
P	3.54	0.13	2.93
N	0.13	2.37	3.30
O	2.93	3.30	3.40

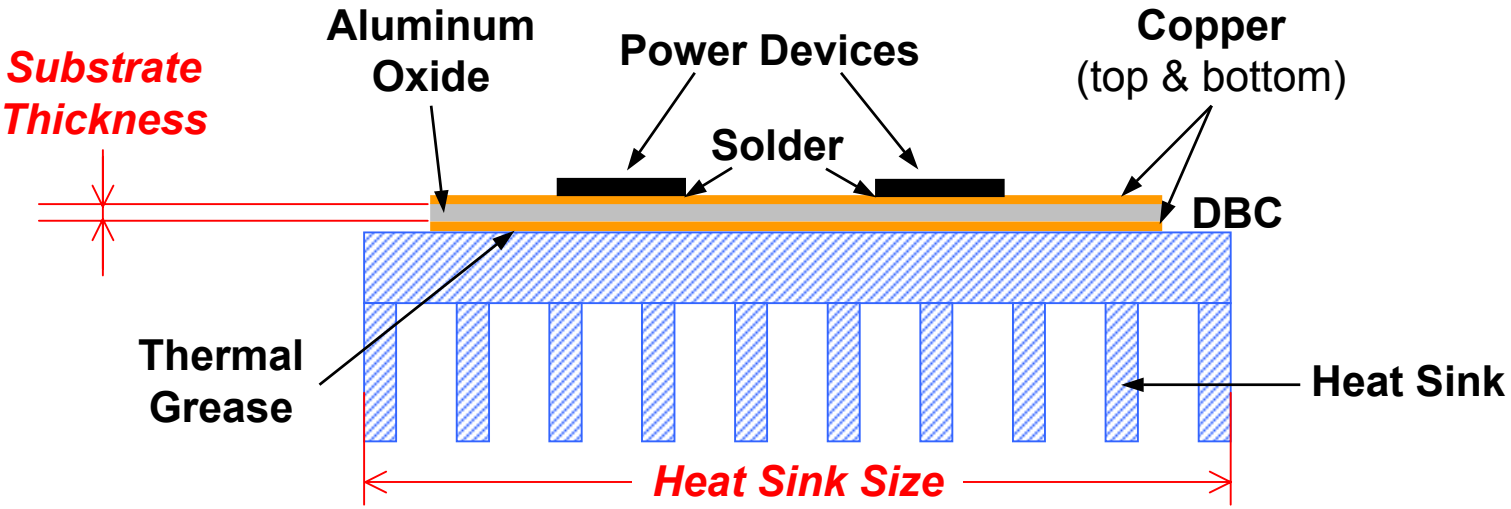


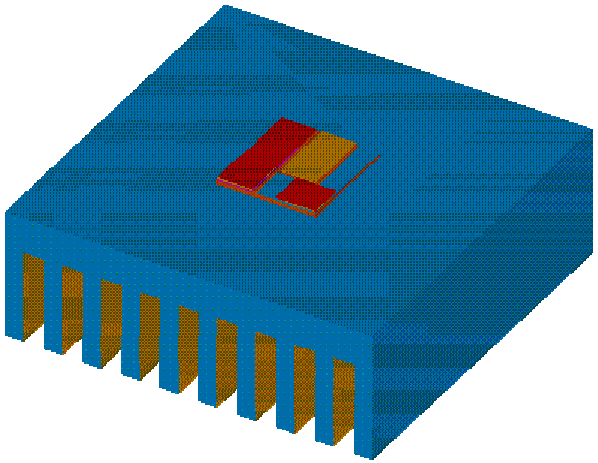
IPEM Model in Saber



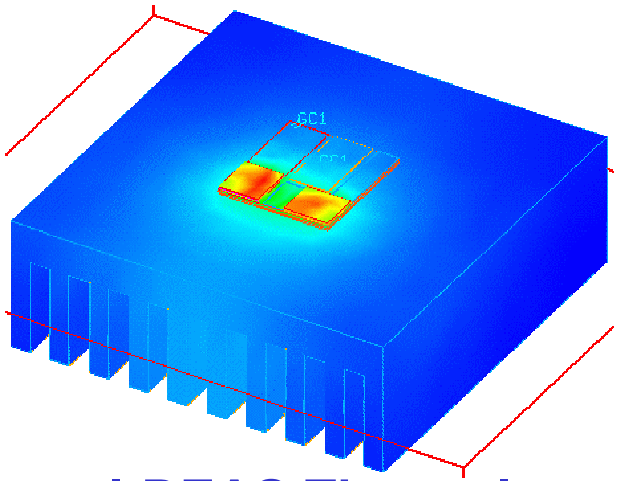
3D Solid Body Geometry and Finite Element Thermal Modeling

Example: Parametric study of junction temperature and common mode EMI as a function of the substrate thickness and heat-sink size.



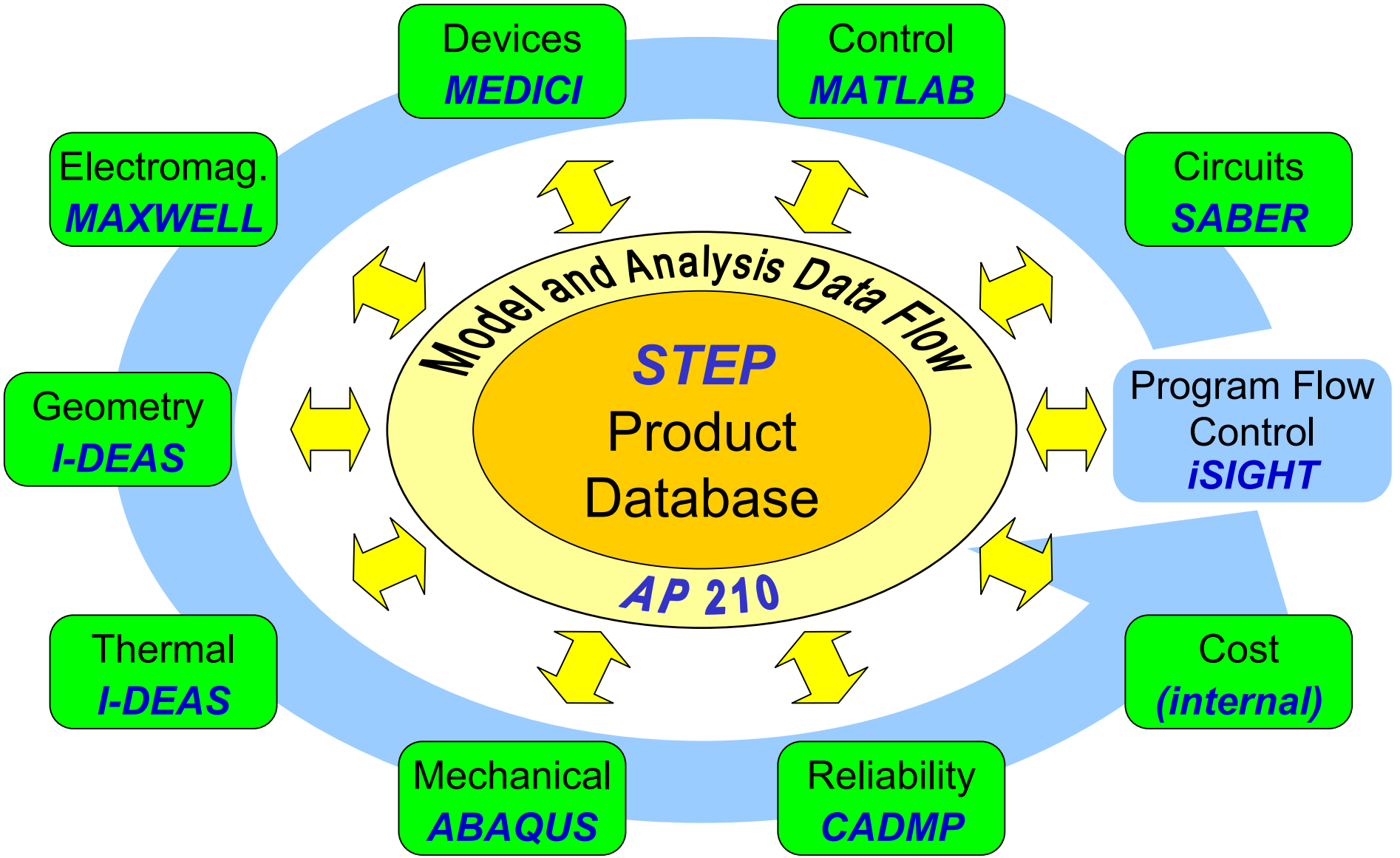


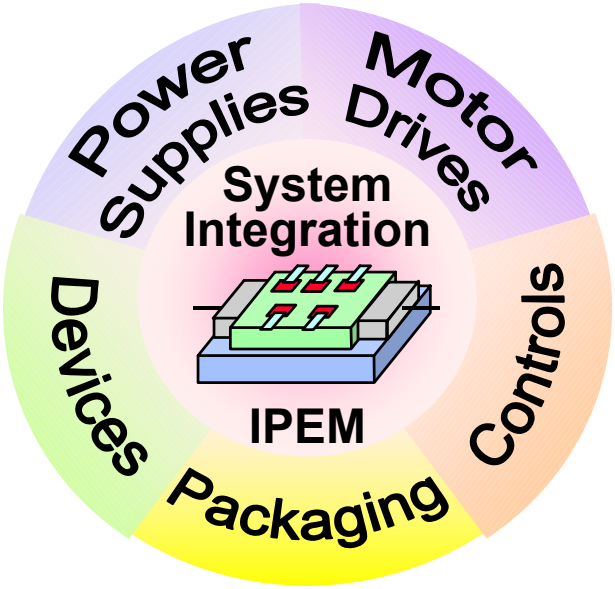
I-DEAS Geometry



I-DEAS Thermal

Integration of Software Analysis and Design Tools





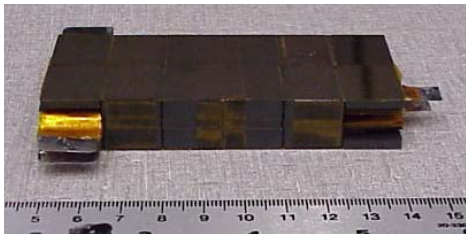
Distributed Power Systems (DPS)

Fred C. Lee

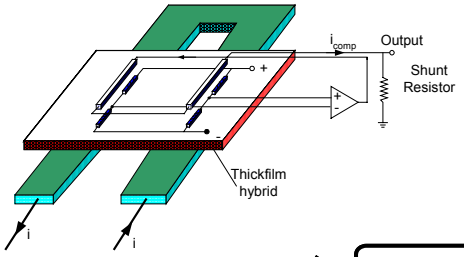
Virginia Tech
DPS Leader

DPS Testbed (GEN II)
Multi-Disciplinary Integrated Team Effort

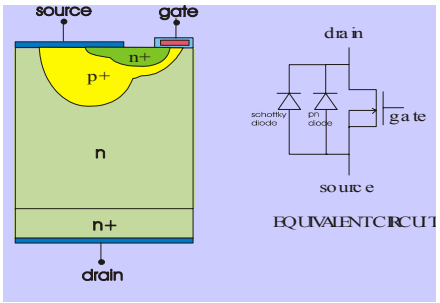
Passive IPEM (IP)



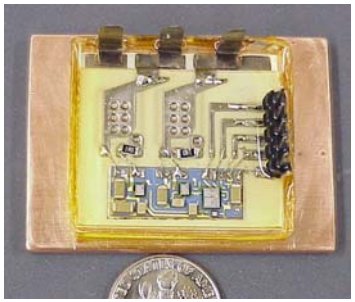
Current Sensing (CSI)

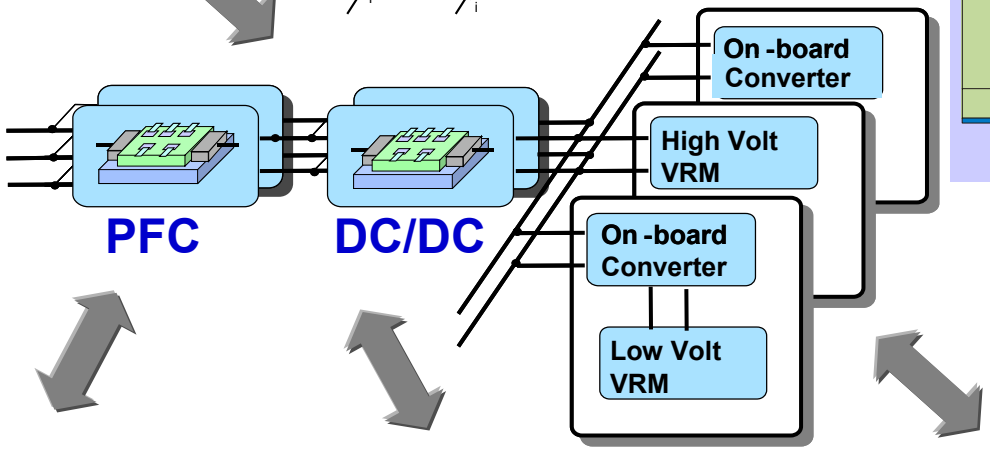


DMOSFET with Fast Diode (APSD)



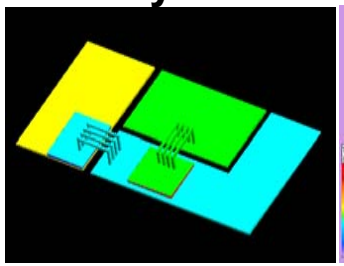
GEN II IPEM (IP)



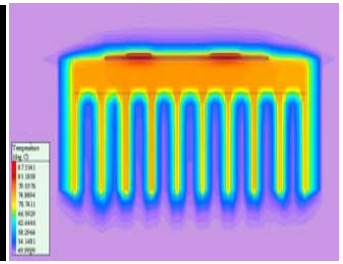


IPEMS

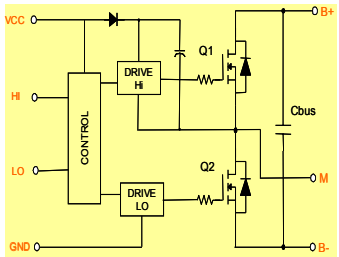
Layout



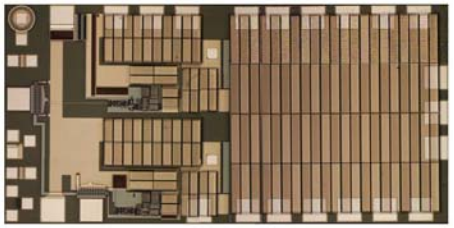
Thermal



Active IPEM

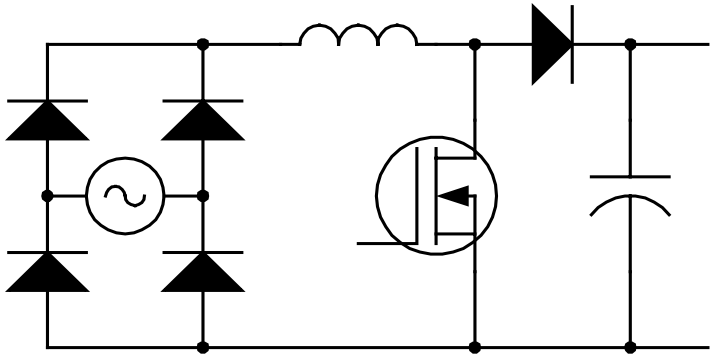


VRM Power ICs (APSD)



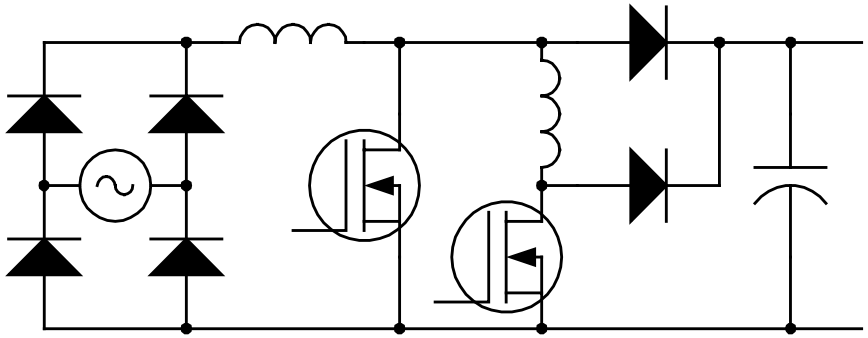
Front-End PFC
Soft Switching Topologies

Conventional Boost

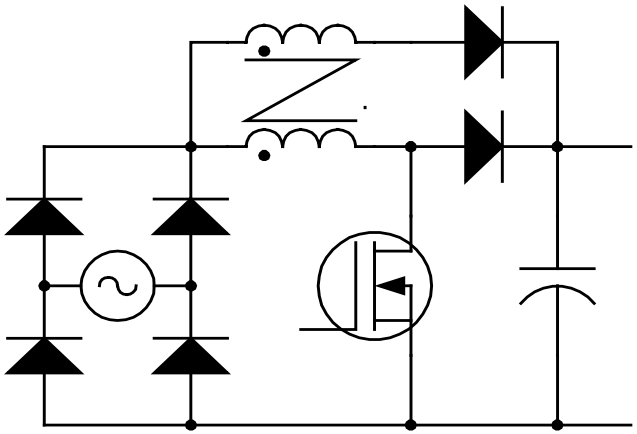


(Baseline)

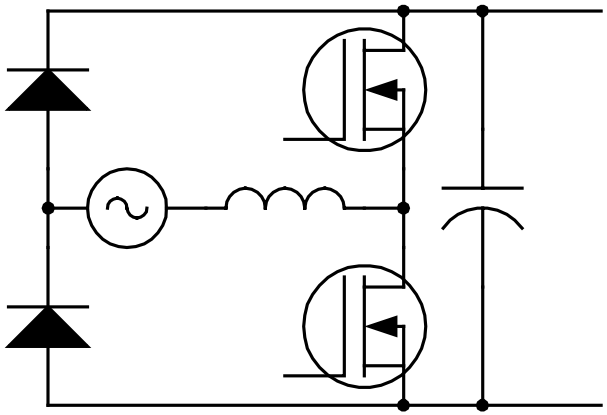
ZVT Boost



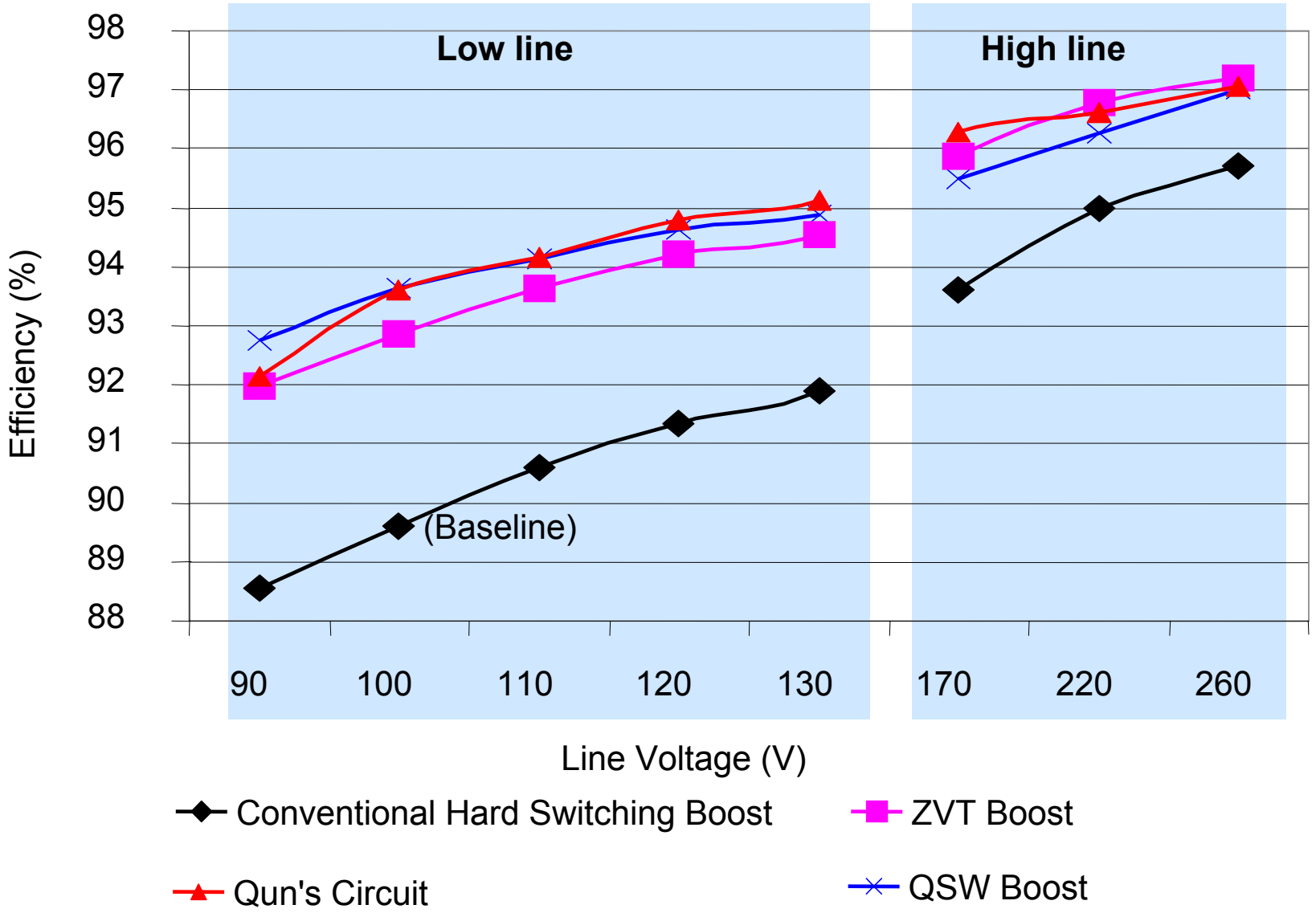
Qun's Boost



QSW Boost

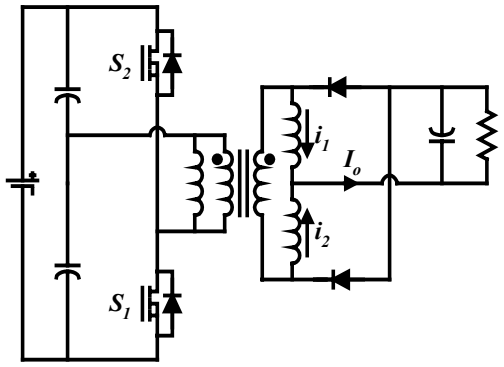


Front-End PFC Efficiency of Soft Switching Topologies

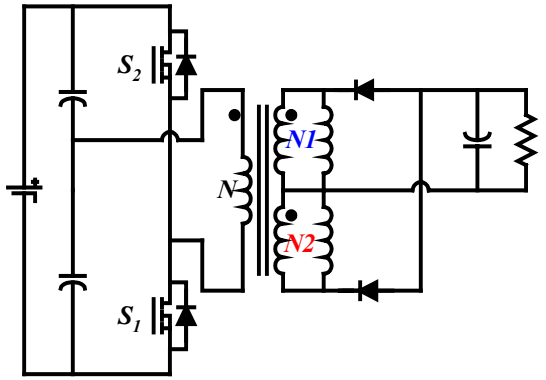


Front End DC/DC
Half-Bridge DC/DC Converters

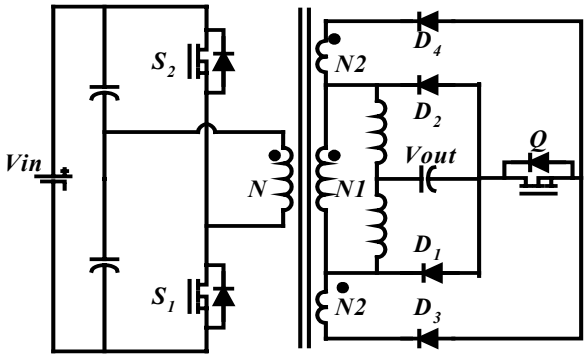
Asymmetrical HB



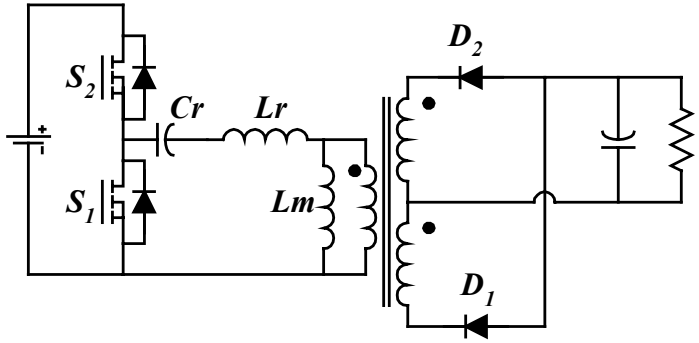
Asymmetrical HB + Asymmetrical Turns Ratio



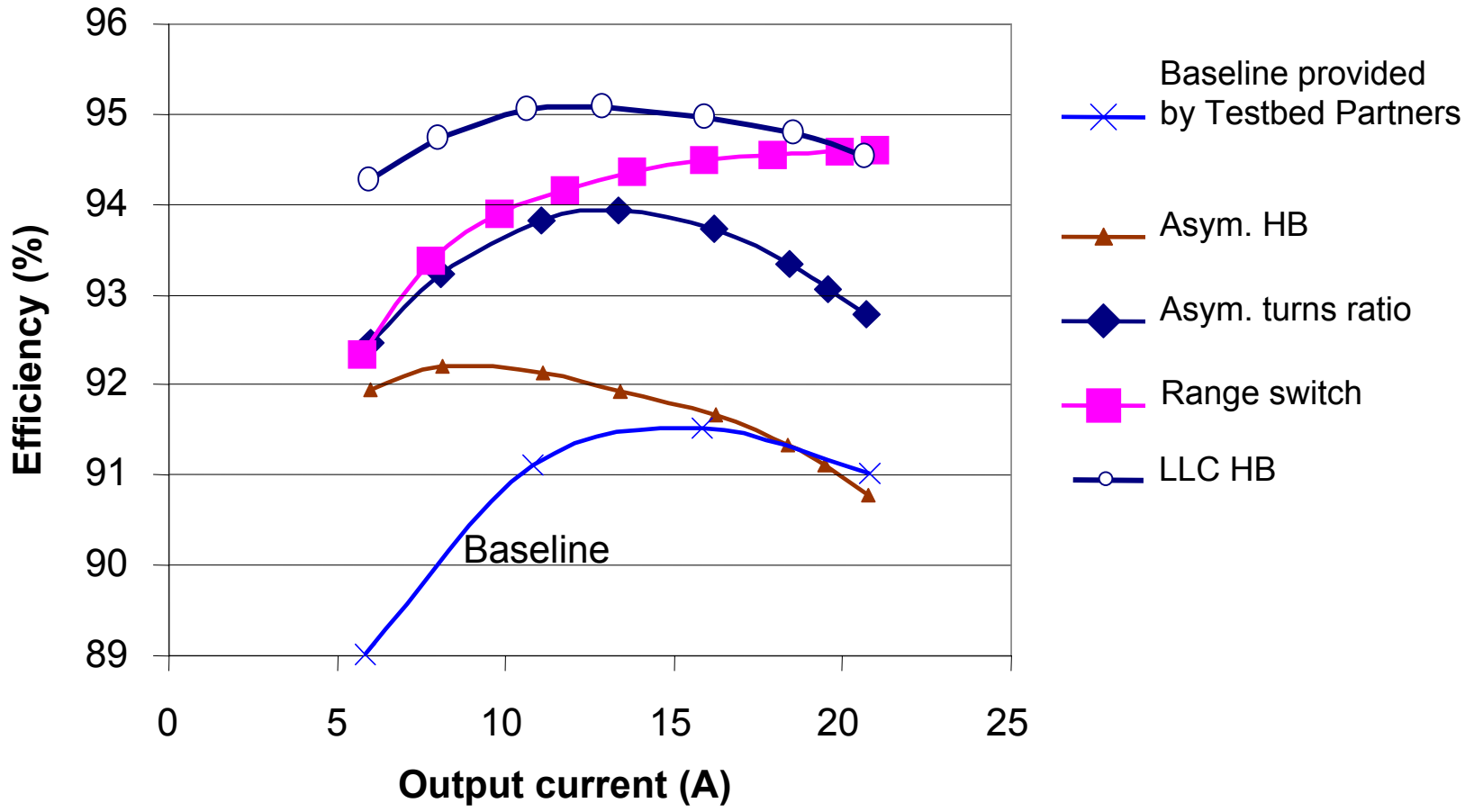
Asymmetrical HB + Range Switch



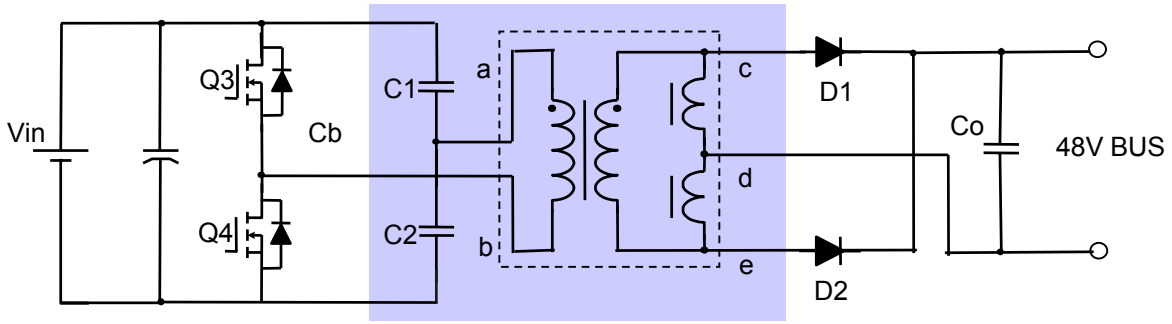
LLC Resonant Half Bridge



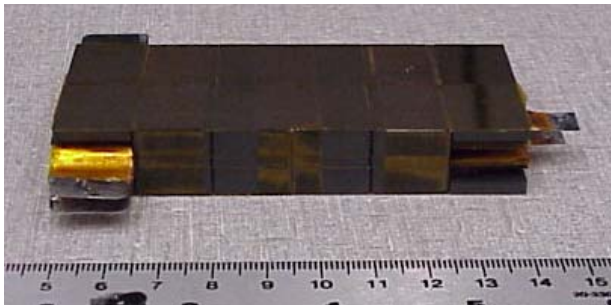
Experimental Efficiency Comparison

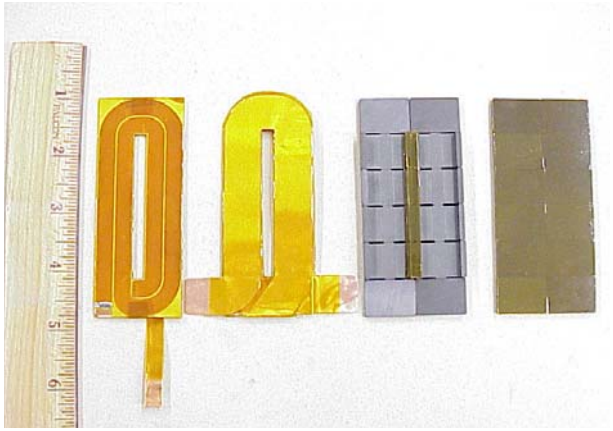


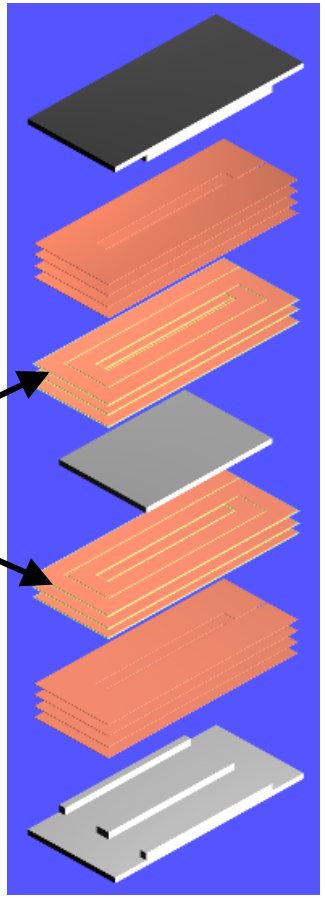
Integrated Passives



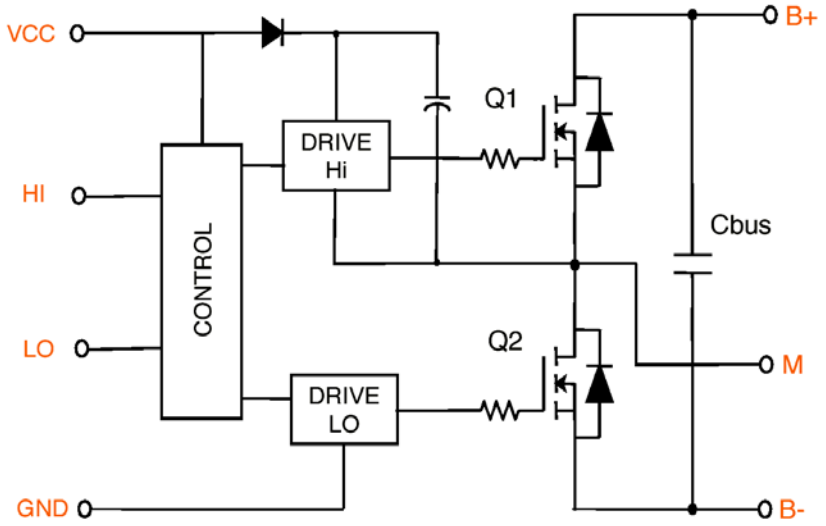
Passive IPEM



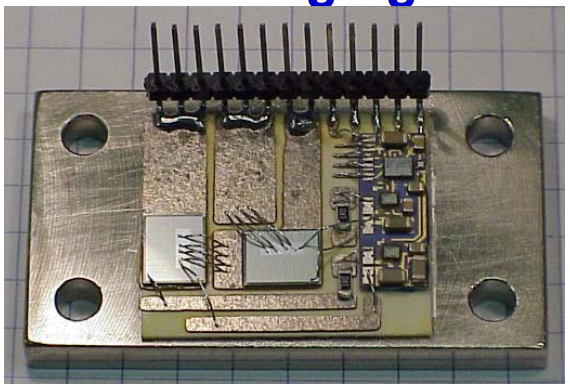




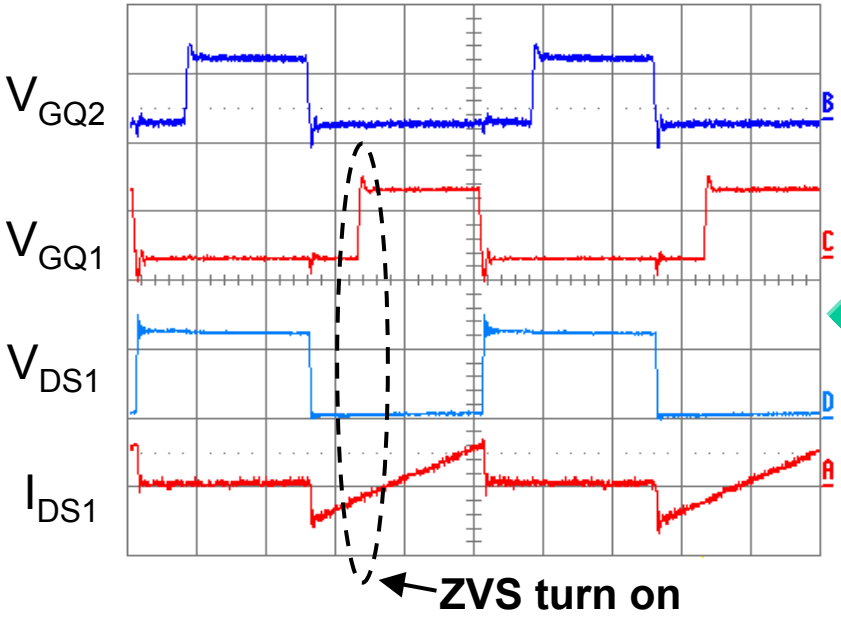
Active IPEM (Gen II)



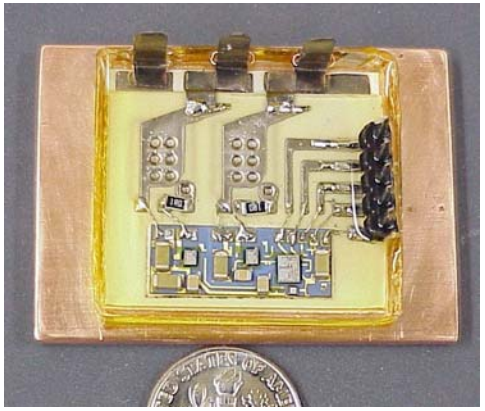
Chip and Wire-Bond Packaging



Gen I IPEM



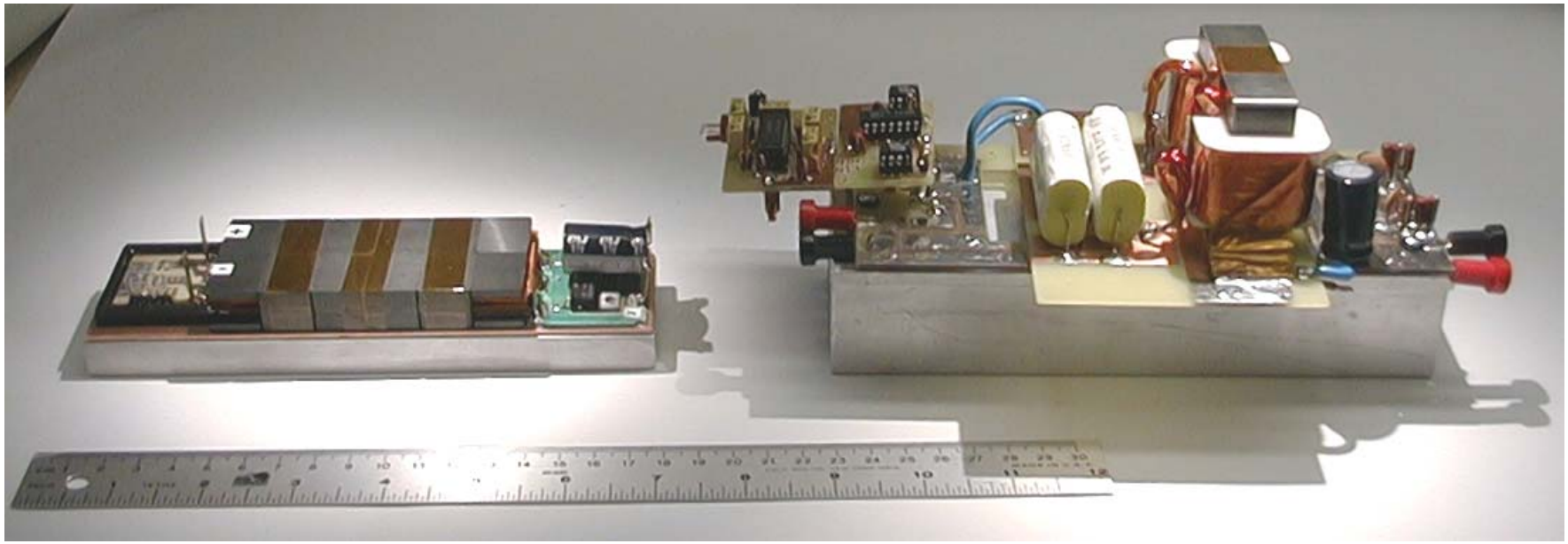
Embedded Power



Gen II IPEM

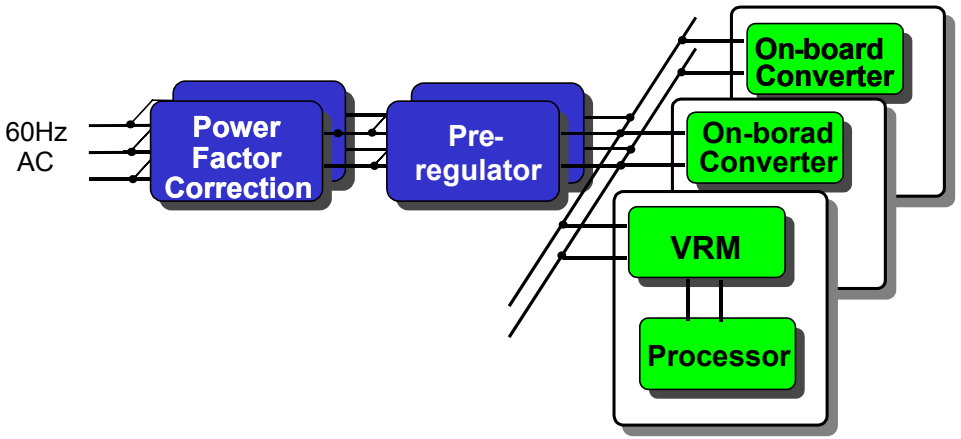
Implementation of Asymmetrical Half-Bridge Using Active and Passive IPEMs

Active and Passive IPEMs **Discrete Components**

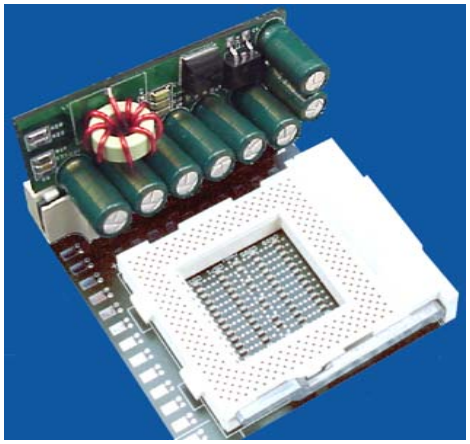


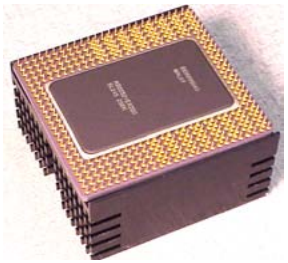
An integrated approach leads to:
- **Improved thermal management**
- **Higher power density (X4)**

Voltage Regulator Module (VRM) for Microprocessors



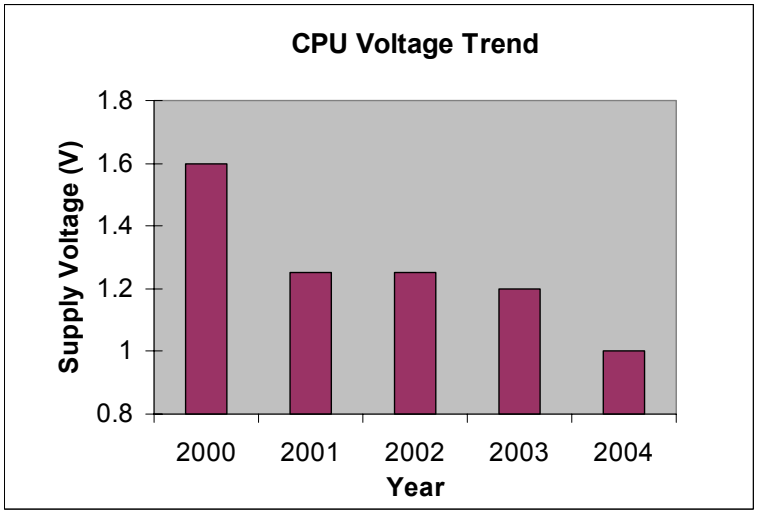
Voltage Regulator Module (VRM)

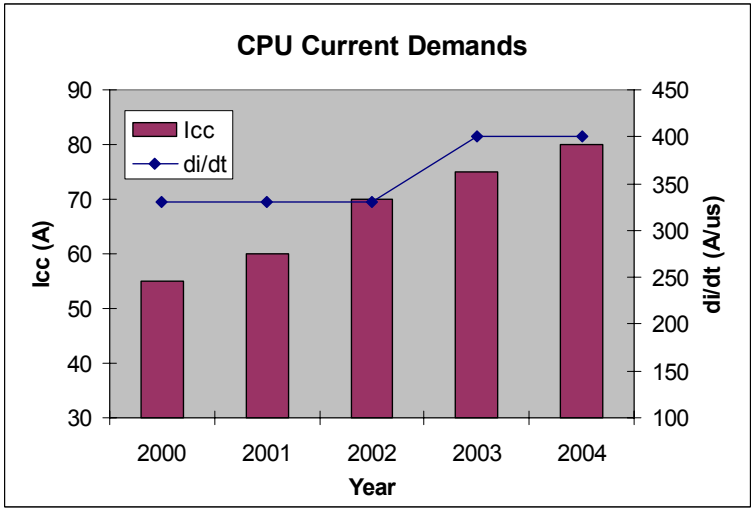




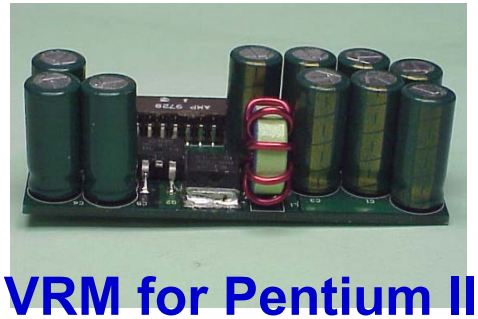
Processor

Intel Roadmap (Desktop)

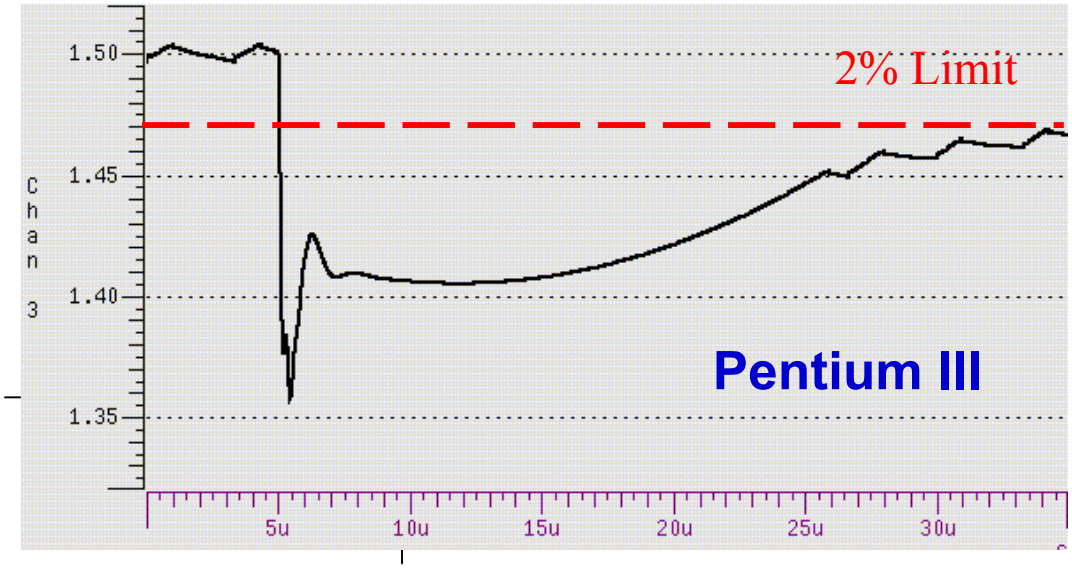


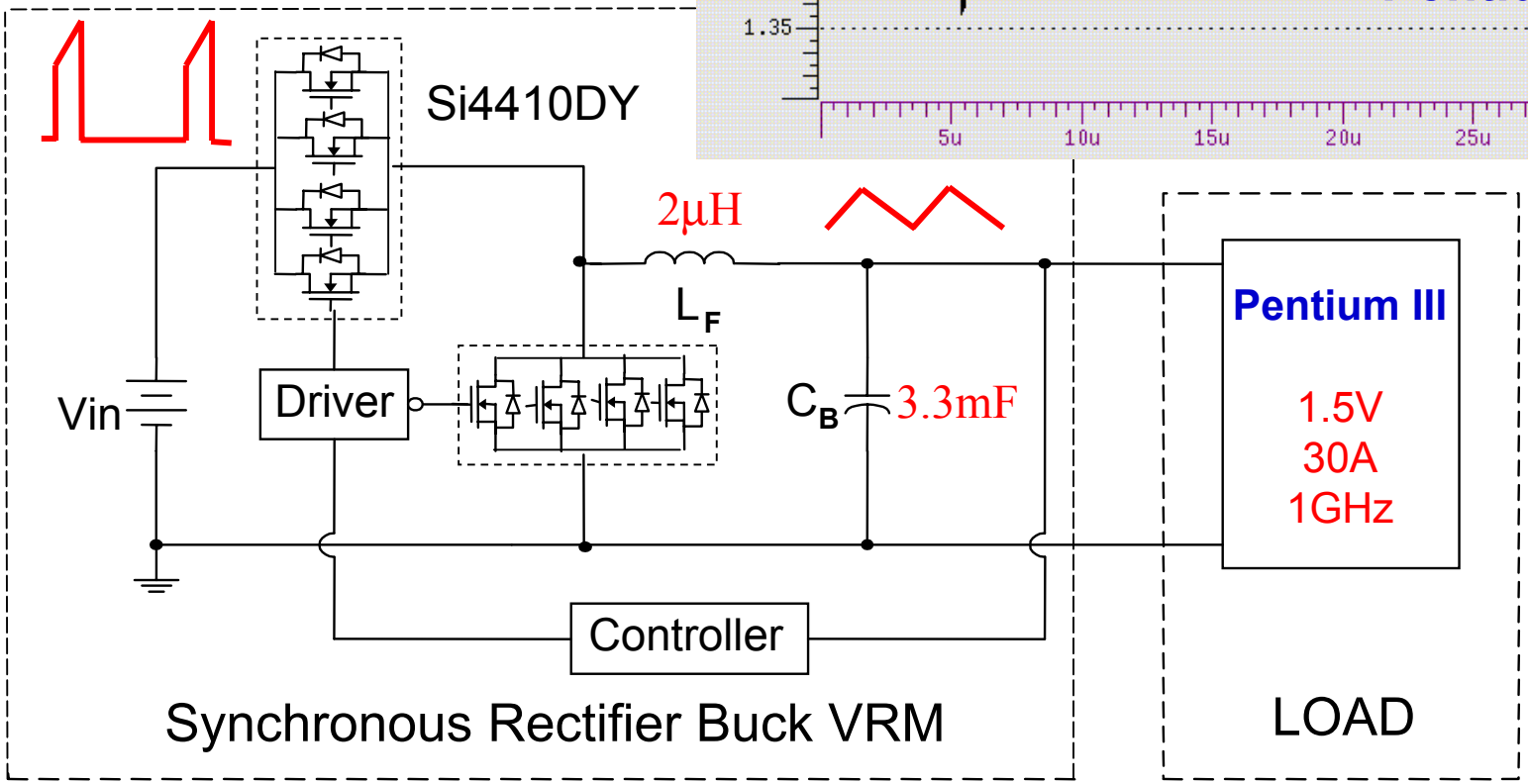


Conventional VRM

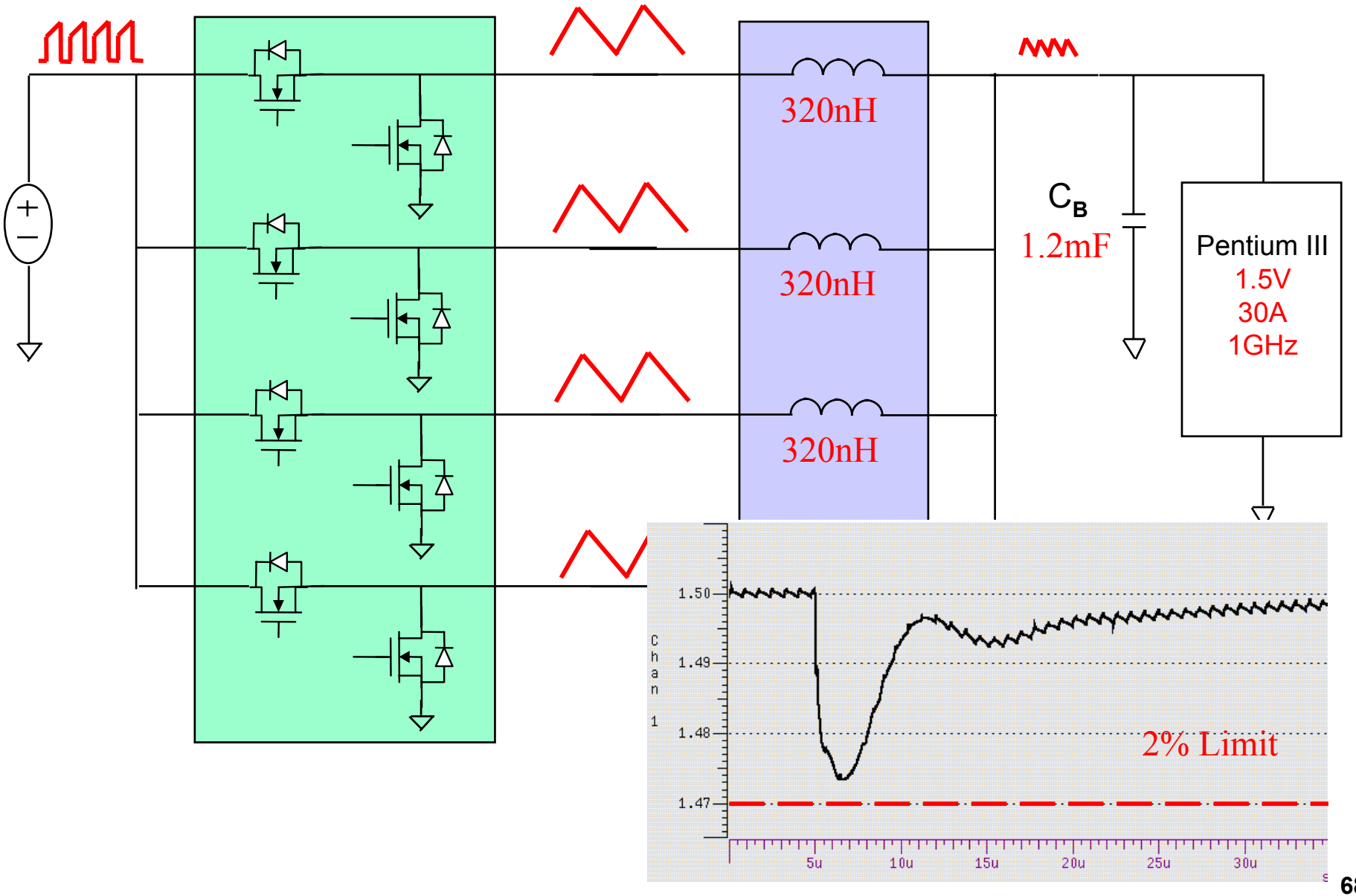


VRM for Pentium II





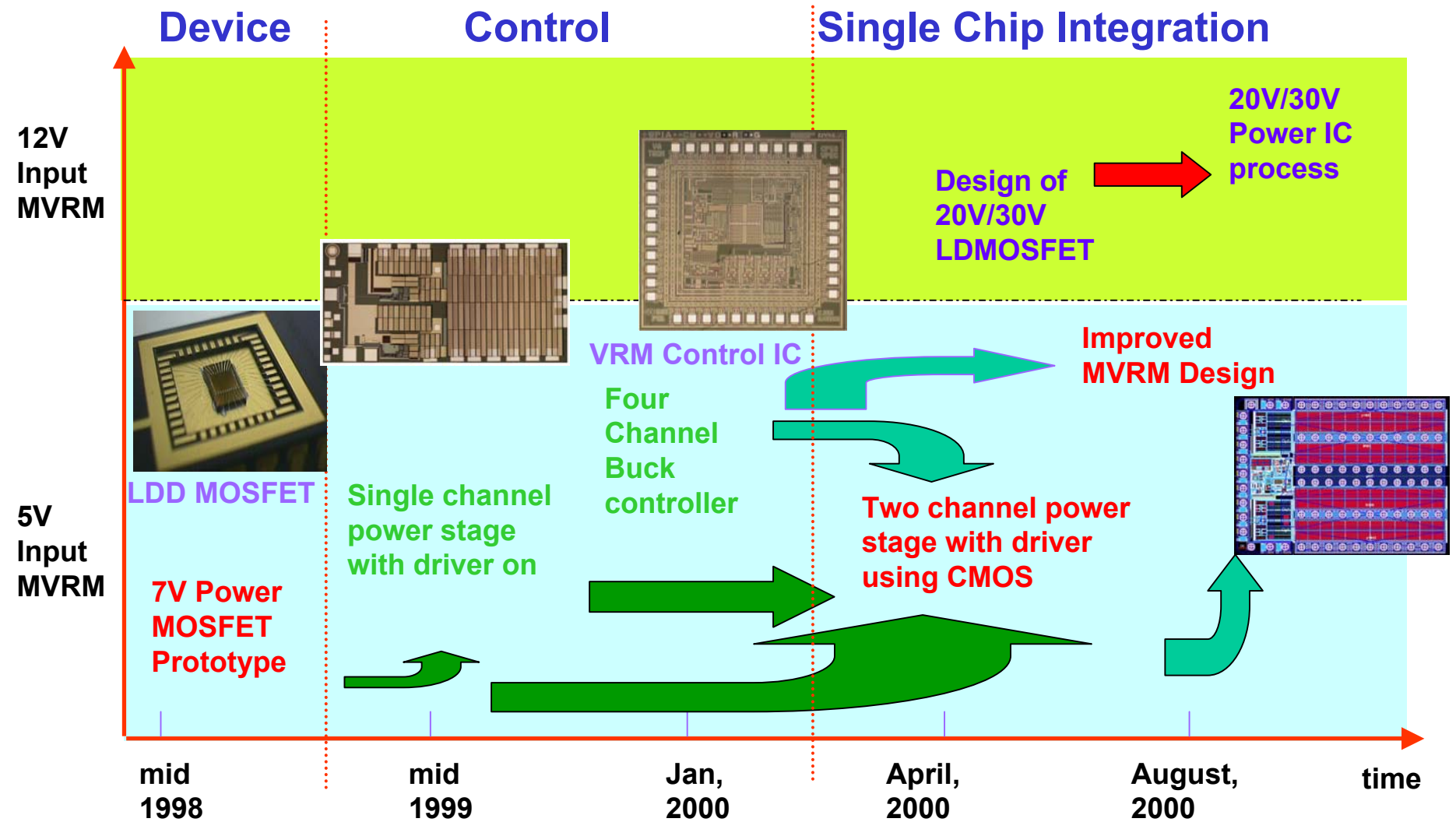
Alternative: Interleaved Multi-Phase QSW Buck VRM



VRM Comparisons

	 Conventional VRM (300KHz)	 CPES 4-Ch QSW VRM (300KHz)	 CPES 4-Ch QSW VRM (500KHz)	 CPES 4-Ch QSW VRM (2MHz)
Power Density (W/in^3)	5	30	45	50
Profile (inch)	1	0.35	0.35	0.25
Output Inductance (μH)	3	0.3	0.2	0.05
Output Capacitance (μF)	7500	1200	1000	350
Transient Voltage (mv)	150	40	40	
Full load Efficiency (%)	85	90	88	78
Output Voltage/Current	2V/15A	2V/30A	2V/35A	1.5V/20A

High Frequency VRM Development Effort



Integration of VRM and Processor