GENERATION OF A NEW FAMILY OF SOFT-SWITCHING VOLTAGE SOURCE INVERTERS

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Abstract – **This work presents the generation of a new family of soft-switching active-voltage-clamping pulse-width-modulation voltage source inverters. The new inverters topologies combines the advantages of a soft-commutated converter using the zero-voltage-switching technique in a wide range of load current and those of a conventional pulse-width modulation. The maximum voltage applied in all switches is clamped and limited in a reduced value and it does not produce excessive current stress. The switching losses and dv/dt of the power device can be significantly reduced and the reverse recovery problem of main switches can be avoided as compared to the hard switching case. Experimental results taken from a laboratory prototype rated at 2.5 kVA are presented for a member of the new inverters family.**

I. INTRODUCTION

In the output of a voltage source inverter, excellent voltage and current waveforms are expected, and a minimal harmonic content is considered. To achieve a minimal harmonic content and to reduce the audible noise in voltage source inverters it is desirable to operate at high switching frequencies. However, when the switching frequency increases, the efficiency and reliability of the PWM converter deteriorate significantly.

Some efforts have been made to reach this aim and various topologies were proposed to achieve soft-switching in voltage source inverters [1, 2, 3, 4, 5, 6, 7]. The goal of a soft-switching is to achieve less switching losses and noises than that of the traditional hard-switching.

In this work is presented the generation of a new family of soft-switching voltage source inverter. The soft-switching is achieved using the active clamped voltage technique.

The inverters are generated from the six basic dc-dc converters and was based in the Carsten proposition [8]. Carsten did not explore the soft-switching capabilities of his proposed structure to demagnetizing forward converter [8]. Jitaru [9] added a saturate inductor to obtain sot-switching in the forward converter.

Some other authors have been using the active voltage clamping technique, but without a connection with one to the others [10, 11, 12].

This work intends to show a common origin to the active voltage clamping circuits described above and proposes a new family of soft-switching voltage source inverter using the same technique.

II. GENERATION OF THE ACTIVE VOLTAGE CLAMPING CELL

The active-voltage-clamping pulse-width-modulation soft-switching cells (AVC-PWM-SSC) are reversible and based in the operation principle of the six basic dc-dc converters (buck, boost, buck-boost, Cuk, sepic and zeta).

The AVC-PWM-SSC are generated transforming the dc-dc converters main switches and diodes in active switches, allowing a reversible flux of current in the cell; the output capacitors in the clamped capacitors and the input and/or output inductors in the resonant inductors. The transformation of the six basic dc-dc converters to obtain the six active-voltage-clamping (AVC) pulse-width-modulation (PWM) soft-switching cell (SSC) is shown in the Fig. 1. The letters "a", "b" and "c" indicate the points where the connections will be made to generate the novel family of inverters.

To generate the active-voltage-clamping converters we should apply two simple rules of elements connection given below:

1 – between the points ***a*** and ***c*** of the commutation cell, we should connect elements with voltage source characteristics, like voltage source and capacitors;

2 – between the points ***a*** and ***b*** and/or ***b*** and ***c*** of the commutation cell, we should connect elements with current source characteristics, like current source and inductors in series with a voltage source.

Applying these two rules to the commutation cells, shown in the Fig. 1, it can be obtained some converters with active-voltage-clamping action. A generated family of DC-DC ZVS PWM AVC buck converters is shown in the Fig. 2. Like the buck family of converters it can be generated the boost family, the buck-boost family, the Cuk family, the sepic family and the zeta family of converters.

The rules have universal use and can be applied to generate a family of soft-switching inverters. The new family of soft-switching active-voltage-clamping pulse-width-modulation voltage-source-inverter (SS-AVC-PWM-VSI) is shown in the Fig. 3.

This new family of inverters is formed by six members, where each one have a different active-voltage-clamping action and combines the goals of soft switching commutation in all active switches, high frequency capability, conventional PWM strategy and no excessive

additional voltage or current stress [14, 15, 16]. The active-voltage-clamping actions are based on the six conventional dc-dc converters: buck, boost, buck-boost, Cuk, sepic and zeta.

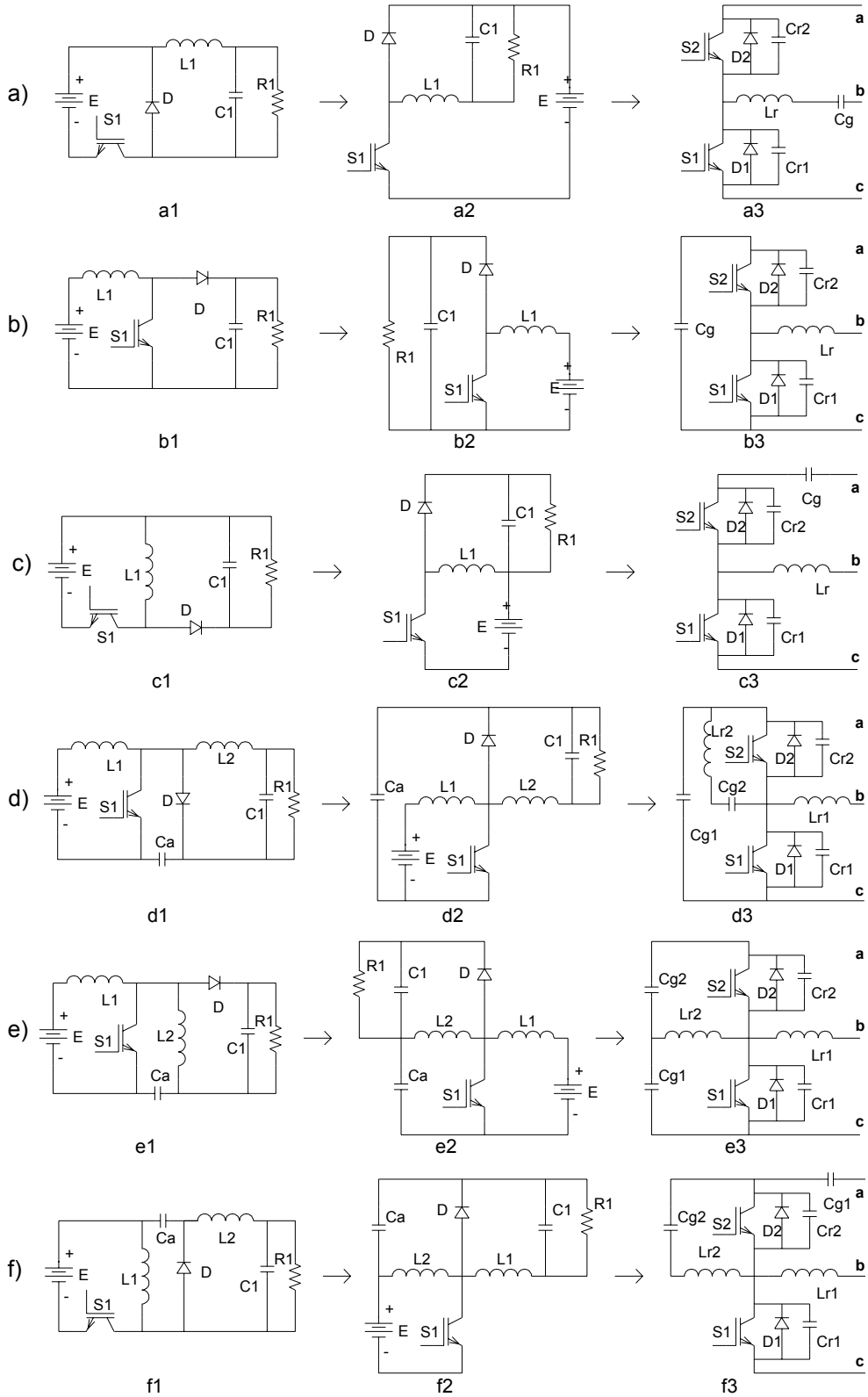

Figure 1 – Generation of the active-voltage-clamping pulse-width-modulation soft-switching cells (AVC-PWM-SSC): a) buck cell; b) boost cell; c) buck-boost cell; d) Cuk cell; e) sepic cell and f) zeta cell.

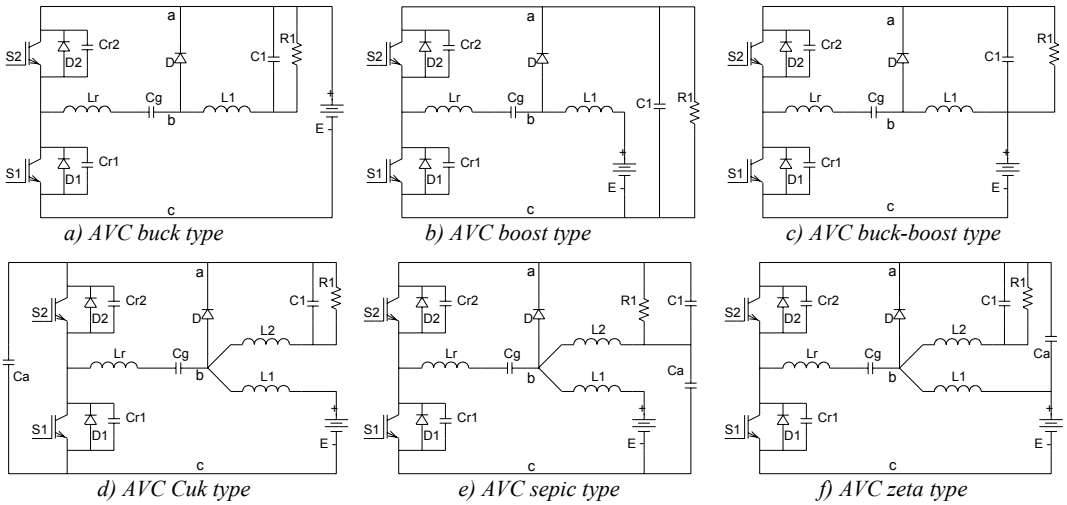

Figure 2 – Family of DC-DC ZVS-PWM-AVC buck converters.

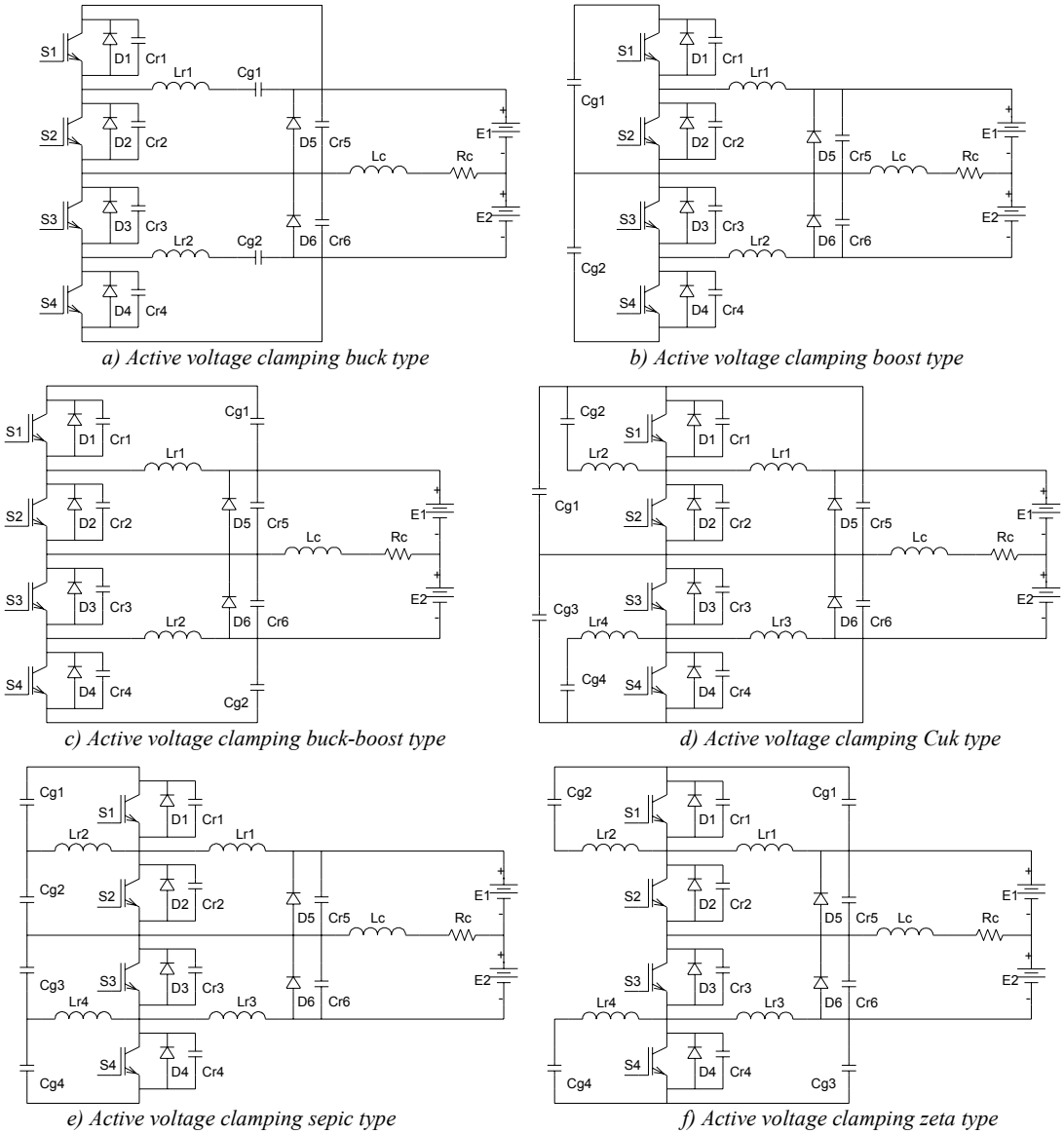

Figure 3 – The new family of soft-switching active-voltage-clamping pulse-width-modulation voltage source inverters.

The use of active-voltage-clamping technique produces a favorable situation to obtain soft commutation in the active switches and regeneration of the commutation energy to the voltage source (DC bus). In the main switches zero-voltage-switching (ZVS) commutation is achieved at rated load, and a quasi ZVS commutation is guaranteed under all other load current conditions. This characteristic do not affect the efficiency of the new family of inverters, because the losses are smaller than the hard-switching case at non rated load. The commutation of the auxiliary switches is ZVS under all load condition.

III. PRINCIPLE OF OPERATION

To analyze the principle of operation it was choose the new zero-voltage-switching pulse-width-modulation voltage-source inverter with buck-boost active voltage clamping action, shown in the Fig. 3.c. This inverter consists of two main switches (*S2* and *S3*), two auxiliary switches (*S1* and *S4*), six diodes (*D1*-*D6*), six resonant capacitors (*Cr1*-*Cr6*), two resonant inductors (*Lr1* and *Lr2*) and two clamping capacitors (*Cg1* and *Cg2*), besides the DC bus and the load.

The topological stages for one period of commutation are shown in Fig. 4. The novel soft commutation inverter presents nine stages of operation, explained as follows.

First Stage (t_0, t_1): in this stage the main switch *S2* is conducting. The current through *Lr1* is equal to the load current and the current through *Lr2* is equal to zero. During this stage energy is transferred to the load.

Second Stage (t_1, t_2): at the instant *t1*, switch *S2* is turned-off and the resonant capacitors *Cr2* and *Cr5* are linearly charged. The voltage across *Cr1* varies from *zero* to $E+vg1$ and the voltage across *Cr5* varies from *zero* to *E*. The resonant capacitors *Cr1* and *Cr6* are discharged and the voltages across their terminals vary from $E+vg1$ and *E* to *zero*, respectively. The resonant current *iLr1* remains constant and equal to the load current.

Third Stage (t_2, t_3): when the voltage across *Cr2* equals $E+v_{g1}$ the voltage across *Cr1* becomes null, and diode *D1* starts to conduct. Simultaneously the voltage across *Cr5* becomes equal to *E*, the voltage across *Cr6* becomes null, and diode *D6* starts to conduct the load current. The inductor *Lr1* demagnetizes through the clamping capacitor *Cg1* via *D1*. During this stage switch *S1* must be gated on, so that in the next stage soft commutation is achieved.

Fourth Stage (t_3, t_4): when i_{Lr1} becomes zero, diode *D1* is blocked and switch *S1* starts to conduct without commutation losses. Current i_{Lr1} changes its direction and increases linearly in a negative sense.

Fifth Stage (t_4, t_5): at the instant *t4*, the switch *S1* is blocked. Capacitor *Cr1* is charged and capacitor *Cr2* is discharged linearly, while the current through *Lr1* remains constant and equal to the load current. The voltage across *Cr1* increases from *zero* to $E+v_{g1}$, while the voltage across *Cr2* decreases from $E+v_{g1}$ to *zero*.

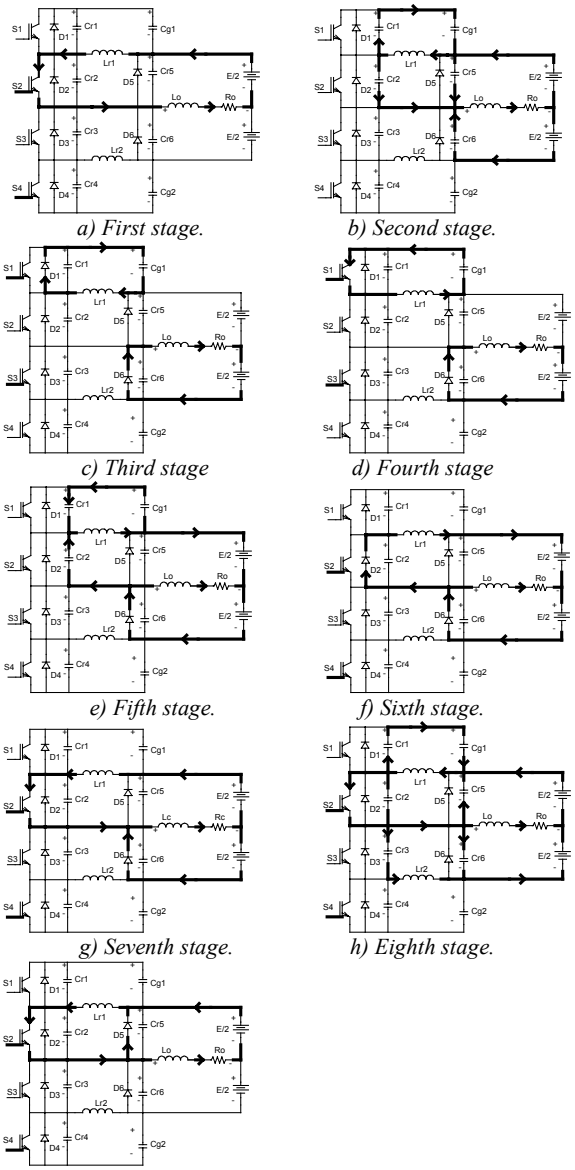

Figure 4 – Topological stages for one switching period.

Sixth Stage (t_5, t_6): when v_{Cr2} becomes equal to zero, diode *D2* starts to conduct the current i_{Lr1}. In this stage *Lr1* is demagnetized through *E* and its energy is recovered.

Seventh Stage (t_6, t_7): at the instant *t6* the current through *Lr1* becomes null and diode *D2* is blocked. Switch *S2* starts to conduct without commutation losses. The current through *Lr1* increases sharply, fed by *E* via *S2* and *D6*.

Eighth Stage (t_7, t_8): when i_{Lr1} becomes equal to the load current, the current in diode *D6* becomes null, blocking it. A resonance involving *Lr1*, *Cr1*, *Cr3*, *Cr5* and *Cr6* begins. The current through *Lr1* increases in a sinusoidal fashion. The voltages across *Cr1* and *Cr5* decrease from $E+v_{g1}$ to v_{g1} and from *E* to *zero*, respectively. The voltages across *Cr3* and *Cr6* increase from *zero* to *E*.

$$i_{Lr1}(t) = i_o(t) + \frac{E}{Zn} sin(w_o t) \qquad (1)$$

Where: $Zn = \sqrt{\frac{Lr}{4Cr}}$ and $w_o = \frac{1}{\sqrt{4LrCr}}$

$Lr = Lr1 = Lr2$ and $Cr = Cr1 = Cr2 = ... = Cr6$

Ninth Stage (t_8, t_9): when the voltage across *Cr6* equals *E*, the voltage across *Cr5* becomes null and diode *D5* starts to conduct. The current through *Lr1* decreases as a consequence of the resistive elements present in the loop formed by *S2*, *Lr1* and *D5*. When the current through *Lr1* becomes equal to the load current, the first stage of operation restarts and one switching period is completed.

IV. EXPERIMENTAL RESULTS

In order to prove the principle of operation a laboratory prototype of a 2.5kVA soft-switching active-voltage-clamping pulse-width-modulated voltage-source inverter (SS-AVC-PWM-VSI) was designed to drive an induction motor.

The clamping voltages across *Cg1* and *Cg2* are shown in the Fig. 5 and the resonant current through *Lr1* is shown in the Fig. 6.

The voltages across and the currents through the auxiliary switch *S1* and the main switch *S2* are shown in the Figs. 7 and 8, respectively. It can be seen that despite of the IGBT tail current, the commutations are lossless.

In a ZVS condition MOSFETS are more indicated, but in this case was used IGBT because it is the most used transistor in induction motor drivers. The use of IGBT transistors do not disturb the commutation cell operation and do not affect the inverter efficiency.

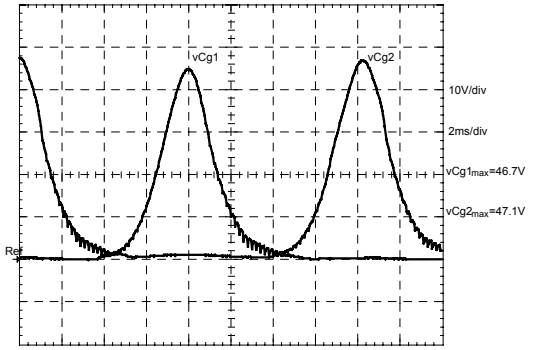

Figure 5 – Clamped voltages in Cg1 and Cg2.

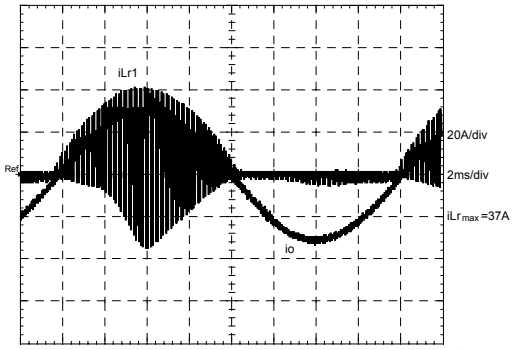

Figure 6 – Current through Lr1 superposed with the load current.

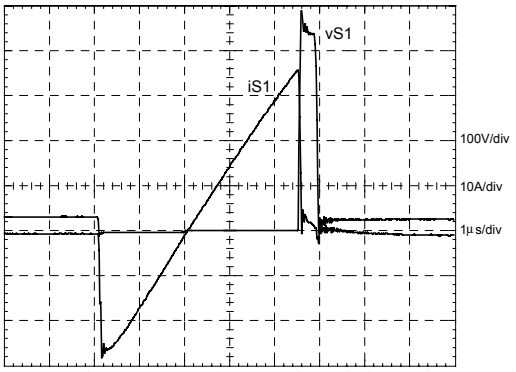

Figure 7 – Voltage across and current through the auxiliary switch S1.

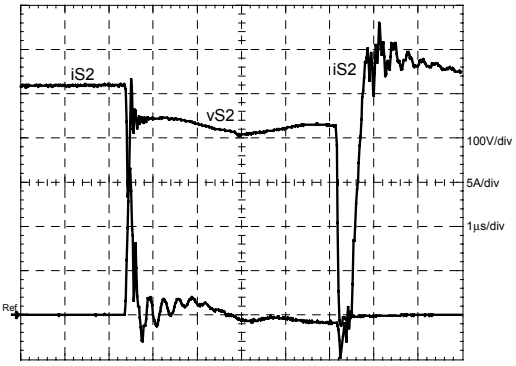

Figure 8 – Voltage across and current through the main switch S2.

A detail of the turn-off process in the main switch *S2* is shown in the Fig. 9. It can be seen the effect of the IGBT tail current. Fig. 10 shows the main switch *S2* turn-on process at no rated load current. This commutation is quasi ZVS and it occurs because exists an insufficient resonant current circulating through the *Lr1* inductance.

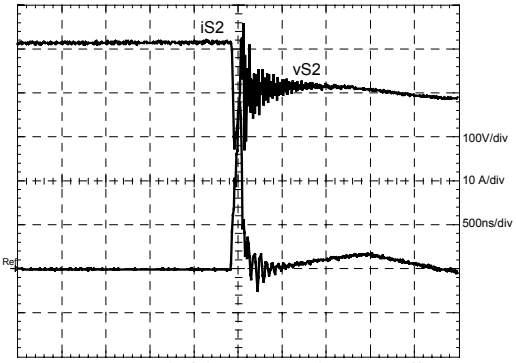

Figure 9 – Detail of the main switch S2 turn-off process.

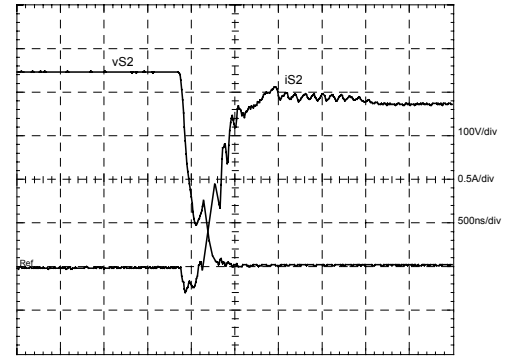

Figure 10 – Main switch S2 turn-on process under quasi ZVS condition.

The commutation under quasi ZVS condition do not interfere in the efficiency of the inverter, it is shown in the Fig. 11. At full load condition the measured efficiency was 96.1%.

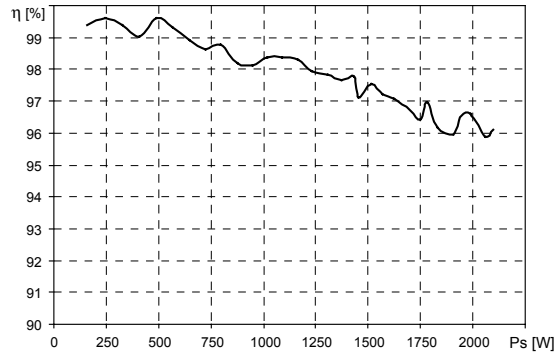

Figure 11 – Efficiency of the new inverter.

V. CONCLUSION

In this work was presented the generation of a new family of soft-switching active-voltage-clamping pulse-width-modulated voltage-source inverters (SS-AVC-PWM-VSI). To generate the inverters were used two universal rules of circuit element connection. The soft-switching active-voltage-clamping pulse-width-modulated (SS-AVC-PWM) generated cell were derived from the six dc-dc basic converters: buck, boost, buck-boost, Cuk, sepic and zeta. Experimental results obtained from a member of the new family of soft-switching voltage-source inverters indicate that it is suitable for voltage source inverter applications. Some characteristics of the new family inverters are better than the characteristics of the other topologies applied to obtain soft switching. The new inverter topology combines the advantages of a soft-commutated converter using the zero-voltage-switching technique in a wide range of load current and those of a conventional pulse-width modulation. Out of the soft-switching region the commutation is quasi ZVS, and this characteristics do not affect the efficiency. The measured efficiency at full load condition was 96.1%. The current and voltage stress was limited to 30% of the load current and 11% of the DC bus, respectively.

VI. REFERENCES

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