Implementation of an Integrated DC-DC Converter using CMOS Standard Technology and employing Smart Power Principles

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***Abstract* – The current tendency in complete integration of systems employed in Electronic Industry which seek to be compact, flexible and reliable in association with lower productions costs has become a mandatory topic in recent technology issues. In this sense, VLSI technologies available worldwide show themselves to be a natural choice. It is through the use of such technology that a monolithic DC-DC converter containing fully integrated active devices and using *Smart Power* concepts is presented for educational purposes.**

I. Introduction

In a time of quickly advancing technology, *Smart Power* technologies represent an answer to the ever increasing market demand of integrated systems where both the signal processing part and true power actuators can be combined. The integration of systems brings several advantages in terms of improved reliability, reduction of electromagnetic interference (EMI), volume, weight and manufacturing expenses as well. Moreover, such improvements and economic requirements are of great interest from a manufacturer's point of view [1].

The efforts made to improve logic performance and power characteristics for a given die size, lead to the development of some specific *Smart Pow*er technologies which allow for integration of power stages with optimized device performance and their control circuit including driver protection and diagnostic elements. These devices are used for a wide range of applications including automotive systems, lamp ballasts, motor drivers, automated systems and robotics [2].

The higher voltage and current handling capability associated with thermal concerns in integrated circuit applications is the most limiting factor in *Smart Power* design. As an alternative approach for implementing *Smart Power* systems integrating both the controlling circuitry and power stages of typical applications like a step motor driver, the VLSI standard CMOS process would be a good choice in light of its availability and cost. Moreover, integrated circuits manufacturers are searching for better devices in terms of their voltage and current capabilities. In fact, some foundries present a sub-micron standard CMOS process and make a high voltage NMOS transistor available. This device can handle a DRAIN-SOURCE voltage up to 50V, which encourages designers to think about integrating control and power circuits using standard CMOS technology [3].

In evaluating the feasibility of this technology regarding its advantages and limitations a conventional DC-DC switched converter was implemented. In order to achieve this an arrangement of pre-defined components inside a monolithic chip, set up to be externally configured for fast breadboarding, was employed. The active parts of the power and control circuits are inside the chip, leading to a simplified assembly of the converter.

II. Proposed Circuit

The main specifications of the monolithic switched DC-DC converter follow:

-Only passive components external
-Input Voltage: 5V
-Output Voltage: 3.3V
-Maximum output current: 500mA
-PWM control
-Switching frequency: 60KHz

A block diagram depicts the main parts of the DC-DC forward converter, showing the integrated parts (inside the dotted lines) and the external ones. The passive auxiliary components used to set up proper operation are external. The design follows the guidelines used to implement conventional converters however a different approach should be given.

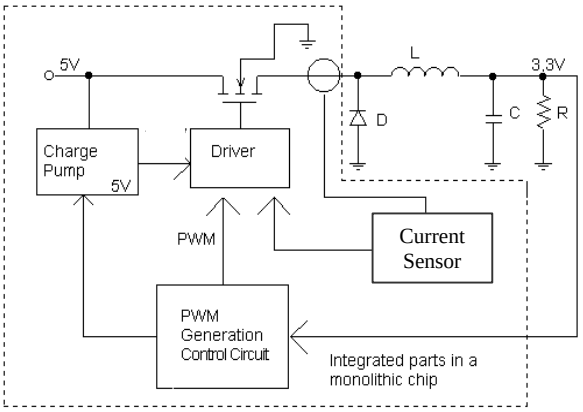

Fig.1 Generic Diagram of the proposed Circuit

III. Guidelines Analysis and Design

The parts of the proposed circuit are described and some guidelines are given.

1) **Power Transistor**: This device is the key to the design. The parameters needed for design were obtained from manufacturer process specifications. For a 0,8μm

standard CMOS currently in use some of them are summarized in the following table:

TABLE I

PARAMETERS FOR DESIGN-NMOS TRANSISTOR (HIGH VOLTAGE)

Parameter	Typical Value	Unit
Threshold Voltage	0,7	V
Breakdown Drain-Source Voltage (3μ)	50	V
On Resistance (8μ)	60	KΩ.μm

The Value in parenthesis refers to specified length channel.

Limiting either the power dissipated on the transistor for full load or the drop of voltage between drain and SOURCE terminals at the same condition sets a specific condition for calculating the physical dimensions of the transistor. For instance, following manufacturer guidelines, one can choose a maximum level of dissipated power as 0,5W per encapsulated die. Assuming that all power dissipated is due the transistor operation, the equivalent resistance of the transistor channel can be calculated from the maximum continuous output current (500mA), resulting a 2Ω channel equivalent resistance. This value of resistance would cause a 1V-voltage drop across the transistor's terminals, a very high value for the intended application. In this case, we can choose a suitable drop and therefore calculate the final resistance. This procedure lessens the maximum continuous dissipated power inside the chip to about 150mW. Once the equivalent resistance has been calculated, the effective width (for a channel length of 8μ) can be solved. Looking at the table, one can determine an effective transistor channel width of 10^5 μm.

The drawing of large integrated transistors in layout design is suitable from predefined structures that can be arranged in multiple shapes allowing the designer to quickly draw a transistor of any size [4]. Part of these structures is shown in Fig. 2. In such structure a pattern drawn contains the transistor's terminals (GATE, DRAIN AND SOURCE) which can be connected by levels of metal that allow individual transistors to be put in parallel. This CMOS contains 400 individual transistors that can be arranged in several ways just by drawing the last metal layer in layout design. Each transistor is 8 μm long per 462.4 μm wide. The total number of transistors that should be connected to form an effective channel width of 10^5 μm is 217. For both safety and practical purposes the number of transistors connected were 250 leading to a total channel width W=114080 μm and channel length L=8μm.

1) **Charge Pump:** As stated before, the voltage supply is 5V. However, to put the NMOS power transistor into full conduction, a higher voltage should be applied to GATE terminal to surpass the threshold voltage (0,7V as indicated in tab.1) plus the SOURCE voltage (less than 5V). If the transistor is supposed to act as switch, the GATE voltage applied should be at least two or three times the 5V supply.

A voltage multiplier technique [5] generates a high enough voltage to switch the transistor on. Fig. 3 shows the circuit also called *Charge Pump* and its equivalent circuit. A switching scheme driven by a clock enables the

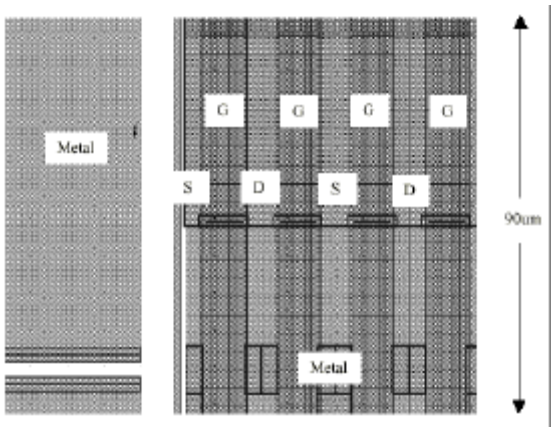

Fig.2 Segment of the structure for the power NMOS transistor implementation

diodes to turn on and off synchronously by pumpingcharges across the circuit so at the end of the network a higher voltage can be achieved. The higher the switching frequency the faster the charging process, thus keeping a nearly stable high voltage at its output.

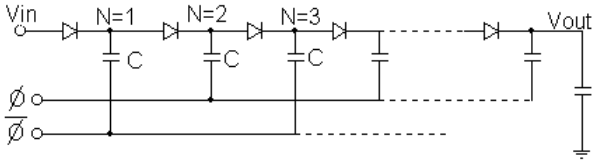

Fig.3 Voltage Multiplier (Charge Pump)

The Charge Pump circuit has a non-load voltage output and a resistance output given by (1) and (2) respectively, where N is the number of stages, V_D the diode voltage drop, C the capacitance, f the switching frequency and V_Φ the amplitude of clock signal.

$$V_{out} = V_{in} - V_D + N \cdot \left(V\phi - V_D\right) \tag{1}$$

$$R_S = \frac{N}{C \cdot f} \tag{2}$$

In a practical implementation, the load current must be given in order to evaluate the charge pump parameters. The charge pump load is the GATE-SOURCE capacitance of the power transistor given by (3)

$$C_L = \frac{2}{3} \cdot \mu \cdot C_{ox} \cdot W \cdot L \tag{3}$$

Knowing the dimensions W and L of the power transistor and the manufacturer's specs where $\mu.C_{ox}$=2.03 fF/μ^2 the calculated GATE-SOURCE capacitance is 1.23 nF. Such capacitance results in an equivalent load resistance given by (4). By applying the equation, we find an equivalent load resistance of 13550Ω.

$$R_{eq} = \frac{1}{f \cdot C_L} \tag{4}$$

The number of stages of the charge pump must be limited to the maximum GATE - SOURCE voltage allowed by current technology. In such case, we choose N=3.

Supposing a diode voltage drop V_D of 0,5V, Vϕ=5V and using C=10nF, (1) and (2) give us respectively the non-load output voltage of V_{out} =18.1V and the output resistance R_S =5000Ω. Fig. 4 shows the equivalent circuit. It is straightforward to deduce the output voltage effectively applied to the power transistor. The 13.2V resulting voltage is applied to the circuit driver and hence to the power transistor GATE terminal. The losses caused by the next driver circuit were not taken into account in this calculation. If they had been, an equivalent resistance would be placed in parallel with the 13550Ω one. The output capacitor affects only the start-up and can be set at 10 μF.

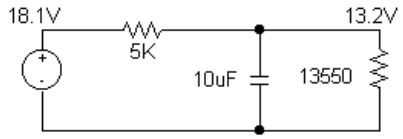

Fig.4 Equivalent Charge Pump Circuit

Fig. 5 shows the implemented charge pump circuit. The diodes and capacitors are external.

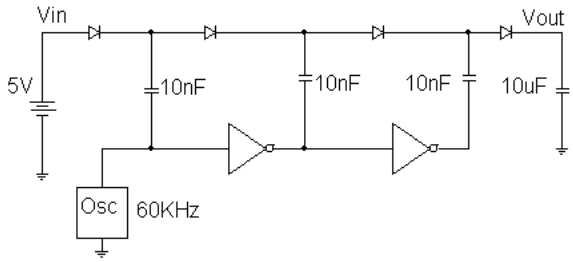

Fig. 5 Implemented Charge Pump

3) **Driver**: A fully integrated circuit drives the GATE of the power transistor. The PWM signal swings between 0 and 5V and is applied to driver input, which generates the high voltage pulses to switch the power transistor on and off. The Charge Pump circuit supplies the driver circuit. The availability of only N-Channel High-Voltage transistors in current technology lead to the "Body Effect" occurrence in one of the driver's transistors. As consequence, a lower output voltage is delivered to the GATE of the power transistor. Equation 6 shows the Threshold Voltage for the transistor that affects the driver output voltage.

$$V_T = V_{TO} + \gamma \cdot \left(\sqrt{2 \cdot \phi - V_{BS}} - \sqrt{2 \cdot \phi}\right) \quad (6)$$

In (6), V_{TO} is the nominal Threshold voltage (when V_{BS}=0), γ the body factor and ϕ the Fermi Potential. For 0,8μm NMOS transistor: V_{TO}=0.76V, γ=0.78 $V^{1/2}$, ϕ=0,6 V. The BODY-SOURCE voltage V_{BS} depends from the transistor operation.

The drain current of a MOS transistor is given by (7), where K_P=95μA/V^2. All of these parameters are given by current technology.

$$I_D = \frac{K_P}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T\right)^2 \quad (7)$$

The driver circuit is shown in Fig.6 (a). We can suppose that the GATE voltage swing applied to the transistor (the transistor subjected to body effect is enclosed by dotted lines) is 0 to V_H. The load "seen" by this transistor at its SOURCE terminal is the equivalent resistance generated by the charge pumping process into the power transistor GATE terminal as illustrated in Fig. 6 (b). Equations (6) and (7) may be used to calculate the effective switched voltage applied to the power transistor GATE terminal, or V_G as indicated, once the charge pump full-load output voltage is known. We have supposed here that no losses occur in the driver.

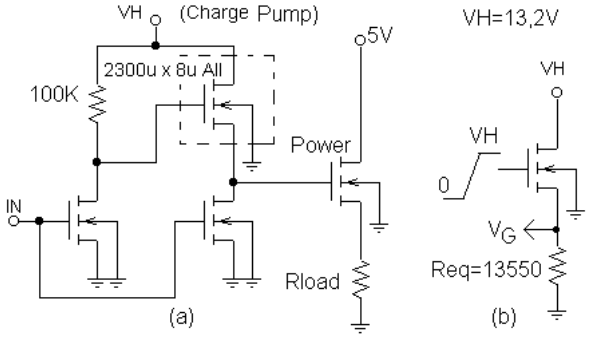

Fig. 6 (a) Circuit Driver and (b) Equivalent Circuit

Evaluating (6) and (7) on the circuit (b) of Fig. 6 and using the process parameters already indicated, the two following equations can be written:

$$V_T = V_{TO} + \gamma \cdot \left(\sqrt{2 \cdot \phi - V_G} - \sqrt{2 \cdot \phi}\right) \quad (8)$$

$$\frac{V_G}{R_{eq}} = \frac{K_P}{2} \cdot \frac{W}{L} \cdot \left(VH - V_G - V_T\right)^2 \quad (9)$$

Solving the equations system we can find an effective switched voltage V_G =10.5V. This level is enough to switch the power transistor on, keeping loss at a minimum. Also, the both equations are solved with a set of V_H output voltage values and the results are depicted in Fig. 7.

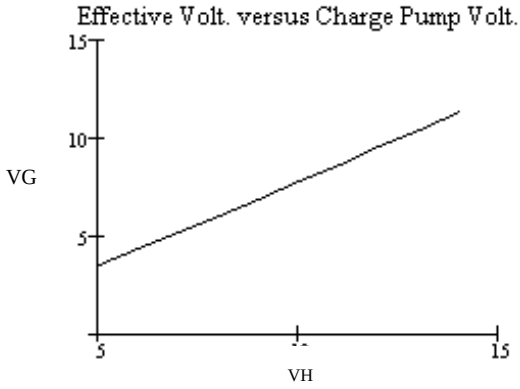

Fig. 7 Graphing V_G (peak amplitude) versus V_H

Fig. 8 shows the simulation result that validates the previous analysis. From the top down, (a) the non-load charge pump output voltage V_H, (b) the loaded one, (c)

effective switched voltage V_G. The simulation shows the transient response of turning on the converter as well.

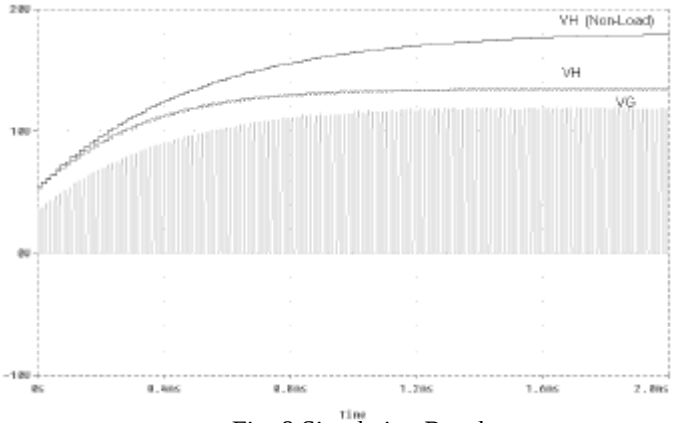

Fig. 8 Simulation Results

4) **Current Sensor Circuit**: Looking for better performance and reliability the protection circuit in *Smart Power* applications should be integrated [2]. The current sensor can be implemented as shown in Fig. 8. Since all transistors have the same characteristics, the current will be shared between them according their respective areas. This minor current will cause a voltage drop on a sensor resistor and integrated supervisor circuits will process this differential voltage.

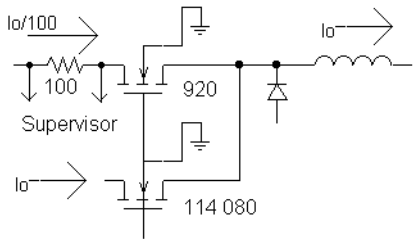

Fig. 8 Scheme to monitor the power transistor current

The processing signal circuit is shown in Fig. 9. The resistors were implemented externally, however it can be done monolithically. The current sensor circuit output signal could activate either a fold-back over-load circuit or an over-current protection one. In this case a Flip-Flop may be used as memory element forcing a system reset in case of failure. The DC transfer characteristic of the circuit is given by (10).

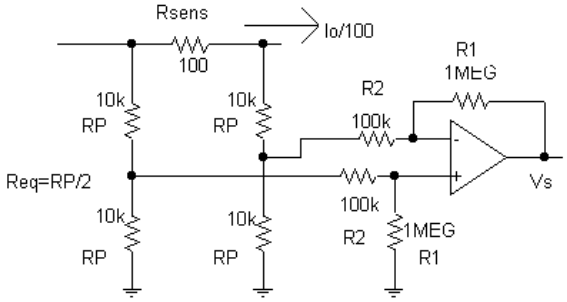

Fig. 9 Current Sensor circuit

$$V_S = \frac{\frac{R_1}{2}}{R_{eq} + R_2} \cdot R_{sens} \cdot \frac{I_o}{100} \qquad (10)$$

The internal op-amp compensation capacitor filters out the rapid transitions of the power transistor current. Whenever implementing short-circuit protections the amp-op should be replaced by a non-compensated circuit and feedback should not be used.

5) **PWM Generator** This signal function is conventional and can be integrated. When looking for a flexible design, one choice is to draw integrated structures like op-amps, gates, and current SOURCES and connect them outside the chip by means of jumpers. This would be a good approach for academic purposes and bench tests allowing designers change the circuit rapidly according their convenience.

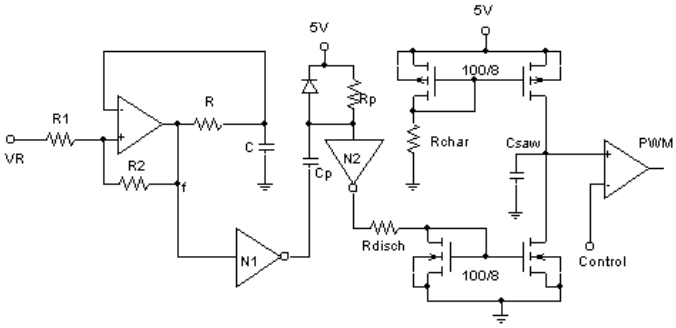

Fig. 10 PWM generator circuit

The PWM signal is generated as follows: An oscillator circuit generates a nearly square waveform that is formatted by GATE N_1. Next, the signal passes through a RC filter which will produces output pulses whenever the input signal changes rapidly. A GATE N_2 formats these pulses generating short positive going pulses that will be used in next stage of the circuit.

A P-type mirror current feeds a capacitor generating a linear rising of voltage across it. External R_{char} gives the slope of voltage variation. The discharging process of the capacitor is a controlled one given by the external resistor R_{disch} connected to an N-type current mirror. The duration of N_2 GATE pulses is approximately given by (11).

$$\Delta t = 0.693 \cdot R_P \cdot C_P \qquad (11)$$

Equation (12) shows the design equations to implement the oscillator. Note that V_R is a constant voltage reference. It can be chosen around $V_{CC}/2$.

$$V_{LL} = \frac{R_2 \cdot V_R}{R_1 + R_2} \qquad V_{HH} = \frac{(V_{CC} - V_R) \cdot R_1}{R_1 + R_2} + V_R$$
$$f = \frac{1}{2 \cdot R \cdot C \cdot \ln\left[\frac{(V_{LL} - V_{CC})}{(V_{HH} - V_{CC})}\right]} \qquad (12)$$

The saw-tooth waveform thus generated is compared with the controlling signal coming from the controller circuit, which generates the PWM signal.

6) **Controller**: The design of the controller follows the classical procedure [6]. Considering the Buck converter operating at CCM (Continuous Conduction Mode) and the specifications given above the filter elements can be calculated. This led to L=1.87mH and C=20uF.

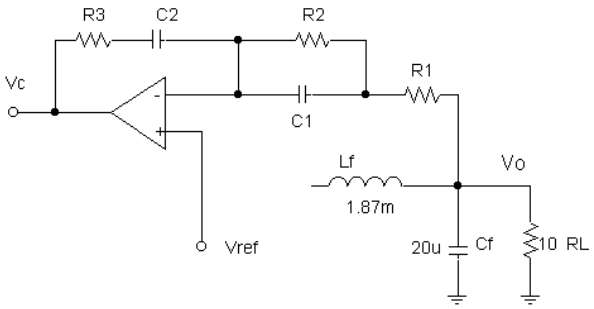

Fig. 10 Controller Circuit

The transfer function V_C/V_O of the controller is given by (13).

$$H(s) = \frac{-1}{(R_1 + R_2)\cdot C_2} \cdot \frac{(1 + s\cdot R_2\cdot C_1)\cdot(1 + s\cdot R_3\cdot C_2)}{s\cdot\left(1 + s\cdot\frac{R_1\cdot R_2\cdot C_1}{R_1 + R_2}\right)} \qquad (13)$$

Using the design parameters, the open loop transfer function of the converter is depicted in (11). As we can see the system is inherently stable.

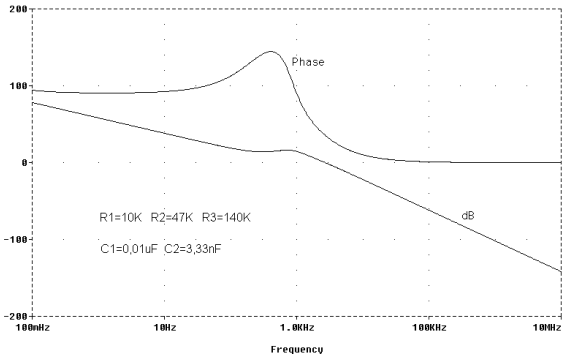

Fig. 11 Open loop gain of the Converter versus frequency

IV. Experimental Results

To evaluate the previous approach in designing a forward converter with fully integrated active devices some experimental results are shown. In Fig. 12, the Charge Pump operation is depicted, showing the transient behavior of the circuit.

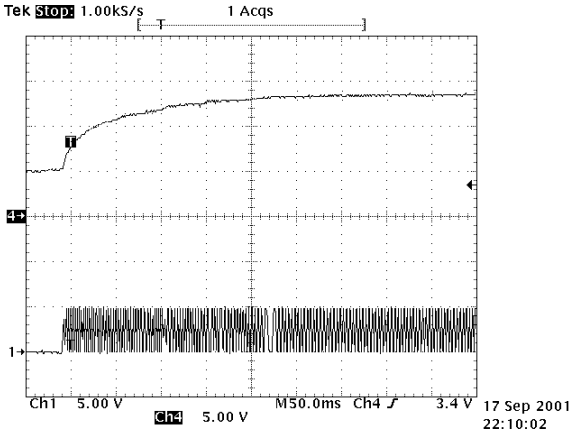

Fig. 12 Charge Pump Start

In Fig. 13, we can see the output voltage from the driver circuit whose level reach nearly the initial value calculated (around 10,5V) when a switched input of 5V is applied to it. Note that the driver works as an inverter gate.

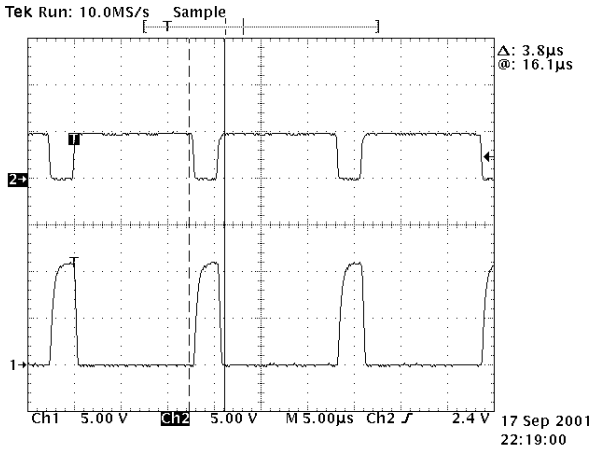

Fig. 13 Driver Circuit Waveforms

Fig.14 shows the PWM generating signals. From top to bottom, (a) The waveform from oscillator circuit, (b) the output pulses from the RC filter circuit, (c) the resetting pulses from the inverter GATE and (d) the saw-tooth waveform.

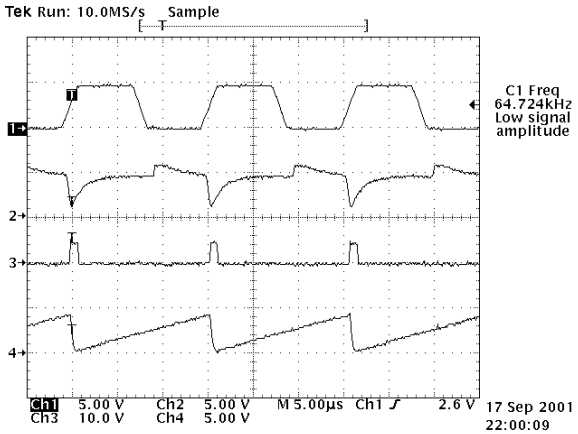

Fig. 14 PWM generator circuit signals

Fig. 15 shows the picture for full load operating point. From top to bottom (a) the output voltage applied to filter LC, (b) saw-tooth waveform and controlling voltage, (c) Output DC voltage.

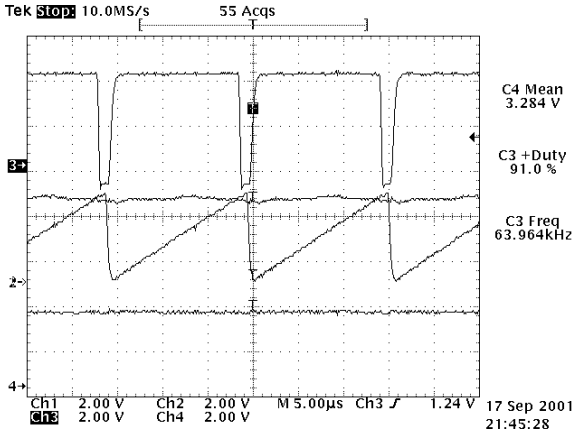

Fig. 15 Full-Load Operation

Fig. 16 shows transient response from non-load to full-load switching condition.

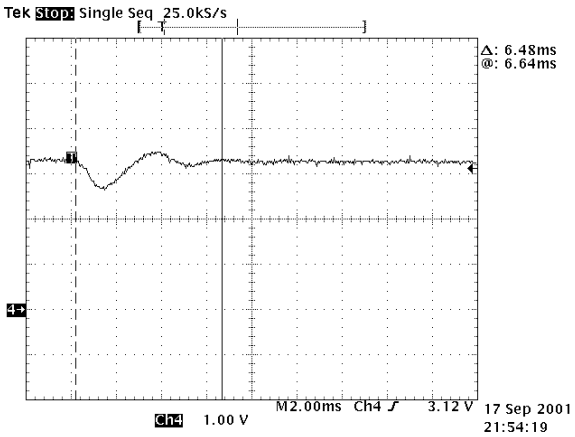

Fig. 16 Transient Response

TABLE II

CONVERTER EFFICIENCY

	[V]	[I]	[P]	Non-Load Chip Consumption	Non-Load Converter Consumption
In	5.0V	0,48A	2.4W	40mA	55mA
Out	3.3V	0,50A	1.6W		

67% Efficiency on full load condition

Fig. 17 shows the microphotography of the die.

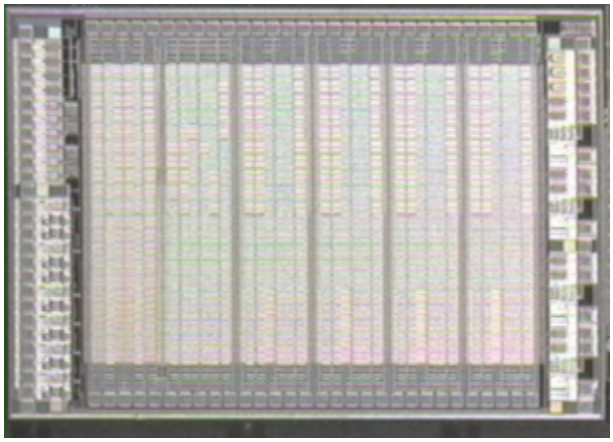

Fig. 17 Chip Microphotograph

V. CONCLUSIONS

This study aims at advancing towards concept of *Smart Power* and its applications, with both its advantages and disadvantages. Also contributes to the development of integrated power devices and shows that they are feasible if restrictions stated by manufacturers are followed. A step toward a true *Smart Power* design would be the *auto diagnostic feature* of some parts of the circuit. In this sense, the controlling system could be able to detect a malfunction of part of the system and for instance take some decision. This kind of feature would require extra processing functions, feasible employing of either microprocessors or digital circuitry. In both situations, the standard CMOS technology allows it, however complex the design may be.

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The technology employed in manufacturing of the circuit was the CXQ-0.8µm from Austria Micro Systems. For more detailed information see www.amsint.com.

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