A PHASE MODULATED DGPS TRANSMITTER IMPLEMENTED WITH A CMRC

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Abstract: **In this paper a clamped-mode resonant converter is proposed to be used as a transmitter which broadcasts correction signals in a Differential Global Positioning System (DGPS). A high efficiency design of the power converter and the T filter that couples the power to the antenna, is achieved using a procedure previously developed by the authors. The carrier frequency is set at 300 kHz and the digital information of the DGPS modulates it with a Stepped Binary Phase Shift Keying (S-BPSK) method. This method allows keeping the converter´s operation in soft switching mode and improving the spectrum of the transmitted signal. An experimental prototype was implemented to generate 300 W at 300 kHz on a 50Ω load. Extensive operation under impedance mismatch and modulation conditions confirm that the soft switching mode is preserved.**

I. INTRODUTION

The Global Positioning System (GPS) concept was born in the early 60s. The system allow to determine position, velocity and time, continuously anywhere in the world. Measuring the arrival time of a signal sent at least by four time-synchronized satellites is the basic request of a GPS system to compute position. GPS is rapidly becoming an integral component of emerging global information infrastructure [1][2]. In civil applications the quality of the position estimate depends upon the geometry of the satellite constellation and the different errors sources. A way to improve this accuracy is to use the Differential GPS (DGPS). In this method, earth stations whose positions are accurately known, measure the difference between their actual positions and the GPS measurements. With this information they generate and transmit a correction signal to a GPS receiver. The use of DGPS enhances the accuracy of the position estimates on land transportation, maritime traffic, civil aviation, ecc. The U.S. Coast Guard (USCG) provides the differential correction for free on marine radiobeacon frequencies (285KHz-325KHz) [3][4]. A DGPS-radiobeacon broadcast network is attractive since it does not interfere with the marine and aviation direction finders. The radiobeacon could become available at low cost in the near future, it propagates in groundwave mode, so it reaches distances which are well beyond the radio horizon. It is also very attractive for applications other than navigation, like precise surveying and geological studies [5].

This paper deals with the design of a voltage clamped-mode resonant converter as a RF power amplifier which broadcasts the correction signal from the earth station to the GPS receiver. Given the application at hand, the corrections have to be sent a long distance, and an adequate band for it is radiobeacon. The DGPS correction information has to be phase modulated into the RF power amplifier. Since it is digital information, a stepped binary phase modulation scheme (S-BPSK) is developed. The S-BPSK is a binary phase modulation introducing a smooth phase transition between adjacent bits. Thus, it allows concentrating the spectrum avoiding to invade adjacent channels. This design and modulation method allows maintaining the converter working in soft switching mode [7]. As a result the number of power components needed decreases and high efficiency is obtained, even during the modulation process.

The paper is organized as follows. In section II the CMRC with T filter is presented. In section III the power amplifier is designed. The experimental setup and results are also shown. Section IV presents the stepped binary phase shift modulation and its implementation with field programmable gate array (FPGA). In section V experimental results are shown. Section VI concludes the paper.

II. VOLTAGE-CLAMPED CONVERTERS WITH T FILTER

The voltage-clamped resonant converter is shown in Fig. 1 a) together with a transformer, a low-pass T filter and the load (antenna plus transmission line). Each column switches at a fixed frequency with a 50% duty cycle. The phase shift between both columns ($\varphi = \omega_s t_\varphi$) determines the duty cycle on the output voltage v_{ab}, as shown in Fig. 1 b) [8-10].

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Depending on the load characteristics, the switching frequency and the duty cycle, the four transistors can turn-on with null voltage (ZVS). It is important to meet this condition because in this case there is no need for high speed free-wheeling diodes. Indeed, it suffices to use the built-in diodes of the power MOSFETs, reducing the number of power devices. The switching losses are minimized through soft turn-on of the MOSFETs. The conduction losses are also diminished since the diodes in series with MOSFETs, which are required when external diodes are used for freewheeling, are no longer needed. The reduced power components count also allows improving the implementation with regards to EMI control, cost and reliability.

II.1 Operating modes A and B

In order to switch all the MOSFETs as ZVS, the switching frequency should be above the cut-off frequency of the resonant circuit, and the duty cycle of the voltage v_{ab} should be larger than a certain limit which depends on the different load conditions. Here, this operation mode is denoted *mode A* and any other way of operation is denoted *mode B*. The limit duty cycle D (=δ/π) is defined as the boundary between modes A and B. It depends on quality factor, cut-off frequency, and characteristic impedance of the filter and the switching frequency of the converter [7].

The boundary between modes A and B is obtained using a piecewise linear model in steady state [7]. This boundary is represented in different plots which are very useful to design the power amplifier with different loads and operating conditions These plots will be used in the next section.

III. POWER AMPLIFIER DESIGN

The design of the RF power amplifier with a CMRC is centered in the design of the low-pass filter. The filter attenuates the components of undesired frequencies and it also matches the impedances between the CMRC and the load. The antenna impedance may depart from its nominal value. It changes from inductive, over the resonance frequency, to capacitive below the resonance frequency. On the other hand, the impedance of the coaxial cable, used in the connection, is not fixed. It varies depending on the cable length. So there is some impedance mismatch between the output filter and the load.

The design of the CMRC with T filter must guarantee operation in the mode A, avoiding changes to mode B operation even when impedance mismatches occur. In order to use the plots developed in [7], the filter and load should be modelled either as a series equivalent resonant (SRL) or a parallel equivalent resonant (PRL). Due to their topology the best approximation is obtained with a PRL.

III.1 Parallel equivalent circuit of the filter

The carrier is obtained by filtering the voltage v_{ab} with a Butterworth low pass filter of three elements (Fig. 1). Fig. 2 shows the actual filter and its parallel equivalent circuit (PRL–E). PRL-E is obtained equating the impedance of both circuits in the figure at the frequency of parallel resonance between the inductors L_1, L_2 and capacitor C:

$$\omega_0 = \frac{1}{\sqrt{L\,C}}\sqrt{\frac{l_1 + l_2}{c_1 l_1 l_2}} = \omega_c\,\omega_f$$

where $\omega_C = 1/\sqrt{LC}$ is the cut-off frequency of the filter, and ω_f depends only of the type filter which is used.

The equivalence is valid only over narrow frequency range so it is important to fix the switching frequency in this range. Thus, the equivalent resistance and capacitance are

$$R_e = R_0\left[1+\left(\omega_f\, l_2\right)^2\right] \quad (1)$$

and

$$C_e = \frac{-l_2\, L}{R_0^2\left[1+\left(\omega_f\, l_2\right)^2\right]} \quad (2)$$

as well as the equivalent cut-off frequency

$$\omega_{ce} = \frac{1}{\sqrt{l_1 L\left(c_1 C + C_e\right)}}. \quad (3)$$

III.2 Filter design

The PRL equivalent of the T filter is obtained for the nominal load condition $R_0 = Z_0 = \sqrt{L/C} = 50\,\Omega$. Then, the parameters of the filter C and L are expressed by

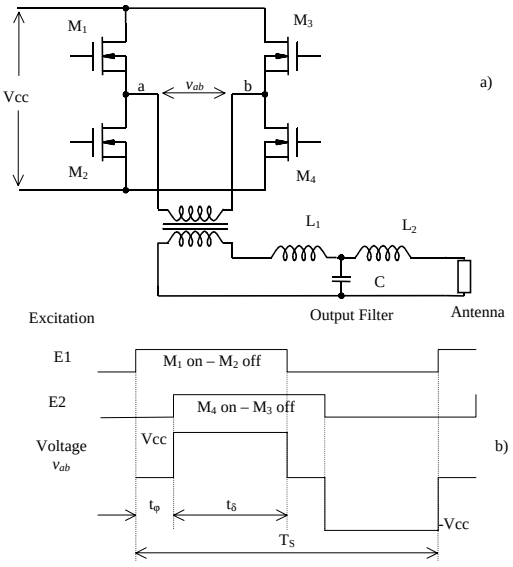


Fig. 1: a) Resonant converter, b) Output voltage and driving signals

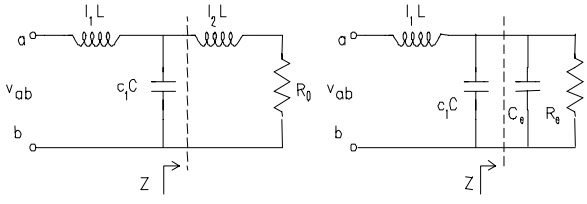


Fig. 2: The "T" filter and its PRL-E

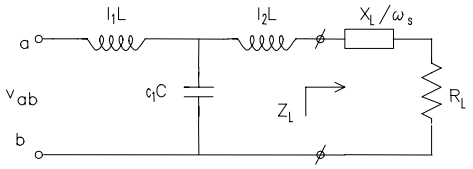


Fig. 3: "T" filter with a load Z_L

$$C = Q_{Pe}\frac{\omega_n}{\omega_s}\frac{1}{R_0\left\{c_1\left[1+\left(\omega_f\, l_2\right)^2\right]-l_2\right\}} \tag{4}$$

$$L = \frac{\omega_n}{\omega_s}\frac{R_0\left[1+\left(\omega_f\, l_2\right)^2\right]}{l_1\, Q_{Pe}} \tag{5}$$

where $\omega_n = \omega_s / \omega_{ce}$ and Q_{Pe} is the equivalent quality factor

$$Q_{Pe} = \sqrt{\left[1+\left(\omega_f\, l_2\right)^2\right]\left[\frac{c_1}{l_1}+\left(\frac{l_2}{l_1}\right)^2\right]} \tag{6}$$

This factor is determined by the coefficients l_1, l_2 and c_1 of the filter. Having chosen the T filter the value of Q_{Pe} is fixed. From (4) and (5) L and C are obtained, using a plot of Q_p as a function of ω_n and adopting a suitable value of ω_n, for mode A operation.

Load impedance variation

The mismatch between the inverter and the load is measured by means of the standing wave ratio (SWR). A SWR equal to or less than 2 is considered acceptable. This SWR determines that the actual load may depart from its nominal and resistive value as shown in Fig. 3. Actually, the load will remain inside a circular section of the impedance plane, as indicated in (7),

$$\left(R_L-\frac{5}{4}R_0\right)^2+X_L^2=\left(\frac{3}{4}R_0\right)^2 \tag{7}$$

When this load variation is considered, the natural frequency of the resonant circuit changes, since the inductance at the output of the filter is modified by the reactive part of the load. The reactance of the load is defined as,

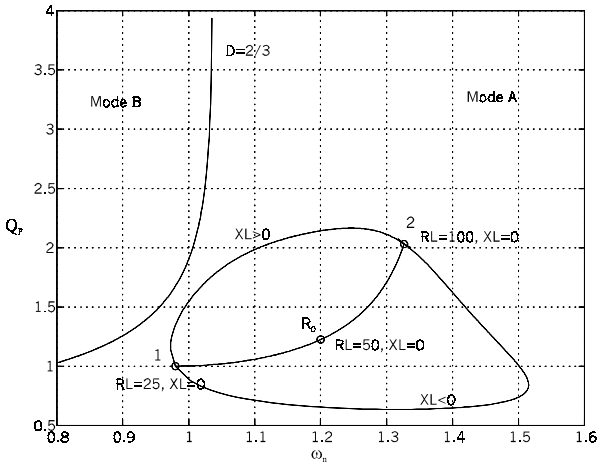


Fig. 4: Operation area for PRL-E with SWR=2

$$X_L = \omega_s L_L \qquad X_L > 0$$

$$X_L = -1/\omega_s C_L = \omega_s\left(-L_L\right) \qquad X_L < 0$$

Then, a new inductance is defined at the output of the filter,

$$L_2' = l_2.L + X_L/\omega_s \tag{8}$$

The output voltage of the inverter is a quasi-square wave with a duty cycle equal to 2/3. For a 3rd order Butterworth T filter the coefficients of the filter are equal to $l_1 = 3/2$, $l_2 = 1/2$, $c_1 = 4/3$ and result $\omega_f = \sqrt{2}$ and $Q_{pe} = \sqrt{3/2}$.

In addition, the switching frequency is 300 kHz, and the load has a nominal value $R_0 = 50\Omega$. In order to determine L and C with (4) and (5), a value of ω_n should be chosen. There exists a trade off between the requirement to operate in mode A and the attenuation of the filter. Thus, it is advisable to select the minimum value of ω_n that satisfies the first condition. Fixing $\omega_s = \omega_c$, the filter gain at the switching frequency is equal to –3 dB, which is a reasonable attenuation. The normalized frequency is obtained from

$$LC = \frac{1}{\omega_c^2} = \left(\frac{\omega_n}{\omega_s}\right)^2 \frac{1}{l_1}\frac{\left[1+\left(\omega_f\, l_2\right)^2\right]}{\left\{c_1\left[1+\left(\omega_f\, l_2\right)^2\right]-l_2\right\}} \tag{9}$$

Considering that $\omega_s = \omega_c$, the value of ω_n is given by,

$$\omega_n = \sqrt{l_1} = 1.2 \tag{10}$$

and the values of L and C are found to be

$L = 26\ \mu Hy$ and $C = 10.4\ nf$.

Fig. 4 represent the plot of the quality factor as a function of the ω_n for a PRL and D=2/3. It shows the operating region for the variable load indicated in (7), and the filter designed in this section. The nominal load is characterized by a single point labelled $R_L = 50$, $X_L = 0$. The line drawn inside the operating region represents the operation of a pure resistive load. The points above this line correspond to an inductive load, while those below the line represents a capacitive load. It is seen that a high inductive load pushes the operating point towards the boundary between modes A and B.

III.3 Power amplifier

Fig. 5 shows the experimental set-up. The power amplifier is fed directly from the mains through a diode bridge rectifier with a capacitor filter. A high frequency

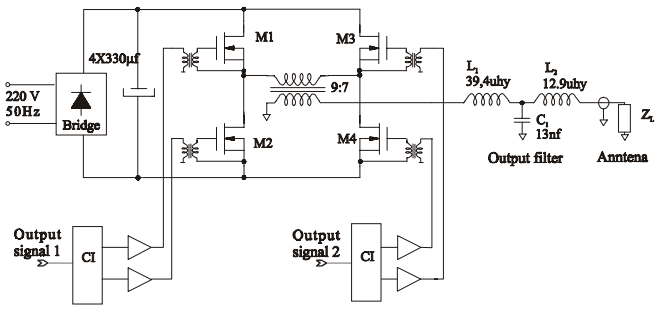
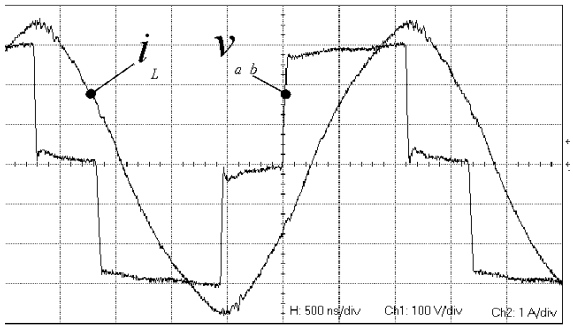
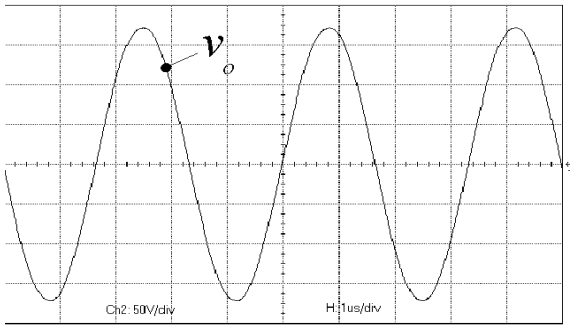


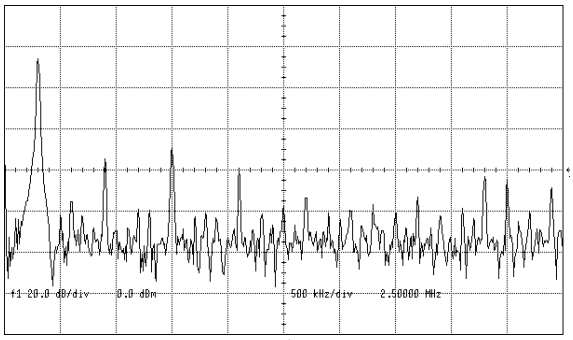
Fig. 5: Power amplifier



a)



b)



c)

Fig. 6: Nominal load R_L = 50 Ω. a) Voltage and current supplied by the inverter (100V/div, 1A/div, 500ns/div), b) Load voltage (50 V/div.), c) Carrier spectrum (20 dB/div. 500 kHz/div.)

transformer provides electrical isolation as well as voltage level transformation to achieve 300 W on the nominal load R_0 = *50Ω*. The power inverter was implemented with power MOSFETs IRF720. Taking into account the values of *L* and *C* obtained in the previous section, the output filter was implemented with a capacitance of 13nf, an input inductor of 39.4µHy and an output inductor of 12.9µHy.

Fig. 6 and Fig. 7 ilustrate some experimental result . Those corresponding to the nominal load are shown in Fig. 6. The output voltage and current of the inverter are shown in Fig. 6 a). It is possible to see that when the voltage pulse is applied the current should be taken by the corresponding diode and then the MOSFETs are turned-on as ZVS. The angle between the voltage pulse and the zero crossing of the current is about 30°, proving that the converter is operating well inside mode A, as predicted by the design. The voltage at the filter output is shown in Fig. 6 b). This waveform of 122V voltage rms is applied to the antenna and the power delivered is 289W, very close to the design value. The full-bridge has an efficiency of 97%, and the

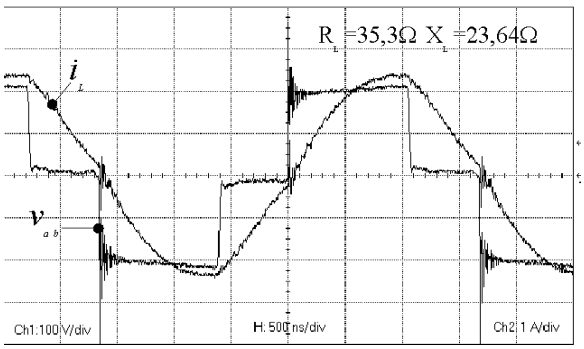


Fig. 7: Voltage and current at the filter input with inductive load R_L=35.3Ω, X_L=23.64Ω. (80V/div, 1A/div, 500ns/div)

filter and transformer efficiency is 95%. The overall efficiency is 92%. The output voltage spectrum is shown in Fig. 6 c). The fundamental component at 300Khz is observed along with some odd harmonics. The 5th and 7th harmonics are -45db and -55db below the fundamental component respectively; while the 3rd harmonic at -50db and its multiples are not exactly cancelled. The total harmonic distortion (THD) is 0.67%.

Fig. 7 shows the most critical case of mismatch that pushes the converter to operate very near of the boundary between the mode A and B, see Fig. 4. The zero crossing of the current occurs immediately after application of the voltage pulse. This situation corresponds to a load impedance equal to R_L = 35.3Ω y X_L = 23.64Ω.

IV. STEPPED BINARY PHASE SHIFT MODULATION

The information to be transmitted is of digital nature, so it is convenient to adopt a digital modulation scheme adequate to the information rate that is being transmitted. A binary phase shift keying (BPSK) has been adopted. In this way, a 180° phase shift is introduced to the carrier each time the data level changes. The expression for the BPSK modulated carrier is

$$v(t) = A\sin(2\pi f_c t + \theta) \qquad (11)$$

The amplitude A is constant, also the carrier frequency f_c and θ is the modulation parameter which has two values 0 or π. The carrier waveform at the instant when the digital data changes sign is shown in Fig. 8.

The power spectral density of BPSK with a non return to zero (NRZ) signalling contains 90% of the energy in its main lobe. There are secondary lobes that decay slowly over the sidebands due to the fast transitions in the digital data [6]. This spectrum is not acceptable for the bandwidth

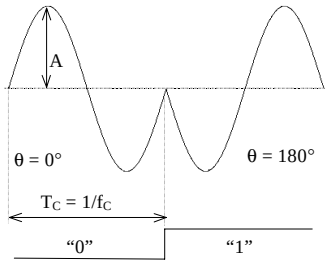


Fig. 8: BPSK Modulation

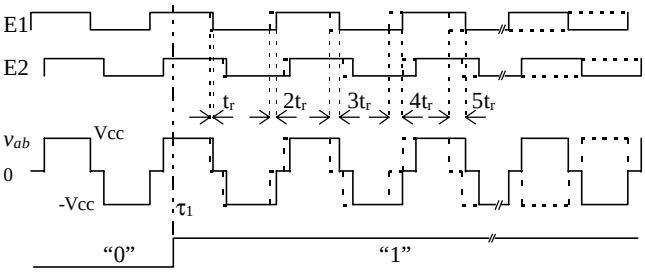


Fig. 9: S-BPSK modulation

assigned to the communication channel. It is also unacceptable from the point of view of the converter operation, since it could enter mode B during the transient.

The transmission rate is in the order of 50 to 200 bits per second, much smaller than the carrier frequency. So there are several carrier cycles between two consecutive data transitions. This means that it is possible to introduce a gradual modulation to reduce the bandwidth and to avoid leaving mode A operation. Then, the required 180° phase shift is implemented with several smaller phase shifts distributed among several carrier cycles. This modulation method is denominated stepped binary phase modulation (S-BPSK). In the next section it will be experimentally seen that S-BPSK allows maintaining the converter operating in mode A, even during the modulation process.

IV.1 CMRC with S-BPSK modulation

BPSK on the CMRC is obtained changing the phase of the driving signals E1 and E2 in π rad. This is equivalent to a half period delay on E1 and E2. In this way, the carrier on the filter output changes its phase in 180°. S-BPSK on the CMRC is made dividing the total delay ($T_C/2$) on E1 and E2 in several carrier cycles.

Fig. 9 depicts with solid line the resulting voltage v_{ab} and the driving signals E1 and E2 when a change of symbol occurs. The dashed line shows the voltage v_{ab} with zero phase shift. It should be noted that the modulation process begins at $t = \tau_1$. From this time, successive t_r delays during n cycles are introduced in the driving signals. After 2n half-cycles the modulation process finishes. The final phase voltage v_{ab} is π rad out of the phase with respect to the original wave form. The delays are introduced in the voltage pulse v_{ab} to increase the duty cycle. In this way, operation in mode A is guaranteed. The delay time (t_r) must be located in opposed semi-periods of the carrier so that the product of time-voltage on v_{ab} is null.

Adopting n=15 for the transition from one symbol to another, a 6° phase shift is introduced in each half-cycle. Therefore t_r is

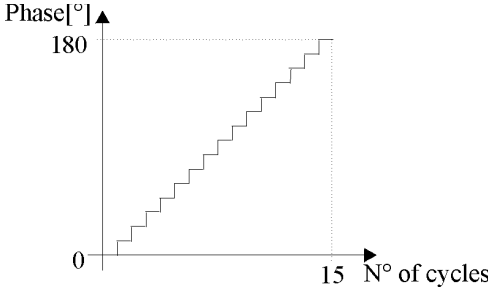


Fig. 10: Linear profile of the phase

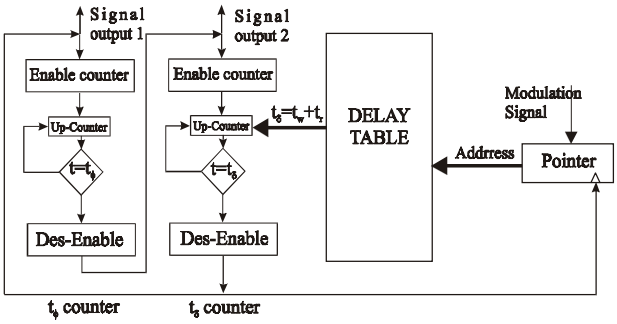


Fig. 11: S-BPSK modulator implemented with FPGA

$$t_r = \frac{6^\circ}{180^\circ}\frac{T_C}{2} = \frac{T_C}{60}$$

Fig. 10 shows the phase changes in the carrier as a function of the number of cycles. Each phase change corresponds to the time $2t_r$ generating a "lineal" profile. It is possible to generate different profiles controlling the time delay which is introduced in each cycle of the carrier.

IV.2 Logic scheme of the modulator

In Fig. 11 shown a logic scheme to implement S-BPSK on the CMRC, suitable testing several phase transition profiles. This figure shows two counters that generate the time intervals t_φ and t_δ on the voltage v_{ab} (Fig. 1 b). These counters set up the sequence of the driving signals E1 and E2. The time counter of t_φ defines the time interval when the voltage v_{ab} is null, whereas the time counter of t_δ determines the voltage pulse width (±Vcc) Both counters are programmable. The first counts a fixed time t_φ ($T_c/6$). The second counts the value of pulsewidth time ($t_w = T_c/3$) corresponding to the non modulated carrier, plus the time delay t_r that is introduced by the S-BPSK, this is $t_\delta = t_w+t_r$. The counter reads the time t_δ from a table which stores all the possible time delays. This table is addressed by a pointer. Normally the pointer addresses a location where $t_\delta = t_w$. When a symbol changes the pointer moves it following the address where $t_\delta = t_w+t_r$ is store. After each cycle it increases one position to locate the new time delay. After n cycles it stops and returns at the initial position ($t_\delta = t_w$). Each time a counter ends its count, it generates an output pulse. This signal starts the other counter, and is used to conform the driving signals of the power switches, as shown in Fig. 12.

V. EXPERIMENTAL RESULTS OF S-BPSK

The modulator signal output 1 and 2 directly drives the

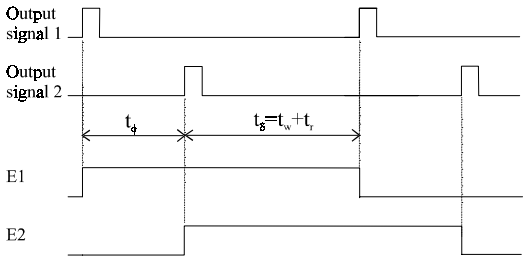


Fig. 12: Output signal of the modulator and excitation signal

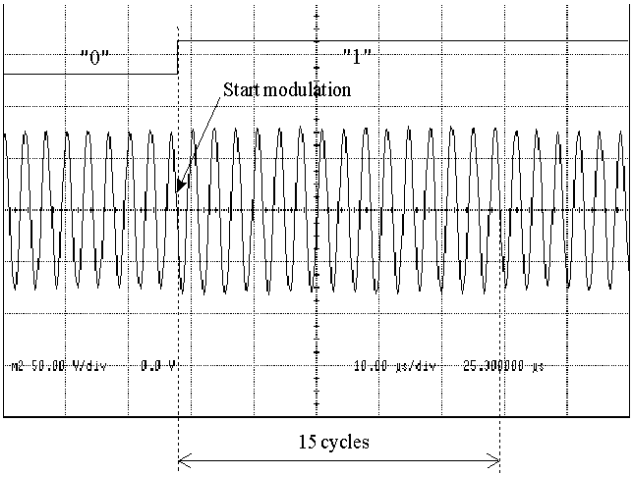


Fig. 13: Carrier wave modulated (50V/div, 10μs/div)

power converter shown in Fig. 5. Experimental results obtained with phase modulated CMRC are shown in Fig. 13 and Fig. 14. This test was performed with nominal load. In Fig. 13 the filter output signal of the CMRC is depicted. It shows the use of 15 carrier cycles to make the transition from one symbol to the next. This is equivalent to shifting the phase of the carrier 12 degrees per cycle. It also shows that after 15 cycles, the carrier changed its phase in π rad. The small increase of the amplitude is due to the decreasing of the transmission frequency during the modulation process.

Fig. 14 depicts the pulse width voltage v_{ab} and the output current of the inverter when the modulation process starts. It shows that the MOSFETs are turned-on as ZVS and that the pulse width increases 38 nsec from the carrier pulse width 1.1 μsec.

VI. CONCLUSIONS

A voltage-clamped mode voltage resonant converter was employed in the implementation of DGPS transmitter. Based on design tools previously developed by the authors, the converter and the output filter were designed, guaranteeing that the four MOSFETs of the converter turn-on with zero voltage. The proposed design improves the efficiency of the transmitters through soft turn-on of the power switches and reduce the number of power components. In addition, it provides safe operation under load variation in a controlled and predictable neighbourhood the operation point.

A stepped binary phase shift keying (S-BPSK) was proposed to modulate the transmitter carrier with the GPS signal. S-BPSK allows maintaining the CMRC operating in mode A and reduce the bandwith of the transmitter signal. The digital implementation of the modulator on a FPGA helped applying S-BPSK directly on the drive of the MOSFETs. The CMRC was built and experimental results show that it is capable of managing a SWR equal or less than 2 between output of the converter and the load even during the modulation process.

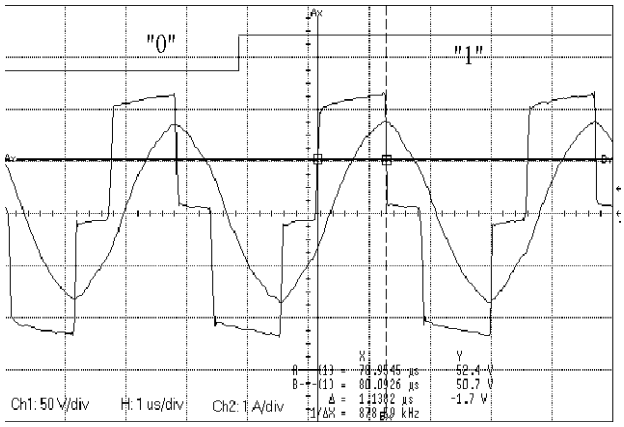


Fig. 14: Voltage and current wave forms at the output of the CMRC when modulation star (50V/div, 1A/div, 1μs/div).

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