The Use of a Soft-Switched Converter (Modified ACRDCL) In Switched Reluctance Drives

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Abstract **- In this paper we propose the use of a Soft - Switched Converter, implemented as a Modified Actively Clamped Resonant DC Link (Modified ACRDCL) converter, to drive a Switched Reluctance Machine. Our objective is to show that the combination of this kind of soft-switched converter with a switched reluctance machine is one of the best combinations for medium-power AC drive applications**.

I. INTRODUCTION

In many motion control applications, it is desirable to attain a high power density. In other words, excessive weight and volume are mostly unwanted characteristics in motion systems [1]. Lipo [2] has shown that the "principle of using a switching power converter to deliver currents of optimum waveform to match that of the emf of energy conversion within the machine" allows the construction of an electric motor of higher power density. With this purpose, a switched reluctance machine has been developed and pointed by Lipo as a model for this family of machines.

The problem now is to find out a converter that has a higher switching frequency with low losses. One way to achieve this goal is to try to force the current or voltage, at the instant of switching, to go down near zero. The resonant converters allowed us to do this. Many kind of topologies of resonant converters has been tried so far. The Actively Clamped Resonant DC link (ACRDCL) converter has been determined by several authors as the best soft - switching converter topology for medium - power AC drive applications as described in [3]. In this work we will use a resonant converter, which has been denominated by Rolim [1] as the Modified ACRDCL converter, and show some advantages of this converter over a simple ACRDCL converter.

II. SRM DRIVES: BASIC OPERATION

As described in [4] SRMs are doubly salient, singly excited electric motors with passive (winding less) rotors. Their concentrated coil phases are turned on sequentially, to produce torque, through D.C. voltage pulses which result in unipolar controlled current. The rotor position displayed in fig.1 is defined as the aligned position with respect to the marked phase. At this position, for this phase, the reluctance is minimum or the inductance is maximum. In a 6/4 SRM, when the rotor is displaced by 45º in any direction, a unaligned position is reached. When it happens, its reluctance is maximum. Energizing phase A, as shown

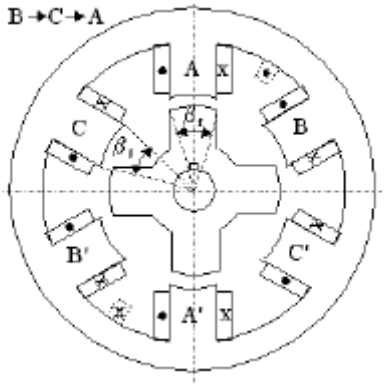

Fig. 1: Cross Section of a 6/4 SRM.

in Fig.1, while the other phases are not conducting, the rotor will move. This movement will align the poles in order to get the minimal reluctance. Sequentially energizing phase B, while the other phases are not conducting, the rotor will move in order to get the minimal reluctance. The same will happen to phase C. This commutation process is repeated periodically, which make sure that the rotor will move stepwise, like a stepping motor. This kind of movement will bring some drawbacks, like very poor stability and a limited torque capability output. This problem of the movement can be overcome if the commutation is synchronized with the rotor position, using a sensor to inform the position of the rotor, or by means of some position estimation method, which fed back this estimation to the motor controller, and each phase receives a current pulse immediately before the rotor reaches the aligned position [5]. Because of its simple mechanical construction, in comparison to other motors, the SRM has considerable advantages. Due to lower heat losses and absence of temperature-sensitive structures in the rotor, the need of few material and lower capital investments in manufacturing machinery and finally due to the fact that a concentrated stator windings are less prone to faults between phases, the SRM has a higher efficiency, better thermal behavior, low production costs, a high reliability and easiness of repair.

Besides these advantages, the SRM has some problems so that, in many applications, its use is not advisable. Maybe its worst drawback is the torque pulsation, which can only be reduced with a more improved current control and the necessity of position feedback for the motor to operate at all [6]. These factors are currently preventing the application of SRM, for example, in many-produced con-

sumer goods, general-purpose drive systems or servo-drives.

III. The Converter chosen to drive the SRM

First of all, it's important to explain how a converter works. We will explain the 'asymmetric bridge' converter, which is also termed 'classic' converter topology by VUKOSAVIC, as shown in figure 2. This converter, according to [6], has the follow operation properties:

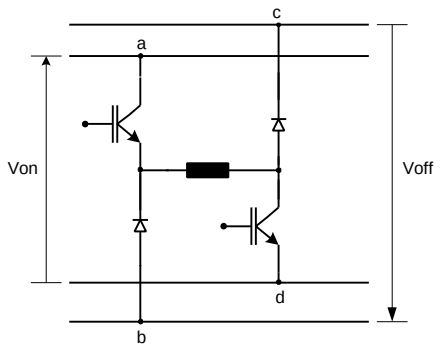

Fig. 2: One phase of a Classic SRM Converter with Turn-on and Turn – off Voltages

- This converter is capable to apply voltage pulses of reverse polarity in one phase, that allow a fast demagnetization when the switch is turned-off, and the current is commutated to the next one. Is this circuit, the demagnetization voltage is equal to the voltage supply in each one of the phases. The turn-on and the turn-off schematic are also shown in figure 2.
- In this converter, the current can have different controllers for each one of the phases. It allows that an operation with any degree of phase current overlaps.

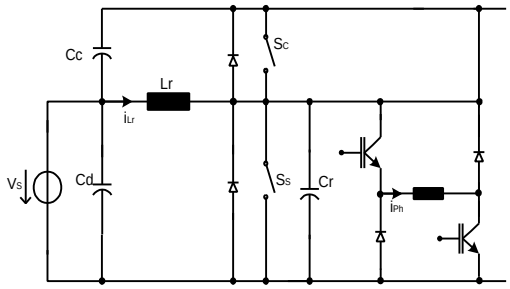

Fig.3 : The modified ACRDCL SR converter proposed

The chosen converter circuit has its schematic shown in figure 3. Rolim [1] defined it as ***modified ACRDCL SR converter***. Its topology is very similar to the ACRDCL converter. The difference consists in connecting the upper diodes of each phase leg directly to the clamp rail as described in [1] and short circuiting the resonant capacitor Cr, during the boost period of the resonant link, due by the Ss switch. The reason to use this converter is a better efficiency with a SR drive in relation to a simple ACRDCL converter. As described in [6], the proposed modification is cost effective and allows the connection of a higher voltage on the phase windings during the period when the phase current (i_{Ph}) is commutated (turned-off).

IV. Operation of the proposed converter

An equivalent circuit for the ACRDCL converter is shown in Fig. 4. In this converter the load current is represented by the current source i_0. As in the standard ACRDCL circuit, the DC link in the proposed converter pulsates continuously between zero and $K_c V_s$; the output switches will be able to change their state only when the DC link voltage is zero, as shown in figures 5 and 6. Therefore, it is possible to affirm that the losses in the output stage will be lower than in the standard ACRDCL converter.

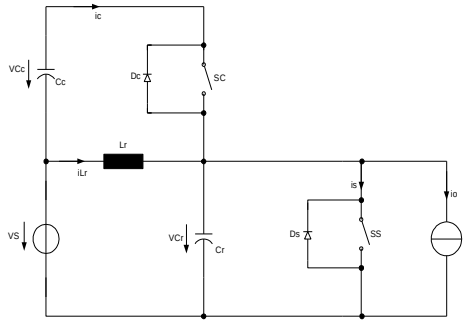

Fig.4: Equivalent circuit for ACRDCL

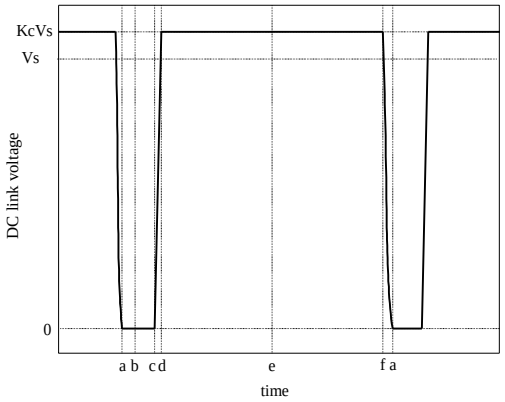

Fig. 5: DC Link Voltage

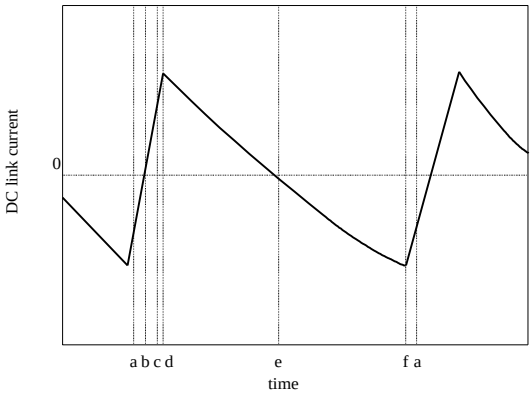

Fig. 6: DC Link Current

Table 1: Operating sequence of ACRDCL

Instant	States Sequence
a	Ds Conducts
b	Ds turns off , Ss Conducts
c	Ss turns off
d	Dc Conducts
e	Dc turns off , Sc conducts
f	Sc turns off

The sequence of states in one cycle of the DC Link is described in table one. The cycle period of this converter can be summarized in four steps that can be described as **boost time** (from instant **a** to **c**), **rising resonant transition** (from **c** to **d**), **clamp period** (from **d** to **f**) and **falling resonant transition** (from **f** to **a**). A better explanation of each step is described below.

- *Boost Time (from instant **a** to **c**)*

During the period of time between a to b, the diode *Ds* conducts the link current from the preceeding cycle, which flows back to the DC supply. The magnitude of i_{Lr} decreases linearly thereby, under the influence of the supply voltage V_S. While *Ds* is conducting, the switch S_S can be turned on under nearly zero voltage, with low turn -on losses. There will be an instant when i_S reverses and begins to flow through S_S, which will be closed for a short period of time. During this time, I_{Lr} is further linearly boosted. When I_S reaches a preset 'trip' current level I_T, S_S is switched off at ZVS conditions, because C_r doesn't allow a sudden change of the voltage across it.

- *Rising resonant transition (from instant **c** to **d**)*

At $t = t_C$, the switch S_S is turned off and the link current is diverted into the resonant capacitor C_r. The initial current in C_r will be the 'trip' current value I_T, which was flowing through S_S at the end of the boost period. The voltage v_{Cr} will then immediately start a rising oscillation toward its natural peak. This period ends when v_{Cr} reaches the clamping voltage level $K_C V_S$.

- *Clamp period (from **d** to **f**)*

The diode begins to conduct (instant *d*) when the DC link voltage reaches the clamping level $K_C V_S$. While D_C is conducting, the clamp switch S_C can be turned on under ZVS conditions. If the clamp capacitor is large enough, the link voltage v_{Cr} and the clamp voltage v_{Cc} remain approximately constant during the whole clamping process. In this case, the current i_{Lr} decreases almost linearly, until the clamp current i_C reverses and begins to flow through the switch S_C (instant *e*). S_C conducts until i_C reaches a preset value I_C, when S_C is turned off, ending the clamp period. S_C is also switched off under ZVS conditions, because C_C and C_r do not allow a sudden change of the voltage at its terminals.

- *Falling resonant transition (from **f** to **a**)*

As in the case of the rising resonant transition , only the elements of the resonant tank are active. At $t = t_f$, switch S_C is turned off and the link current begins to be drained from the resonant capacitor C_r. The initial current in C_r will be the 'trip' current value I_C, which was flowing through S_C at the end of the clamp perod. The voltage v_{Cr} will then immediately start to falling oscillation, and the period ends when v_{Cr} reaches the zero voltagwe level, when D_S begins to conduct (instant *a*), starting a new cycle.

The total period of the resonant DC link pulsation is given by the period of time that describes all the steps above, and the 'boost factor' k_b and, consequently, the DC link frequency can be determinated using the equations as described below.

$$K_b = \frac{I_T \cdot Z_r}{Vs} \tag{1}$$

$$f = \frac{w_r}{2 \cdot \left[k_b + \sin^{-1}\left(\frac{(K_c - 1)}{\sqrt{1+(k_b)^2}} \right) - \tan^{-1}(-\frac{1}{K_b}) \right]} \tag{2}$$

V. THE VOLTAGE CONTROL AT THE CLAMP CAPACITOR

The objective now is to create conditions to keep the clamp voltage regulated. It is done by keeping in zero the net charge transferred to the clamp capacitor C_C. This can be achieved by actuating on either the 'trip' current value I_T for the boost period or the turn-off current value I_C for the clamp period. It is used a PI controller to make a closed-loop control of v_C. In this paper, I_C has been selected as the actuanting variable, while I_T is kept constant. However, I_C should not fall below a lower limit, to ensure that the resonant tank will have sufficient energy to resonate the DC link voltage down to zero. An upper limit should also be set, for overcurrent protection. It is important to implement some strategy, as the use of a limiter, to avoid excessive oscillation of the clamp voltage in the event that saturation occurs. This is usual when a PI controller is used with this kind of saturable actuating signal.

If the clamp capacitance is large, so that the clamp voltage changes much slower than the DC link oscillation, then the current that flows into the clamp capacitor can be average. In this case, the small-signal behaviour of the clamp voltage control can be described by the block diagram shown below, where the variation of the average current in the clamp capacitor is considered equal to the variation of the actuating signal DI_C^{ref}, for small changes of the clamp voltage references. If the disturbance input DI_C^d is neglected, the transfer function of this control system can be written as

$$G(s) = \frac{1 + s \cdot T_i}{1 + s \cdot T_i + s^2 \dfrac{T_i C_C}{k_p}} \qquad (3)$$

The response of the clamp voltage control to sudden variations of the current injected in the clamp capacitor, as occurs for instance when the motor is in standstill, can be obtained by neglecting the clamp voltage reference input DV_C^{ref} and taking the disturbance input DI_C^d as the main system input :

$$\frac{\Delta V_C(s)}{\Delta I_C(s)} = \frac{s \cdot T_i}{1 + s \cdot T_i + s^2 \cdot \dfrac{T_i \cdot C_C}{k_P}} \qquad (4)$$

The clamp factor k_C should be chosen acording to the supply voltage and to the voltage rating of the power semiconductor devices. As described in [6], with a industry-standard power modules rated at 600 V and with a rectifier AC voltage equal to 300 V, a clamping factor of approximately 1.5 would be a good choice, yielding a maximum voltage stress of 450 V.

VI. The Active Rectifier in the Input Stage

With respect to the conducted EMI, produced by this converter, if a diode rectifier with large DC link filter capacitance feeds the DC link, no significant improvement can be expected. In this case, the large DC link filter capacitance practically decouples the input rectifier from the rest of the converter, so that it is relatively irrelevant if a hard-switching converter is used in the input stage. However, the input current is very distorted, with poor power factor and high harmonic content if a diode rectifier is used in the input stage. As more and more rigorous standards for energy quality are prescribed, diode rectifiers may become unacceptable due to input EMI filtering requirements.

A potential substitute for diode rectifiers would be an active rectifier with control of the input current as shown in figure 7. If this kind of rectifier is used with ACRDCL converters, then the zero-voltage notches of the resonant DC link can be also used to commutate the input switches under ZVS conditions. Additionally, regeneration is also possible with this topology.

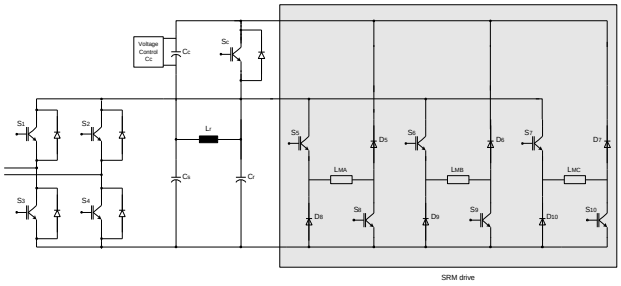

Fig. 7: ACRDCL converter with active rectifier in the input stage

VII. Simulation Analysis

A simulation model for the proposed converter has been developed using Pspice. The main objectives of the digital simulations that have been carried out within the scope of this work is to demonstrate the feasibility of the proposed system. A detailed model of the SR motor has been used, with realistic magnetization and torque production characteristics [7]. Figure 8 shows the input current to the active rectifier, its control reference signal and the mains voltage, indicating that unity power factor is achieved. The control signal amplitude is changing because the steady state has not yet been reached.

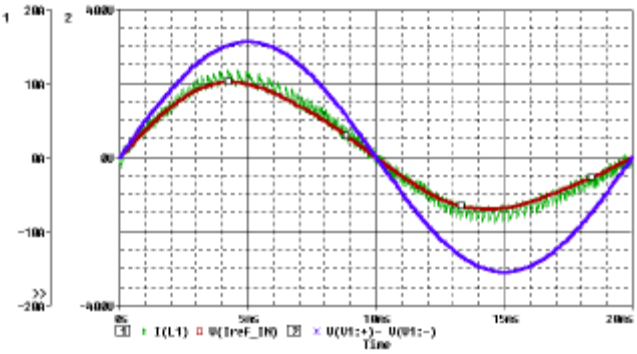

Fig. 8: Input current and voltage

Figure 9 shows the output current pulses to each phase of the SR motor, produced by the modified ACRDCL converter. The motor is driven in the constant current-controlled mode, used for low to medium speeds. The resulting torque waveform is shown in figure 10.

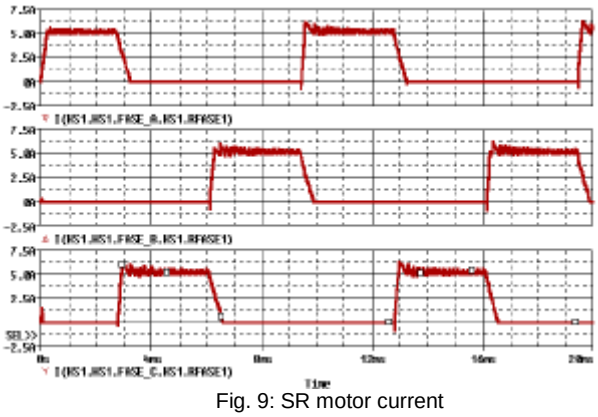

Fig. 9: SR motor current

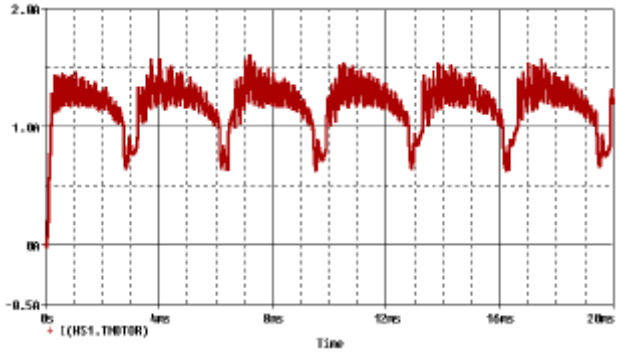

Fig. 10: Torque produced by the SR motor

Figure 11 shows the resonant DC link voltage and the current at one of the input switches and its associated anti-parallel diode, in order to illustrate the soft-switching characteristic.

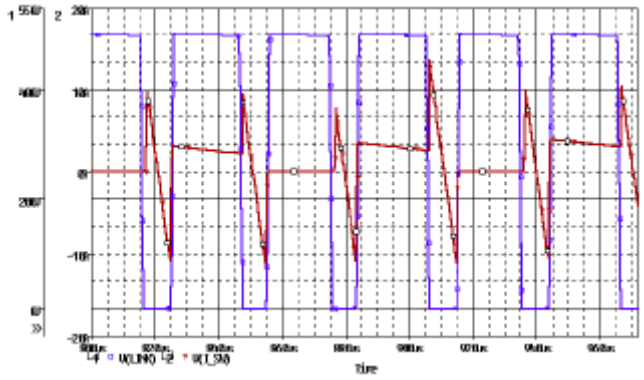

Fig. 11: Input current commutation

VIII. Conclusions and Suggestions for Further Works

In this work a modified actively clamped resonant DC link converter has been simulated. The converter has been applied to a drive system comprising a SR motor and an active rectifier. Simulation results have shown that this configuration has a good potential for implementation in medium-power SR drive systems. The input current can be regulated to achieve a sinusoidal waveform with low-level ripple with controlled power factor. The converter switches operate under zero voltage commutation conditions, allowing for high switching frequency or size reduction of the heat sink. The next steps of this work will be the implementation of the proposed circuit for experimental validation of the simulated results.

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