A Power Recycler for UPS Burn-In Test with Reduced Number of Switches: Analysis, Design and Implementation

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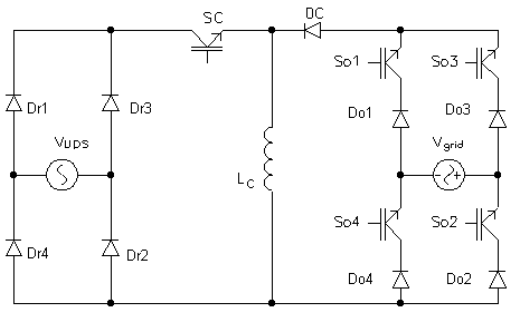
***Abstract* - The aim of this paper is to present a converter to simulate the load in burn-in tests of UPS´s. The use of the power recycler to replace the resistor load bank was proposed in literature to reduce the energy waste in burn-in tests. The test can be accomplished with great energy savings because most of energy that was lost by heating in the resistor load bank can be recycled, i.e., sent back to the grid. As electrical energy is becoming a very strategic product in nowadays, the power recycler has a very useful application in order to reduce the energy waste and the cost of the test. The more efficient is the converter of the power recycler the more energy can be recycled and saved. The proposed converter works in such direction because it has a reduced number of switches compared to the proposals in literature. This fact reduces the converter conduction and switching losses, increasing its efficiency. This fact allows more energy being sent back to the grid and reducing the energy waste. In this paper is presented the analysis of operation in discontinuous conduction mode, a comparative study of the power losses involved and a prototype was implemented in laboratory to confirm the predicted performance. The proposed converter has obtained an efficiency increase compared to a similar converter.**

I. Introduction

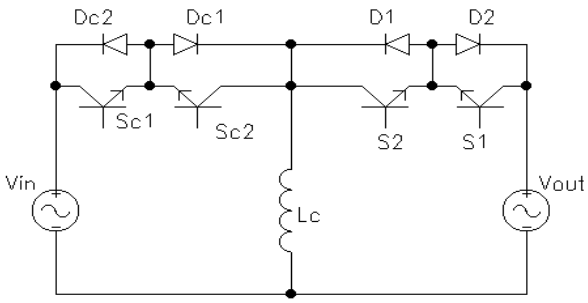
The burn-in test of an AC or DC power supply is accomplished to guarantee the quality of the product. During the test many problems can be detected, avoiding furnishing bad equipment to the market. In the burn-in test the power source is submitted to a 50 to 100% of the nominal load during a period of 24 up to 72 hours. Traditionally a resistor load bank is used to simulate the load. The power recycler replaces the resistor load bank with the advantage that most of energy can be sent back to the grid. This fact results in great energy savings. Typically around 85% of the energy that would be lost by heating if the resistor bank was used can now be reutilized. The power recycler and its economical and ecological advantages were discussed before in literature [1,2,3,4,5]. The proposed topology presents the advantage of having a reduced number of switches. This fact reduces the conduction and switching losses of the converter, increasing its efficiency and reducing the cost of the equipment and of the test.

II. The Proposed Converter

In Fig. 1.a is shown a similar power recycler presented in [1]. The converter is composed by an input rectifier, a DC/DC converter and a current inverter. Input and output LC filters have been omitted but they are necessary to eliminate the high frequency harmonics in the current due to the switching. The input rectifier is responsible for furnishing a rectified sinusoidal voltage to the DC/DC converter. The DC/DC converter imposes its input and output current with a rectified sinusoidal waveform by imposing a sinusoidal current in the inductor of the converter. The current inverter converts the DC/DC converter rectified current into a sinusoidal current to be sent back the grid.

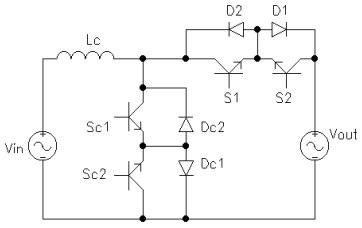


(a)

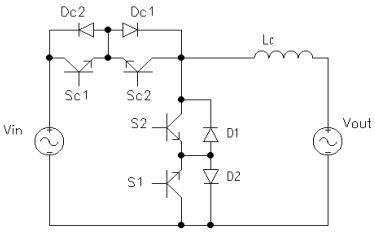


(b)

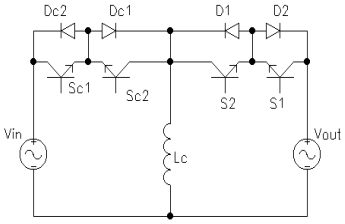
Fig. 1. (a) The power recycler proposed in [1]
(b) The proposed power recycler



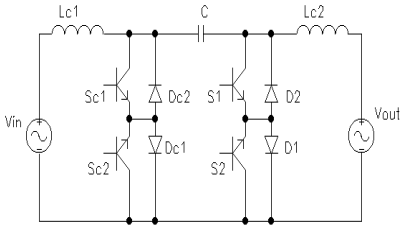
Boost



Buck



Buck-boost



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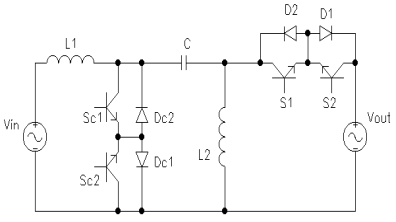

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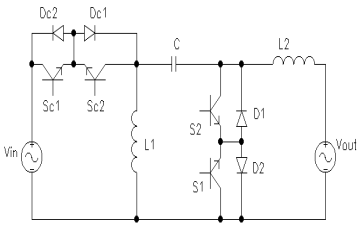


Zeta

Fig. 2 – The six basic structures

In Fig. 1.b the proposed converter is presented and it is possible to notice that a bi-directional converter is used. In this case the use of the AC/AC converter presents a reduction in the number of stages if compared to [1]. This converter has 8 switches and in [1] there are 14. The reduction in the number of switches reduces the losses of the converter and the overall cost of the power recycler. A family of converters can also be obtained using the six basic converters as in [1]. Fig. 2 shows the six basic topologies of the proposed converter.

III. Operation Analysis

To describe the operation principle the buck-boost topology was used. For the positive half cycle of the UPS voltage, the switches S_{C1}, D_{C1}, S_1 and D_1 are utilized. For the negative half cycle of the UPS voltage, the switches S_{C2}, D_{C2}, S_2 and D_2 are used. S_{C1} / D_{C1} and S_{C2} / D_{C2} operate in high frequency and S_1 / D_1 and S_2 / D_2 operate in the grid frequency. S_1 and S2 are alternately active during each half period of the grid to enable the operation of the freewheeling diodes D_1 and D_2, respectively (in fact a small dead time around the zero crossing is used to guarantee a more safe control). Fig. 3 shows the control signals of S_{C1}, S_{C2}, S_1 and S_2 related to the UPS voltage.

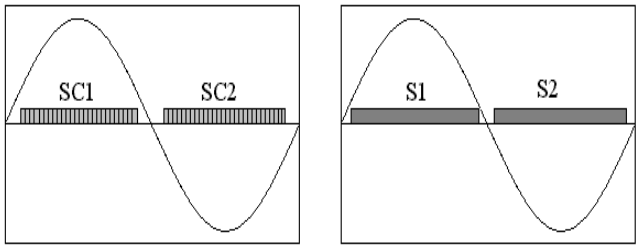


Fig. 3. Control signals of S_{C1}, S_{C2}, S_1 and S_2

To analyze the high frequency operation the positive half cycle of the UPS voltage will be considered because the operation in the negative half cycle is similar. The discontinuous conduction mode is discussed. In a switching period there are 3 stages:

1st Stage (t_s): During this time, S_{C1} is on. The equivalent circuit is shown in Fig. 4a. The UPS current circulates through S_{C1}, D_{C1} and L_C rising linearly from zero. The energy is stored in the inductor during this interval.

2nd Stage (t_d): When S_{C1} is blocked at the end of first stage, diode D_1 turns on to transfer the inductor energy to the output (grid) through S_1. The inductor current decreases linearly, reaching zero at the end of this interval. Fig. 4b shows the equivalent circuit during t_d.

3rd Stage: During this interval the inductor current is zero, all the switches are off and no energy is processed.

In DCM the control is simpler because no current loop is necessary to impose a sinusoidal current at the input or output of the power recycler. Fig. 5a shows the UPS drained current using a smaller switching frequency to emphasize that its peak follows the sinusoidal waveform of the UPS

voltage due to DCM operation. In Fig. 5b the power recycler output current is shown and its peak presents also a sinusoidal shape. The mathematical analysis will be omitted because it has been extensively discussed in [1].

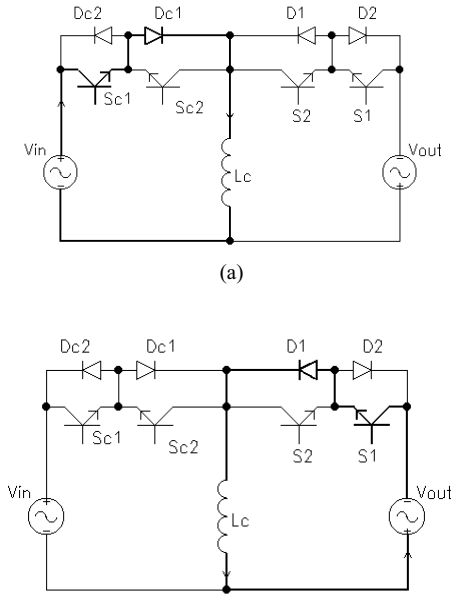


Fig. 4. (a) Equivalent circuit during t_s
(b) Equivalent circuit during t_d

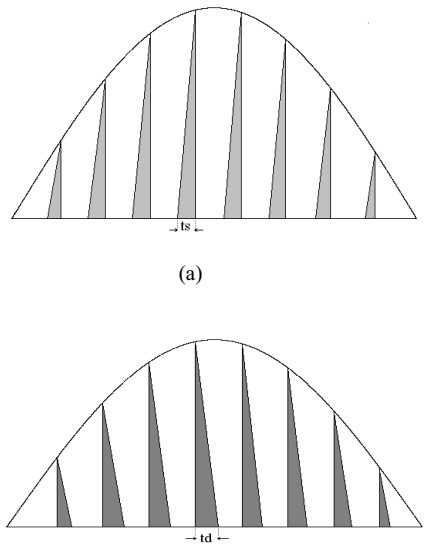


Fig. 5. Input and output current in a smaller switching frequency
(a) UPS drained current
(b) Grid inject current

III. THE EFFICIENCY ANALYSIS

The focus of this work is to verify if the reduction in the number of switches of the proposed topology provokes an inherent reduction in the converter losses and the consequent increase in the efficiency. The efficiency analysis was derived for the proposed structure and for the proposal in [1]. As IGBT´s were used in [1], the same switch was employed in the proposed converter. All losses in the IGBT: conduction, turn on, turn off (including the tail current) according to [6] and in the diodes: conduction and switching were considered.

The losses were first calculated in a switching period. Then, using this result, the losses were obtained by integration in a period of the grid frequency since the UPS and grid voltages vary in a sinusoidal way.

The total power loss in the proposed converter is:

$$P_{T_{AV}} = P_{Sc12\ AV} + P_{S12\ AV} + P_{Dc12\ AV} + P_{D12\ AV} + P_S \quad (1)$$

where:

$P_{T\,AV}$: total power losses of the power recycler;
P_{Sc12AV} : S_{C1} and S_{C2} losses;
P_{S12AV} : S_1 and S_2 losses;
P_{Dc12AV} : D_{C1} and D_{C2} losses
P_{D12AV}: D_1 and D_2 losses;
P_S : snubber circuit loss.

Now each loss presented in (1) will be detailed. The S_{C1} and S_{C2} losses are presented in (2):

$$P_{Sc12_{AV}} = 2.[I_{SCav}.V_{CEsat} + f_s.(\frac{I_{SCpav}.V_{CEblock}.t_{off12}}{2} + \frac{I_T.V_{CEblock}.t_{off23}}{2})] \quad (2)$$

where:

I_{SCav} : average current in the S_C switches and D_C diodes in a grid period;
V_{CEsat} : IGBT saturation voltage;
t_s : on time of IGBT´s;
f_s : switching frequency;
I_{SCpav}: average value of the S_C and D_C current peak;
$V_{CEblock}$: average value of the S_C switches blocking voltage ($\cong 1.8\ V_{UPSrms}$);
t_{off12} : turn off time until the beginning of the tail current $\cong t_f$ ("fall time of the IGBT");
t_{off23} : tail current width ($\cong t_f$);
I_T : IGBT tail current ($I_T \cong I_{SCpav}$).

$$I_{SCav} = \frac{\sqrt{2}\ V_{UPSrms}.D^2}{2\pi\ .\ fs\ .\ Lc} \quad (3)$$

$$I_{SCpav} = \frac{\sqrt{2}\ V_{UPSrms}.D}{\pi\ .\ fs\ .\ Lc} \quad (4)$$

where:

D : duty cycle of S_C switches;
L_c : converter inductance.

The S_1 and S_2 losses are presented in (5):

$$P_{S12_{AV}} = 2.I_{Sav}.V_{CEsat} \quad (5)$$

where:

I_{Sav} : average current in the S_1 and S_2 switches and D_1 and D_2 diodes .

$$I_{Sav} = \frac{\sqrt{2}\, V_{Gridrms}.D^2.\alpha^2}{2\pi\,.\,fs\,.\,Lc} \quad (6)$$

$$\alpha = \frac{V_{UPS}}{V_{Grid}} \quad (7)$$

The D_{C1} and D_{C2} losses are presented in (8):

$$P_{Dc12_{AV}} = 2[V_f \cdot I_{SCav} + f_s.(\frac{1}{2}.V_{Dblock}.I_{rrp}\,.\,t_b)] \quad (8)$$

where:

V_f : diode forward voltage;

I_{rrp}: peak of the diode reverse recovery current;

t_b : time from the occurrence of I_{rrp} to the diode current reaches zero

The low frequency diodes, D_1 and D_2, present only conduction loss due to DCM operation as denoted in (9):

$$P_{D12_{AV}} = 2\,.V_f \cdot I_{Sav} \quad (9)$$

A snubber circuit is normally used and its loss is in (10):

$$P_S = f_s.(\frac{1}{2}.C_s.V_{Cs}^2) \quad (10)$$

The total power losses in [1] is in (11)

$$P_{T_{AV}[1]} = P_{Dr1234} + P_{Sc_{AV}} + P_{Dc_{AV}} + P_{So1234_{AV}} + P_{Do1234_{AV}} + P_S \quad (11)$$

where:

P_{Dr1234} : input rectifier total losses;

P_{Scav} : DC/DC converter switch losses;

P_{Dcav} : converter diode losses;

$P_{So1234av}$: current inverter switches losses;

P_{Do1234} : current inverter diodes losses.

The input rectifier, converter switch, converter diode, inverter switches, inverter diodes losses are described in (12, 13, 14, 15 and 16). The converter diode has only conduction loss because of DCM operation. The snubber losses are the same as the proposed converter.

$$P_{Dr_{1234}} = 4\,f_s \cdot (V_f \cdot I_{SCav}.t_s + \frac{1}{2}.V_{Dblock}.I_{rrp}\,.\,t_b) \quad (12)$$

$$P_{Sc_{av}} = I_{SCav}.V_{CEsat} + f_s.(\frac{I_{SCpav}.V_{CEblock}.t_{off12}}{2} + \frac{I_T.V_{CEblock}.t_{off23}}{2}) \quad (13)$$

$$P_{Dc_{av}} = V_f \cdot I_{Sav} \quad (14)$$

$$P_{So1234av} = 4\,.I_{Sav}\,.V_{CEsat} \quad (15)$$

$$P_{Dr1234av} = 4\,.V_f\,.I_{Sav} \quad (16)$$

To compare the efficiency between the two converters a power recycler for the proposed converter and for [1] was calculated. The design procedures are exactly the same as presented in [1]. The conditions are:

$V_{UPS} = 220\ V_{rms}$, $V_{grid} = 220\ V_{rms}$, $P_o = 500$ W,
$D = 0.4$, $L_c = 387\mu$H, $f_s = 20$ kHz.

The IGBT used in the prototype is IRGPH50KD2. The characteristics of the IGBT itself, the intrinsic diode and the other required data are:

$V_{Cesat} = 3{,}5$V, $t_{off12} = 320$ns, $t_{off23} = 320$ns, $V_f = 3$V,
$I_{rrp} = 10$A, $t_b = 164$ns, $C_S = 6{,}8$ nF.

The obtained power dissipation in [1] is:
$P_{(AV)\ Dr1,Dr2,Dr3,Dr4} = 38.26$W,
$P_{(AV)\ SC} = 16.54$W,
$P_{(AV)\ DC} = 3.07$W,
$P_{(AV)\ So1,So2,So3,So4} = 14.34$W,
$P_{(AV)\ Do1,Do2,Do3,Do4} = 12.29$W,
$P_S = 10.66$W.
Total losses of [1] = 95.16W

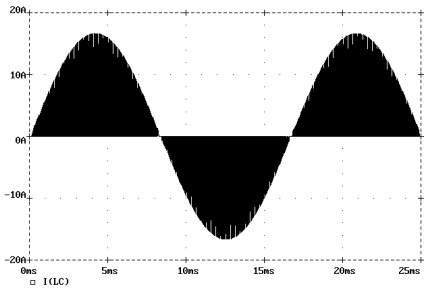
The obtained power dissipation for the proposed converter is:
$P_{(AV)\ SC1,\ SC2} = 33.08$W,
$P_{(AV)\ S1,\ S2} = 7.17$W,
$P_{(AV)\ DC1,\ DC2} = 19.13$W,
$P_{(AV)\ D1,D2} = 6.14$W, $P_S = 10.66$W.
Total losses = 76.18W

Using the referred IGBT, the resulting efficiency is 80,97% for [1] and 84,8% for the proposed converter, corroborating the expect performance.

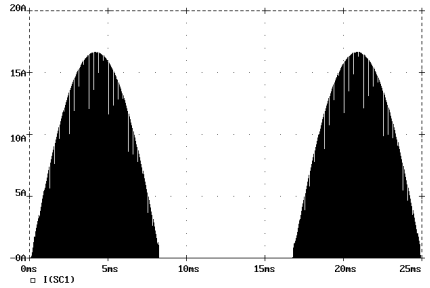
IV. Simulation and Experimental Results

The designed converter was simulated using Pspice. The results have confirmed the performance of the proposed and are shown in Fig. 6.

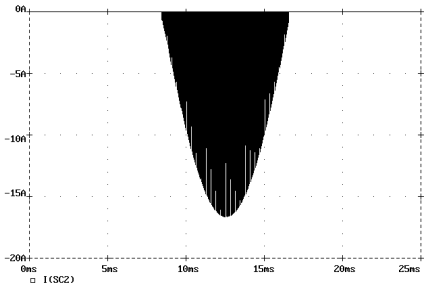
A prototype was implemented in laboratory to confirm the theoretical studies. The IRGPH50KD2 which has a parallel diode included was used. In Fig. 7a are shown the UPS drained current and the UPS voltage. The current sent back to the grid and the grid voltage is in Fig. 7b. In Fig. 7c, the converter inductor current are presented. The currents of the UPS and of the grid have presented low THD and high power factor. The photos of the prototype are shown in Fig. 8. An isolating transformer was used to simulate the UPS. Input and output filters to eliminate the high frequency harmonics in the current were also used. The measured efficiency is presented in Table 1. It is important to notice that the prototype presented in [1] was obtained with other IGBT and diodes. The use of the internal diode of the IGBT which has higher recovery time and higher forward voltage increases the losses. So if external diodes were used the efficiency increase would be increased.



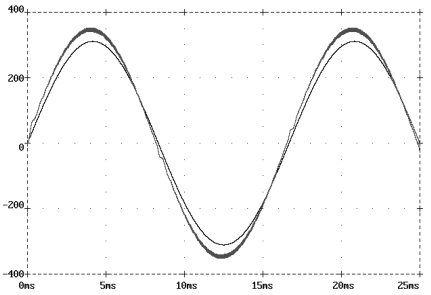
(a) Buck-boost inductor current



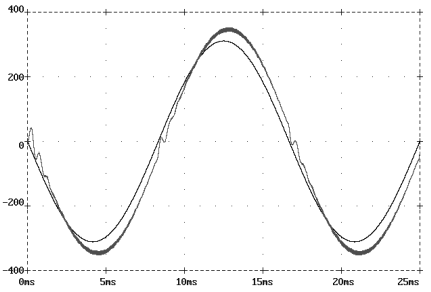
(b) S_{C1} and D_{C1} current



(c) S_{C2} and D_{C2} current

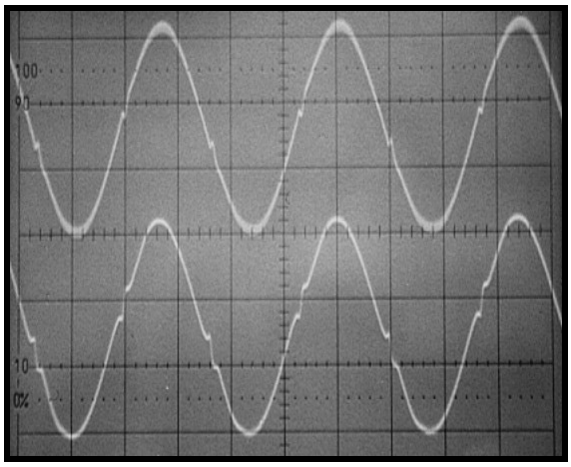


(d) UPS voltage 200V/div and UPS drained current 2A/div

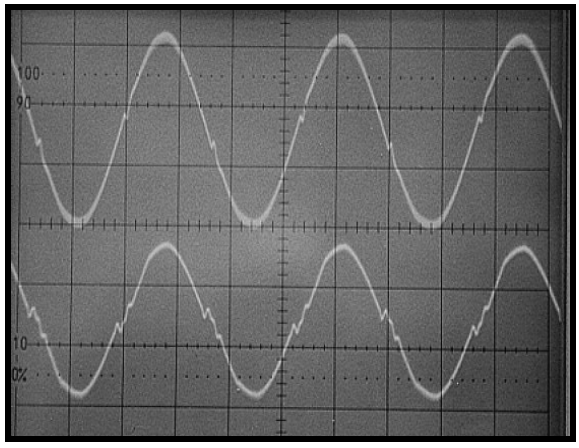


(e) Grid voltage 200V/div and grid injected current 2A/div

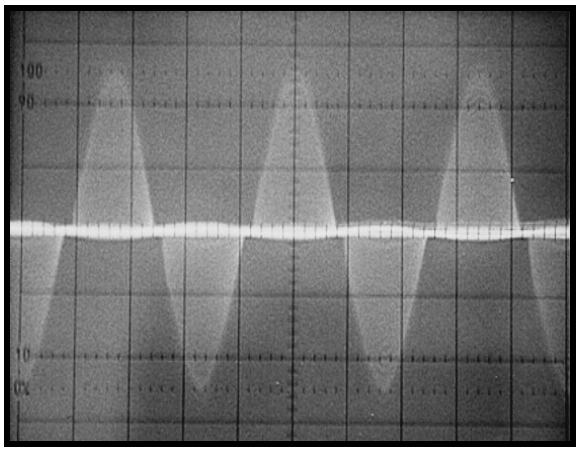
Fig. 6. Simulation Results



(a) Upper trace: UPS voltage 200V/div
Lower trace: UPS drained current 2A/div

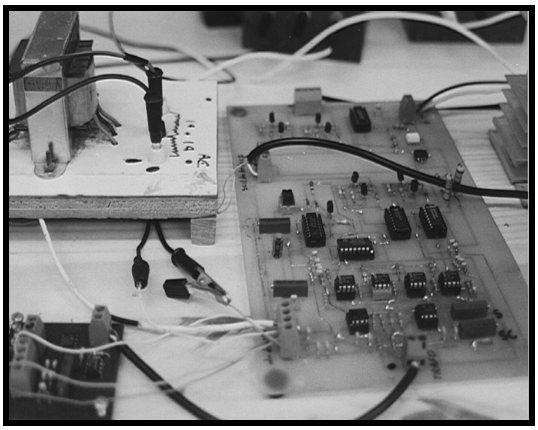


(b) Upper trace: Grid voltage 200V/div
Lower trace: Grid injected current 2A/div

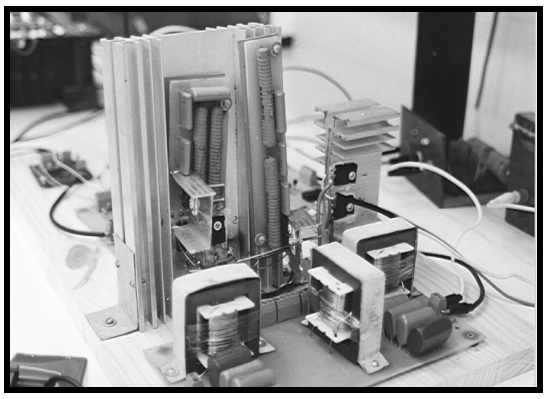


(c) Buck-boost inductor current

Fig. 7. Experimental results



(a) Control circuitry



(c) Implemented prototype

Fig. 8. Photos of the prototype

TABLE 1
CONVERTER EFFICIENCY

P_{in} [W]	94.3	152	212.4	223.8	345
P_{out} [W]	77	124.2	178.5	187.6	290
η [%]	81.6	81.7	84	83.8	84.1

V. CONCLUSION

This paper presents a power recycler with reduced number of switches to be used in the burn-in test of synchronized UPS´s. Using the six basic structures a family of converters can be obtained. A detailed comparative analysis of the total power dissipation of the proposed converter and other structure proposed in literature was done. The proposed converter presented an increase of around 4% in the efficiency. A prototype was implemented in laboratory and the more relevant waveforms and results are presented. As the efficiency of the converter is important soft commutation could be used to improve this parameter.

VI. REFERENCES

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