A New ZCZVT Commutation Cell for PWM DC-AC Converters

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***Abstract* – This paper proposes a new auxiliary commutation cell for PWM inverters that allows the main switches to be turned on and off at zero voltage and zero current with controlled di/dt and dv/dt. The reverse recovery losses of the main diodes are minimized and the auxiliary switches are turned on and off at ZCS. The main switches turn-on at zero current can reduce significantly the undesired effects of the parasitic inductances related to the circuit layout. The commutation losses are practically reduced to zero and the EMI emission can be reduced. The operation of the ZCZVT PWM Full-Bridge DC-AC Converter is analyzed and a design guidelines for the auxiliary commutation cell is derived based on the analysis. Experimental results are presented to demonstrate the feasibility of the proposed commutation cell.**

I. INTRODUCTION

With the growing development of power devices technology, switching mode power conversion moves towards high frequency operation, which can lead to high power density and fast dynamic response. For inverters, the operation at high frequency is required to reduce the audible noise, the volume and the weight of filters, as well as to improve output voltage quality. However, at high frequency operation, switching losses and electromagnetic interference (EMI) become significant and must be analyzed in detail.

Power semiconductor devices commutate under two possible techniques: hard and soft. With hard switching, the devices are required to change their states (on and off), while they are subjected at both finite current and voltage values. High switching stresses produced by the overlapping of voltage and current result in high switching losses. To illustrate, the hard switching is shown in Fig. 1(a). Soft switching techniques aim to reduce the mentioned overlap between voltage and current during the commutation. Thus it is possible to reduce switching losses, enabling high frequency operation and achieving higher power density. Soft switching techniques can be classified into two groups: zero voltage switching (ZVS) and zero current switching (ZCS) [13].

In the literature, several soft switching techniques have been proposed for PWM inverters, and nearly all of them operate with ZVS. Typical examples are the auxiliary resonant commutated pole inverters (ARCP) [1-3], the ZVS [4-7] and ZVT (Zero Voltage Transition) inverters [8]. To perform ZVS, the auxiliary commutation circuit only helps main switches turn-on, while snubber capacitors reduce turn-off losses. To illustrate, the current and voltage waveforms of a power switch with ZVS are shown in Fig. 1(b). In some ZVS inverters, the load current charges the snubber capacitors at main switches turn-off, and as results, there is an important dependence between the load current value and the conduction time of the main diodes. Moreover, at high power application where minority carriers devices are usually employed, the turn-off losses caused by tail current cannot be totally avoided with ZVS technique [9]. Minority carriers devices, such as IGBT and MCT, present better performance with zero current switching, which can minimize substantially the mentioned turn-off losses. So, several ZCS techniques applied to PWM inverters are being investigated in the literature [10-12]. However, main switches turn-on losses and the adverse effects of the main diodes reverse recovery were not totally solved yet [12]. Fig. 1(c) shows the ZCS commutation.

In order to overcome the drawbacks of the above mentioned soft switching techniques, in this paper is proposed a new auxiliary commutation cell for PWM inverters, denominated Zero Current and Zero Voltage Transition (ZCZVT). It allows main switches commutations to happen simultaneously with zero voltage and zero current, at both turn-on and turn-off, and in addition it slows di/dt and dv/dt. So, the reverse recovery losses of the main diodes are minimized and the auxiliary switches are turned on and off at ZCS. The main switches turn-on at zero current can reduce significantly the undesired effects of the parasitic inductances related to the circuit layout. The commutation losses are virtually reduced to zero and the EMI emission can be reduced. The zero voltage and current switching is illustrated in Fig.

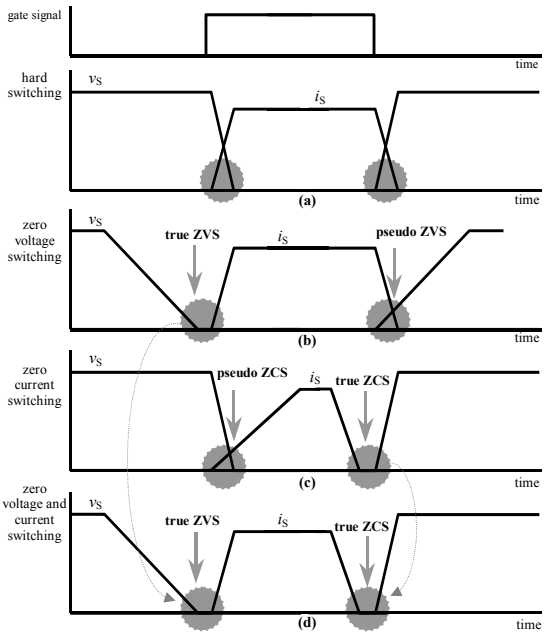

Fig. 1 – Commutations waveforms.

1(d).

The operation of the proposed ZCZVT commutation cell applied to a full-bridge PWM inverter is theoretically analyzed in Section II. Section III presents a design guidelines and a design example. The command circuit strategy is presented in Section IV. The experimental results obtained from a 1 kW ZCZVT full-bridge inverter IGBT based are given in Section V. The last section summarizes the conclusions drawn from this investigation.

II. Principle of Operation

A. The ZCZVT PWM Full-Bridge Inverter

Fig. 2(a) shows the ZCZVT PWM full-bridge inverter. It differs from a hard-switching PWM full-bridge inverter by the presence of an additional shunt resonant network composed of two resonant capacitors C_{R1} and C_{R2}, two resonant inductors L_{R1} and L_{R2}, and two bi-directional auxiliary switch S_{A1}-D_{A1} and S_{A2}-D_{A2}. The auxiliary commutation cell is activated during the switching transitions only.

B. Operation Principles

To simplify the analysis, the output current I_o is considered constant into one switching cycle. The operation of the auxiliary commutation circuit is symmetrical for the cases of $I_o < 0$ and $I_o > 0$. So the operation principle will be explained for one case only, i.e., commutations from D_2-D_3 to S_1-S_4 and from S_1-S_4 to D_2-D_3. As shown in Fig. 3, there are sixteen operating stages during one switching cycle. They are described below:

Stage 1. **(t_0, t_1):** Output current I_o flows through main diodes D_2 and D_3. During this stage the resonant capacitors voltages $v_{CR1}(t)$ and $v_{CR2}(t)$ are clamped at –2E and E respectively.

Stage 2. **(t_1, t_2):** At t_1, S_{A1} is turned on under ZCS. As the current $i_{LR1}(t)$ increases due to the resonance among L_{R1}, C_{R1} and C_{R2}, the current through the main diode D_2 decreases at the same rate. This stage ends when main diode current D_2 reaches zero.

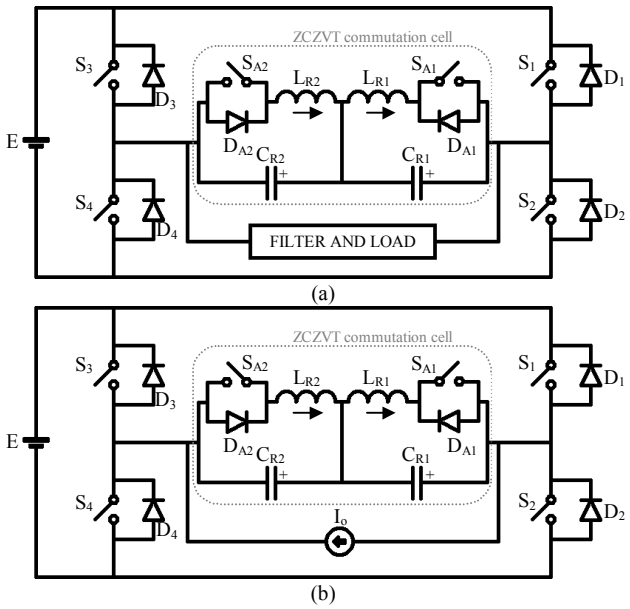

Fig. 2 – ZCZVT full-bridge converter.

Stage 3. **(t_2, t_3):** In this stage, the output current linearly discharges capacitor C_{R2}. The capacitor voltage $v_{CR1}(t)$ increases due to the resonance between L_{R1} and C_{R1}. When $v_{CR2}(t)$ reaches zero, diode D_{A2} begins to conduct.

Stage 4. **(t_3, t_4):** During this stage the resonant capacitor voltages $v_{CR2}(t)$ $v_{CR1}(t)$ evolve in a resonant way. When the sum of $v_{CR1}(t)$ and $v_{CR2}(t)$ reaches input voltage, diodes D_1 and D_4 begin to conduct.

Stage 5. **(t_4, t_5):** While D_1 and D_4 are conducting, main switches S_1 and S_4 must be turned-on to assure ZCS and ZVS. When the current through D_1 and D_4 reaches zero, the main switches S_1 and S_4 turn-on.

Stage 6. **(t_5, t_6):** During this stage current $i_{LR1}(t)$ decreases and when it reaches zero, the diode D_{A1} begins to conduct.

Stage 7. **(t_6, t_7):** When current $i_{LR2}(t)$ reaches zero, diode D_{A2} turns off. During this stage the auxiliary switch S_{A1} must be turned off to assure ZCS and ZVS.

Stage 8. **(t_7, t_8):** When current $i_{LR1}(t)$ reaches zero, diode D_{A1} turns off.

Stage 9. **(t_8, t_9):** Operation circuit at this stage is similar to that of hard-switching PWM full-bridge converter. Output current I_o flows through main switches S_1 and S_4.

Stage 10. **(t_9, t_{10}):** At t_9, the auxiliary switch S_{A1} is turned on again under ZCS. The current $i_{LR1}(t)$ increases due to the resonance among L_{R1}, C_{R1} and C_{R2}. When the current through the main switches S_1 and S_4 reaches zero, the diodes D_1 and D_4 begin to conduct. The voltage across main switches S_1 and S_4 are clamped at zero.

Stage 11. **(t_{10}, t_{11}):** The resonance evolves until the current through the main diodes D_1 and D_4 reaches zero. During this stage the gate signals of main switches S_1 and S_4 can be removed to assure ZVS and ZVS.

Stage 12. **(t_{11}, t_{12}):** In this stage the capacitor C_{R2} is linearly discharged to zero by output current. At this moment diode D_{A2} begins to conduct.

Stage 13. **(t_{12}, t_{13}):** During this stage the resonant inductor current $i_{LR1}(t)$ decrease due to the resonance among L_{R1}, L_{R2}, C_{R1} and C_{R2}. When the current $i_{LR1}(t)$ reaches zero, the diode D_{A1} begins to conduct.

Stage 14. **(t_{13}, t_{14}):** The resonance continues. When the current $i_{LR1}(t)$ reaches zero again, the diode D_{A1} is turned off naturally.

Stage 15. **(t_{14}, t_{15}):** In this stage the capacitor C_{R1} is

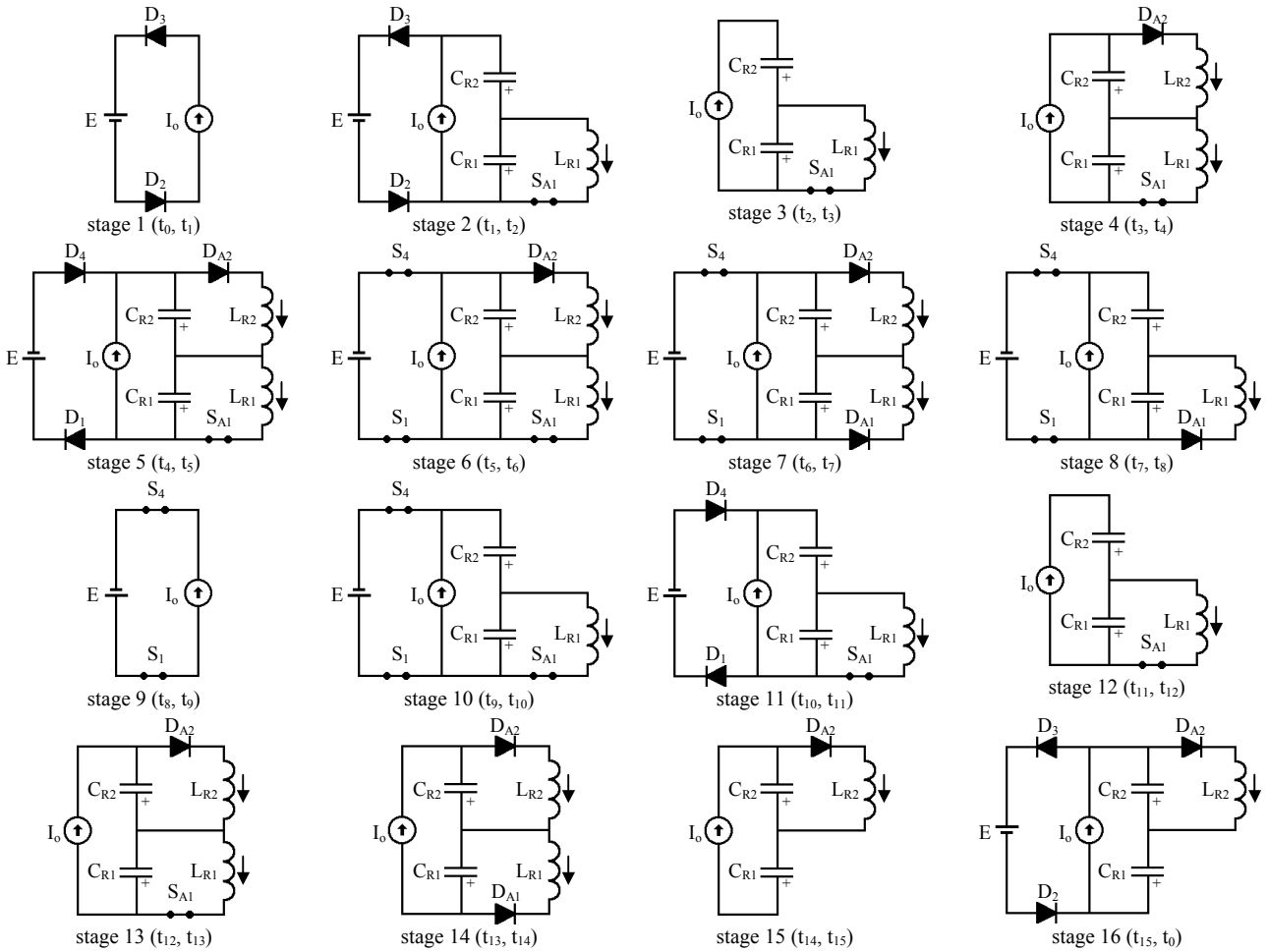

Fig. 3 – Operating stages.

linearly discharged by the output current and the resonant capacitor voltage $v_{CR2}(t)$ increase due to the resonance between L_{R2} and C_{R2}. When the sum of the resonant capacitor voltages $v_{CR1}(t)$ and $v_{CR2}(t)$ reaches the negative of the input voltage, the diodes D_2 and D_3 begin to conduct.

Stage 16. **(t_{15}, t_0):** During this stage the resonant inductor current $i_{LR2}(t)$ decrease due to the resonance among L_{R2}, C_{R1} and C_{R2}. When the resonant inductor current $i_{LR2}(t)$ reaches zero the diode D_{A2} turns off, beginning another switching cycle.

Fig. 4 shows the theoretical waveforms of the converter operation.

III. Resonant Tank Design Guidelines and Example

This section presents a design procedure and an example to determine the resonant tank elements values of the proposed ZCZVT commutation cell. The given inverter specifications consists of:

Output Power	P_o = 1000 W
Input Voltage	E = 200 V
Output Voltage	V_o = 110 Vrms
Output Frequency	f_o = 60 Hz
Output Current Ripple	ΔI = 20%

The design procedure consists of four steps, which are:

a) Find the output current peak. From the specifications:

$$I_o = \frac{\sqrt{2}P_o}{V_o}(1+\Delta I) = 15.43 \text{ A} \qquad (1)$$

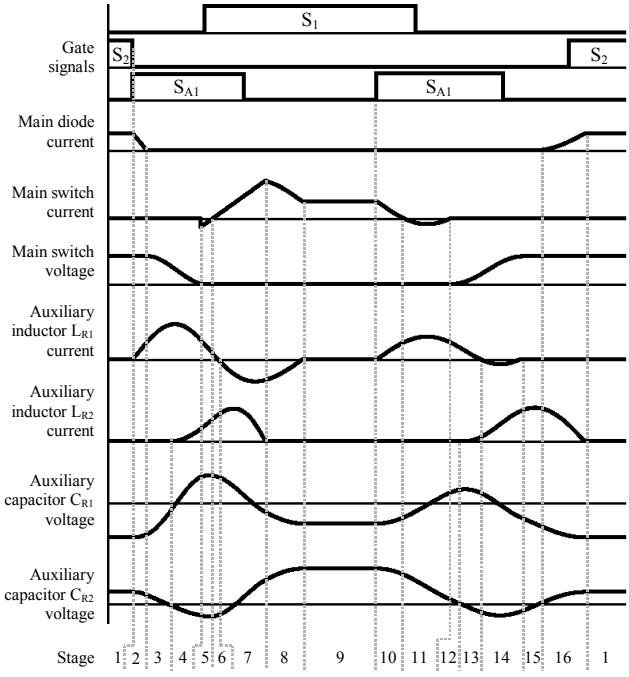

Fig. 4 – Theoretical waveforms.

b) Determine the characteristic impedance. To assure main switches turn-off under ZCS and ZVS, during stages 10 and 11, the current peak diverted from main switch to auxiliary circuit must be larger than the output current peak. From these stages, the current peak through capacitor C_{R2} is given by:

$$I_{pk} = \frac{E}{\sqrt{2}Z} \qquad (2)$$

By (1) and (2), a parameter *k* can be defined as follows:

$$k = \frac{I_{pk}}{I_o} \quad \text{where} \quad k \geq 1 \qquad (3)$$

Choosing $k = 1.1$, which is a practical design value to compensate parasitic losses, the characteristic impedance *Z* is given by:

$$Z = \frac{E}{\sqrt{2}kI_o} = 8.34\,\Omega \qquad (4)$$

c) Determine the resonant frequency. To minimize main diodes reverse recovery, resonant frequency of stage 2 can be chosen to control the di/dt rate during turn-off. The di/dt rate of main diodes at stage 2 can be approximate by

$$\frac{di}{dt} \approx \frac{I_o\omega}{\sqrt{2}asin\left(\frac{1}{2k}\right)} \qquad (5)$$

By using (5), the resonant frequency ω can be obtained as follows:

$$\omega = \frac{\frac{di}{dt}\sqrt{2}asin\left(\frac{1}{2k}\right)}{I_o} \qquad (6)$$

d) Compute the resonant components values. With values of the characteristic impedance *Z*, the resonant frequency ω and adopting a di/dt rate of 80 A/μs [14], the resonant components values can be defined as follows:

$$L_{R1} = L_{R2} = \frac{Z}{\omega} = 2.4\,\mu H \qquad (7)$$

$$C_{R1} = C_{R2} = \frac{1}{Z \cdot \omega} = 34.7\ \text{nF} \qquad (8)$$

IV. Command Circuit Strategy

The block diagram of the open-loop command circuit for the full-bridge ZCZVT inverter presented in this paper is shown in Fig 5. It is composed of an EPROM, where the PWM signal is recorded, and an Erasable Programmable Logic Device (EPLD). The simplicity and programmability of the EPLD make it a good choice for prototyping digital systems. With the PWM and the output current direction, the gate signals are generated in the EPLD. Fig. 6 shows the PWM and the gate signals generated in the command circuit represented in Fig. 5 for $I_o > 0$. For $I_o < 0$, the main switches gate signals are swapped, and auxiliary switch S_{A2} is used instead of S_{A1}.

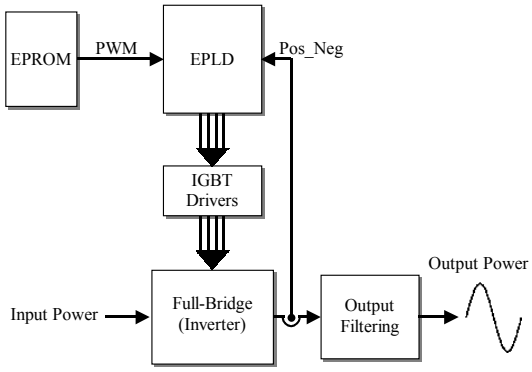

Fig. 5 – Block diagram of the command and power circuits.

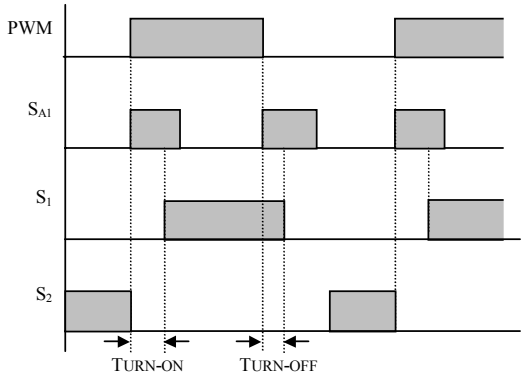

Fig. 6 – Command circuit waveforms.

V. Experimental Results

To verify the operation of the proposed ZCZVT full-bridge converter, a laboratory prototype has been implemented. The power stage circuit is shown in Fig. 2(a), and the components and parameters used are summarized in Table I. The active switches were implemented with an UFS (ultrafast switches) series IGBTs from Intersil Semiconductors, which present built-in antiparallel hyperfast diodes. The open-loop command circuit has been implemented using a single EPLD EPM7128SLC84-15 from Altera Corporation.

Figures 7, 8, 9, 10 and 11 show the experimental waveforms obtained at full load. They confirm the analysis made in Section II. As can be seen in Fig. 7, the commutations of the main switches occurs truly without losses, i.e., with ZCZVS for full load range. This is a very interesting feature introduced by ZCZVT commutation cell. Due to the slowed di/dt rate, main diodes reverse recovery losses are negligible. Fig. 8 shows zero current switching of the auxiliary switch S_{A1}. In Fig. 9 and 10 are

TABLE I

Utilized Components and Parameters

Component	Parameter
V_{in} (input voltage)	200 V
L_{R1} and L_{R2}	2.5 μH
C_{R1} and C_{R2}	33 nF
L (output filter)	500 μH
C (output filter)	4 μF
R (load)	12 Ω
Power Semiconductor Devices	HGTG27N60C3D
f_{out} (output frequency)	60 Hz
f_S (switching frequency)	30 kHz

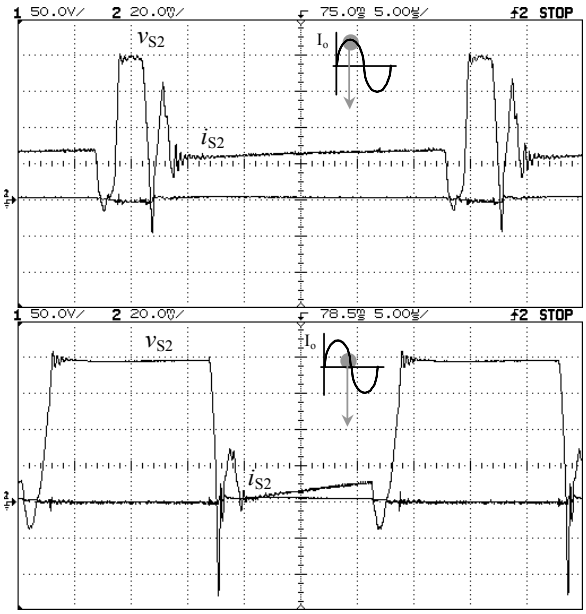

Fig. 7 – Main switch S_2 voltage and current.
(scales: 50 V/div.; 10A/div.; 5μs/div.)

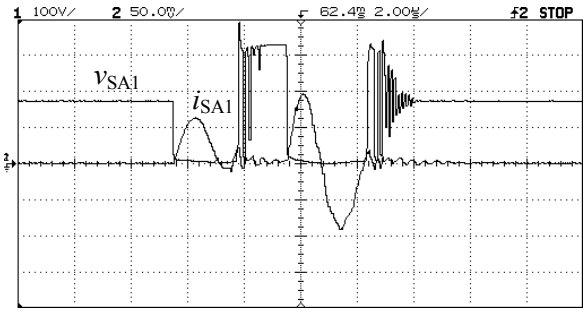

Fig. 8 – Auxiliary switch S_{A1} voltage and current.
(scales: 100 V/div.; 25A/div.; 1μs/div.)

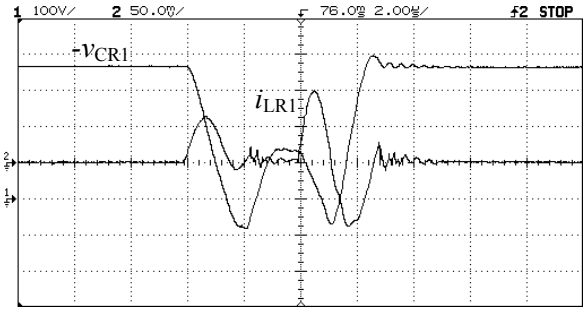

Fig. 9 – Resonant elements waveforms ($i_{LR1}(t)$ and $-v_{CR1}(t)$).
(scales: 100 V/div.; 25A/div.; 1μs/div.)

shown the waveforms of the resonant elements.

Fig. 11 shows the output voltage of the converter. As can be seen, there is a distortion in the output voltage waveform, which is noticed close to zero crossing. This distortion occurs because the converter output voltage stays with the same polarity even after the PWM signal to have changed, and it is owed to the action of the auxiliary commutation cell. This way, the load duty cycle is not equal to the PWM duty cycle. Fig 12 shows the variation of duty cycle of ZCZVT converter over an output voltage period. As can be seen, the relationship between the load duty cycle and the PWM duty cycle is directly proportional

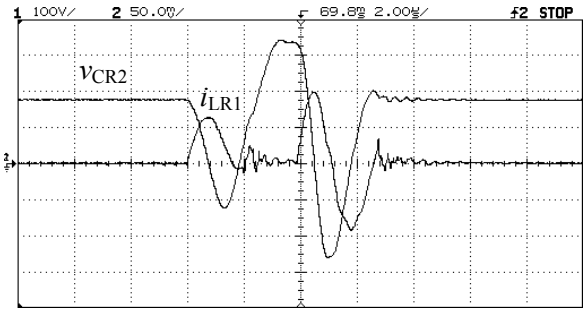

Fig. 10 – Resonant elements waveforms ($i_{LR1}(t)$ and $v_{CR2}(t)$).
(scales: 100 V/div.; 25A/div.; 1μs/div.)

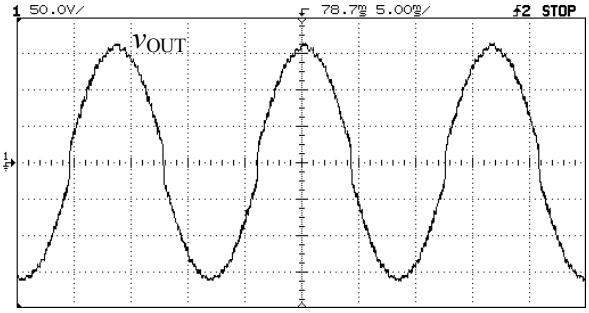

Fig. 11 – Output voltage.
(scales: 50 V/div.; 5ms/div.)

to the switching frequency of the converter.

To compensate the variation in the modulation due to the action of the auxiliary commutation cell, a modified PWM signal was generated. Fig. 13 shows the conventional reference signal and the modified one. These reference signals are for an amplitude modulation ratio of 0.778 and a switching frequency of 30 kHz. Fig. 14 shows the output voltage obtained with the ZCZVT full bridge converter operating with the modified PWM signal. Alternatively, the output voltage distortion can be solved with a closed loop operation.

VI. CONCLUSIONS

A new ZCZVT full-bridge PWM inverter was proposed in this paper. Operating principles was described and verified by experimental results obtained from a 30 kHz laboratory prototype rated at 1 kW, input voltage of 200V and output voltage of 110Vrms.

As shown by theoretical analysis and experimental results, the main attributes obtained are as follows:

- There are no additional voltage stresses on main power semiconductor devices;
- Commutation under ZCS and ZVS at both turn-on and turn-off for the main switches.
- Commutation under ZCS at turn-on and under ZCS and ZVS at turn-off for the auxiliary switches;
- The ZCZVT commutation cell is suitable for both minority and majority carriers semiconductor device applications such as MOSFETs, IGBTs, MCTs, Thyristors, etc.;
- The main diodes are commutated under ZVS and its

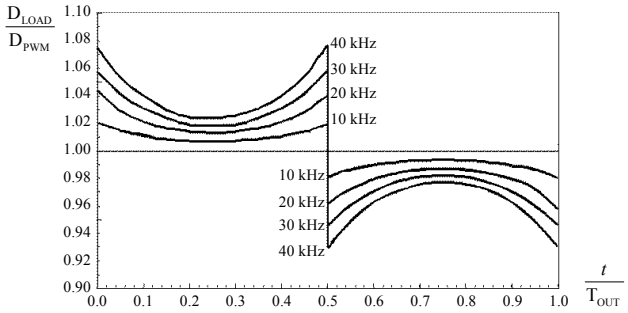

Fig. 12 – Variation of duty-cycle over an output voltage period.

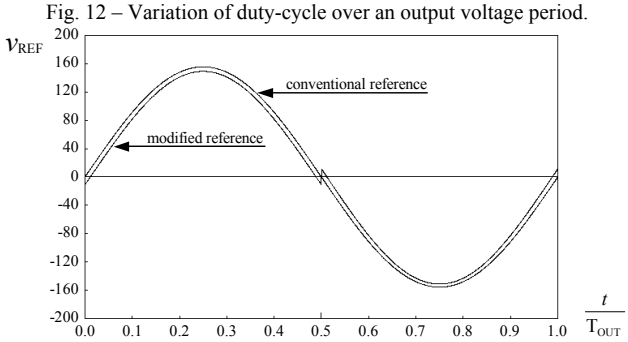

Fig. 13 – Reference signals.

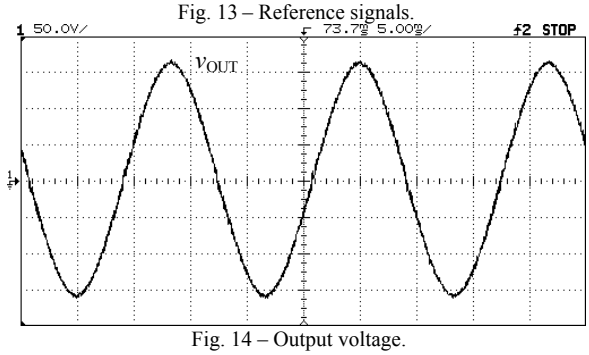

Fig. 14 – Output voltage.

reverse recovery are minimized;

- The auxiliary commutation cell is activated during the switching transitions only;
- Soft switching at full load range is guaranteed;
- The amount of auxiliary components is practically the same of that employed in the previously mentioned soft switching techniques;
- The converter is regulated by the conventional PWM technique at constant frequency;
- The output voltage waveform distortions caused by the auxiliary commutation cell can be minimized with modifications in the reference signal and/or with a closed loop operation;
- The auxiliary switches use the same ground signal of the upper main switches.

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