

A 300A DYNAMIC LOAD BASED ON MODIFIED BUCK+BOOST INTERLEAVED CONVERTER

Falcondes José Mendes de Seixas¹, Carlos Alberto Canesin¹ and Claudiner Mendes de Seixas²

¹ UNESP – São Paulo State University
DEE - Department of Electrical Engineering
LEP – Power Electronics Laboratory – Fax: 18-3743-1163
15385-000 - Ilha Solteira – SP - Brazil
falcon@dee.feis.unesp.br, canesin@dee.feis.unesp.br

² INDEL – Indústria Eletrônica Ltda
Av. Ver. João B. Sanches, 1144 – Fax: 44-266-1849
870650-130 - Maringá – PR - Brazil
assistec@indel.com.br

Abstract – This paper presents a novel dynamic load applied in load regulation tests of switching-mode power supplies, operating at high-current levels. The proposed device is based on the use of a modified Buck+Boost Interleaved converter, without the use of the boost diodes, and the output filters (capacitors). So, the dynamic load circuitry is very simple, effective and capable to feed high pulsed-current levels. A prototype was implemented to validate the proposed structure, operating at 10V-20V dc input voltage range, 190A-290A amplitude range of the input pulsed-current (nominal value is $240A \pm 20\%$), with adjustable pulse-width between 4ms (adjustable time-period of 200ms) until 6ms (adjustable time-period of 350ms). The main experimental results, obtained from the implemented prototype, are presented to validate the proposed Dynamic Load, which is capable to perform experimental tests of transient load regulation for switching-mode power supplies.

KEYWORDS

Interleaved converter, Dynamic load, Pulsed-current.

I. INTRODUCTION

The dynamic characteristics of switching-mode power supplies involve their behavior as a result of non-steady loads, transients, and, in general, alternating currents that are superimposed on the dc output level.

If a voltage-regulated power supply is to be used with circuitry that generates pulses or spikes, it is not enough to specify low output impedance over an appreciable sine-wave frequency range. Switching transients can prevent realization of the output impedance, which prevails for a passive, “clean” load. Switching-mode power supplies require a relatively long time to recover from the effects of abrupt load or line changes. Although specification criteria differ among manufacturers, the underlying philosophy is essentially similar. An abrupt change in load current provokes an oscillatory response that is generally characterized by

overshoot and undershoots through the limits of the static-regulation band. The severity of the overshoot and undershoot, as well as the number of oscillations that are required to return to the regulation band, varies with different designs [01-02].

In this context, this paper presents a novel Dynamic Load operating as a necessary product, specified by a manufacturer (Power Electronics Company), capable to absorb high pulsed currents with specified time-period and pulse-width, to perform experimental tests of transient load regulation for switching-mode power supplies [03].

II. DEFINITION OF THE PROPOSED CONVERTER

The initial challenge was to develop a group of loads with high current capacity with both controlled pulse-width (t_c) and magnitude (I), as shown in Fig. 1.

It should be noticed that several circuits were analyzed. Among of them, the simplest solution, but not efficient, is using a fixed value resistor (as a static load) added to several independent switches to allow that all of the resistors can be connected in parallel (as a dynamic load), as shown in Fig. 2.

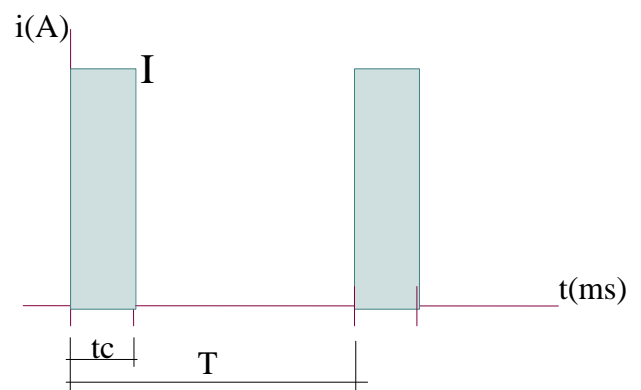


Fig. 1 – The desired current waveform.

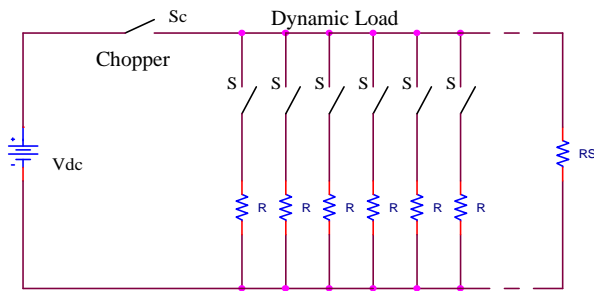


Fig. 2 - Dynamic load based on switched resistors.

The dynamic load should attend the following specifications:

- DC voltage range operates between 10 and 20V.
- Nominal magnitude of the demanded current pulses equal to 240A, with continuous variation of $\pm 20\%$, i.e., amplitude of the pulsed-current from 190 to 290A, approximately.
- Adjustable pulse-width between 4ms and 6ms.
- Period among adjustable pulses between 200 and 350ms.

The minimum value of load can be implemented starting from a fixed value of resistance, while the variable portion of the current, added to the fixed value, should have continuous variation and to be represented by a variable load.

Therefore, as a first attempt, was looked for to implement a Buck + Boost converter topology, according to the Fig. 3. In this proposed circuit, the minimum value of load (or static load) is defined for the conduction of the switch S1 through RS, during the time interval t_c . The dynamic load (specified by C and RD) depends of the switching function of the boost converter. The input current of the converter (through the voltage source Vdc) has the same ripple that the current through the boost inductor. A high value of the inductance for this inductor guarantees low current ripple, however, it implicates in a high rise time of the pulsed-current.

The interleaved power conversion refers to the strategic interconnection of multiple switching cells for which the conversion frequency is identical, but for which the internal switching instants are sequentially phased over equal fractions of a switching period. This arrangement reduces the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses. An interleaved system can therefore realize a savings in filtering and energy store requirements, resulting in greatly improved power conversion densities without sacrificing efficiency [04].

Therefore, to perform low current ripple, without committing the rise time of the current, it was proposed an interleaved topology for the dynamic load, as shown in Fig. 4.

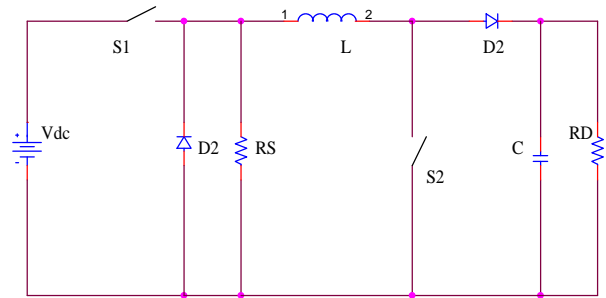


Fig. 3 - Topology of the Buck + Boost converter.

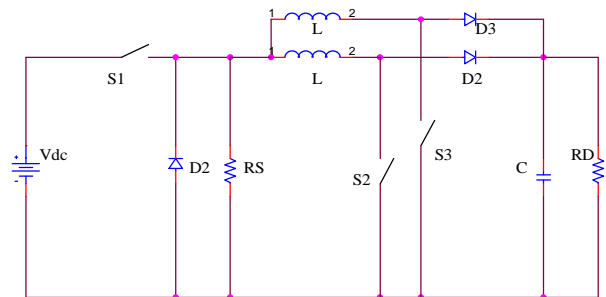


Fig. 4 - Topology of the interleaved Buck + Boost converter.

The main aim of this project is produce a pulsed-current with closed shape to the Fig. 1, in the input of the converter. Thus, the output variables have low importance to reach the announced purpose. In this case, the high recovery currents of the diodes D2 and D3, through the switches, are very important limits to the design of the boost converter.

A simple technique to solve the problem of recovery current of the diodes, and still to become the input current extinction fastest, is to remove the two boost diodes and also to remove the output filter capacitor. The voltage over the resistor RD and its respective current become pulsed. In conclusion, Fig. 5 shows the approach topology of the proposed converter for the dynamic load, based on modified Buck+Boost interleaved converter.

The switches Sa and Sb, the inductors La and Lb and the PWM command circuit perform the Dynamic Load, that are responsible to execute the peak current variation of $\pm 20\%$, over its nominal value. This pulsed-current range is obtained by the variation of the voltage over the load resistors Ra and Rb, through the duty cycle control (D) of the switches Sa and Sb.

The chopper is formed basically by the switch Sp, one drive circuit, that include an optic coupler, the diode Dp and the resistor Rp, that define the Static Load. The duty cycle controls of the switch Sp allow to define the width and the frequency of the pulsed-current.

Despite a constant value of the input current conducting due to Rp, there is a variable portion for the dynamic load that also circulates through the switch Sp.

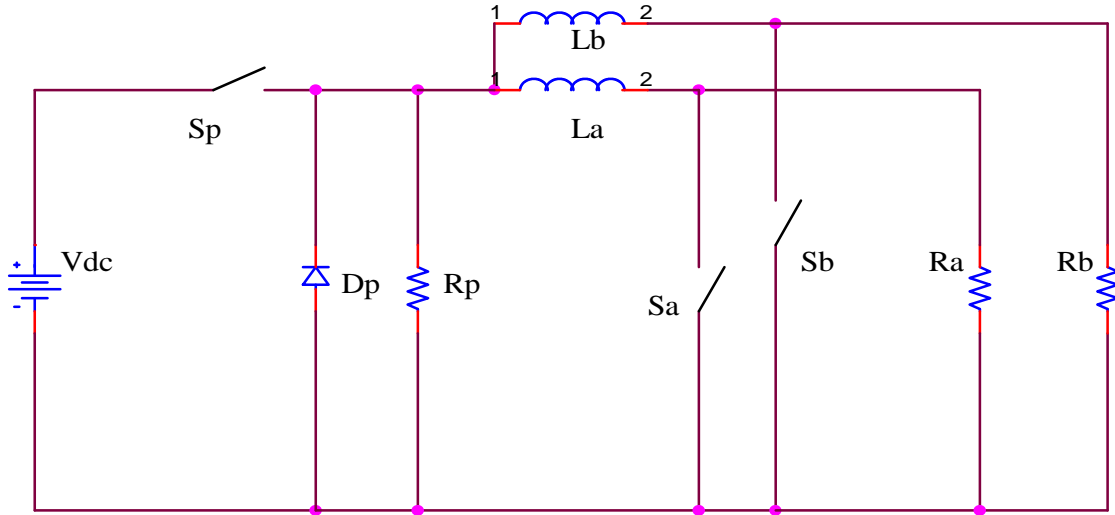


Fig. 5. Proposed converter for the Dynamic Load.

The diode D_p assumes the total peak current of the dynamic load, when S_p is turned off, until that all of the energy stored in L_a and L_b are dissipated in R_a and R_b , respectively. Although the demagnetization processes of the inductors are fast (with low value of average current), the diode D_p should be specified considering its repetitive peak current value.

III. EXPERIMENTAL RESULTS

Due to the converter involves high pulsed-current and low voltage values, several switches with low on-resistance, are connected in parallel as well as the load resistors (R_p , R_a , and R_b).

The main components used in the implemented prototype are:

1) Chopper:

- S_p : 5 x MOSFET IRF1104
- D_p : 1 x Schottky Diode 81CNQ045
- R_p : 7 x 1 /60W
- Optic coupler : HP2211

2) Dynamic Load:

- S_a : 2 x MOSFET IRF1104
- S_b : 2 x MOSFET IRF1104
- $R_a = R_b$: 5 x 1 /60W
- $L_a = L_b = 10$ H, 8 turns of 50 x 22AWG wire, Core : EE65-26
- PWM : LM3525

Fig. 6 and 7 show details of the implemented prototype. The main experimental results, obtained from the prototype, are presented in the figures below.

Fig. 8 shows details of the current through the inductors L_a and L_b , and Fig. 9 shows the pulsed-current through one of the inductors (L_a) of the dynamic load. It is observed that,

due to the phase displacement of the inductor currents, the input current ripple results smaller than the individual inductor current ripple, and the input current ripple presents a frequency twice the individual frequencies of the currents through L_a and L_b .

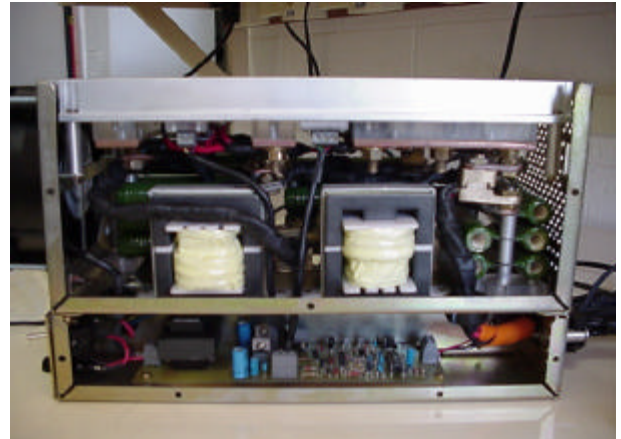


Fig. 6. Details of the Interleaved Inductors.

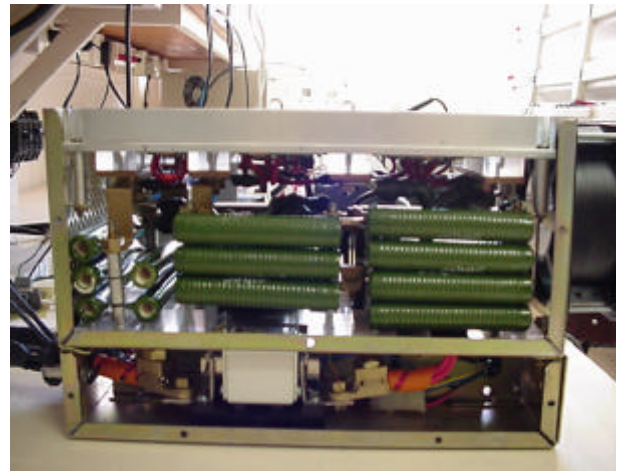


Fig. 7. Details of the Load Resistors.

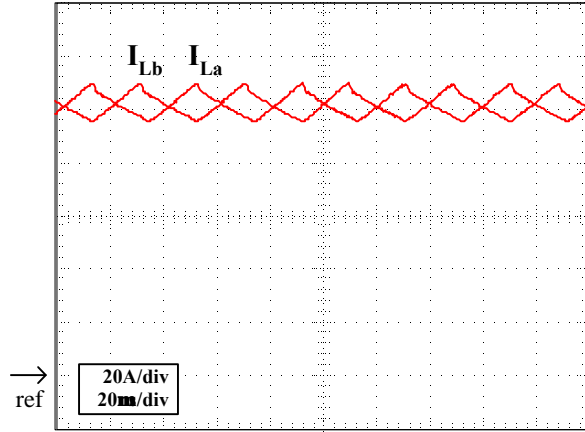


Fig. 8. Details of the currents through the inductors La and Lb (D=0.45).

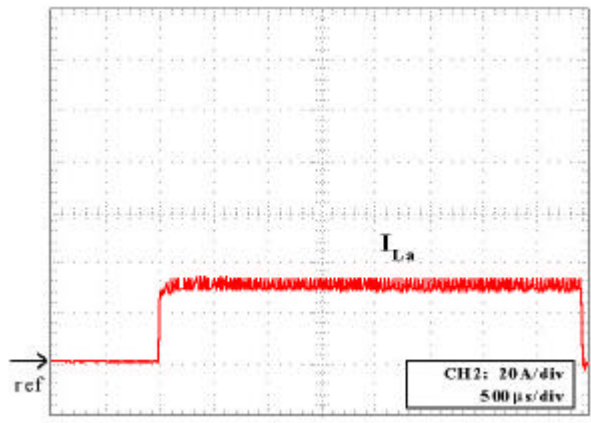


Fig. 9. Pulsed-current through La (D=0.45).

Fig. 10 shows the detail of the rise time of the input current, for equivalent duty cycle (D) at 0.45. It is observed that the switching frequency of the dynamic load is 25kHz.

Fig. 11 shows the input pulsed-current, being considered a pulse-width of approximately 4ms. The pulse-width control of the static load is defined by an external auxiliary signal (for the purpose of these experimental tests, an external board, based on the mono-stable oscillator circuit UC4528, was implemented to perform the variation of the pulse-width control up to 6ms).

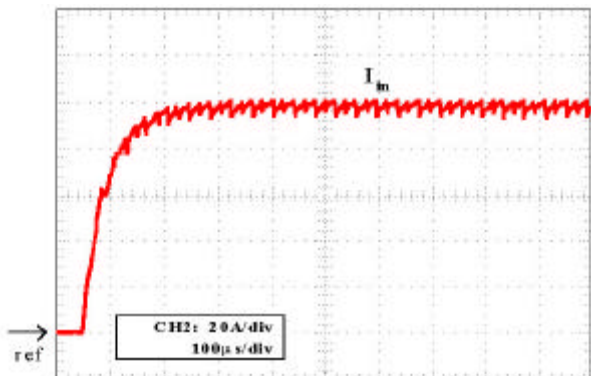


Fig. 10. Detail of the rise time of the input current (D=0.45).

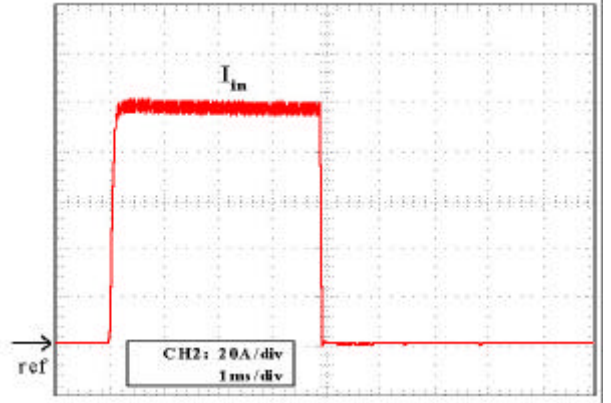


Fig. 11. Input pulsed-current (D=0.45).

Fig. 12 shows the pulsed-current through one of the dynamic loads (Ra). In Fig. 13 it can be observed the dynamic variations of the input pulsed-current, driven by the command circuit strategy of the dynamic load.

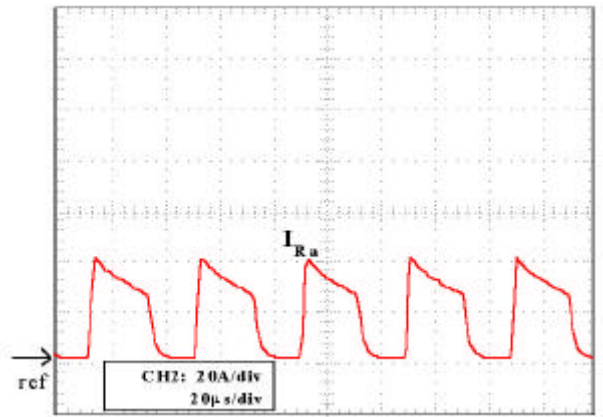


Fig. 12. Pulsed-current through Ra (D=0.45).

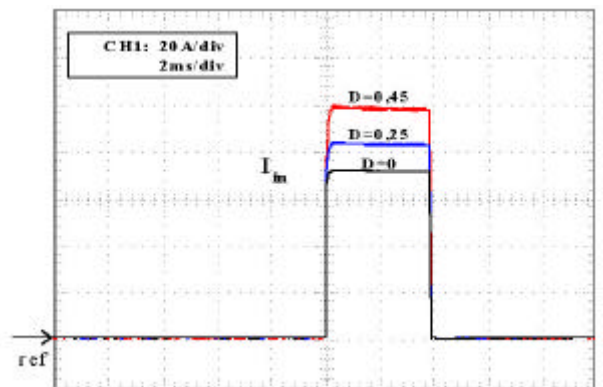


Fig. 13. Dynamic variation of the input pulsed-current (D=0 to 0.45).

IV. CONCLUSION

A novel modified buck+boost interleaved converter, to perform a dynamic load with high level of pulsed current was proposed. The proposed topology uses one static and one dynamic loads without the use of boost diodes and the output

filtering capacitor, performing an input pulsed-current range of 190A until 290A. The pulse-width, the magnitude and the period time of the input pulsed-current are controlled by a simple circuit strategy.

The main experimental results were presented to validate the proposed dynamic load, capable to perform tests of load regulation for switching-mode power supplies, according to the manufacturer request.

REFERENCES

- [01]BROWN, M. –“Practical switching power supply design”, Academic Press Inc., Motorola Series in Solid State Electronics, pp. 132-135, 1990;
- [02]CHRYSSIS, G. C. –“High-frequency switching power supplies–Theory & Design”, McGraw-Hill Publishing Company, pp. 260-263, 1989;
- [03]Project-Contract TC-P004-00, “INDEL Indústria Eletrônica Ltda”, 2000;
- [04]MIWA, B. A. et al, “High efficiency power factor correction using interleaving techniques”, in Proceedings of the IEEE-APEC Conference, pp. 557-568, 1992.