ACTIVE POWER FLOW CONTROL OF A THREE-PHASE LINE-INTERACTIVE UPS SYSTEM WITH SERIES-PARALLEL ACTIVE POWER-LINE CONDITIONING

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***Abstract*-This paper describes the active power flow behavior of a three-phase line-interactive uninterruptible power supply system with series-parallel active power-line conditioning capabilities. The control algorithm uses synchronous reference frame (SRF)-based controller, which allows an effective harmonic and reactive power compensation, generated from any configuration of non-linear load. The control of the active power flow in the dc-bus of the UPS is obtained through an additional voltage dc-bus controller. Under normal line conditions, the UPS system works with universal filtering capabilities, such as, compensating the input currents and the output voltages. Two pulse width modulation (PWM) converters are used to perform the series and parallel active power-line conditioning. The active power flow control of the UPS system is discussed taking into account battery charging and undesired conditions, such as, input voltage unbalances, total harmonic distortion of the load currents and displacement factor ($\cos\varphi_1$). The control algorithm using SRF method are described and analytically studied. The performance of the UPS system is evaluated in three-phase, three-wire system. Experimental results are presented to confirm the theoretical studies.**

KEYWORDS

UPS system, Active filter, Active power flow.

I. INTRODUCTION

The large use of non-linear loads, such as, personal computers, uninterruptible power supplies (UPS's), etc., have increased in the last years, causing problems on the power supply systems. The harmonic currents drawn by non-linear loads from utility have contributed to reduce the power factor and to increase the total harmonic distortion (THD) in the utility input voltages. Thus, UPS systems must use any active power-line compensating method to improve the power source quality when it is providing clean and uninterruptible power to critical loads, such as, industrial process controls, computers, medical equipment, data communication systems, etc. [1-7]. In [6] and [7], three-phase parallel processing UPS have been presented with harmonic and reactive power compensation, but the output voltages and the input currents cannot be controlled simultaneously. Three-phase UPS systems with series-parallel active power-line conditioning have been controlled using different approaches [1-3]. In [2], a three-phase UPS system was controlled using synchronous reference frame (SRF)-based controller, but details about the control of the active power flow of the UPS system was not discussed. The design procedures of the two pulse width modulation (PWM) converters, used to perform the series and parallel active power-line conditioning, should be take into account the input voltage variations (undervoltage, overvoltage, etc.), THD of the load currents, displacement factor ($cos\,\phi_1$) and battery charging.

This paper describes the active power flow control of a three-phase line-interactive UPS system with series-parallel active power-line conditioning capabilities. The SRF-based controller allows an effective harmonic and reactive power compensation generated from any configuration of non-linear load. The control of the active power flow in the dc-bus of the UPS system is obtained from the interaction between an SRF-based controller and an additional voltage dc-bus controller.

The control algorithm using an SRF method are described and analytically studied. The performance of the UPS system is evaluated in three-phase, three-wire system. Experimental results are presented to confirm the theoretical studies.

II. OPERATION OF THE LINE-INTERACTIVE UPS TOPOLOGY

The topology of the line-interactive UPS system is shown in Fig. 1. Two PWM converters, coupled with a common dc-bus, are used to perform the series active filter and parallel active filter functions. The series active filter is connected in series with the line and the load through three single-phase linking transformers. A battery bank is placed in the dc-bus and a static switch '*sw*' is incorporated to the circuit to provide a fast disconnection between the UPS system and the power supply when an occasional interruption of the incoming power occurs.

The series active power filter acts as a sinusoidal current source and the parallel active power filter acts as a sinusoidal voltage source [2]. The parallel active power filter controls the UPS to have constant rms output voltages (v_{fa}, v_{fb}, and v_{fc}) with low THD. An SRF-based controller is used to control the series active power filter making the source currents (i_{sa}, i_{sb}, and i_{sc}) balanced and sinusoidal with low THD, also. The output UPS voltages and the source currents are controlled to be in phase with respect to the line voltages (v_{sa}, v_{sb}, and v_{sc}), respectively. Both the parallel and the series filter use three independent controllers acting on half-bridge inverters. In this line-interactive UPS system, an effective power factor correction is carried out.

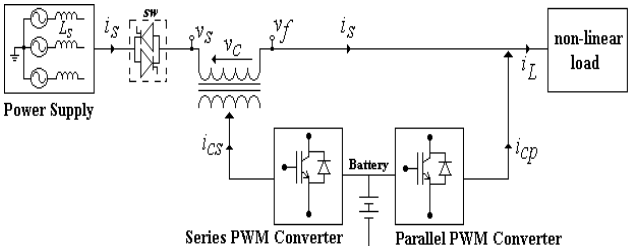


Fig. 1. Line-interactive UPS system topology.

Design procedures of the three-phase PLL (Phase-Locked Loop) system used in the SRF-based controller are presented in [2]. The PLL system is also employed to generate the reference output voltages of the parallel PWM converter. The input signals of the PLL system are the sampled line-to-neutral voltages v_{sa}, v_{sb}, and v_{sc}.

A. SRF-Based Controller for Current Compensation (Standby Mode).

An SRF-based controller is used to provide and to control the compensating reference currents (i_{ca}^*, i_{cb}^*, and i_{cc}^*) for the series PWM converter shown in Fig. 1. The block diagram of the control scheme for current compensation is shown in Fig. 2. The three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) are measured and transformed into a two-phase stationary reference frame $(dq)^s$ quantities (id^s, iq^s) based on the transformation (1). Then, these quantities are transformed from a two-phase stationary reference frame $(dq)^s$ into a two-phase synchronous rotating $(dq)^e$ reference frame, based on the transformation (2), where $\theta = \omega t$, is the angular position of the reference frame. The unit vectors $sin\theta$ and $cos\theta$ are obtained from PLL system. The currents at the fundamental frequency ω (id^e and iq^e) are now dc quantities and all the harmonics, transformed into non-dc quantities, can be filtered using a low pass filter (LPF) as shown in Fig. 2. Now, id_{dc}^e represents the fundamental active component of the load current in dq axis and iq_{dc}^e represents the fundamental reactive component of the load current in dq axis.

An additional dc-bus controller is responsible for regulating the current I_{dc} and the voltage V_{dc}. Apart from the conventional active power filter applications, in which only the dc-bus voltage is controlled, the UPS dc-bus controller is able to control the dc-bus current for adequate charging of the battery bank. The dc-bus controller is also responsible to control the active power flow of the UPS system. Its output ib_{dc} is added to the active current in the d axis id_{dc}^e as given by (3) and, thus, the amplitude of the series reference currents can be controlled by id_c^e.

$$\begin{bmatrix} id^s \\ iq^s \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} id^e \\ iq^e \end{bmatrix} = \begin{bmatrix} \cos\theta & sin\theta \\ -sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^s \\ iq^s \end{bmatrix} \quad (2)$$

$$id_c^e = id_{dc}^e + ib_{dc} \quad (3)$$

Now, the dc components of the synchronous reference frame id_c^e and iq_{dc}^e can be transformed into the stationary reference frame $(dq)^s$. The inverse transformation matrix from two-phase synchronous reference frame to two-phase stationary reference frame is given by (4). As only the fundamental active component reference needs to be obtained, (4) can be replaced by (5).

The matrix that provides the linear transformation from two-phase system to three-phase stationary reference frame system is given by (6). Thereby, the dc component of the synchronous reference frame id_c^e is transformed into the stationary reference frame $(dq)^s$ and yields the fundamental reference components (i_{ca}^*, i_{cb}^*, i_{cc}^*). Such reference currents are generated in software. The single-phase block diagram of the current controller is shown in Fig. 3, which is presented in details in [2].

$$\begin{bmatrix} id_f^s \\ iq_f^s \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\theta \\ sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id_{dc}^e \\ iq_{dc}^e \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} id_f^s \\ iq_f^s \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\theta \\ sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id_{dc}^e \\ 0 \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} i_{ca}^* \\ i_{cb}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} id_f^s \\ iq_f^s \\ i_o \end{bmatrix} \quad (6)$$

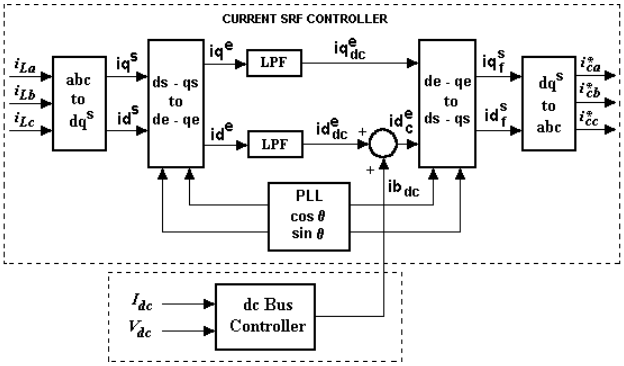


Fig. 2 - Block Diagram of the Current SRF Based Controller.

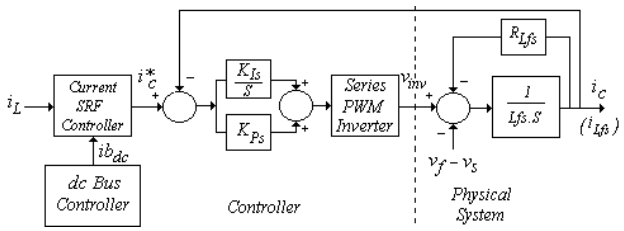


Fig. 3. Single-Phase Current Controller of the Series Active Filter.

III. Active Power Flow of the Three-Phase UPS System

Depending on the difference between the mains voltage and the output voltage, the active power flow of the UPS system can change its direction. When the rms mains voltage V_s is greater than the rms output voltage V_f the active power flows from the mains to the dc-bus via series converter and from the dc-bus to the load via parallel converter, as shown in Fig. 4 (a). When V_s is less than V_f the active power flows from the mains to the dc-bus via the output of the parallel converter and from the dc-bus to the line via series converter, as shown in Fig. 4 (b). Therefore, controlling the amplitudes of the series reference currents (i^*_{ca}, i^*_{cb}, i^*_{cc}), the dc-bus furnishes and absorbs power to make the balance of the active power.

If the line voltage V_s is equal to the output voltage V_f and the UPS is feeding a linear resistive load, there isn't any active power flow through both the series and the parallel converters, as shown in Fig. 4 (c).

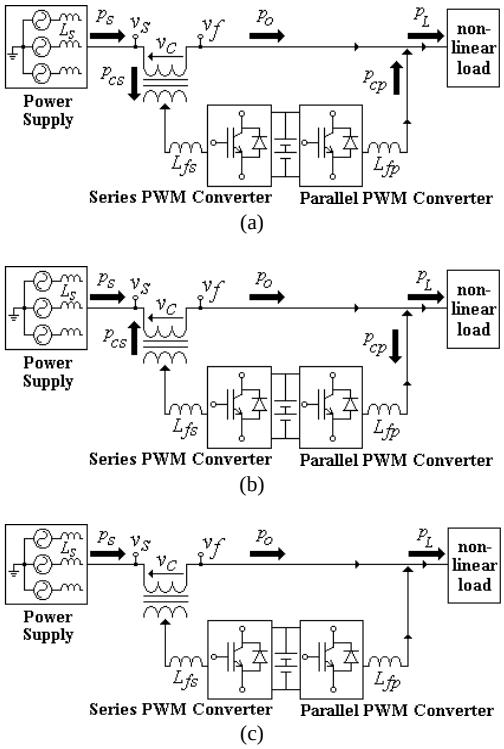


Fig. 4. Power flow of the UPS system: (a) $V_s > V_f$; (b) $V_s < V_f$; (c) $V_s = V_f$.

A. Current SRF Controller (Standby Mode)

When the UPS system is providing power to non-linear load, the parallel PWM converter supports harmonic and reactive currents. Besides the ratio between the output and input rms voltages (V_f / V_s), the apparent powers handled by the series converter S_s and by the parallel converter S_p depend on both the displacement factor ($\cos\varphi_1$) and the THD of the load current i_L (THD_{iL}). The parallel converter must have low impedance, enough to absorb the harmonic currents of the load, while the series converter must have high impedance, enough to isolate the line from the load with respect them.

In standby mode the complex powers required by the series and the parallel converters are, respectively, given by

$$\boldsymbol{S_s} = \left(\boldsymbol{V_s} - \boldsymbol{V_f}\right)\boldsymbol{I_s^*} \tag{7}$$

$$\boldsymbol{S_p} = \boldsymbol{S_L} - \boldsymbol{V_f}\,\boldsymbol{I_s^*} \tag{8}$$

Thus, in the steady state, assuming a balanced sinusoidal system, the normalized powers handled by the parallel converter $|S_p/S_L|$ and by the series converter $|S_s/S_L|$ can be given by (9) and (10), respectively. The quantities S_L, P_L, Q_L and H_L are the apparent, active, reactive, and harmonic powers of the load, respectively.

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P^2.\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P^2+Q^2+H^2}} = \frac{\cos\varphi_1\sqrt{\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{1+THD^2}} \tag{9}$$

$$\left|\frac{S_p}{S_L}\right| = \frac{\sqrt{P^2.\left(1-\frac{V_f}{V_s}\right)^2+Q^2}}{\sqrt{P^2+Q^2+H^2}} = \sqrt{\frac{\cos^2\varphi_1\frac{V_f}{V_s}\left(\frac{V_f}{V_s}-2\right)}{1+THD_{i_L}^2}} \tag{10}$$

It can be seen from (10), that the lower is $\cos\varphi_1$ or the higher is THD_{iL}, the higher the apparent power that the parallel PWM converter could support.

When the charging of the batteries is taking into account, additional active power P_b, given by (11), can be included in the analysis.

$$P = P_L + P_b = (1+k_b)P_L \tag{11}$$

Where the charging factor k_b, is given by

$$k_b = \frac{P_b}{P_L} \tag{12}$$

Thus, the general form of the normalized powers, in which the charging factor $k_b \geq 0$, is given by (13) and (14).

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P^2\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P_L^2+Q_L^2+H_L^2}} = \frac{\cos\varphi_1\sqrt{\left[(1+k_b)\left(1-\frac{V_f}{V_s}\right)\right]^2}}{\sqrt{1+THD_{i_L}^2}} \quad (13)$$

$$\left|\frac{S_p}{S_L}\right| = \sqrt{\frac{\cos^2\varphi_1\frac{V_f}{V_s}(1+k_b)\left(\frac{V_f}{V_s}(1+k_b)-2\right)}{1+THD_{i_L}^2}+1} \quad (14)$$

When additional energy is employed to charging the battery bank, the direction of the power flow can change, as shown in Fig. 5 (a), (b), and (c), for $V_s/V_f < 1$, $1 < (V_s/V_f) > (1+k_b)$, and $(V_s/V_f) > (1+k_b)$, respectively. Thus, the charging job of the battery bank is sharing between the two PWM converters, depending on the difference between the mains voltages and the output voltages of the UPS system, and the charging factor k_b. The plots of the normalized powers for different k_b are shown in Fig. 6 (a) and (b).

The great advantage of this UPS topology is that during the standby mode, the power handled by the parallel converter is ever less than 100% of the load power rate, while the power handled by the series converter can be less than 25%.

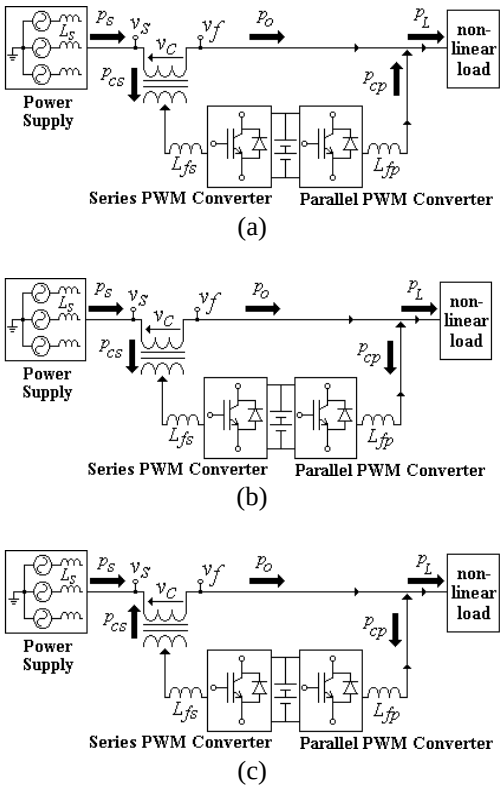


Fig. 5. Power flow of the UPS system for $k_b \neq 0$: (a) $V_s/V_f < 1$; (b) $1 < V_s/V_f < (1+k_b)$; (c) $V_s/V_f > (1+k_b)$.

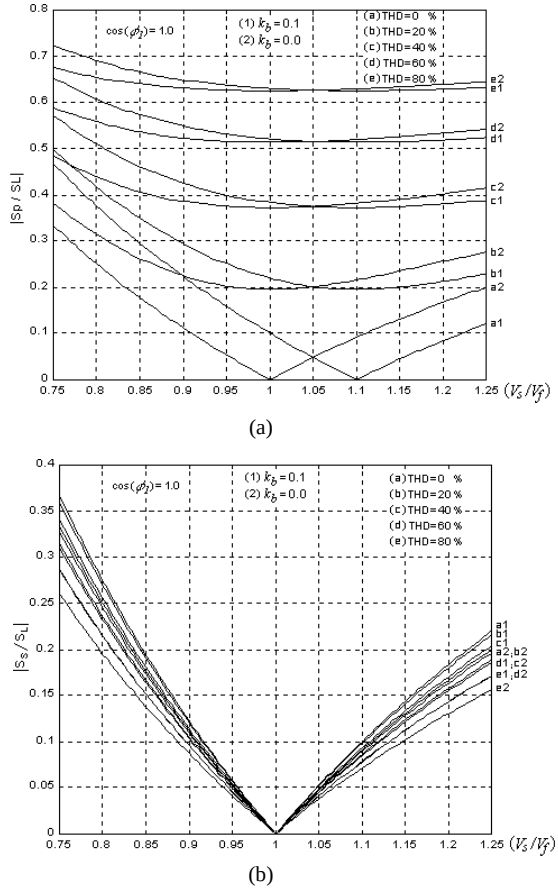


Fig. 6. Normalized Powers Handled by the Parallel and Series Active Filters ($\cos\varphi_1 = 1$).

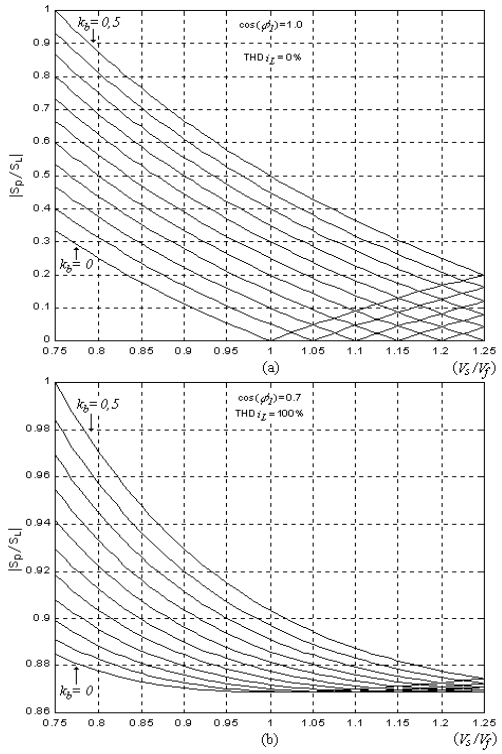


Fig. 7. Parallel Normalized Power $\left|S_p/S_L\right|$: (a) $\cos\varphi_1 = 1$, THD_{iL} =0%; (b) $\cos\varphi_1 = 1$, THD_{iL} = 100 %.

IV. Experimental Results

The complete scheme of the three-phase line-interactive UPS system is shown in Fig. 9. To verify the performance of the UPS system, a prototype was developed and tested. A 2.5 kVA non-linear load ($THD_{iL} \cong 30\%$) used to test the UPS system is a three-phase diode rectifier. The parameters used in the prototype are: L_{fp} = 300µH, L_{fs} = 1.4mH, C_{fp} = 130µF; R = 30Ω (dc load); C_{dc} = 2200µF, nominal rms line-to-neutral output voltages $V_{fa,b,c}$ = 115V and dc bus voltage - V_{dc} = 570V.

The part of the scheme shown in the shaded area uses a 400MHz PC computer, a 12 bits resolution data acquisition system and a 12 bits resolution D/A converter board. Both current SRF controller (Fig. 6) and PLL scheme (Fig. 2) are implemented in software and are responsible to generate the current and voltage references for the current and voltage analog controls. Both data acquisition systems and digital controllers run at 5kHz frequency.

The three-phase input voltages $v_{sa,b,c}$ and the output voltages $v_{fa,b,c}$ are shown in Fig. 10 (a) and (b), respectively. The output voltages ($v_{fa,b,c}$) are almost sinusoidal with constant rms voltages. The THD of the output voltages (THD_{vf}) are approximately 3%. The input voltages (v_{sa}), the output voltage (v_{fa}), and the difference between them (v_{ca}) are shown in Fig. 11 (a), (b), and (c), for three different rms input voltages ($V_{sa} \cong V_{fa}$, $V_{sa} > V_{fa}$, and $V_{sa} < V_{fa}$). Fig. 12 (a), (b), and (c), show the reference currents ($i^*_{sa,b,c} = i^*_{ca,b,c}$) obtained from the SRF-based controller of Fig. 2, taking into account the voltage conditions presented in Fig. 11 (a), (b) and (c), respectively. As can be seen, controlling the amplitude of the series reference current, the dc-bus can furnishes and absorbs power to make the active power balance of the UPS.

Based on Fig. 2, Fig. 13 (a) shows the quantities id^e_{dc}, which represents the fundamental active component of the load current in *dq* axis, for the three voltage conditions: (*1*) $V_{sa} \cong V_{fa}$, (*2*) $V_{sa} > V_{fa}$, and (*3*) $V_{sa} < V_{fa}$. Supposing that the load not varies and the rms output voltages are constant, the magnitudes of id^e_{dc} are equal for the three voltage conditions. The quantities ib_{dc}, responsible for controlling the active power flow of the dc-bus controller are shown in Fig. 13 (b), taking into account the conditions (*1*), (*2*), and (*3*). It can be noted that ib_{dc} varies depending on the ratio between the output and input rms voltages (V_f / V_s), for realize the active power flow control. The dc-bus controller output (ib_{dc}) is added to the active current in the *d* axis (id^e_{dc}) and the result (id^e_c) is shown in Fig.13(c).

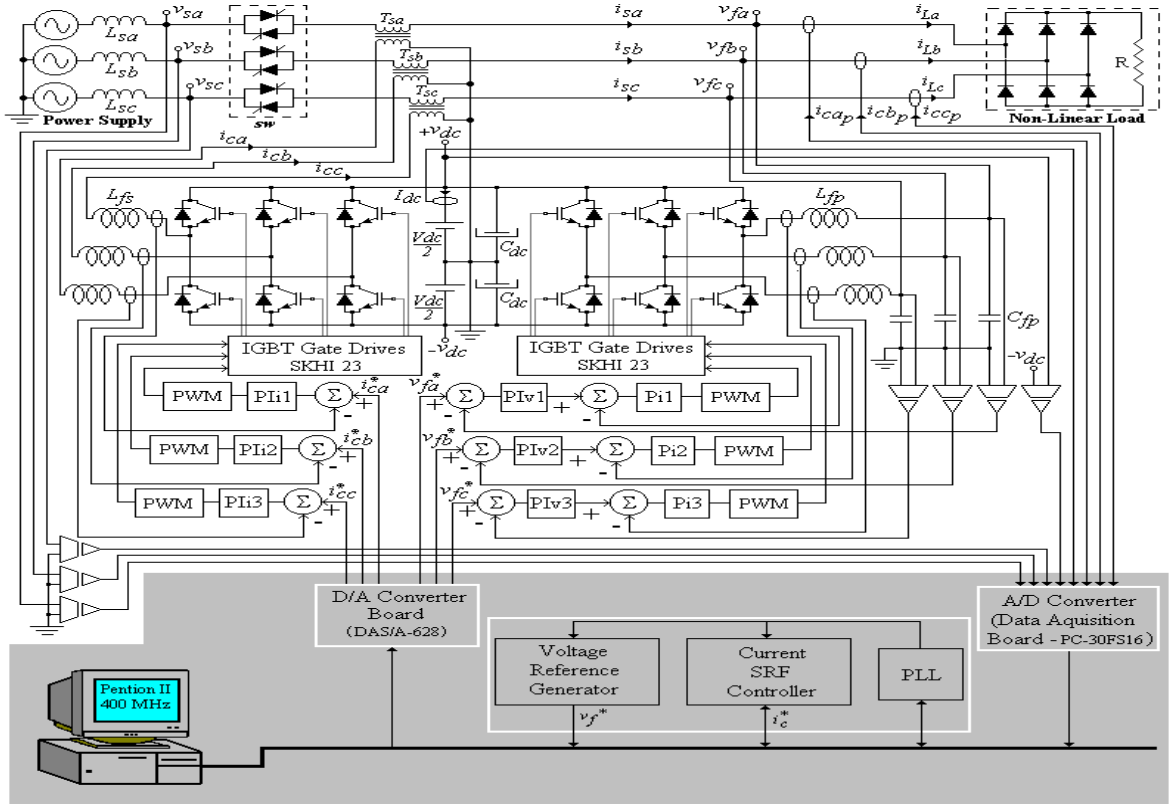


Fig. 9. Complete Scheme of the Line-Interactive Series-Parallel UPS System

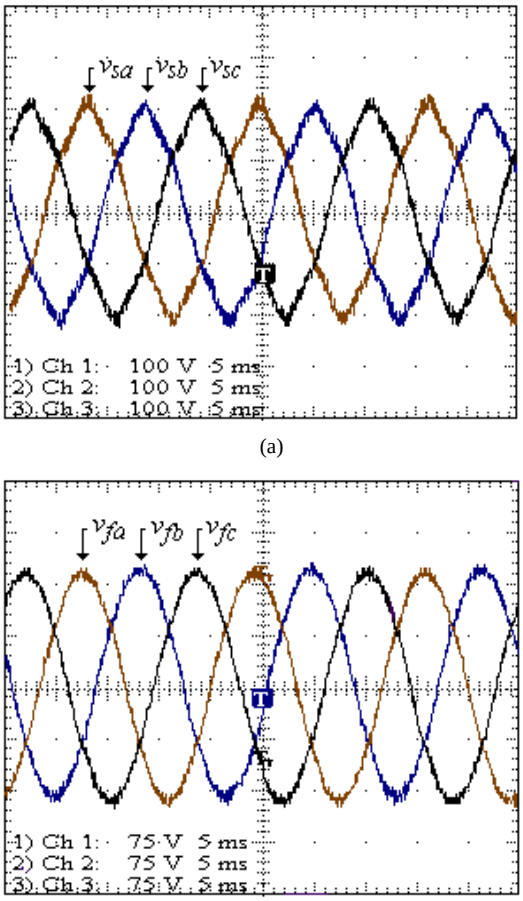


Fig. 10. UPS voltages: (a) Input voltages ($V_{sa,b,c}$), (b) Output Voltages ($V_{fa,b,c}$).

Thereby, the dc component of the synchronous reference frame id_c^e can be transformed into the stationary reference frame $(dq)^s$ and yields the fundamental reference current components of the series converter ($i^*_{sa,b,c} = i^*_{ca,b,c}$).

Figs 14 (a) and (b) show the three-phase load currents ($i_{La,b,c}$) and the three-phase parallel compensating currents, (i_{ca,b,c_p}), respectively. Details of the compensated source current ($i_{sa,b,c}$), the parallel compensation currents, and the load currents are shown in Fig. 15 (a), (b), and (c).

The source currents are shown in Fig.16 (a), which are almost sinusoidal and balanced. The THD of the source currents are approximately 4%. Fig. 16 (b) shows the phase *a* source current i_{sa} and the input voltage v_{sa}. Fig. 16 (c) shows the phase *a* source current i_{sa} and the output voltage v_{fa}, respectively. Both the source current and the output voltage are in phase with respect the input voltage. The measure power factor ($cos\varphi$) is equal to 0,99.

The quantities v_{fa}, i_{sa}, i_{La} and i^*_{sa} (reference input current) are shown in Fig. 17 (a), for standby to backup transition mode that occurs at 0.02s. When the input power is out the input switch '*sw*' is opened and the input current i_{sa} drops to zero, but the output voltage v_{fa} remains providing power to the load. Thus, the PLL system forces the UPS to operate at a fixed reference frequency (ω^* = 377 rad/s). The transition from backup to standby operation mode of the UPS system occurs at 0.31s, as shown in Fig. 17 (b) and (c). When the input power returns, the PLL system synchronizes the UPS system with respect the then utility and the switch '*sw*' is closed. Thereby, immediately the input current i_{sa} follows the reference i^*_{sa}. Note that the output voltage is unaffected by the transitions from standby to backup mode and from backup to standby mode. Fig. 17 (d) shows the UPS operating in standby mode.

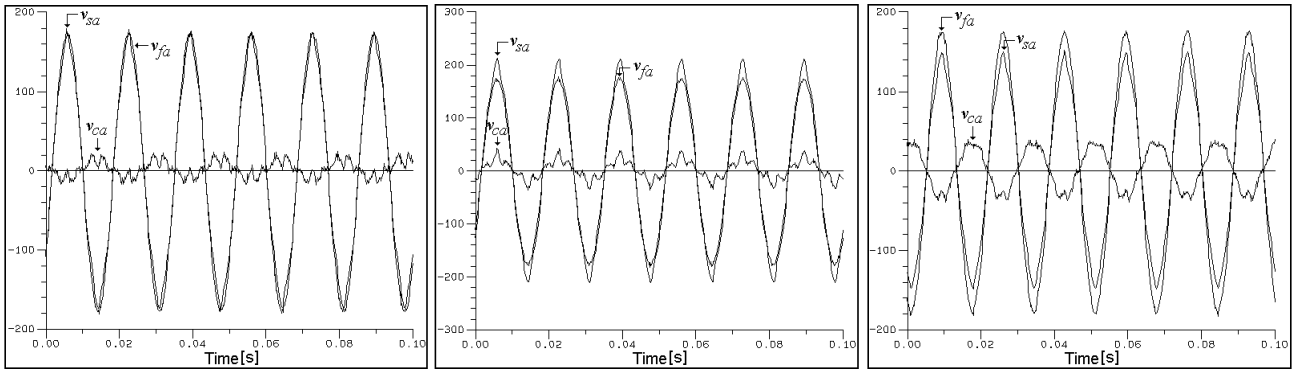
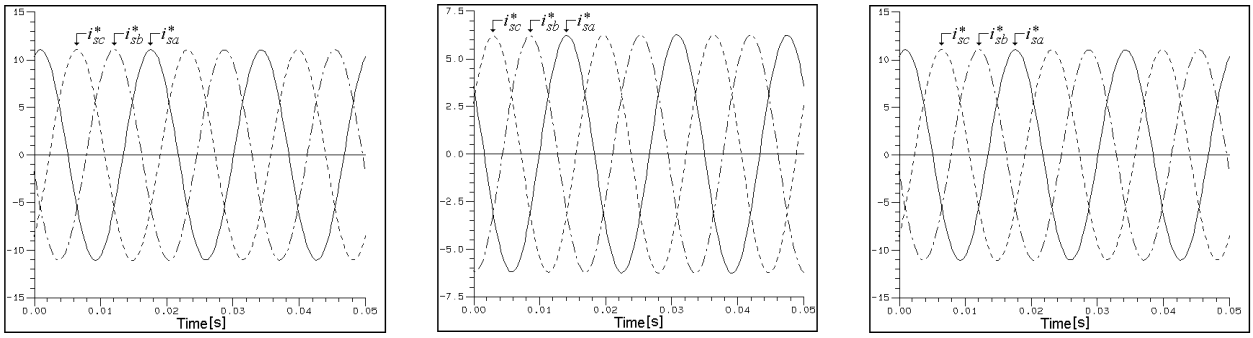
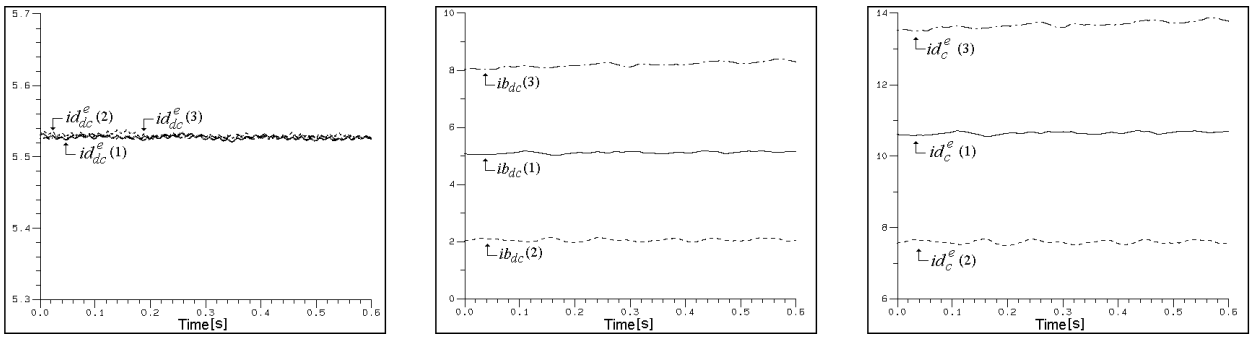


Fig. 11. Phase *a* Input voltage v_{sa}, Output voltage v_{fa}, and Series voltage v_{ca}: (a) $V_{sa} \cong V_{fa}$; (b) $V_{sa} > V_{fa}$, and (c) $V_{sa} < V_{fa}$.



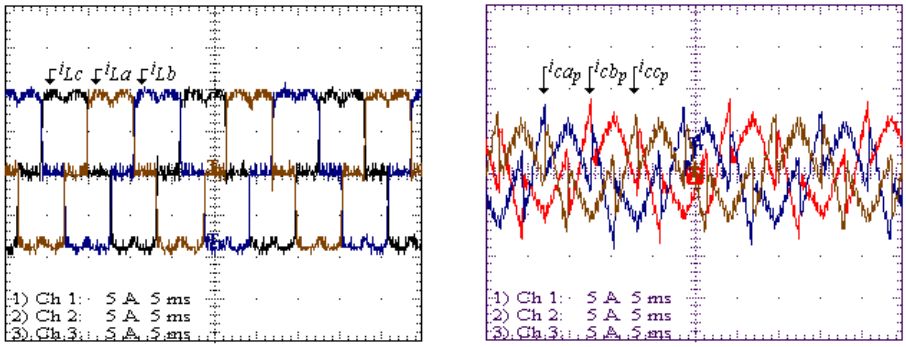
(a) (b) (c)

Fig. 12. Reference current s ($i^*_{sa,b,c} = i^*_{ca,b,c}$): (a) $V_{sa} \cong V_{fa}$; (b) $V_{sa} > V_{fa}$, and (c) $V_{sa} < V_{fa}$.



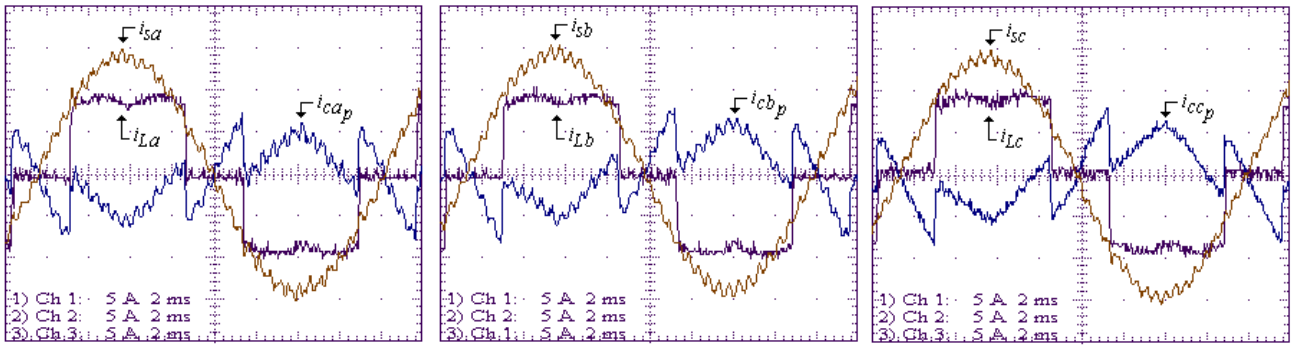
(a) (b) (c)

Fig. 13. SRF-based controller currents: (a) Fundamental active component of the load current in *dq* axis id^e_{dc} ; (b) dc-bus controller output ib_{dc} ; dc component of the synchronous reference frame id^e_c .



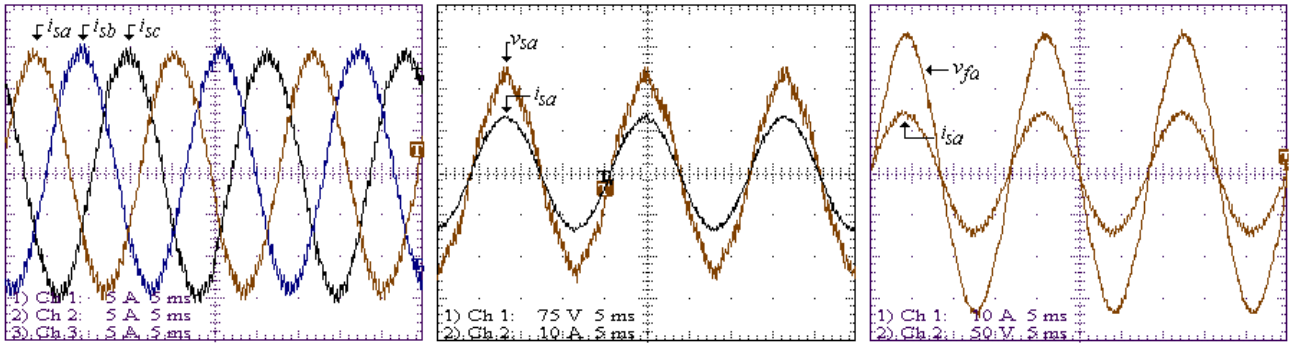
(a) (b)

Fig. 14. UPS currents: (a) Three-phase load currents $i_{La,b,c}$; (b) Three-phase parallel compensating currents i_{ca,b,c_p} .



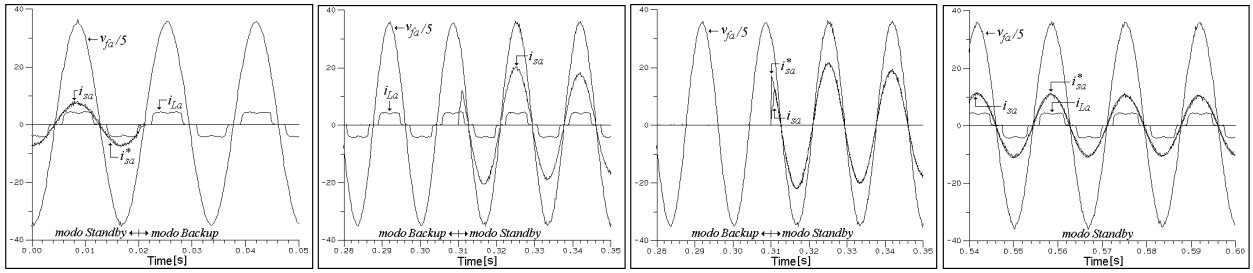
(a) (b) (c)

Fig. 15. Details of the input currents $i_{sa,b,c}$, load currents $i_{La,b,c}$, and parallel compensation currents i_{ca,b,c_p} : (a) Phase *a*; (b) Phase *b*; (c) Phase *c*.



(a) (b) (c)

Fig. 16. (a) Three-phase input currents $i_{s\,a,b,c}$; (b) Input voltage v_{sa} , and input current i_{sa} ; (c) Output voltage v_{fa} , and input current i_{sa} .



(a) (b) (c) (d)

Fig. 17. Transition modes: (a) Standby-Backup transition mode – output voltage v_{fa} , input current i_{sa} , reference input current i^*_{sa} and output current i_{La} ; (b) and (c) Backup-Standby transition mode; (d) Standby mode

V. CONCLUSIONS

Performance analysis of a three-phase line-interactive UPS system with series-parallel active power-line conditioning capabilities has been presented. The control algorithm using SRF-based controller was described and experimentally tested. The active power flow control, obtained from an additional voltage dc-bus controller, was discussed taking into account battery charging and undesired conditions, such as, input voltage variations (undervoltage, overvoltage, etc.), total harmonic distortion of the load currents, displacement factor ($\cos\phi_1$). Such analysis allows designing both the series and the parallel converters with an adequate power rating.

An advantage of the implemented and tested line-interactive UPS system is the smaller power rating handled by both series and parallel converters during the UPS standby mode of operation. Thereby, the efficiency of the system is increased.

Sinusoidal and regulated output voltages, sinusoidal input currents and high input power factor were obtained. Thus, it has been demonstrated that the obtained experimental results confirm the presented theoretical studies.

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