ELECTRONIC BALLAST FOR FLUORESCENT LAMPS WITH THE PFC STAGE INTEGRATED TO THE RESONANT INVERTER

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Abstract – **Studies about the integration of the PFC stage with the dc-ac conversion on electronic ballasts for fluorescent lamps are presented on this paper. The extension of the Moisin's topology is made for the use of a full-bridge rectifier stage. The design procedures developed are also extended for the continuous input current charge pump power factor correction (CIC-CPPFC). The analysis is focused on reliability, simplicity, and lowers the component count for electronic ballasts. Experimental results from a prototype designed with the methodology developed on this work, are also shown. Showing the simplicity for achieving high power factor of the proposed methodology, experimental results of several integrations applied on commercial electronic ballast will be presented on the final version.**

I. INTRODUCTION

Fluorescent lamps have negative impedance characteristics in the desired operation region [1]. Therefore, they cannot be connected directly to the utility line, but require some form of current-limiting control to prevent their destruction by excessive current, i.e. ballast. The ballast must provide the operating and starting voltage and also limit the lamp current.

In order to obtain compact electronic ballast and eliminate undesirable characteristics like audible noise, flickering and stroboscopic effects, the operating frequency must be raised. In the case of fluorescent lamp operating at high frequency, the luminous efficacy increases by about 20% [2], which reduces the energy consumption of the system.

The high-frequency electronic ballast converts the utility line frequency to high-frequency output. Normally, it consists of a full bridge diode rectifier and a dc-ac inverter operating at high frequency to drive the lamp.

With no power factor correction (PFC), the current drawn by the ballast from the utility line will contain significant harmonics, and consequently will operate at poor power factor [3]. A simple solution to improve the power factor is adding a passive filter. However, the passive filter is inefficient and heavy since it operates at the line frequency [4].

The usual solution to meet the line input current harmonics and improve the power factor is the addition of a second power processing stage, called the PFC stage. In this solution, an active power factor correction stage is added. Normally employing the discontinuous current mode boost converter, as shown in Fig. 1, these stage make the line current naturally follow the sinusoidal line voltage waveform [5]. The PFC stage also generates a regulated dc bus.

However, the two stages approach increases the cost, besides reducing reliability and efficiency [6], since the power is processed twice.

To relieve these shortcomings, several single-stage electronic ballasts have been proposed [7]. The main idea is that the PFC stage and the inverter share a common switch so one switch and its controller can be eliminated and the cost is reduced, as shown in Fig. 2. The use of this solution brings some drawbacks like high dc bus voltage stress during the lamp start-up, so high-voltage rating bulk capacitor and power switches have to be used. Additionally, the use of self-oscillating command is inviable due to one of the switches take the current not only from the inverter but also from the dc-ac inverter.

In this paper, a topology, proposed on the U.S patent 5.691.606 [8] by Moisin et al., which overcomes the drawbacks of the previous solution is extended for the use of a full-bridge input rectifier and design methodology are developed with practical results. The analysis shows that the CIC-CPPFC [9] concept can be derived from the topology proposed, so new design procedures for this kind of converter are developed. Proving the simplicity of the proposed design methodology, results coming from the integration of several commercial electronic ballasts will be shown

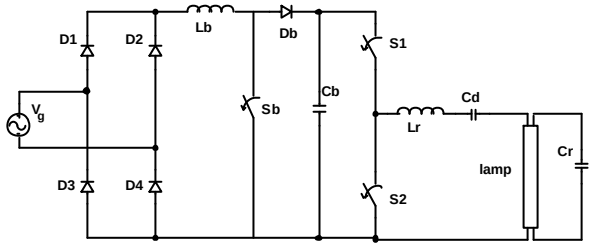


Fig. 1 – Electronic ballast with PFC boost converter.

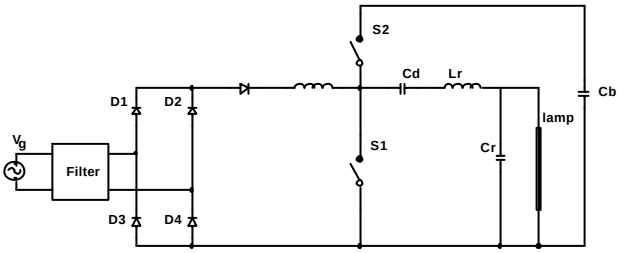


Fig. 2 – Integrated single-stage PFC electronic ballast.

II. PROPOSED TOPOLOGY

A. *Circuit Derivation.*

The topology proposed by Moisin et al., therefore in this paper called Moisin's topology, is shown in Fig. 3. The circuit includes a feedback capacitor (C_{in}) which provides a feedback path for a portion of the high frequency current to the rectifier. The feedback capacitor reduces the non-linear characteristics of the input rectifier, thus providing almost a linear load on the input power supply. The inductor L_{in} reduces the input current ripple minimizing the input filter's (L_f-C_f) volume.

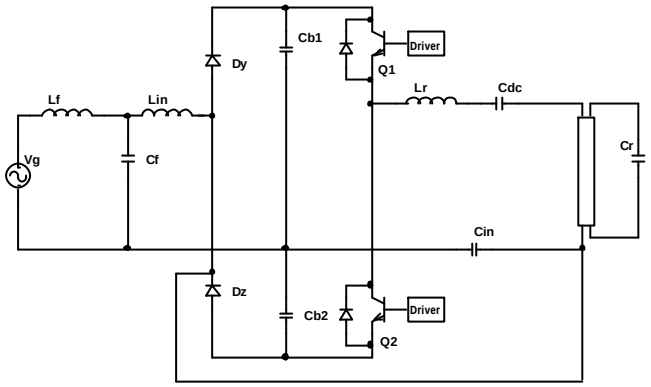


Fig. 3 – Topology proposed by Moisin et al.

While V_g is positive, the circuit can be represented by its equivalent shown in Fig. 4(a). Replacing the inverter and the resonant tank by a high frequency current source and ignoring the ripple on the dc bus voltage, the circuit presented in Fig. 4(b) can be obtained. The voltage source $|V_g|$ can be replaced by a full-bridge rectifier as shown in Fig. 5. Therefore the structure can be used in 220V lines without the drawback of the high dc bus voltage present on the original topology.

The capacitor C_{in} can be shifted to parallel with D_y with no effects on the input current at all and the resulting circuit is presented in Fig. 6(a). Although the absence of the diode D_x, the circuit derived from the original topology has the same operating characteristics of the CIC-CPPFC [9], shown in Fig. 6(b).

B. *Unity Power factor Condition.*

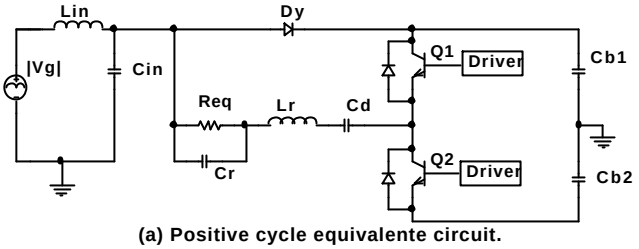
In steady state analysis, three assumptions are made on the circuit shown in Fig. 7:

The voltage across C_b is assumed constant.

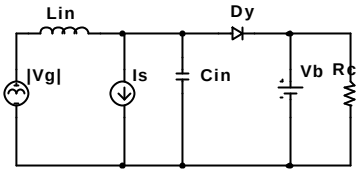
Due to the presence of the input inductor L_x, the current i_x is continuous.

The switching frequency is much higher than the line frequency so that the line voltage can be assumed to be constant over a switching cycle.

Two topological stages exist in one switching cycle in steady state, as shown in Fig. 8. The main switching waveforms are presented in Fig. 9.



(a) Positive cycle equivalente circuit.



(b) Substituion of the inverter and load by a current source.

Fig. 4 – Equivalent circuits while V_g is positive.

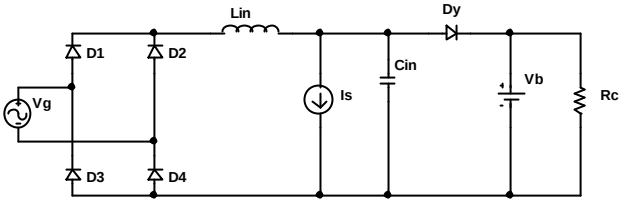
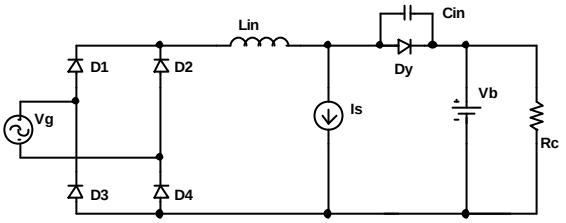
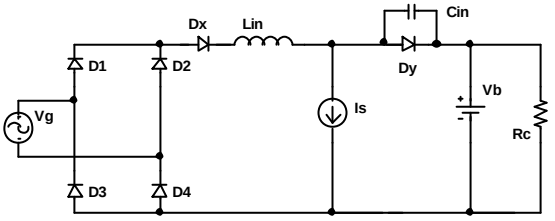


Fig. 5 – Full-bridge rectifier applied on the structure under analysis.



(a) Extended circuit.



(b) CIC-CPPFC circuit.

Fig. 6 –Comparison between the extended and the CIC-CPPFC equivalent circuit.

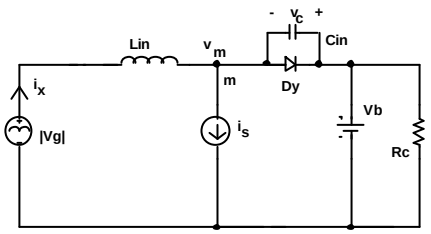


Fig. 7 – Circuit under analysis.

During the first mode (D_y-off) the rectified input current is:

$$i_x(t) = I_s \sin(q)\cos(w_o t) + \frac{|v_g(t)| \quad V_B}{Z_o}\sin(w_o t) + g \qquad 0 < t < t_2 \qquad (1)$$

Where: $w_o = \frac{1}{\sqrt{L_{in}C_{in}}}$, $Z_o = \sqrt{\frac{L_{in}}{C_{in}}}$ and

$$g = \frac{I_s w_o^2}{w_s^2 \quad w_o^2} \; sen(w_o t + q) \quad sen(w_s t + q) \; + \frac{I_s w_o \cos(q)}{w_s + w_o} sen(w_o t)$$

During the second mode (D_y on) the input current is:

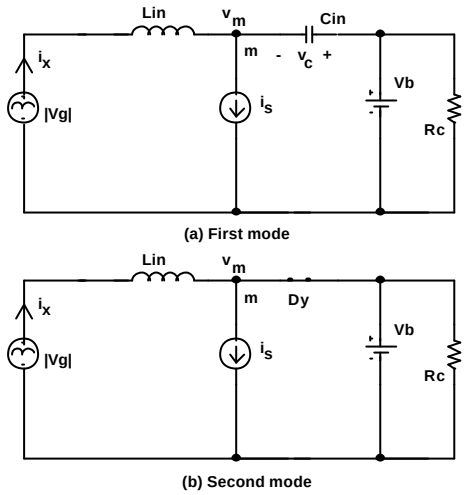


Fig. 8 – Two topological stages of Fig. 7.

$$i_x(t) = i_x(t_2) + \frac{|v_g(t)| \quad V_B}{L_{in}}(t \quad t_2) \quad t_2 < t < t_3 \qquad (2)$$

The average rectified line input current is equal to the average inductor current over a switching cycle and is given by:

$$I_x = \frac{1}{T_s}\int_0^{t_3} i_x(t)dt = \frac{1}{T_s}\left[\int_0^{t_2} i_x(t)dt + \int_{t_2}^{t_3} i_x(t)dt\right] \qquad (3)$$

After substituting (1) and (2) into (3), the simplified solution can be found:

$$I_x = \frac{|v_g(t)|}{Z_o w_o T_s} \; 1 \quad \cos(np) \; + y \qquad (4)$$

Where: $n = \frac{w_o}{w_s}$,

$$y = \frac{I_s}{2p} \; \frac{n\sin(np)}{1 \quad n^2} + \frac{1}{1+n} \; 1 \quad \cos(np) \; + \frac{P_o}{V_p} \; \frac{V_B}{Z_o w_o T_s} \; 1 \quad \cos(np)$$

and P_o V_o are the output power and line peak voltage, respectively. Unit power factor can be obtained when $y = 0$, which is:

$$I_s = \frac{2p \; \frac{V_B}{Z_o w_o T_s} \; 1 \quad \cos(np) \quad \frac{P_o}{V_p}}{\frac{n\sin(np)}{1 \quad n^2} + \frac{1}{1+n} \; 1 \quad \cos(np)} \qquad (5)$$

Under the condition of (5) unity power factor can be obtained since (4) becomes proportional to the line input voltage. The dc bus voltage is approximated by:

$$V_B = \frac{I_s}{2p} \; \frac{n\sin(np)}{1 \quad n^2} + \frac{1}{1+n} \; 1 \quad \cos(np) \; + \frac{P_o}{V_p} \; \frac{hV_p^2}{2P_o} \; 1 \quad \cos(np) \qquad (6)$$

C. Extension of the topology for a electronic ballast

Since the series resonant parallel-loaded tank can be considered a high frequency current source, the electronic ballast obtained is shown in Fig. 10.

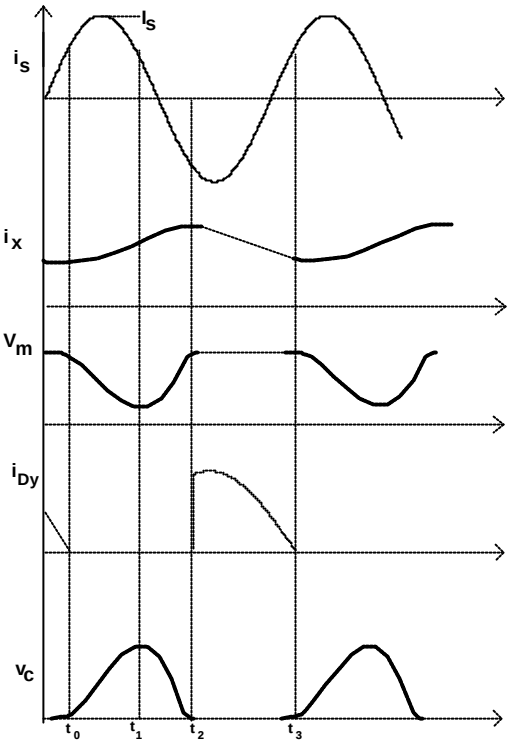


Fig. 9 – Switching waveforms.

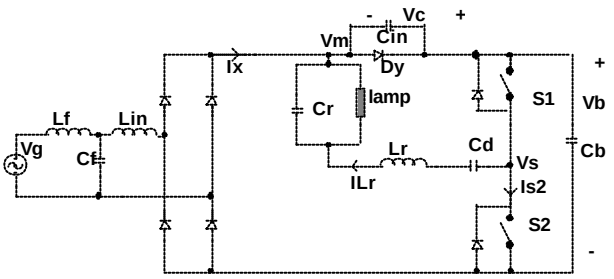


Fig. 10 – Electronic ballast derived from the analysis of the Moisin's topology.

III DESIGN CONSIDERATIONS

The objective of the design is to choose the best value of 'n', and consequently find the values of V_B, C_{in}, and the input inductor L_{in}. Taking the dc bus voltage as a limiting parameter, the value of 'n' can be obtained employing (6). Operating under unity power factor condition, the instantaneous input power is:

$$p_{in}(t) = \frac{|v_g(t)|^2}{Z_o w_o T_s} \; 1 \quad \cos(np) \qquad (7)$$

Taking the average over one half line cycle yields:

$$P_{in}(t) = \frac{V_p^2 f_s}{2 Z_o w_o} \; 1 \quad \cos(np) \qquad (8)$$

Since $P_o = hP_{in}$, C_{in} can be obtained manipulating (8):

$$C_{in} = \frac{2P_o}{h f_s V_p^2 \ 1 \ \cos(np)} \quad (9)$$

The value of L_{in} can be found trough the relationship between the switching frequency and the resonant frequency defined by L_{in} and C_{in}.

$$L_{in} = \frac{hV_p^2}{4n^2 p^2 f_s P_o} \quad (10)$$

IV EXPERIMENTAL VERIFICATIONS

To verify the proposed power factor correction topology, a 2x40W proof-of-concept prototype was built. The schematic diagram is presented in Fig. 11. Fig. 12 shows the dc bus voltage as a function of the 'n' parameter for the electronic ballast proposed. Choosing $n = 0.6$ the dc bus voltage is approximated 390V.

Operating at 40 kHz with 110V rms line input the circuit parameters are the following:

L_{in}=3.6mH L_r=1.81mH C_d=150nF
C_{in}=18nF C_r=15nF C_b=47µF

The experimental results are:

P_{in}=84W PF=0.989 THD=13.18%
CF=1.65 V_b=390.8V ?=91.3%

The measured line input current and its harmonic spectrum are presented in Fig. 13. The line harmonics components satisfy IEC 51000-3-2 for lightning applications. The measured lamp current is shown in Fig. 14 and the measured crest factor is about 1.65. The I_{in} current is presented in Fig. 15. The current ripple is very small when compared with the traditional DCM solution for PFC. Fig. 16 presents the switch voltage and current waveform, as can be seen the inverter operates at ZVS reducing the switching losses. During the startup process the dc bus voltage increases due to the rising of the resonant tank current. This characteristic can be avoided with the use of self-oscillating drivers on the inverter stage.

Investigating the commercial feasibility of the proposed topology, commercial ballasts available on the market were tested. With power ranging from 1x40W to 2x110W, every ballast tested could attend the IEC 51000-3-2. Fig. 17 shows for the input voltage and current for the 1x40W ballast before the insertion of the PFC circuit proposed.

On the 1x40W electronic ballast the following components were added:

L_f=77.3mH L_{in}=4.1mH
C_f=27nF C_{in}=15nF

After the inclusion of the circuit, as shown in Fig. 18, the input current could clearly satisfy the IEC rules. The input current THD in this case was reduced from 142% to 11.92%. The same characteristics can be observed in Fig. 19 and Fig. 20 where the results for the 2x110W are presented. For the 2x110W electronic ballast the parameters are as follows:

L_f=14.6mH L_{in}=0.475mH
C_f=100nF C_{in}=68nF

The input current THD was reduced from 139.8% to 28.7% resulting the rise of the total power factor from 0.63 to 0.972. Fig. 21 shows the dc bus voltage during the startup process.

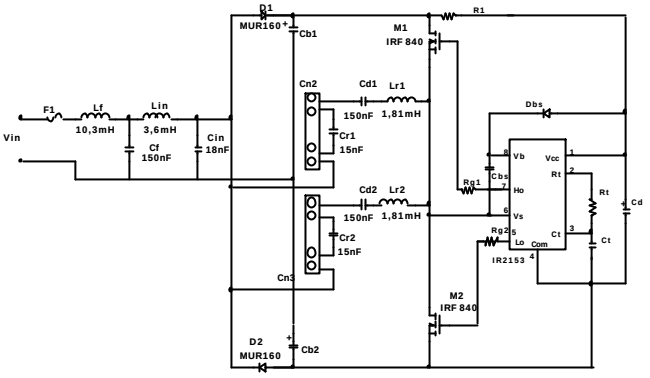


Fig. 11 – Diagram of the prototype implemented.

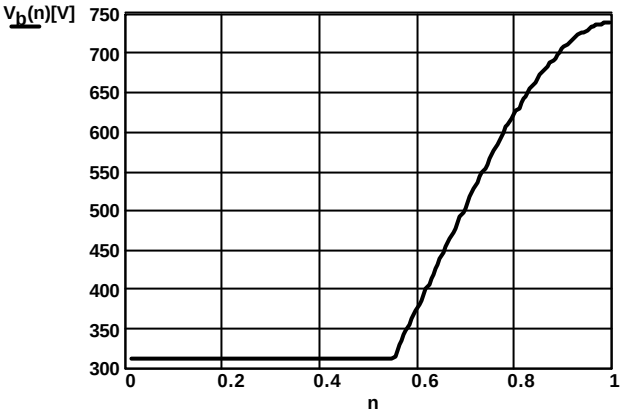


Fig. 12 – Dc bus voltage as a function of the 'n' parameter.

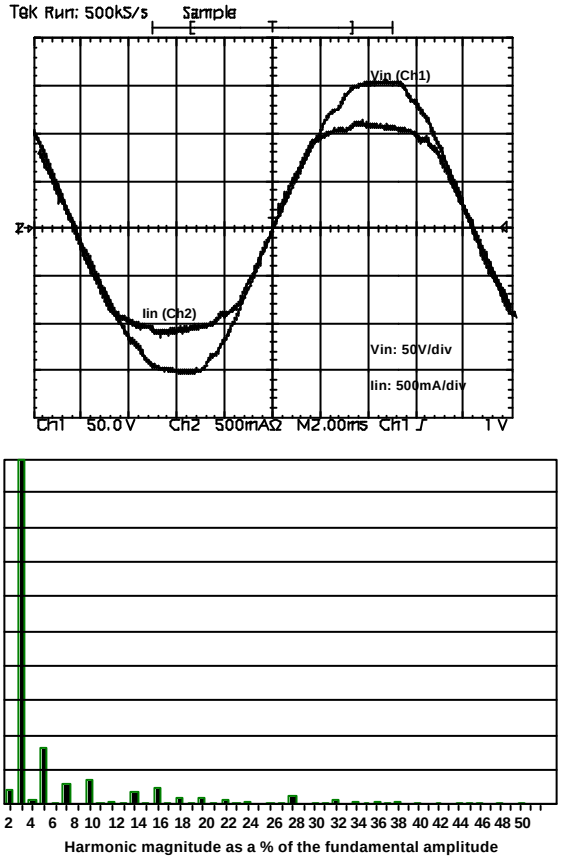


Fig. 13 – Measured line input current and its harmonic spectrum (t: 2ms/div).

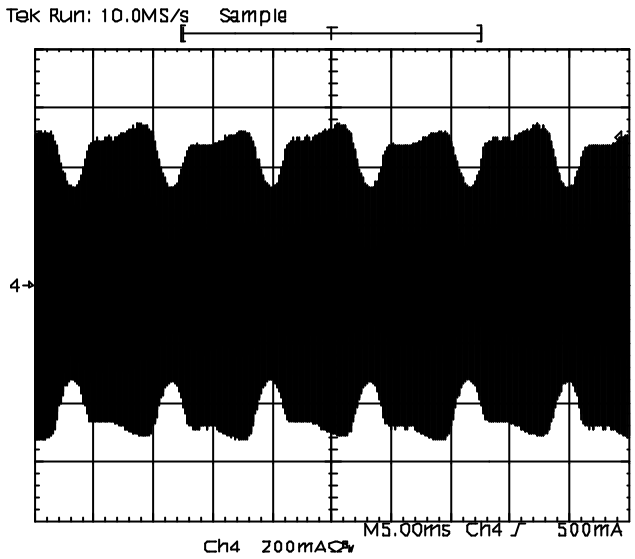


Fig. 14 – Measured lamp current waveform (i:200mA/div;t: 5ms/div) .

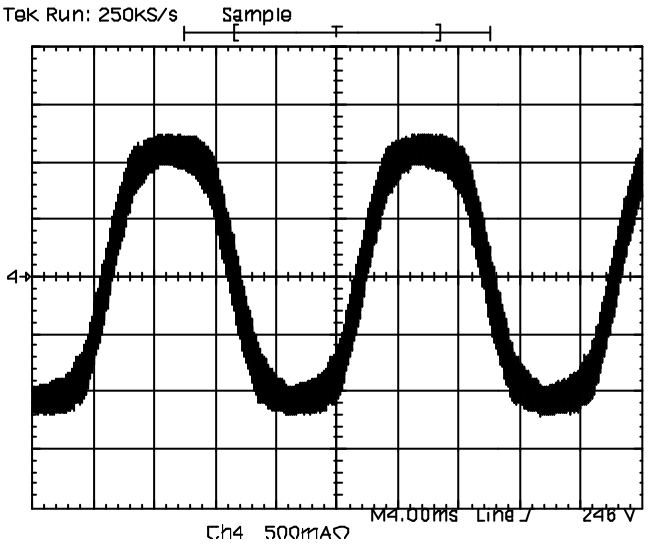


Fig. 15 – L_{in} current. (i:500mA/div;t:5ms/div).

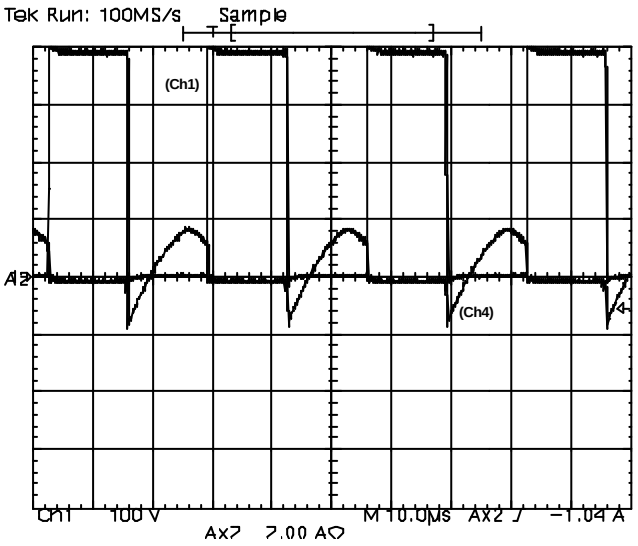


Fig. 16 – Switching voltage and current (i:2A/div;v:100V/div;t:5ms/div)

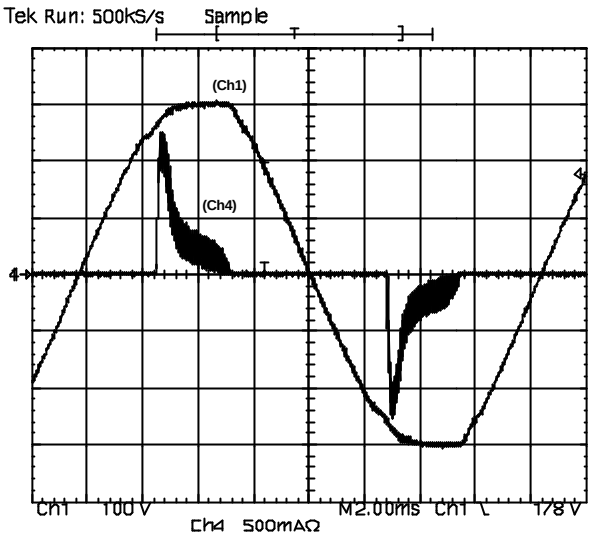


Fig. 17 – Input waveforms for the 1x40W commercial ballast. (i:500mA/div;v:100V/div;t:2ms/div)

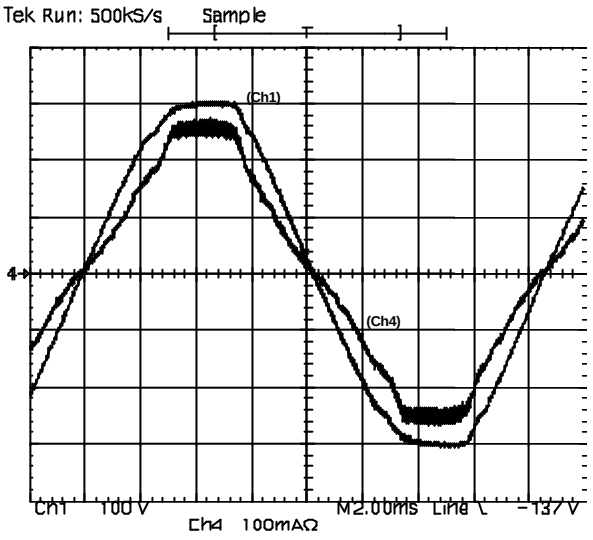


Fig. 18 – Input waveforms for the 1x40W commercial ballast with the PFC circuit proposed. (i:100mA/div;v:100V/div;t:2ms/div)

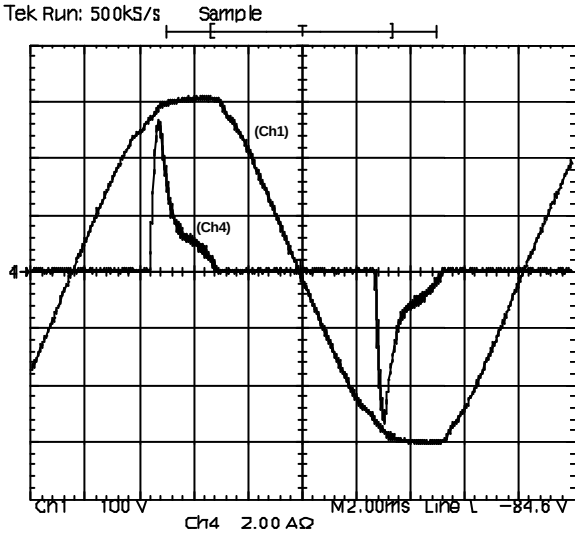


Fig. 19 – Input waveforms for the 2x110W commercial ballast. (i:2A/div;v:100V/div;t:2ms/div)

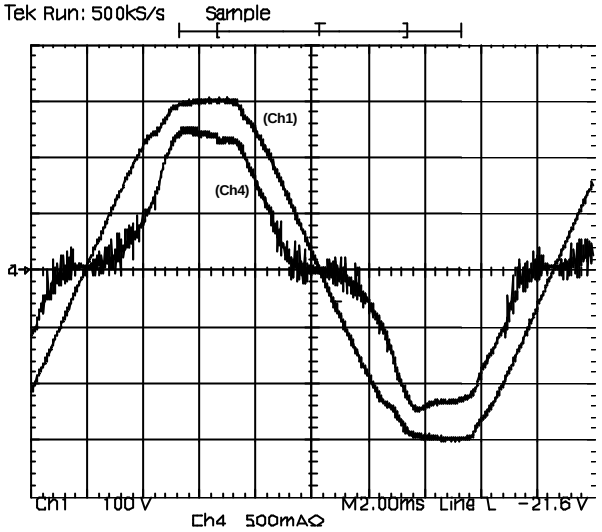


Fig. 20 - Input waveforms for the 2x110W commercial ballast with the PFC circuit proposed. (i:500mA/div;v:100V/div;t:2ms/div)

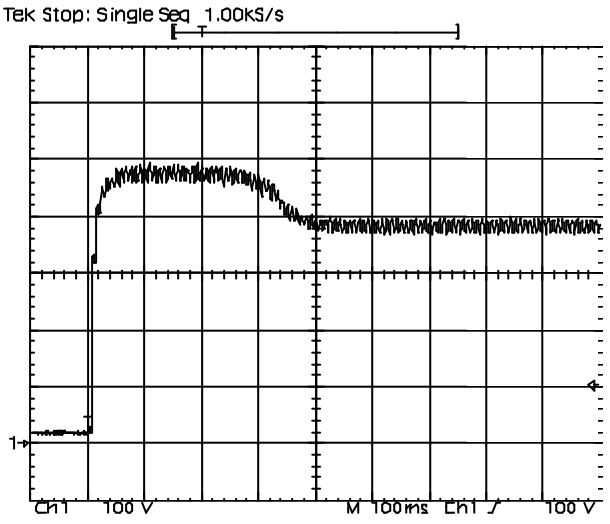


Fig. 21 – Dc bus voltage during the startup process.

V CONCLUSIONS

The extension of the Moisin's topology was presented, analyzed and implemented. Due to the similarity between the equivalent circuits, the design methodology proposed on this paper can be also used on the CIC-CPPFC electronic ballast. Differently from the previous design methodology proposed [9], the analysis developed on this paper takes account, and try to find the optimum value of the relationship between the switching frequency and the resonant frequency defined by L_{in}-C_{in}. Another improvement of the methodology proposed is the evaluation of the dc bus voltage.

The power switches carry only the resonant inductor current so low current rating devices can be used, when compared with others integration solutions. This characteristic allows the use of a self-oscillating driver, like in commercial electronic ballasts.

Therefore, the developed ballast has potential low cost and reliability compared with previous single-stage high power factor electronic ballasts. The low input current ripple allows the reduction of the input filter's volume, a very important feature when compared with previous solutions employing DCM. The experimental results verify the theoretical analysis and circuit operation.

REFERENCES

[1] Yang, Y. & Chen, C., **Steady-State Analysis and Simulation of a BJT Self-Oscillating ZVS-CV Ballast Driven by a Saturable Transformer**, IEEE Transactions on Industrial Electronics, vol.46, n° 2, April 1999, pp.249 – 260.

[2] E. E. Hammer & McGowan, T. K., **Characteristics of Various F40 Fluorescent Systems at 60Hz and High Frequency**, IEEE Trans. Ind. Applications., vol. 21, n.1, pp. 11-16, 1985.

[3] Grotzbach, M., **Line side behavior of uncontrolled rectifier bridges with capacitive DC smoothing**, Proc. European Conference on Power Electronics and Applications (EPE),1989, pp. 761-764.

[4] Redl, R., & Balogh, L., **Power factor Correction in Bridge and Voltage-Doubler Rectifier Circuits with Inductors and Capacitors**. Proc. European conference on Power Electronics and Applications (EPE), 1999, pp. 466-472.

[5] Liu, K. H. & Lin, Y.L., **Current Waveform Distortion in Power Factor Correction Circuits Employing Discontinuous Mode Boost Converter**, IEEE Power Electronics Specialists Conf.,1989,pp.293-298.

[6] Brumatti, M., Resende, C. Z., Có, M. A., Simonetti, S. L. & Vieira, L. F., **Single Stage Self-Oscillating HPF Electronic Ballast**, IEEE Industry Applications Society – Annual Meeting, 2002.

[7] Alves, J.A., Perin, A.J., Barbi, I., **An Electronic Ballast with High Power Factor for Compact Fluorescent Lamp**, IEEE Industry Application Society – Annual Meeting, 1996, pp.2129 – 2135.

[8] Moisin et al., M. S., **Ballast Circuit for Fluorescent Lamp**, United States Patent 5.691.606, November, 1997.

[9] Qian, J. & Lee, F.C., **A New Continuous Input Current Charge Pump Power Factor Correction (CIC-CPPFC) Electronic Ballast**, IEEE Industry Application Society – Annual Meeting, 1997, pp.2299 – 2306.

[10] Maehara, M., **Inverter Device for Stable, High Power Factor Input Current Supply**, United States Patent 5.274.540, December, 1993.

[11] Pitel, I. J., **Tuned Oscillator Ballast Circuit**, United States Patent 4.045.711, August, 1977.

[12] Kulka, R. J., **Low harmonic Compact Fluorescent Lamp Ballast**, United States Patent 5.223.767, June, 1993.

[13] Wong, J. M., **Fluorescent Lamp Ballast with Regulated Feedback Signal for Improved Power Factor**, United States Patent 5.387.848, February, 1995.