SINGLE AND THREE-PHASE DIGITAL PLL STRUCTURES BASED ON INSTANTANEOUS POWER THEORY

Sigmar Maurer Deckmann Fernando Pinhabel Marafão Marcelo Suzart de Pádua

State University of Campinas – UNICAMP
School of Electrical and Computer Engineering – FEEC
P.O. Box 6101 – 13081-970 – Campinas – SP – Brazil
sigmar,fmarafao@dsce.fee.unicamp.br

***Abstract* – This paper discusses the design and analysis of digital Phase Locked Loop (PLL) algorithms for power electronics applications. The design is based on a stationary *abc* frame model using instantaneous active or non-active power definitions as the PLL reference. Both three-phase and single-phase structures are considered. Since the fundamental waveform and frequency tracking is of great interest for utility connected devices, the PLL steady state and transient dynamic performances are analyzed under different supply disturbing conditions. Simulation results validate the models and experimental results using a DSP board system confirm the expectations.**

KEYWORDS

Phase-locked loop, instantaneous power theory, frequency identification, fundamental component, synchronization.

I. INTRODUCTION

Accurate and fast detection of the utility mains frequency and fundamental waveforms are of great interest for power systems control and power electronics applications. The controllers of most electronic equipments, such as power systems relays, active power filters, uninterruptible power supplies (UPS), controlled rectifiers, FACTS devices, etc, must be synchronized with the fundamental frequency of the utility voltage. For this reason, different algorithms and circuits have been proposed in the last decades in order to provide the necessary information [1-4]. Fast dynamic response, precision in steady state and robustness under the presence of harmonics or transients have been the most important issues to deal with.

The methods of frequency identification or synchronization are usually derived from zero crossing techniques, adaptive discrete Fourier transform, demodulation techniques and phase-locked loop (PLL) systems [1,2]. Each of these methods presents advantages and disadvantages, depending on the final application, utility conditions and the characteristics of the digital system they are implemented.

Originally the PLL systems were derived from the classical feedback control structure using a phase detector, a voltage controlled oscillator (VCO), a low-pass filter and a comparator. Their use in a vast sort of different applications showed useful results in electronic devices, power system control and communications networks [2]. However, the recent and increasing use of digitally processed systems have pointed to the necessity of an improved digital PLL design, best suited for this new context. In the case of power system control, the most promising approaches have been derived from the instantaneous power definitions [5,6,8].

Some of the recent works were based on synchronous frame (*dq*) transformation, and present quite useful results, although at the expense of increased complexity due to such transformation [3,4,7]. Other interesting strategies use stationary frames (*ab* or *abc*) [5,6] to model the three-phase PLL system and are also based on instantaneous power references.

This paper discusses a methodology to design and analyze digital PLL structures for both, three or single-phase applications. The PLL is based on a stationary *abc* frame model and instantaneous active or non-active power definitions. Since the precision and dynamic behavior of the PLL is extremely dependent on its proportional-integral (PI) regulator, common to all conventional models, the design and practical aspects of implementing such regulator are also discussed. Simulation results validate the model under different conditions and experimental results using a Digital Signal Processor (DSP) confirm the expectations.

II. THREE-PHASE POWER SYSTEM PLL

The interest on a three-phase power system PLL algorithm can easily be explained since it does not need any kind of low-pass filter. The resulting lower order structure has an improved dynamic response compared to the traditional PLL circuits using VCO and phase detectors.

The power based PLL structure is described in Fig. 01 and uses a proportional-integral (PI) controller to track the system angular frequency ($\omega = 2\pi f$) and a digital integrator to transform the evaluated angular frequency (ω) into the angular phase function $\theta(t) = \omega t$. Since the interest is to develop a digital PLL, a sampling delay function may be added to the PLL model in order to represent the sampling process (sampling time T_s). A feed-forward signal ($\omega_{ff} = 2\pi f_n$) is also included to improve the initial dynamic performance of the PLL system, where f_n is the utility nominal frequency.

A. Stationary abc Frame PLL Model

The approach is based on using phase or line derived voltages as the PLL input signals [5], represented by v_{xa}

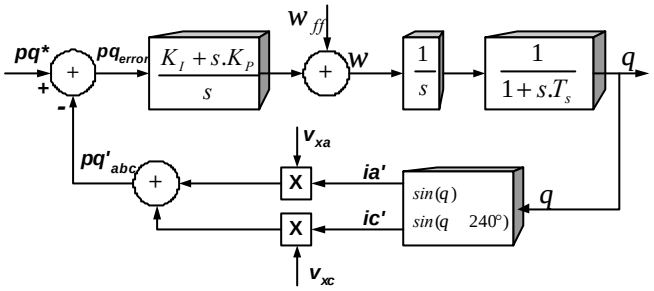

Fig. 01 – Generalized Three-Phase Power System PLL Model.

and v_{xc} in Fig.01. Fictitious feedback current signals are synthesized from the final evaluated angular frequency (w) (or phase angle function $q=w.t$) and used to calculate a fictitious instantaneous active or non-active power component symbolically represented by (pq'_{abc}). If necessary, a fundamental waveform generation block could use to emulate the fundamental positive sequence components of the input voltages.

B. Fictitious Active (p-PLL) and Non-Active (q-PLL) Instantaneous Power References

In terms of ab components, as discussed in [6], the three-phase PLL reference could be based on instantaneous active or non-active power components.

However, using directly the stationary frame abc variables, equations (1) and (2) can be used [10], depending on which reference is selected (active or non-active power), respectively:

$$p_{abc} = v_a.ia' + v_b.ib' + v_c.ic' . \quad (1)$$

$$q_{abc} = \frac{1}{\sqrt{3}} \times (v_{ab}.ic' + v_{bc}.ia' + v_{ca}.ib') . \quad (2)$$

Since the fictitious feedback currents are mathematically imposed to be sinusoidal and balanced (they always sum up to zero, $i_a'+i_b'+i_c'=0$), the above fictitious powers could also be calculated, even in the presence of neutral wire (three-phase four wire system), thus:

$$p_{abc} = v_{ab}.ia' + v_{cb}.ic' = v_{xa}.ia' + v_{xc}.ic' . \quad (3)$$

$$\begin{aligned} q_{abc} &= \frac{1}{\sqrt{3}} \times [(v_{bc} + v_{ac}).ia' + (v_{ac} + v_{ab}).ic'] \\ &= \frac{1}{\sqrt{3}} \times [v_{xa}.ia' + v_{xc}.ic'] . \end{aligned} \quad (4)$$

The filtering and controlling capabilities of the PI regulator will try to ensure that the sinusoidal and balanced fictitious currents are mathematically in phase or orthogonal to the corresponding measured voltages, according to the suitable features originated from the instantaneous active and non-active power definitions [11].

Therefore, depending on the available number of voltage sensors and the information intended to be extracted from the PLL, it is possible to choose the instantaneous power reference from (1-4). Notice that v_{xa} and v_{xc} have different values depending on choosing active or non-active power reference.

Considering the system's frequency identification as the most important task, the reference choice does not matter. However, for some applications, it could be interesting to track the utility phase-angle function (q) in order to generate a fundamental waveform reference in-phase or orthogonal to the mains voltages. Such strategies are used, for example, in active controlled rectifiers, shunt and series active filters, UPS, distributed power generation systems, etc. In these cases, choosing the reference depends on the desired control strategies and goals.

If the instantaneous power reference is set to zero ($pq^*=0$) and the control error signal is defined by the difference ($pq_{error} = pq^* \pm pq_{abc}$), it is worth to comment on the expected results concerning the PLL performance [6]. In order to cancel the instantaneous power error, the fictitious power must also converge to zero. If the active power (p_{abc}) were defined as reference, the *p-PLL* will force the fictitious feedback currents to be orthogonal to the measured voltages and the resulting orthogonality ($\pm 90^o$), depends on the sign used to calculate the error: current advanced ($+90^o$) if negative sign ($-p_{abc}$) and delayed (-90^o) if positive ($+p_{abc}$) sign were chosen.

On the other hand, if the non-active power (q_{abc}) were used as reference, the *q-PLL* will force the fictitious currents to be in-phase (0^o) or in opposite (180^o) to the measured voltages, respectively if negative or positive sign were attributed for (q_{abc}).

If, e.g., instantaneous active power reference with positive sign were defined and the evaluated angular frequency (w) closely tracks the measured voltage frequency, the fictitious phase currents are perfectly orthogonal lagging (-90^o) the corresponding fundamental phase voltages. Nevertheless, if for any reason the utility voltage frequency deviates from its nominal value (w_{ff}), the PI regulator will set its output to correct the final PLL angular frequency (w) so that the orthogonality between the fictitious currents and original phase voltages will be guaranteed.

Thus, using simple trigonometric manipulation, adding or subtracting a fixed known phase angle f, which could be either ($+/-90^o$) or (180^o) to the calculated PLL phase function $q(t)$, the fundamental voltage waveforms could be synthesized, e.g., using the resulting angle as the argument to a sinusoidal function table or polynomial approximation to speed-up the fictitious current calculation.

C. Design Methodology

As mentioned before, one of the most important points on designing the digital PLL is the correct tuning of the proportional and integral PI controller gains, which are closely related to its precision and dynamic behavior.

Although several papers have discussed this problem [3,7,8], there is great interest in a methodology capable of providing the best tuning for both, three and single-phase application. This paper also considers the question of tuning the PI regulator's gains as a classical control problem.

Assuming that the usual sampling frequencies are

considerable higher than the systems bandwidth, the non-linear feedback functions of Fig.01 can be simplified to the linear structure of Fig.02. This is possible because small variations of yield $sin(\ )$ [3,4].

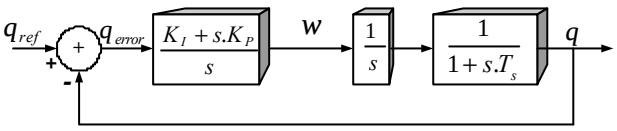

Fig. 02 – Simplified Three-Phase Power System PLL Model.

Given that the feed-forward term (w_{ff}) is just used for the initialization procedure, there is no need to consider it in the transfer functions.

Thus, assuming that the digital integrator and the sampling delay function represent the plant to be regulated by the PI controller, its transfer function can be expressed as following:

$$H_{plant}(s) = \frac{1}{s} \times \frac{1}{1+s.T_S}. \qquad (5)$$

The resulting open and close-loop transfer functions, including the controller and the plant, become respectively:

$$H_{OL}(s) = PI(s) \times H_{plant}(s) = \frac{K_I + s.K_P}{s} \times \frac{1}{s} \times \frac{1}{1+s.T_S}, \qquad (6)$$

$$H_{CL}(s) = \frac{H_{OL}(s)}{1+H_{OL}(s)} = \frac{K_p s + K_i}{s^3 T_S + s^2 + K_P s + K_I}. \qquad (7)$$

The resulting third-order system should be ideally controlled with fast time response, good dynamic performance, and small steady-state error, besides it should be robust under transients and noisy input. However, in practical applications this tuning is a very hard task, and the designer may choose to focus on the most important features, for each particular project.

Since no general methodology is capable of defining the optimum control gains to achieve the ideal PLL performance, different tuning methods can be applied.

The *symmetrical optimum method* used in [3,5,9] might be an efficient alternative for this problem. Such method defines the controller gains, so that the amplitude and phase frequency responses of (7) are symmetrically related to the *open-loop* crossover frequency (w_c), which is centered at the geometric mean of the pass-band frequencies of (7). According to this method, the proportional and integral gains can be associated with the crossover frequency by means of a normalizing factor ( ) and calculated by equations (8):

$$K_P = w_c, \qquad K_I = \frac{w_c^2}{a}, \qquad w_c = \frac{1}{a.T_S}. \qquad (8)$$

Equation (9) associates the factor with the theoretical damping factor [9], which defines the damping or filtering capabilities and the dynamic performance of the PLL model.

$$a = 2.V + 1. \qquad (9)$$

As it could be graphically verified [3], the bandwidth w_c decreases exponentially with the linear increasing of the damping or factor. In other words, as lower this factor is, as faster the PLL dynamics will be, but poorer will be its filtering capability, thus reducing the PLL robustness under distorted utility conditions.

Under the assumption of small sampling delays, the third order system (7) could be reduced to the *canonical form of second order system* (10), without affecting the control capabilities. Such consideration is possible since the pole relative to the sampling delay, placed in the left side of the s-plane, is quite far from the origin and the other two dominant poles. Thus

$$H_{CL}(s) = \frac{2x w_n s + w_n^2}{s^2 + 2x w_n s + w_n^2} = \frac{K_p s + K_i}{s^2 + K_P s + K_I} \qquad (10)$$

and the gains of the PI regulator could be designed as:

$$K_P = 2x w_n, \qquad K_I = w_n^2. \qquad (11)$$

where w_n is the *closed-loop* crossover frequency and is the damping factor.

D. Stability Analysis and Dynamic Performance

Considering a particular design with closed-loop crossover frequency (w_n) defined as 45 rad/s and =0.707, Fig. 03 shows the frequency response of the closed-loop system using *the second order method* (10-11), where K_P=64 and K_I=2,025. The step response in this case is depicted in Fig. 04 and confirms that the system is stable.

Fig. 05 and 06 illustrate, respectively, the open-loop and closed-loop response if the design were based on the *symmetrical optimum method* (7-8). The open-loop crossover frequency (w_c) was defined as 64 rad/s and the sampling frequency as 12kHz, then K_P=64 and K_I=22.

For both methods, if the closed-loop bandwidth were decreased, the convergence of the step response would be slower, however the PLL rejection to input noise and distortions would be increased. For practical applications, an interesting approach could be initialize the PLL with an extended bandwidth and then decrease it to the desired one.

III. SINGLE-PHASE POWER SYSTEM PLL

Since it could be necessary to track the frequency in single-phase applications, it is suited to modify the previous structure in order to ensure that it works in such situations.

All the discussions for the three-phase PLL are still valid. However in this case, the very convenient characteristic of automatically rendering constant active or non-active fictitious power is lost.

To overcome this problem, a digitally designed adaptative moving average window is used as a fast dynamic response low-pass filter and applied to the error signal (p_{error}), as depicted in the diagram of Fig. 07.

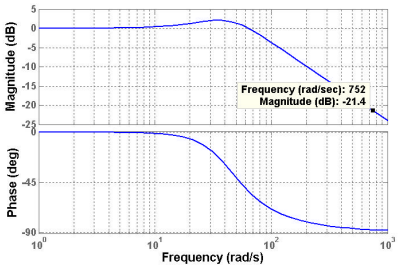

Fig. 03- Bode Diagram of the 3 PLL using second order method – closed-loop.

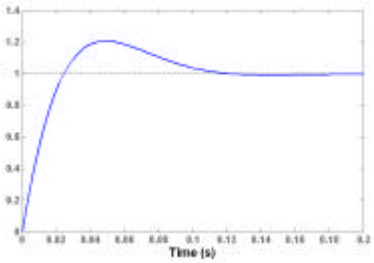

Fig. 04- Step Response of the 3 PLL using second order method.

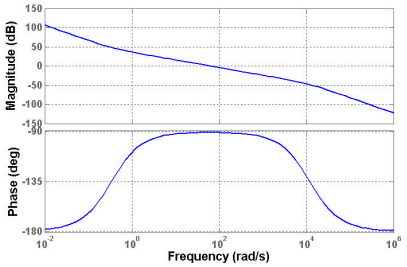

Fig. 05- Bode Diagram of the 3 PLL using symmetrical optimum method – open-loop.

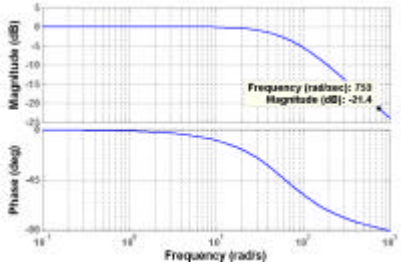

Fig. 06- Bode Diagram of the 3 PLL using symmetrical optimum method – closed-loop.

A. Stationary Single Phase PLL Model

Now, the approach is based on a single-phase voltage (v) measuring and the fictitious feedback current (i') to define the fictitious active power reference as following:

$$p = v.i' \quad . \tag{12}$$

So, the calculated power error is applied to the moving average filter in order to extract its mean value, which is forced to be zero in the same way as in the three-phase *p-PLL*. Thus the fictitious current is forced to be orthogonal to the input measured voltage.

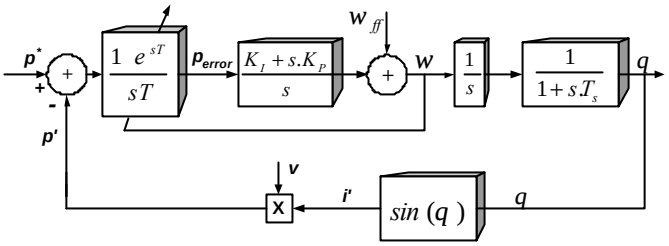

Fig. 07 – Generalized Single-Phase Power System PLL Model.

B. Adaptative Moving Average Filter

The moving average filter is designed in such a way to extract from the instantaneous oscillatory power (12), its constant mean value as in (13):

$$P = \frac{1}{T}\int_0^T p(t)dt \quad . \tag{13}$$

where T is the input fundamental period, which is dependent of the instantaneous evaluated angular frequency.

Considering the filter impulse response as $h(t)$ and using the following convolution, its output should be:

$$p(t) * h(t) = \int p(t)h(t-t)dt \quad . \tag{14}$$

Comparing (13) and (14), it is possible to notice that $h(t)$ is a rectangular pulse defined between 0 and T, with amplitude equal to 1/T:

$$h(t) = \frac{1}{T}[u(t) - u(t-T)] \ , \tag{15}$$

where $u(t)$ is the unit step function.

Thus, the moving average filter can be represented in the Laplace domain as:

$$H_{filter}(s) = \frac{1 - e^{-sT}}{sT} \quad . \tag{16}$$

Using Taylor series, the non-linear filter transfer function (16) can be simplified resulting the linear approximation as in (17). And since the values of the terms of order superior than 1 are insignificantly small at 60Hz, they can be neglected, rendering an almost constant and unitary gain:

$$H_{filter}(s) = \frac{1 - [1 - sT + \frac{(sT)^2}{2!} - \frac{(sT)^3}{3!} ...]}{sT} \approx 1 \quad . \tag{17}$$

In order to ensure that the number of samples in the fundamental window is always constant, this strategy needs to alter the window size or the sampling frequency according to the grid frequency variations. Such task can be done e.g., by manipulating the evaluated real angular frequency or taking into account the number of samples between two consecutive zero crossing of the generated (sinusoidal) fictitious current.

Hence, the single-phase PLL model leads to the same expressions of the three-phase case and the plant, open-loop and close-loop transfer functions yield identical. In addition, the simplified single-phase structure is equal to that presented in Fig. 02. Thus, all the previously discussed methodology of tuning the PI regulator gains is valid for both structures, as well as the stability and dynamic analysis.

IV. SIMULATION RESULTS

The most important problems affecting the PLL performance may be observed if the input signals are corrupted by harmonics, high-frequency noise, frequency variations, line notching and unbalances. Since these kinds of disturbing become more and more common in the supply networks, it is important to evaluate the PLL performance under such conditions. The simulations were carried out using the software PSIM/SIMCAD and C++ routines.

With the parameters adjusted according the *symmetrical optimum method*, the three-phase *p-PLL* was submitted to the following two simulation cases. The sampling frequency is 12kHz and w_c was set to 64 rad/s. Fig. 08 shows that even with 10% of harmonics and 5% of unbalance in the input three-phase voltages, the PLL is able to track the input frequency and phase angle ( ) in such a way that the fictitious currents are orthogonal (+90º) to the inputs. If the input fundamental waveforms are required, a waveform generator using (-90º) as argument can be used.

Then, adjusting the single phase PLL accordingly (10-11), with w_n = 45 rad/s and =0.707, Fig. 09 illustrates its good filtering and tracking performance.

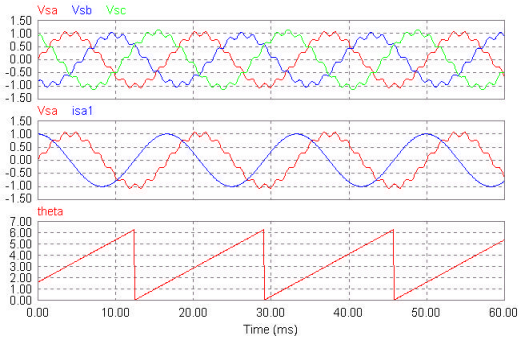

Fig. 08- 3 PLL with unbalanced and distorted input (h=11,10%).

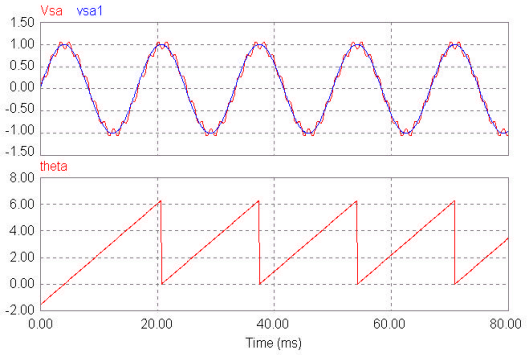

Fig. 09- 1 PLL with distorted input (h=11,10%).

V. DIGITAL IMPLEMENTATION AND EXPERIMENTAL RESULTS

While simulating or implementing in floating-point DSP, the PLL algorithms usually present good performance and are relatively simple to implement. However, if fixed-point microcontrollers or DSP were used, additional attention must be directed to ensure the desired performance.

The most important points are probably related to the saturation routines and anti wind-up strategies. Since the expected angular frequency is previously known (w_{ff}), it is recommended to limit the PI output (w) within an appropriate range (a percentage of the nominal angular frequency, e.g., 5%, 10%, etc.). This may avoid instabilities or even that the system converges to an undesired point.

Hence, in order to validate the previous simulations and discussion, next figures present preliminary results of the three-phase power system *p-PLL*, implemented using a 16 bits fixed-point DSP (ADMC401). The PI regulator gains were designed based on (10-11) and the sampling frequency was set to 12kHz.

Using w_n = 23.63 rad/s and =0.707 (K_P=32, K_I=5,122) Fig. 10 shows one of the input phase voltages and its corresponding fictitious current (upper traces), which follows the phase angle ( ) generated by the PLL tracking system (lower traces) and is advanced (+90º) to the input.

Fig. 11 and 12 present the input phase voltage (lower trace), its fundamental waveform (upper trace - generated using a sine function with [- 90º] as argument) and the PI input error (around zero). Note how the dynamic response can be improved changing the closed-loop bandwidth (w_n) from 23.63 rad/s to 90 rad/s. However, this could decrease the PLL filtering capabilities and its robustness to distorted, noise and unbalanced inputs.

As mentioned above, it is advisable to limit the PI output in a certain range. Nevertheless, if the range were quite narrow, it can affect significantly the dynamic response of the PLL. Note the difference between Fig. 13 (10% limit) and Fig. 14 (2% limit), where the time scales were 10ms and 20ms, respectively. The narrow range constrains the PI tracking dynamics, even if the system keeps working.

Finally, Fig. 15 presents an input phase voltage and its fundamental waveform (generated from -90º) and shows that the PLL frequency and phase angle tracking are not affected by a significant input voltage variation.

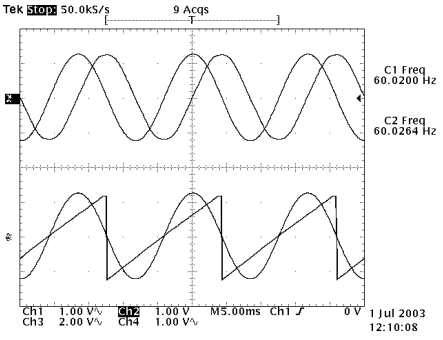

Fig. 10 – Input phase voltage, the PLL phase angle and the corresponding fictitious current.

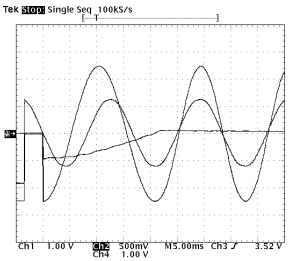

Fig. 11 – Input voltage, its fundamental waveform and the PI input error (w_n = 23.63 rad/s).

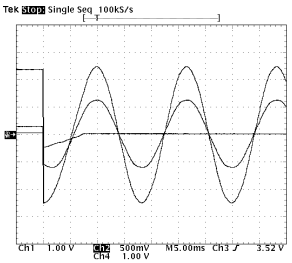

Fig. 12 – Input voltage, its fundamental waveform and the PI input error(w_n = 90 rad/s).

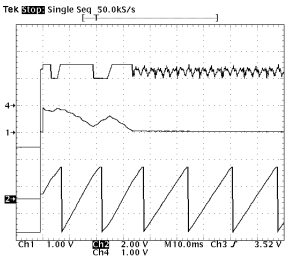

Fig. 13 – Instantaneous angular frequency (w - 10% limit), PI input error and .

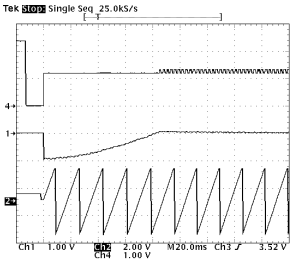

Fig. 14 - Instantaneous angular frequency (w - 2% limit), PI input error and .

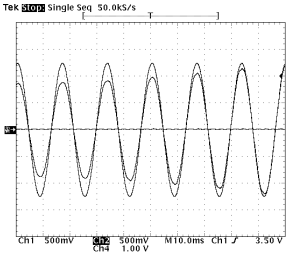

Fig. 15 – Input variation and its fundamental waveform.

VI. CONCLUSIONS

This paper proposes the design and analysis of digital Power System PLL structures, which are equally valid for three-phase and single-phase systems. Using stationary *abc* frame, the PLL model is based on active and non-active power definitions. Simulations and preliminary results have shown the performance and tracking capabilities of the digital PLL system. Moreover, practical aspects if implementing the PLL in fixed-point digital systems have been discussed.

ACKNOWLEDGEMENT

Support for this research comes from FAPESP, CAPES and Analog Devices. The authors thank Dr. E. A. Vendrusculo and Eng. L. A. Silva for the assistance on the experimental implementation.

REFERENCES

[1] Begovic, M.M., Djuric, P.M., Dunlap, S., Phadke, A.G., "Frequency Tracking in Power Networks in the Presence of Harmonics", *IEEE Transaction on Power Delivery,* Vol. 8, No. 2, April 1993, pp. 480-486.

[2] Hsieh, G.C., Hung, J.C., "Phase-Locked Loop Techniques – A Survey", *IEEE Transaction on Industrial Electronics,* Vol. 43, No. 6, December 1996, pp. 609-615.

[3] Kaura, V., Blasko, V., "Operation of a Phase Locked Loop System Under Distorted Utility Conditions", *IEEE Transaction on Industry Applications,* Vol. 33, No. 1, January/February 1997, pp. 58-63.

[4] Arruda, L.N., Silva, S.M., Filho, B.J.C., "PLL Structures for Utility Connected Systems", *IEEE Industry Application Annual Meeting Records,* Vol. 4, 2001, pp. 2655-2660.

[5] Silva, S.A.O., Donoso-Garcia, P., Cortizo, P.C., Seixas, P.F., "A Three-Phase Line-Interactive UPS System Implementation with Series-Parallel Active Power-Line Conditioning Capabilities", *IEEE Transaction on Industry Application,* Vol. 38, No. 6, November/December 2002, pp. 1581-1590.

[6] Sasso, E.M., Sotelo, G.G., Ferreira, A.A., Watanabe, E.H., Aredes, M., Barbosa, P., "Investigação dos modelos de circuitos de sincronismo trifásicos baseados na teoria de potências real e imaginária instantâneas (p-PLL e q-PLL)", *Congresso Brasileiro de Automática*, Natal - Brazil, 2002, pp.480-485, (*in portuguese*).

[7] C. Zhan, C. Fitzer, V. K. Ramachandaramurthy, A. Arulampalam, M. Barnes, N. Jenkins, "Software Phase-Locked Loop applied to Dynamic Voltage Restorer (DVR)", *IEEE Power Engineering Society Winter Meeting*, Vol.03, 2001, pp. 1033-1038.

[8] D.R. Costa, L. G.B. Rolim, M. Aredes, "Analysis and Software Implementation of a Robust Synchronizing Circuit – PLL Circuit, *IEEE International Symp. of Industrial Electronics*, Rio de Janeiro, Brazil, ISBN 0-7803-7913-6, 2003.

[9] Leonhard, W., *Control of Electrical Drives*, Springer-Verlag, Berlim, Germany, 1990.

[10] T. Furuhashi, S. Okuma, Y. Uchikawa, "A Study on the Theory of Instantaneous Reactive Power", *IEEE Trans.on Industrial Electronics,* Vol. 37, No. 1, Feb. 1990, pp. 86-90.

[11] F.P. Marafão, "Contributions to the Instantaneous Power Theory and its Applications in Power Quality", MSc. Dissertation, Campinas, Brazil, March 2000, (*in Portuguese*).