A NOVEL SINGLE-PHASE HIGH POWER-FACTOR INTERLEAVED BOOST ZCS RECTIFIER

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Abstract— **This paper presents a new single-phase high power factor interleaved boost rectifier operating in critical conduction mode, where the switches and boost diode performing zero-current commutations during its turn-off, eliminating the disadvantages related to the reverse recovery losses and electromagnetic interference problems of the boost diode, when operating in the continuous conduction mode. The interleaving technique is applied in the power cell, providing a significant input current ripple reduction in comparison to discontinuous mode of operation, due to its input current continuous conduction operation. This paper presents a complete modeling for the converter operating in critical conduction mode, resulting in an improved design procedure for interleaved techniques with high input power factor, a complete design procedure, and main simulation from a designed prototype with two interleaved cells rated at 1kW, 400V output voltage and 220V rms input voltage.**

KEYWORDS

Interleaved techniques, active power factor correction, boost zcs-fm, critical conduction mode.

I. INTRODUCTION

In recent years, due to the power factor correction requirement, the single-ended boost converter has been widely used as the front-end single-phase PFC converter due to its step-up voltage conversion ratio, continuous input current, simple topology, and high efficiency [1].

However, a couple of things are still of concern. For high power applications, the boost inductor will become one of the major factors affecting the system cost, volume, and weight. For high voltage applications, high voltage devices have to be used, which produces high conduction losses and high switching losses. When voltage is higher than a certain level, some types of devices are even not available. Therefore, it is very desirable to use smaller inductor and lower voltage devices [2].

Due to the high output voltage, the boost converter requires the use of a diode, which allows fast recovery and supports high voltage. At high switching frequencies, fast recovery rectifiers produce significant reverse recovery related losses when switched under "hard" switching conditions. These losses can be significantly reduced providing high efficiency even at high frequencies by employing soft switching technique, as such ZCS (Zero Current Switching) or ZVS (Zero Voltage Switching) [3,4].

Another method of achieving high efficiency in boost converters is operating the boost converter at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In this operation mode the switching frequency is variable, and the reverse recovery related losses are then eliminated, because there is no stored charge in the boost diode at switch turn on [4-5].

However, boundary operation requires additional input current filtering and produces peak currents that are at least two times the input current averaged over the switching cycle. This is generally undesirable for high power and power- factor correction applications.

In another way, the drawbacks of the boundary operating boost converter can be alleviated if two or more converters are interleaved. Interleaving reduces the input-ripple current and peak input current while retaining the benefits of soft switching in boost diode and switch. Nevertheless, the interleaving of variable frequency power- factor correction boost converters requires a relatively complex control circuit [1-8].

In dc to dc and/or ac to dc converters with boost topology, the employment of interleaved techniques becomes especially appropriate, minimizing the need of voluminous input filter, due to the elimination of the pulsating nature of the input current, present in single structures, when operating in critical conduction mode. In this way, the levels of EMI can be drastically reduced.

II. PRE REGULATOR AC TO DC BOOST ZCS-FM INTERLEAVED WITH TWO CELLS

Interleaved power conversion refers to the strategic interconnection of multiple switching cells for which the conversion frequency is identical, but for which the internal switching instants are sequentially phased over equal fractions of a switching period. This arrangement lowers the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses. An interleaved system can therefore realize a savings in filtration and energy storage requirements, resulting in greatly improved power conversion densities without sacrificing efficiency [6].

Therefore, the main advantage of interleaving is that it effectively increases the switching frequency without increasing the switching losses.

In this context, Fig. 1 shows a novel pre-regulator boost ZCS interleaved with two cells that can reduce the switching losses, including the diode reverse recovery losses, yields higher efficiency, high power density, and lower cost. It should be noticed that this paper provides a detailed and complete modeling for the proposed converter that facilitate the analysis for a generic N interleaved cells and its dynamic performance, providing conditions to reduce the control circuit complexity and assembly costs, through the use of the EPLD – Eprom Programmable Logic Devices.

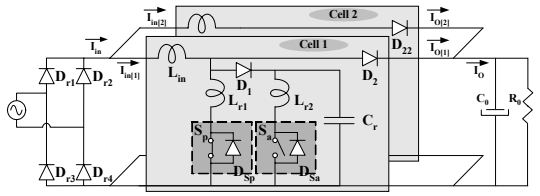

Fig.1 Pre-regulator AC/DC Boost ZCS-FM Interleaved with two cells.

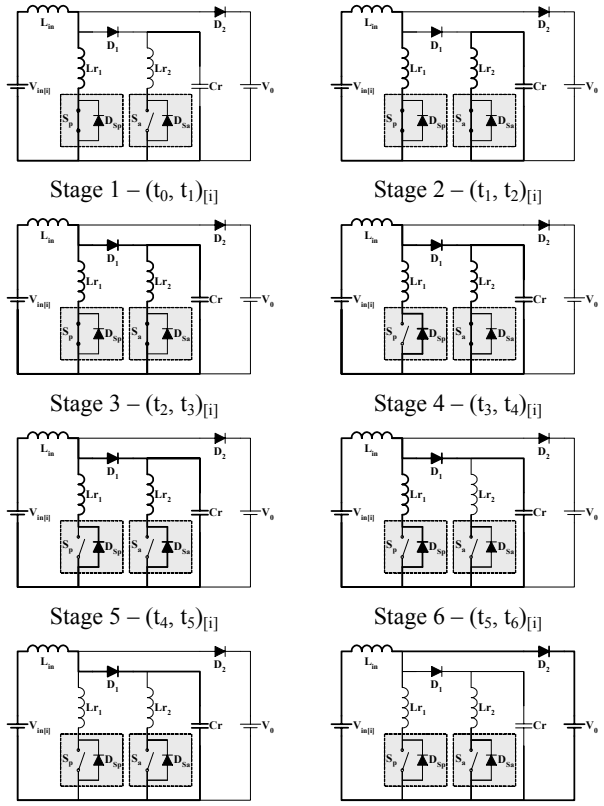

Fig.2 Topological stages for a generic cell of pre-regulator boost zcs in the critical conduction mode, during a generic switching period$_{[i]}$.

A – Principle of Operation

The analysis of this new structure is developed assuming the following simplifying conditions:

all components are ideal;

the output voltage (V_o) is constant.

the variable switching frequency ($f_{s[i]}$) is much higher than the ac line frequency (f_{line}), so the sinusoidal input voltage can be considered practically constant ($V_{in[i]}$) during one generic switching period ($T_{[i]}$);

Therefore, in steady state, during a generic switching period, the circuit of one generic cell goes through eight stages shown in Fig. 2, while the main ideal waveforms are shown in Figs. 3 and 4.

First Stage (t_0, t_1)$_{[i]}$ – This operation stage begins at t=$t_{0[i]}$, when the main switch S_p turns on under zero current (ZCS). The current through boost inductor (L_{in}), leaves of your null value and rises linearly as a function of input voltage and L_{r1} resonant inductance.

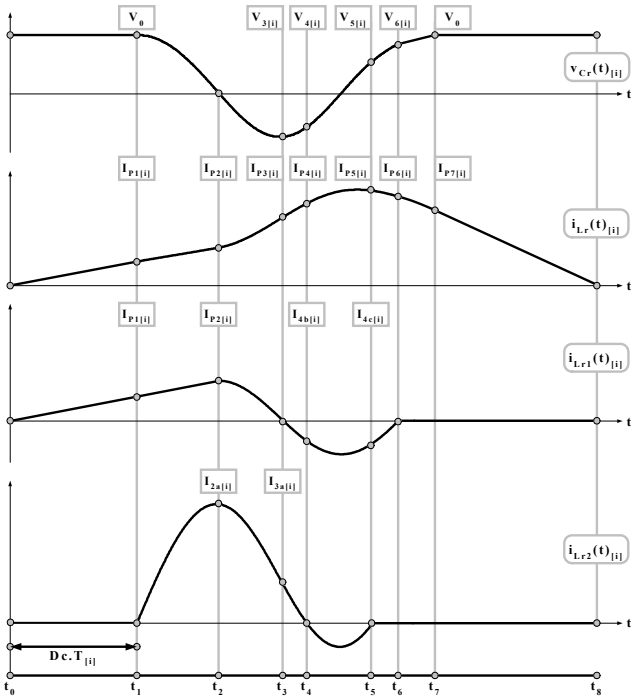

Fig.3 Main ideal waveforms for a generic cell of pre-regulator boost zcs in the critical conduction mode, during a generic switching period$_{[i]}$.

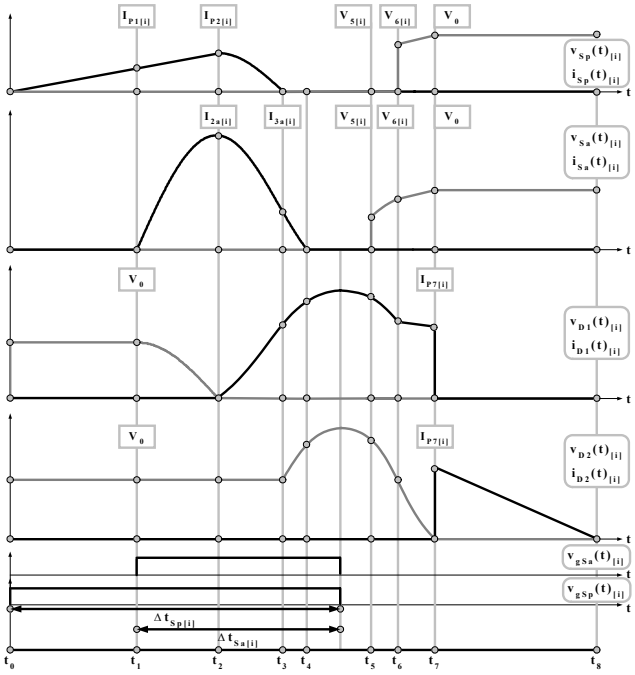

Fig.4 Stresses waveforms in semiconductors for a generic cell of pre-regulator boost zcs in the critical conduction mode, during a generic switching period$_{[i]}$.

While the resonant capacitor voltage $v_{Cr}(t)_{[i]}$ keeps clamped in V_0. The main state variables are given as follows:

$$i_{Lin}(t)_{[i]} = i_{Lr1}(t)_{[i]} = \frac{V_{in[i]}}{L_{in} + L_{r1}} \cdot t \quad (1)$$

$$V_{Cr}(t)_{[i]} = V_0 \quad (2)$$

The time interval of this operating stage is determined by (3).

$$\Delta t_{1[i]} = D_c \cdot T_{[i]} \quad (3)$$

Where :

$$T_{[i]} = \frac{1}{f_{s[i]}}$$

D_c : constant auxiliary critical duty cycle;
$T_{[i]}$: generic switching period;
$f_{s[i]}$: generic switching frequency.

Second Stage $(t_1, t_2)_{[i]}$ – At the instant $t=t_{1[i]}$ the auxiliary switch S_a is turned on under zero current (ZCS).

The current through L_{in} and L_{r1} remains rising in a linear rate. This stage finishes at $t=t_{2[i]}$, when the voltage $v_{Cr}(t)_{[i]}$ reaches zero, providing zero-voltage turn on (ZVS) process for the diode D_1. The state variables are given by (4), (5) and (6).

$$i_{Lin}(t)_{[i]} = i_{Lr1}(t)_{[i]} = I_{P1[i]} + \frac{V_{in[i]}}{L_{in} + L_{r1}} \cdot t \tag{4}$$

$$i_{Lr2}(t)_{[i]} = \sqrt{\frac{C_r}{L_{r2}}} \cdot V_O \cdot \sin(\omega_{O2} \cdot t) \tag{5}$$

$$v_{Cr}(t)_{[i]} = V_O \cdot \cos(\omega_{O2} \cdot t) \tag{6}$$

The time interval of this stage can be expresses by (7).

$$\Delta t_{2[i]} = \frac{1}{\omega_{O2}} \cdot \frac{\pi}{2} \tag{7}$$

Where :

$$\omega_{O2} = \frac{1}{\sqrt{L_{r2} \cdot C_r}} \tag{8}$$

Third Stage $(t_2, t_3)_{[i]}$ - When D_1 is turned on at $t=t_{2[i]}$ there is a link among two circuits which were working apart in the previous stage, then a new resonance angular frequency ω_{03}, expressed by (9), determine the evolution of this stage.

$$\omega_{O3} = \sqrt{\frac{L_{in} \cdot (L_{r1} + L_{r2}) + L_{r1} \cdot L_{r2}}{L_{in} \cdot L_{r1} \cdot L_{r2} \cdot C_r}} \tag{9}$$

The currents $i_{Lr1}(t)_{[i]}$ and $i_{Lr2}(t)_{[i]}$ decrease in a resonant way until the current $i_{Lr1}(t)_{[i]}$ reaches zero at $t=t_{3[i]}$. The main state variables are given as follows:

$$\begin{aligned} i_{Lin}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in}} \cdot \frac{\sin(\omega_{03} \cdot t)}{\omega_{03}} + I_{P2[i]} \cdot \cos(\omega_{03} \cdot t) \\ &+ \frac{V_{in[i]}}{L_{in} \cdot C_r} \left(\frac{L_{r1} \cdot L_{r2}}{L_{r1} + L_{r2}} \right) \cdot \left(\frac{t}{\omega_{03}^2} - \frac{\sin(\omega_{03} \cdot t)}{\omega_{03}^3} \right) \\ &+ \frac{(1 - \cos(\omega_{03} \cdot t))}{\omega_{03}^2} \cdot \left(\frac{I_{P2[i]}}{C_r} \cdot \left(\frac{L_{r1} \cdot L_{r2}}{L_{r1} + L_{r2}} \right) + \frac{(I_{P2[i]} + I_{2a[i]})}{L_{in} \cdot C_r} \right) \end{aligned} \tag{10}$$

$$\begin{aligned} i_{Lr1}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in} \cdot L_{r1} \cdot C_r} \cdot \left(\frac{t}{\omega_{03}^2} - \frac{\sin(\omega_{03} \cdot t)}{\omega_{03}^3} \right) \\ &+ \frac{(1 - \cos(\omega_{03} \cdot t))}{\omega_{03}^2} \cdot \left(\frac{I_{P2[i]}}{C_r} \cdot \left(\frac{1}{L_{in}} + \frac{1}{L_{r2}} \right) + \frac{(I_{P2[i]} - I_{2a[i]})}{L_{r1} \cdot C_r} \right) \\ &+ I_{P2[i]} \cdot \cos(\omega_{03} \cdot t) \end{aligned} \tag{11}$$

$$\begin{aligned} i_{Lr2}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in} \cdot L_{r2} \cdot C_r} \cdot \left(\frac{t}{\omega_{03}^2} - \frac{\sin(\omega_{03} \cdot t)}{\omega_{03}^3} \right) \\ &+ \frac{(1 - \cos(\omega_{03} \cdot t))}{\omega_{03}^2} \cdot \left(\frac{I_{P2[i]}}{C_r} \cdot \left(\frac{1}{L_{in}} + \frac{1}{L_{r1}} \right) \right) \\ &+ I_{2a[i]} \cdot \cos(\omega_{03} \cdot t) \end{aligned} \tag{12}$$

$$\begin{aligned} v_{Cr}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in} \cdot C_r} \cdot \left(\frac{1}{\omega_{03}^2} - \frac{\cos(\omega_{03} \cdot t)}{\omega_{03}^2} \right) \\ &+ \frac{(\sin(\omega_{03} \cdot t))}{\omega_{03}} \cdot \left(\frac{I_{P2[i]}}{C_r} \cdot \left(\frac{L_{r1}}{L_{in}} + \frac{L_{r1}}{L_{r2}} \right) + \frac{(I_{P2[i]} - I_{2a[i]})}{C_r} \right) \\ &- I_{P2[i]} \cdot L_{r1} \cdot \omega_{O3} \cdot \sin(\omega_{03} \cdot t) \end{aligned} \tag{13}$$

The time interval of this stage cannot be expressed by one generic expression because involves a solution of a non linear equation with many parameters. To solve these problems was employed the well known method of Newton-Rhapson.

Fourth Stage $(t_3, t_4)_{[i]}$ – This stage begins when D_{Sp} (intrinsic and antiparallel diode of S_p) turns on. This stage finishes at $t=t_{4[i]}$, when $i_{Lr2}(t)_{[i]}$ arrives to zero, providing that diode D_{Sa} (intrinsic and antiparallel diode of S_a) turns on.

The equations that govern the state variables of this stage are the same of the previous stage, and the time interval of this stage is obtained through a non linear solve method.

Fifth Stage $(t_4, t_5)_{[i]}$ – This stage begins when D_{Sa} turns on. Such as the two previous stages the main state variables are governed by the same equations and resonance angular frequency ω_{03}.

In this time interval, S_p and S_a are turned off, simultaneously, in zero-current and zero-voltage (ZCZV).

The end of this stage occurs when the current through $i_{Lr2}(t)_{[i]}$ reaches zero again, providing that D_{Sa} turns off under ZCS.

Sixth Stage $(t_5, t_6)_{[i]}$ - This stage begins when D_{Sa} turns off under ZCS, removing circuit part of the commutation cell regarding auxiliary switch S_a and resonant inductor L_{r2}.

The current $i_{Lin}(t)_{[i]}$ and the voltage $v_{Cr}(t)_{[i]}$ evolve in a resonant way, determined by the following equations:

$$i_{Lr2}(t)_{[i]} = 0 \tag{14}$$

$$\begin{aligned} i_{Lin}(t)_{[i]} &= \frac{(V_{in[i]} - V_{5[i]})}{L_{in}} \cdot \frac{\sin(\omega_{06} \cdot t)}{\omega_{06}} \\ &+ I_{P5[i]} \cdot \cos(\omega_{06} \cdot t) + \frac{V_{in[i]}}{L_{in} \cdot L_{r1} \cdot C_r} \cdot \left(\frac{t}{\omega_{06}^2} - \frac{\sin(\omega_{06} \cdot t)}{\omega_{06}^3} \right) \\ &+ \frac{(1 - \cos(\omega_{06} \cdot t))}{\omega_{06}^2} \cdot \left(\frac{I_{P5[i]}}{C_r \cdot L_{r1}} + \frac{(I_{5b[i]})}{L_{in} \cdot C_r} \right) \end{aligned} \tag{15}$$

$$\begin{aligned} i_{Lr1}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in} \cdot L_{r1} \cdot C_r} \cdot \left(\frac{t}{\omega_{06}^2} - \frac{\sin(\omega_{06} \cdot t)}{\omega_{06}^3} \right) + I_{P5[i]} \cdot \cos(\omega_{03} \cdot t) \\ &+ \frac{V_{5[i]}}{L_{r1}} \cdot \frac{\sin(\omega_{06} \cdot t)}{\omega_{06}} + \frac{(1 - \cos(\omega_{06} \cdot t))}{\omega_{06}^2} \cdot \left(\frac{I_{P5[i]}}{L_{r1} \cdot C_r} + \frac{I_{5b[i]}}{L_{in} \cdot C_r} \right) \end{aligned} \tag{16}$$

$$\begin{aligned} v_{Cr}(t)_{[i]} &= \frac{V_{in[i]}}{L_{in} \cdot C_r} \cdot \left(\frac{1}{\omega_{06}^2} - \frac{\cos(\omega_{06} \cdot t)}{\omega_{06}^2} \right) \\ &+ \frac{\sin(\omega_{06} \cdot t)}{\omega_{06}} \cdot \left(\frac{I_{P5[i]}}{C_r} + \frac{L_{r1}}{L_{in} \cdot C_r} \cdot I_{5b[i]} \right) \\ &- I_{P5[i]} \cdot L_{r1} \cdot \omega_{06} \cdot \sin(\omega_{06} \cdot t) + V_{5[i]} \cdot \cos(\omega_{06} \cdot t) \end{aligned} \tag{17}$$

Where:

$$\omega_{06} = \sqrt{\frac{L_{in} + L_{r1}}{L_{in} \cdot L_{r1} \cdot C_r}} \tag{18}$$

Seventh Stage (t_6, t_7)$_{[i]}$ – This stage begins when D_{Sp} turns off under ZCS. The state variables are given as follows:

$$i_{Lin}(t)_{[i]} = \frac{\left(V_{in[i]} - V_{6[i]}\right)}{L_{in}} \cdot \frac{\sin\left(\omega_{07} \cdot t\right)}{\omega_{07}} + I_{P6[i]} \cdot \cos\left(\omega_{07} \cdot t\right) \quad (19)$$

$$v_{Cr}(t)_{[i]} = V_{in[i]} - \left(V_{in[i]} - V_{6[i]}\right) \cdot \cos\left(\omega_{07} \cdot t\right) + \sqrt{\frac{L_{in}}{C_r}} \cdot I_{P6[i]} \cdot \sin\left(\omega_{07} \cdot t\right) \quad (20)$$

Where:

$$\omega_{07} = \frac{1}{\sqrt{L_{in} \cdot C_r}} \quad (21)$$

When the voltage $v_{Cr}(t)_{[i]}$ reaches the output voltage value, provides that D_2 turns on under ZVS and D_1 turns off under ZVS.

The time interval of this stage is equal to:

$$\Delta t_{7[i]} = \frac{1}{\omega_{07}} \cdot \operatorname{asin}\left(\frac{K_{1[i]} \cdot K_{2[i]} - \sqrt{K_{2[i]}^{\,2} + 1 - K_{1[i]}^{\,2}}}{K_{2[i]}^{\,2} + 1} \right) \quad (22)$$

Where: $K_{1[i]} = \frac{V_O - V_{in[i]}}{V_{in[i]} - V_{6[i]}}$; $K_{2[i]} = \sqrt{\frac{L_{in}}{C_r}} \cdot \frac{I_{P6[i]}}{V_{in[i]} - V_{6[i]}}$;

Eighty Stage (t_7, t_8)$_{[i]}$ – This stage begins when D_2 turns on under ZVS, accomplishing the link among energy charge element with the load, represented by voltage source V_0, transferring energy to the load.

The current $i_{Lin}(t)_{[i]}$ decreases in a linear way, while the voltage $v_{Cr}(t)_{[i]}$ is clamped in V_0.

$$i_{Lin}(t)_{[i]} = I_{P7[i]} - \frac{\left(V_O - V_{in[i]}\right)}{L_{in}} \cdot t \quad (23)$$

The end of this stage occurs at $t=t_{8[i]}$, when $i_{Lin}(t)_{[i]}$ arrives to zero, providing that D_2 turns off under ZCS.

The time interval of this stage can be expressed by equation (24).

$$\Delta t_{8[i]} = \frac{I_{P7[i]} \cdot V_{in[i]}}{V_O - V_{in[i]}} \quad (24)$$

B – Analysis of Commutation

In order to achieve soft-commutation at zero current for both active switches (S_p and S_a) as described before, some constraints must be satisfied:

(a) $\beta_1<1$ and $\alpha_{max}<\beta_2+1$ to guarantee that the current through L_{r1} will reaches zero before the current through L_{r2};

(b) Additionally, to guarantee that all the operational stages occur, the expression (25) must be positive.

$$\left[\left(\frac{A}{C}.\operatorname{acos}\left(\frac{1-G^2}{1+G^2}\right) - G\right) + \frac{V_0}{V_{in(rms)}}.\left[H.\left(1+\beta_2\right)\right]\right] > 0 \quad (25)$$

Where :

$$A = \sqrt{\frac{\beta_1}{\beta_2 \cdot (\beta_1 + 1) + \beta_1}}; \; G = \left(\frac{V_0}{V_{in(rms)}} \frac{1}{C \cdot A \cdot H}\right); \; C = \sqrt{\frac{\beta_2 + 1}{\beta_2}};$$

$$H = \sqrt{\frac{\beta_1}{\beta_2 + 1}}; \; \alpha_{max} = \frac{I_{O[n]}}{V_{in\,min(rms)}} \sqrt{\frac{L_{in} + L_{r1}}{C_r}}; \; \beta_1 = \frac{L_{r2}}{L_{r1}}; \; \beta_2 = \frac{L_{in}}{L_{r1}};$$

$V_{in\,min\,(rms)}$: minimum value of rms input voltage;
$V_{in(rms)}$: nominal value of rms input voltage;
$I_{O[n]}$: nominal value of load current in a generic cell "n".

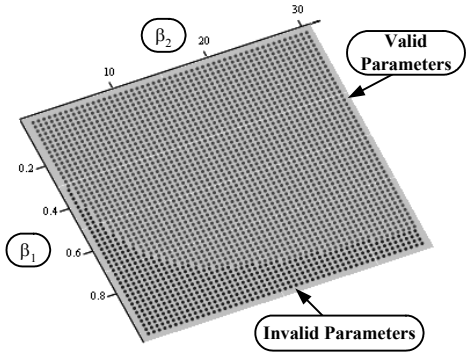

Fig.5 Results of inequality (25) as a function of β_1 and taken β_2 as a parameter, at q equal to 1.81.

Figure 5 shows the results of (25) as a function of β_1 and taken β_2 as a parameter, in order to select parameters that satisfy the constraints, for a specified value of the voltage conversion ratio. The voltage conversion ratio (q) for the rectifier is given by (26).

$$q = \frac{\sum_{n=1}^{N} I_{in[n]}}{I_0} = \frac{I_{in[n]}}{I_{0[n]}} = \frac{V_0}{V_{in(rms)}} = \frac{1 - \dfrac{F_1\left(\beta_1, \beta_2, q, f, T_{[V_{in(rms)}]}\right)}{\alpha_{rms}\left((\beta_1, \beta_2, q, f, T_{[V_{in(rms)}]})\right)}}{1 + \dfrac{F_2\left(\beta_1, \beta_2, q, f, T_{[V_{in(rms)}]}\right)}{\alpha_{rms}\left((\beta_1, \beta_2, q, f, T_{[V_{in(rms)}]})\right)}} \quad (26)$$

Where:

$$\alpha_{rms}\left((\beta_1, \beta_2, q, f, T_{[V_{in(rms)}]})\right) = \frac{I_{O[n]}}{V_{in(rms)}} \cdot \sqrt{\frac{L_{in} + L_{r1}}{C_r}} \quad (27)$$

$$f = \frac{f_{S[Vin(rms)]}}{f_0} \quad (28)$$

$$f_O = \frac{1}{2\pi . \sqrt{\left(L_{in} + L_{r1}\right) \cdot C_r}} \quad (29)$$

$f_{s[Vin(rms)]}$: value of switching frequency at $V_{in(rms)}$;
$I_{in[n]}$: nominal value of input current in a generic cell "n";
I_O : nominal value of load current;
N : number of generic cells.

Figure 6 shows the surface of normalized rms current (α_{rms}) as a function of conversion ratio (q) and the relation *f*, where β_1, β_2 and $T_{[Vin(rms)]}$ are taken as parameters of control. Additionally, Fig. 7 shows a slice of Fig. 6, showing the sectors regarding to discontinuous conduction mode and critical conduction mode. Furthermore, the sector of critical conduction operation employing the critic duty cycle parameter is shown in Fig. 7.

III. DESIGN EXAMPLE

A design procedure is presented in this section providing a closed methodology without approaches with standard boost operating in critical conduction mode that are usually employed. In this context, the input and output data are defined in Table I.

TABLE I
Input and output data

Parameter	Value	Parameter	Value
$V_{in(rms)}$	220 V	$f_{s[Vin(rms)]}$	50 kHz
V_O	400 V	Number of Cells (N)	2
P_O	1 kW	Phase-Shift [rad]	π/2

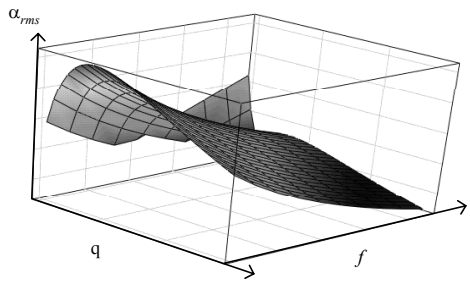

Fig.6 Surface of normalized rms current (α_{rms}) as a function of q and f, where β_1, β_2 and $T_{[Vin(rms)]}$ are taken as parameters.

A – Determination of conversion ratio

$$q = \frac{V_0}{V_{in(rms)}} = \frac{400}{220} = 1.81$$

B – Parameters Selection

From Fig. 5, the parameters adopted for design are β_2=15, β_1=0.7, and the resonant capacitor (C_r) was choose as a commercial value equal to 10nF. It should be noticed that the ratio between the parameters f and α_{rms} is not a linear function, and α_{rms} is a function of f. Figure 8 shows the behavior of this ratio taken β_1, β_2, q and $f_{s[Vin(rms)]}$ as parameters.

$$\frac{f}{\alpha_{rms}\left(\beta_1, \beta_2, q, f, f_{s[Vin(rms)]}\right)} = 0.5529; \quad f = 0.6716; \quad \alpha_{rms} = 1.2146.$$

C – Determination of critical boost and resonant inductances

$$L_{in} = \left(\frac{f}{f_{S[Vin(rms)]} \cdot 2\pi}\right)^2 \cdot \frac{\beta_2}{(1+\beta_2) \cdot Cr} = 428\mu H$$

$$L_{r1} = \frac{L_{in}}{\beta_2} = 28.5\mu H; \; L_{r2} = \beta_1 \cdot L_{r1} = 20\mu H.$$

D – Critical Duty Cycle (D_c)

The value of auxiliary critical duty cycle is obtained based an interactive numerical method, where the solution is the duty cycle that provide a generic operating cycle satisfying the design constraints of switching period and conversion ratio. Thus, $D_c = 0.337$.

E – Input Ripple

Figure 9 shows the normalized rectified input current ripple amplitude, considering the converter operating at $V_{in(rms)}$ and in critical conduction mode. The ripple waveform of a single cell was first determined from analytical equations. Sets of such waveforms, shifted in time by the appropriate amount, were then superimposed to extract the input ripple. One interesting result obtained from Fig. 9 is a demonstration that the optimal inter-cell phase angle is not necessarily (2π/N), for N greater than two.

IV. SIMULATION RESULTS

In order to validate the proposed modeling and design, a two cell pre-regulator boost ZCS FM interleaved topology has been simulated, in order to verify the validity of the proposed approach.

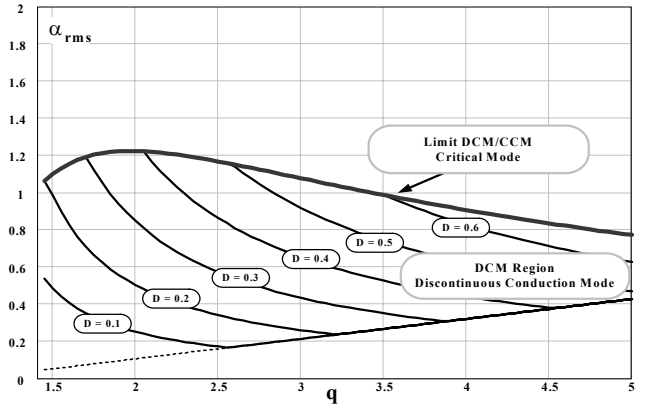

Fig.7 Normalized rms current as a function of q and f, where β_1, β_2 and $T_{[Vin(rms)]}$ are taken as parameters.

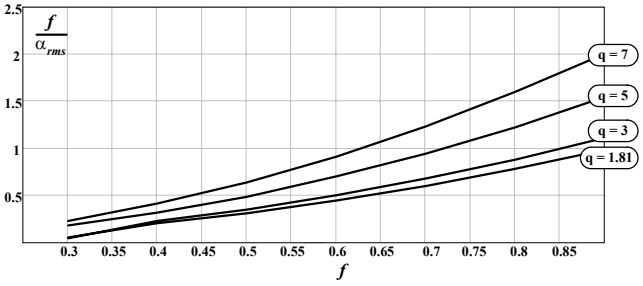

Fig.8 Function (f/α_{rms}) as a function of f, where β_1, β_2, q and $f_{s[Vin(rms)]}$ are taken as parameters.

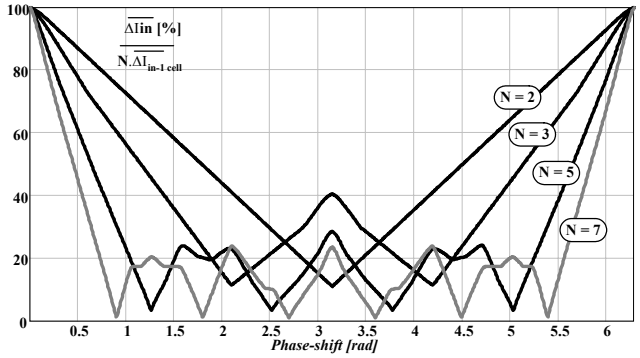

Fig.9 Normalized rectified input current ripple amplitude for the boost ZCS – FM interleaved topology, as a function of phase shift between the cells, operating at nominal rms input voltage.

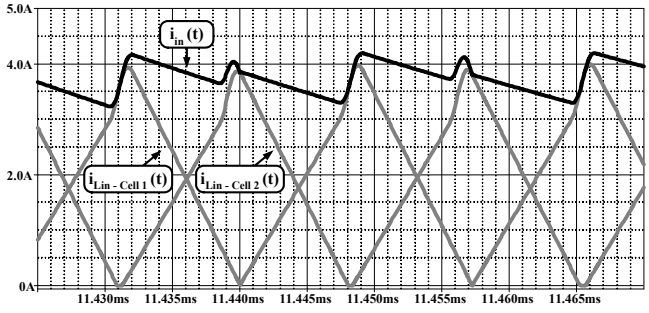

Fig. 10 Rectified input current, and the currents through the boost inductors in each cell, for some generic periods.

The converter's cells have the same parameters, and operate with master and slave control approach using the turn on gate signal of the main switch of master cell to activate an auxiliary signal that provides the phase shifting of the slave cell operation. Figure 10 shows the rectified input current and the currents through the boost inductors in each cell, demonstrating the effects of interleaved technique used.

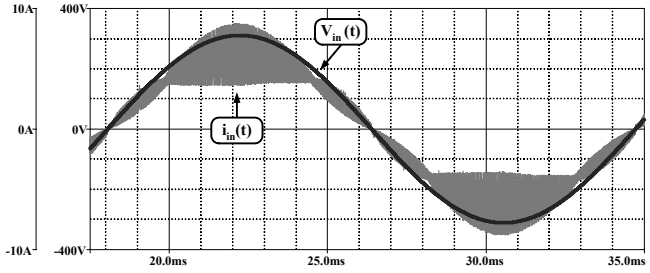

Fig.11 Input current and input voltage during one ac period, at full load.

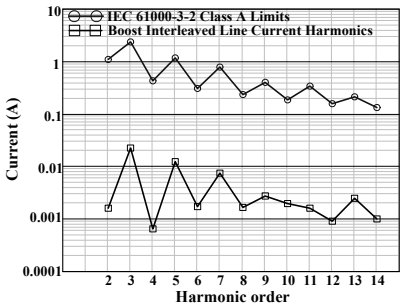

Fig.12 Harmonic current amplitudes from the proposed pre-regulator boost, and the IEC 61000-3-2 Class A Limits.

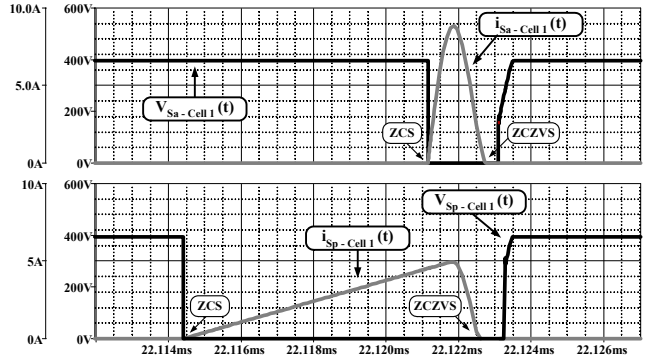

Fig.13 Commutation details, voltage and current through auxiliary switch Sa, and main switch Sp in the master cell, where V_{in} is near to its peak value.

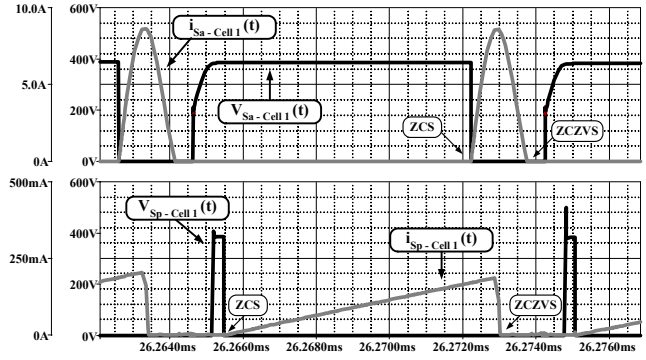

Fig.14 Commutation details, voltage and current through auxiliary switch Sa, and main switch Sp in the master cell, where V_{in} is near to zero.

Figure 11 shows the input current and input voltage during one ac line period, at full load. One can verify in Fig. 12 that the input current THD is reduced, only 0.64%, and in agreement with the limits of IEC 61000-3-2 standard. A commutation details for the voltage and current through the main and auxiliary switches are shown in Figs. 13 and 14. Both figures demonstrate that the soft-commutation are performed for all main, and auxiliary switches used, during the ac line period.

V. CONCLUSIONS

Increased requirements to utility power quality challenge the research on the ac to dc converters which are able to provide unity power factor, low input current total harmonic distortion and low electromagnetic pollution in the line.

In this paper was investigated an interleaved high input-power-factor pre-regulator boost topology operating in critical conduction mode, using a non dissipative commutation cell and frequency modulation.

The main contribution of this paper is a complete modeling and design example for the proposed converter, containing the resonance elements influence, instead of use the usually approach of standard boost design, allowing conditions to implement a close-loop control using EPLD.

For the proposed converter discussed in this paper, the inductance of the boost inductors can be significantly reduced compared with the conventional PFC boost converter. The device current rating is only a fraction of the conventional boost switch current, which is desirable for high power applications, and reduces both conduction and switching losses. Therefore, utilization of smaller inductors and low current devices yields higher efficiency, high power density, and lower cost. The interleaved boost ZCS-FM pre-regulator can further reduce the switching losses, including the diode recovery losses. It would be useful for high switching frequency operation and EMI reduction.

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REFERENCES

[1] J. Zhang, M. M. Jovanovic, F. C. Lee, "Comparison Between CCM Single-Stage PFC and Two-Stage Boost PFC Converters", in *Proceedings of the 2000 IEEE Applied Power Electronics Conference,* CD-ROM Folder.

[2] B. T. Irving, Y. Jang, M. M. Jovanovic, "A Comparative Study of Soft-Switched CCM Boost Rectifiers and Interleaved Variable-Frequency DCM Boost Rectifier", in *Proceedings of the 1999 Power Engineering Society,* CD-ROM Folder.

[3] L. Balogh and R. Redl, "Power-Factor Correction with Interleaved Boost Converters in Continuous-Inductor Current Mode", in *Proceedings of the 1993 IEEE Applied Power Electronics Conference*, pp.168-174.

[4] P. Wong and F. C. Lee, "Interleaved to Reduce Reverse Recovery Loss in Power Factor Correction Circuits", in *Proceedings of the 2000 IEEE Industry Applications Soc.,* CD-Rom Folder.

[5] T. Ishii and Yoshio Mizutani, " Power Factor Correction Using Interleaving Technique for Critical Mode Switching Converters", in *Proceedings of the 1994 IEEE Applied Power Electronics Conference*, pp.404-410.

[6] B. A. Miwa, D. M. Otten and M.F. Schlecht, "High Efficiency Power Factor Correction Using Interleaving Techniques", in *Proceedings of the 1992 IEEE Applied Power Electronics Conference*, pp. 557-568.

[7] J. Zhang, J. Shao, P. Xu, F. C. Lee and M. M. Jovanovic," Evaluation of Input Current in Critical Mode Boost PFC Converter for Distributed Power Systems", in Proceedings of the 2001 IEEE Applied Power Electronics Conference, 0-7803-6618/8/01, CD-ROM Folder.

[8] C. H. Chan and M. H. Pong, "Input Current Analysis of Interleaved Boost Converters Operating in Discontinuous-Inductor Current Mode", in *Proceedings of the 1997 IEEE Power Electronics Specialists Conference*, pp.392-398.