AUXILIARY POWER SUPPLIES TO HIGH POWER CONVERTERS WITH HIGH DC BUS VOLTAGE

Power Electronics Institute - INEP
Dept. of Electrical Engineering
Federal University of Santa Catarina - UFSC
P.O. Box 5119 - 88040-970 - Florianópolis - SC -Brazil
RICARDO L. ALVES, KEFAS D. COELHO AND IVO BARBI.

Abstract **– This work presents a new DC-DC PWM converter for high input voltage applications. The new structure is based in the classical half-bridge converter, keeping similar operation characteristics, however the maximum voltage across the switches is half the DC bus voltage. The voltage reduction in the switches allows the use of cheaper switches, beside to contribute to increase efficiency, whereas reducing losses. The converter is studied to operate as an auxiliary power supply in a high power telecommunication supply. In the study was established the operating principles, theoretical analysis, design procedure, simulation and obtained practical results. The prototype assembled was designed to provide to the output approximately 150W and operate with a DC bus voltage between 400V and 900V. The results obtained showed that this structure presents a good voltage distribution among the switches (half of the DC Bus voltage).**

KEYWORDS

DC-DC converters, high input voltage converter, auxiliary supplies.

I – INTRODUCTION

High power DC-DC converters usually present high voltage levels in DC bus in a way to intend to reduce the semiconductors current. Other factor that contributes to elevate the DC bus voltage is the power factor correction rectifier used as an input stage to compose the main power supply. The commonly topology used to achieve power factor correction is the boost rectifier, which presents an output voltage greater than the peak of the AC input voltage.

In these converters, the auxiliary power supplies are frequently connected at the DC link, thus, is submitted to high input voltages.

The Half-Bridge is a common topology used for the design of switching power supplies with isolated output. The conventional Half Bridge converter, shown in Fig.1, offers the possibility of reducing the size of the transformer by nearly 1/2 compared with the single transistor forward converter, because it uses the transformer flux in both directions. A clamp winding is not employed but the switches are rated with the DC bus voltage.

Energy transfer occurs across the isolation transformer. First, when the power transistor S1 turns on, the primary voltage is reflected across the output windings, and rectified by D3, charging the output inductor. When S1 turns off, the voltage drive across the transformer primary drops to zero, and energy stored in the leakage and magnetizing inductances causes a turn-off overshoot, which is clamped by the body diode of S2. In the third stage, S2 turns on, and the transformer is driven in the opposite direction, resetting the flux balance in the transformer core. Diode D4 is biased charging the inductor Lout.

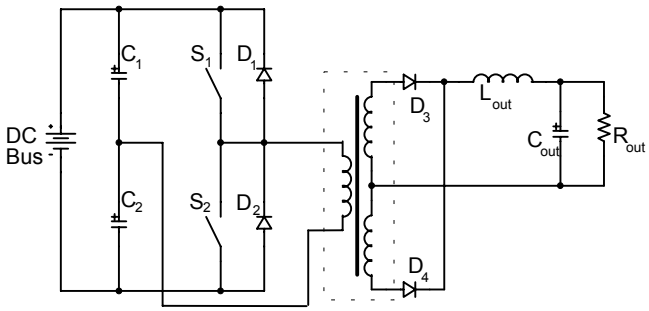

Fig. 1 - Half-Bridge Converter.

The output of the transformer is connected to a half wave rectifier, so the output frequency is twice the input frequency. The output capacitor and inductor store energy and integrate the duty cycle so that the output voltage is proportional to the product of the rectified output voltage and duty cycle as can be observed in Fig.2.

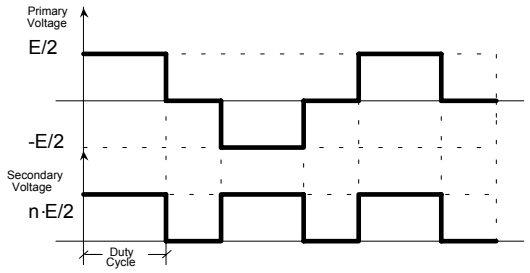

Fig.2 –Half-Bridge Transformer waveforms.

In high DC Bus voltage applications this topology is not appropriated. The high voltage switches are expensive and the switching losses are elevated. Multilevel topologies, where the switch voltage is reduced, can be used to solve this problem. Is this work a new reduced switch voltage topology, the Double Half-Bridge, is presented. This converter is used as an auxiliary power supply connected into DC bus of the PFC stage of the high power converter (27kW).

The Double Half-Bridge version is presented in Fig.3. As can be observed it's a two half-bridge with series connected secondary transformers.

The DC Bus voltage is kept constant by the PFC control loop. In this way, the power supply input voltage represents the PFC output capacitors (Cr1 and Cr2).

The advantages of double half-bridge topology are:

- ✓ Voltage rating required of power switches are half (Vcc) of the half-bridge topology (2Vcc)
- ✓ The series connection of the secondaries assures that the power will be equally divided between each DC bus capacitor.

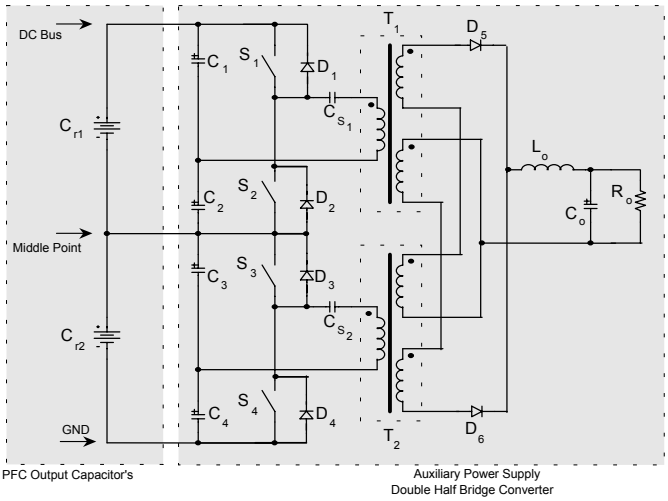

Fig. 3 – Double Half-Bridge Converter.

The disadvantages are:

- ✓ It requires more complex drive circuits for the transistors.
- ✓ Four transistors are required rather than two.

II. OPERATING STAGES

Some considerations are used to simplify the analysis:

- ✓ Steady-state operation.
- ✓ The capacitors C1, C2, C3 e C4 are ideal DC voltage sources (E/4);
- ✓ The semiconductors and the magnetic elements (transformers and inductors) are considered ideals or loss free.

Stage 1: ($t_o < t < t_1$). Switches S_1 and S_3 are turned on. The positive voltage in the secondary windings turns the diode D_5 on. The diode D_6 is reversed biased. During this subinterval power is transferred to the output. The voltages into the switches S_1 e S_3 are zero, and into the switches S_2 e S_4 are equal to E/2.

Stage 2: (t1 < t < t2) Switches S1 and S3 are turned off. During this subinterval the four switches are open. The diodes D5 and D6 conduct the inductor current. The voltage on both secondary windings is zero. The voltages on the switches S1, S2, S3 and S4 are equal to E/4.

Stage 3: (t2 < t < t3) Switches S2 and S4 are turned on. The positive voltage in the secondary windings turns the diode D6 on. The diode D5 is reversed biased. During this subinterval power is transferred to the output. The voltages in the switches S1, S2, S3 and S4 are equal to E/4.

Stage 4: (t3 < t < t4) Switches S2 and S4 are turned off. This stage is identical to second stage.

Relevant waveforms are presented in **Fig.5** and **Fig. 6**.

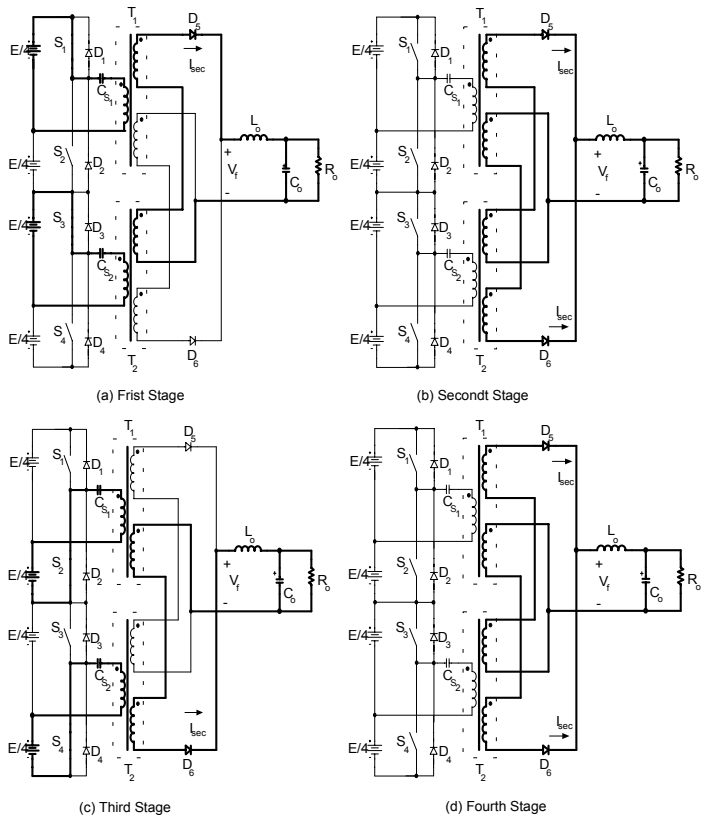

Fig. 4 – Operating Stages

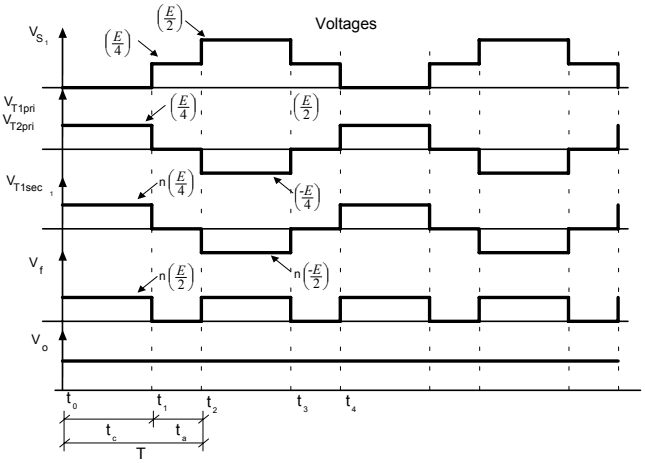

Fig. 5 – Voltages Waveforms

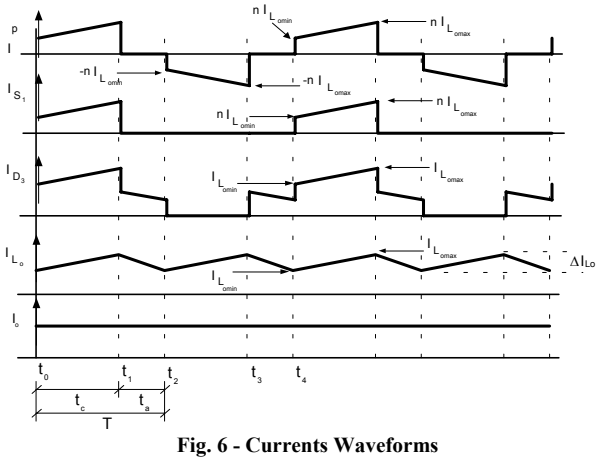

Fig. 6 - Currents Waveforms

In the operation stages presented, the DC bus voltage is provided by a middle point. In applications without this characteristic, the voltage balance among the capacitors C_1, C_2, C_3 e C_4 (Fig 1.1) is guaranteed by a equilibrium capacitor, C_A, connected as showed below:

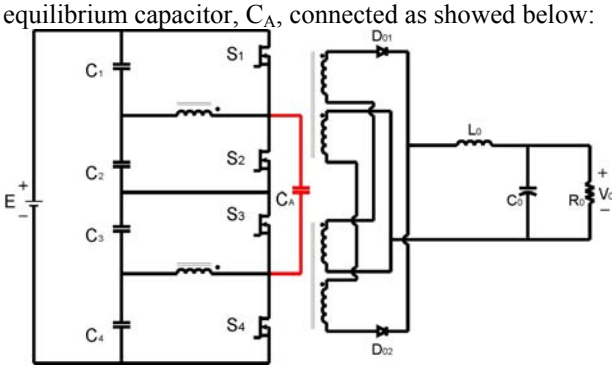

Fig. 7 – Voltage Balance Capacitor

THEORETICAL ANALYSIS:

The mathematical analysis are based in these suppositions:

- ✓ Continuous mode and Steady state operation.
- ✓ Circuit elements are ideals.

Average Output voltage.

The average inductor voltage must be zero. In this way, the average load voltage is equal to the average V_f voltage.

$$V_o = V_{f_{med}} = \frac{1}{T}\cdot\int_0^T v_f(t)\cdot d(t) \qquad (1.1)$$

It results:

$$V_o = \frac{1}{T}\cdot\left(\int_0^{t_c} n\cdot\frac{E}{2}\cdot d(t) + \int_{t_c}^{T} 0\cdot d(t)\right) \qquad (1.2)$$

$$V_o = \frac{1}{2}\cdot\frac{t_c}{T}\cdot n\cdot E \qquad (1.3)$$

Defining:

$$D = \frac{t_c}{T} \qquad (1.4)$$

Were:
$T = V_f$. Wave form period;
$T_s = 2T$ = Switching Period
$f_s = 1/T_s$ = Switching frequency.
t_c = Switch conduction time.
n = transformer turns ratio.
The expression (1.3) can be writing as:

$$V_o = \frac{1}{2}\cdot D\cdot n\cdot E \qquad (1.5)$$

It must be observed that the transformer influences the output voltage.

Average Load Current.

The average load current can be easily obtained by (1.6):

$$I_o = \frac{V_o}{R_o} = \frac{1}{2}\cdot\frac{n\cdot D\cdot E}{R_o} \qquad (1.6)$$

Static Transfer Function:

The Static transfer function (G) can be defined as the ratio between input and output voltages.

$$G = \frac{V_o}{E} = \frac{1}{2}\cdot n\cdot D \qquad (1.7)$$

Inductor current Ripple:

The expression (1.8) defines the current ripple in the filter inductor:

$$\Delta I_{Lo_{\max}} = \frac{n\cdot E}{8\cdot L_o\cdot f} \qquad (1.8)$$

Load Voltage Ripple:

The load voltage ripple is the same of the output filtering capacitor.
To obtain this value the worst case will be considered (duty cycle 50%). In this situation the relevant waveforms (inductor and capacitor currents and voltages) are plotted in Fig.6.

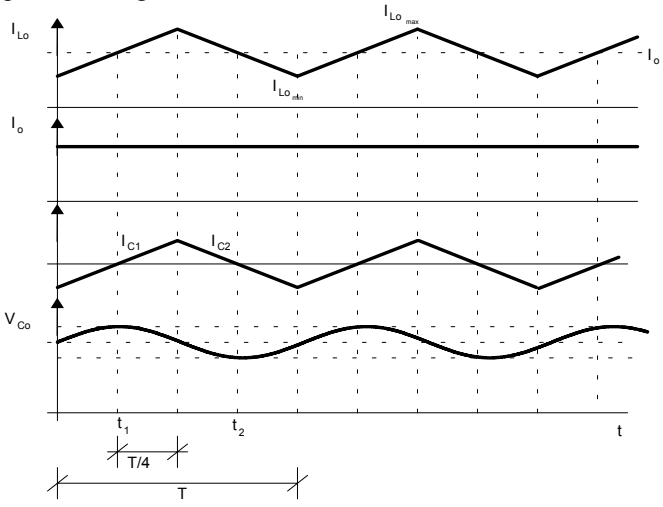

Fig.6 – Relevant waveforms to obtain the output voltage ripple.

From Fig.6, (1.9) is written:

$$\Delta V_o = \frac{n\cdot E}{256\cdot f^2\cdot L_o\cdot C_o} \qquad (1.9)$$

Solving for C_o (10) can be found:

$$C_o = \frac{n\cdot E}{256\cdot f^2\cdot L_o\cdot \Delta V_o} \qquad (1.10)$$

Maximum Switches Voltage:

Observing Fig.5 the maximum switches voltages are obtained:

$$V_{S1\max} = V_{S2\max} = V_{S3\max} = V_{S4\max} = \frac{E}{2} \quad (1.11)$$

Switches Current Peak.

The switches current may be obtained referring the filter inductor current (I_{Lo}) to the primary side of the transformer:

$$I_{S\max} = I_{pri\max} = n \cdot I_{Lo_{\max}} \quad (1.12)$$

Equation (1.12) can be rewritten as:

$$I_{S\max} = n \cdot \left(I_o + \frac{V_o}{2 \cdot f \cdot L_o} \cdot (1 - D) \right) \quad (1.13)$$

In multiple output cases the equation (14) must be used:

$$I_{S\max} = \sum n_k \cdot \left(I_o + \frac{V_{ok}}{2 \cdot f \cdot L_{ok}} \cdot (1 - D) \right) \quad (1.14)$$

Average Switch current:

The average switches current are obtained from expression (1.15):

$$I_{S_{AVG}} = \frac{1}{T_s} \cdot \int_0^{T_s} i_s(t) \cdot dt \quad (1.15)$$

This results:

$$I_{S_{AVG}} = \frac{n}{2} \cdot \left[I_{Lo\min} \cdot D + \left(\frac{(n \cdot E/2) - V_o}{2 \cdot L_o \cdot f} \right) \cdot D^2 \right] \quad (1.16)$$

It can be reduced to:

$$I_{S_{AVG}} = \frac{n \cdot D}{2} \cdot I_o \quad (1.17)$$

To multiple outputs:

$$I_{S_{AVG\max}} = \frac{1}{2} \cdot \sum n_k \cdot D \cdot I_{ok} \quad (1.18)$$

Rms Switch current:

The RMS switches current can be obtained from expression (19):

$$I_{Srms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s} \left(i_s(t) \right)^2 \cdot dt} \quad (1.19)$$

$$I_{Srms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{t_c} \left(n \cdot \left(\left(\frac{\Delta I_{Lo}}{D \cdot T} \right) \cdot t + I_o - \frac{\Delta I_{Lo}}{2} \right) \right)^2 \cdot dt} \quad (1.20)$$

$$I_{Srms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{t_c} \left(n \cdot \left(\left(\frac{\Delta I_{Lo}}{D \cdot T} \right) \cdot t + I_o - \frac{\Delta I_{Lo}}{2} \right) \right)^2 \cdot dt} \quad (1.21)$$

Considering $\Delta I_{Lo} \to 0$:

$$I_{Srms} = n \cdot I_o \cdot \sqrt{\frac{D}{2}} \quad (1.22)$$

To D = 1 the rms current have the maximum value:

$$I_{Srms\max} = \frac{n \cdot I_o}{\sqrt{2}} \quad (1.23)$$

To multiple output:

$$I_{Srms} = \sum n_k \cdot I_{ok} \cdot \sqrt{\frac{D}{2}} \quad (1.24)$$

EXPERIMENTAL RESULTS:

Converter Specifications:

The converter specifications are:

- ✓ Operating Voltage: 380VDC – 900VDC.
- ✓ 9 Isolated Outputs:
- ✓ Switching frequency: 70kHz
- ✓ Efficiency: 70%.

Table 1 – Output Specifications.

Output	*Voltage*	*Current*	*Peak current*	*Ripple voltage*
1	24V	650mA	2.5 A	200mV
2	24V	650mA	2.5 A	200mV
3	24V	650mA	2.5 A	200mV
4	24V	650mA	2.5 A	200mV
5	24V	650mA	2.5 A	200mV
6	24V	650mA	2.5 A	200mV
7	24V	300mA	0.3 A	200mV
8	24V	150mA	0.65 A	150mV
9	24V	650mA	0.65 A	150mV
10*	24V	150mA	0.25 A	100mV

* output #10 is a control output (cross regulation)

The transformers are constructed using two E43007-EC cores (Magnetics.inc) and the experimental results were obtained at 900V DC Bus.

In Fig 8 it can be observed the gate voltage and drain-source voltage in switch S4

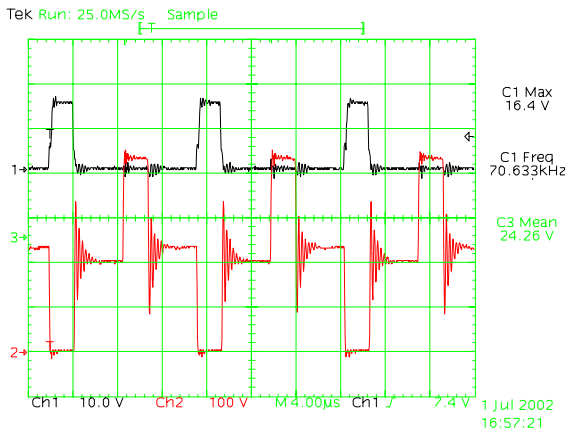

Fig. 8 Gate driver and Drain to Source voltage of switch S4.

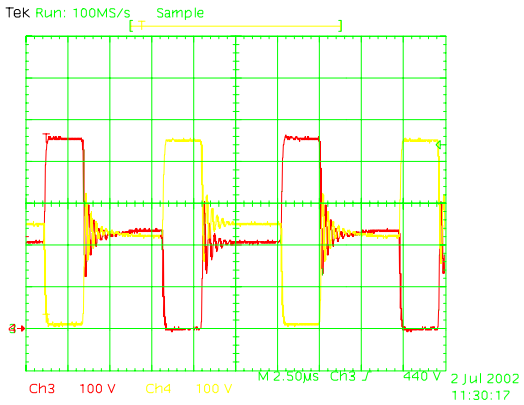

Fig. 9 - S1 and S2 Drain to Source voltages

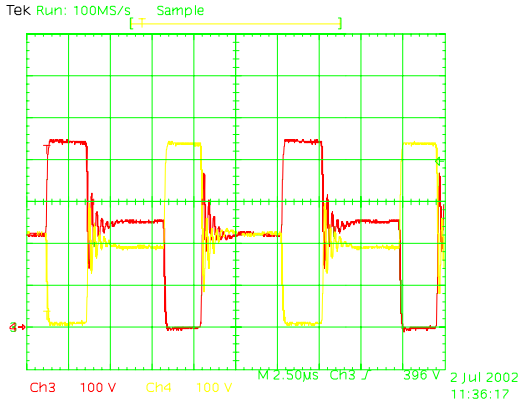

Fig. 10 - S3 and S4 V_{DS} voltages.

The DC bus voltage is presented in Fig.11 where can be observed the 450V in each DC bus capacitor.

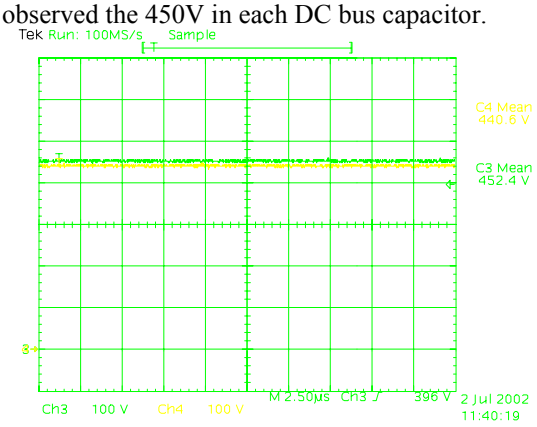

Fig. 11 - DC Bus Voltage.

The double half-bridge output voltages are presented in Fig.12.

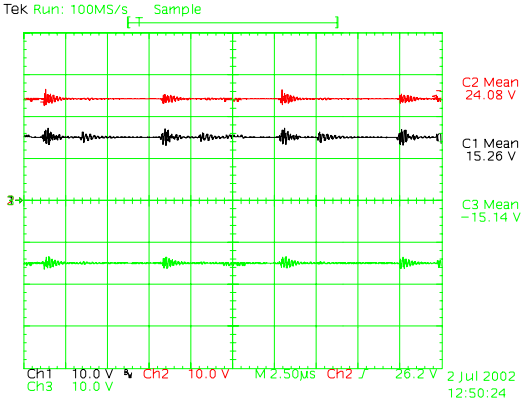

Fig. 12 — Output voltages.

The double half-bridge power supply is presented in Fig. 13:

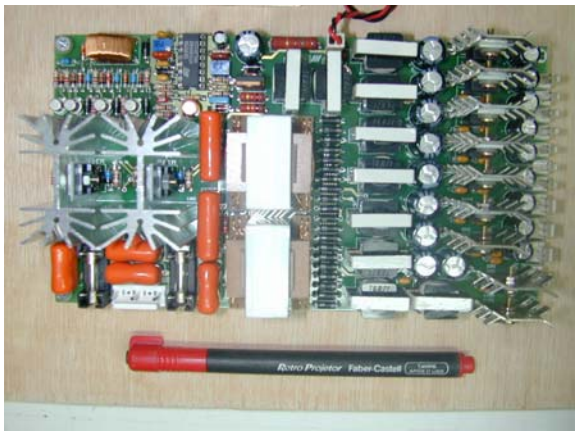

Fig. 13 - Converter Picture.

CONCLUSIONS

A complete analysis of the double Half-Bridge converter was performed. Advantages and disadvantages of Double Half-Bridge versus the conventional version were analysed.
A prototype was tested in rated power and the voltage balance among the switches was obtained.
The structure was concerned to operate with a high input voltage variation (350V-900V) and the results obtained was considered excellent for all voltage variation.

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