ANALYSIS AND DESIGN OF POWER FACTOR PRE-REGULATOR BASED ON A SYMMETRICAL CHARGE PUMP CIRCUIT APPLIED TO ELECTRONIC BALLAST

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***Abstract* - This paper presents the analysis and design of a power factor pre-regulator based on a symmetrical charge pump circuit applied to electronic ballast. The operation stages of the circuit are analyzed and its main design equations are obtained. Simulation and experimental results are presented in order to show the design methodology feasibility.**

KEYWORDS

Power Factor Pre-regulator, Symmetrical Charge Pump, Electronic Ballast.

I. INTRODUCTION

Several circuits can operate as power factor pre-regulator, the most used are based on the DC-DC converters, having these circuits two energy processing stages, which implies that this double conversion of energy increases the losses.

Another family of power factor pre-regulators, are the charge pump circuits which, unlike the former, together with the electronic ballast forms an only stage of energy processing. The high power factor is obtained through the injection of a current or voltage in high frequency.

Reference [1] details the study and design of the first charge pump circuit proposed by Kheraluwala and others.

This principle was applied for power factor correction of electronic ballast for the first time in [2], with the difference that the resonant network of the charge pump circuit is replaced by an inductor, as shown Fig. 1.

Later, new studies were presented, in [3] and [4] were generated three different topologies: the voltage source charge pump (VS-CP-PFC), the current source charge pump (CS-CP-PFC) and a hybrid third type. In Fig. 2 are shown these circuits integrated to electronic ballast.

This paper presents the study of the symmetrical charge pump circuit (Fig. 3) with the purpose of determining the design equations for the charge pump components (L_r, C_{r1} and C_{r2}), to integrate it to electronic ballast used to ignite two fluorescent lamps.

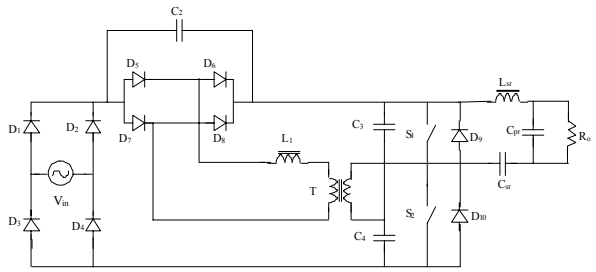
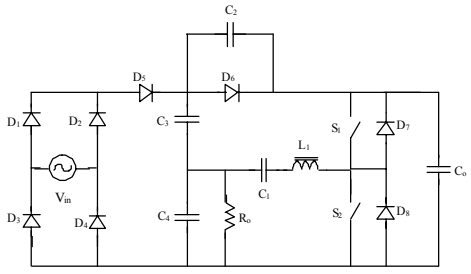
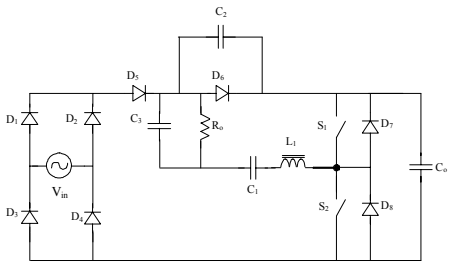


Fig. 1. Electronic ballast charge pump circuit proposed in [2].



(a)



(b)

Fig. 2. Electronic ballast charge pump circuit proposed in [3]-[4]:
(a) Type VS-CP-PFC.
(b) Type CS-CP-PFC.

II. CIRCUIT PRESENTATION

The symmetrical charge pump circuit to be studied was proposed by Güldner and others in [5]. Nevertheless, the design equations of the circuit do not appear, because the main topic is about the state-of-the-art of electronic ballast.

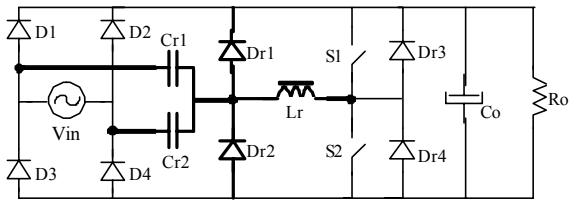


Fig. 3. Symmetrical charge pump circuit.

The components of the circuit are described as follows:

D_1, D_2, D_3 y D_4	: Bridge diodes.
C_{r1}, C_{r2}	: Resonant capacitor.
L_r	: Resonant inductor.
D_{r1}, D_{r2}, D_{r3}, D_{r4}	: Free-Wheeling diodes.
S_1, S_2	: Power transistor.
C_o	: Output capacitor.
R_o	: Load resistor.

III. Steady-State Operation

To describe the operating principles and the analysis all components are considered ideal. The analysis contemplates only positive period of the network because in the negative period it behaves in an analogous form. With this, and considering a period of commutation, we have 6 stages of operation, which are described next:

Stage 1 (t_0-t_1): At $t = t_0$ (Fig. 4) the switch S_2 is turned on, the current in the resonant inductor L_r increases due to the resonance with C_{r1} and C_{r2}, the resonant capacitor C_{r2} discharges through the resonant inductor L_r, whereas the capacitor C_{r1} is charged up by the source v_{in}. The current in L_r is the sum of the current in both capacitors. The output capacitor C_o feeds the load R_o. During this stage the current in the resonant inductor reaches its maximum value i_{Lrmax}, the voltage in the capacitor C_{r2} reaches zero and the capacitor C_{r1} is charged to from the voltage source v_{in}.

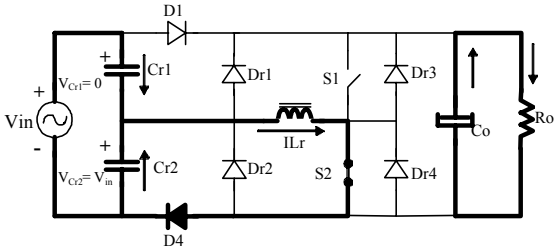


Fig. 4. First stage.

During this stage the current in the resonant inductor is:

$$i_{Lr}(t) = \frac{v_{in}(\theta)}{Z_o} \cdot \sin\left[\omega_o \cdot (t - t_0)\right] \tag{1}$$

Where:

$$\omega_o = \frac{1}{\sqrt{L_r \cdot (C_{r1} + C_{r2})}} \tag{2}$$

$$Z_o = \sqrt{\frac{L_r}{C_{r1} + C_{r2}}} \tag{3}$$

$$v_{in}(\theta) = V_{in} \cdot \sin(\theta) \tag{4}$$

Considering the maximum input voltage, the maximum value of the current in the inductor is:

$$i_{Lr\max} = \frac{V_{in}}{Z_o} \tag{5}$$

The time interval of this stage is deduced of (1) and is given by:

$$\Delta t_1 = \frac{\pi}{2 \cdot \omega_0} \tag{6}$$

At the moment at which the capacitors C_{r1} and C_{r2} are charged and discharged respectively, the diode D_4 is turned off.

Stage 2 (t_1-t_2): At $t = t_1$ (Fig. 5) the diode D_4 is biased inverse and the inductor current circulates in free wheeling through the diode D_{r2} and the switch S_2. The current in this stage is represented by (5).

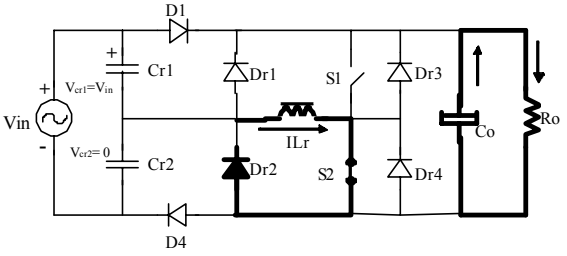


Fig. 5. Second stage.

Stage 3 (t_2-t_3): At $t = t_2$ (Fig. 6) the switch S_2 is turned off, the inductor current circulates through the diode D_{r3} feeding the capacitor C_o and R_o. During this stage the switch S_1 is turned on under zero voltage switching (ZVS). The current i_{Lr} during this stage is:

$$i_{Lr}(t) = \frac{v_{in}(\theta)}{Z_o} - \frac{V_{out}}{L_r} \cdot (t - t_2) \tag{7}$$

The inductor current decreases until reaches zero, blocking the diodes D_{r2} and D_{r3}, finishing this stage.

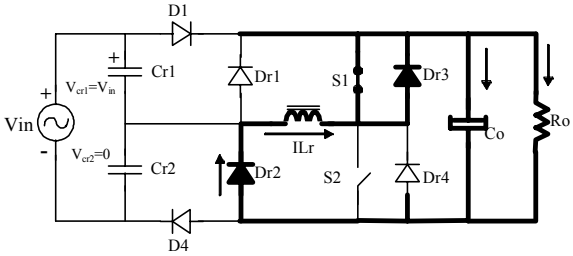


Fig. 6. Third stage.

To the end of this stage the current $_{iLr}$ is zero, then:

$$\Delta t_3 = \frac{v_{in}(\theta)}{V_{out} \cdot \omega_o} \tag{8}$$

Considering the maximum input voltage:

$$\Delta t_3 = \frac{V_{in}}{V_{out} \cdot \omega_o} \tag{9}$$

Stage 4 (t_3-t_4): At t = t_3 (Fig. 7) the switch S_1 is turned on, the diode D_1 is biased directly discharging the capacitor C_{r1} through the inductor L_r, the source v_{in} charge the capacitor C_{r2}, again the inductor current is the sum of the current in both capacitors. The capacitor C_o feeds R_o. During this stage the inductor current reaches its maximum inverse value, which to a maximum input voltage is represented by (5). The voltage in the capacitor C_{r1} is reduced to the zero whereas the voltage in the capacitor C_{r2} is v_{in}, at this moment diode D_1 is turned off, beginning the fifth stage.

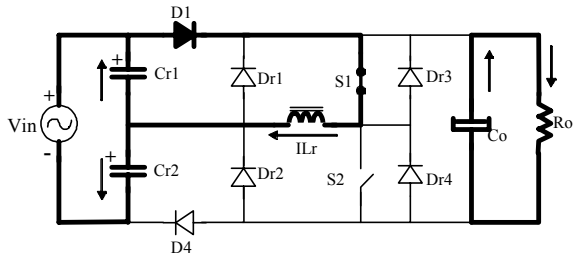


Fig. 7. Fourth stage.

Stage 5 (t_4-t_5): At t = t_4 (Fig. 8) the diode D_1 is biased inverse and the inductor current circulates freely through diode D_{r1} and the switch S_1. The capacitor C_o feeds R_o.

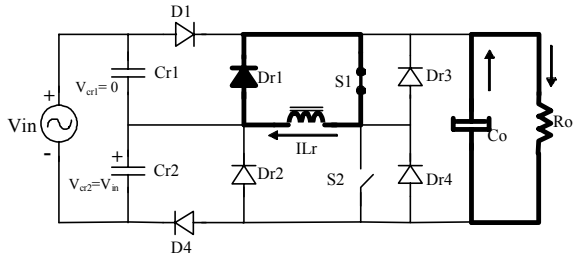


Fig. 8. Fifth stage.

Stage 6 (t_5-t_6): At t = t_5 (Fig. 9) the switch S_1 is turned off and the inductor current circulate through the diode D_{r4} feeding the capacitor C_o and R_o. During this stage S_2 turns on under zero voltage switching (ZVS). The inductor current decreases until zero, blocking diodes D_{r1} and D_{r4} beginning another period. The equations for this stage are analogous to those of the third stage.

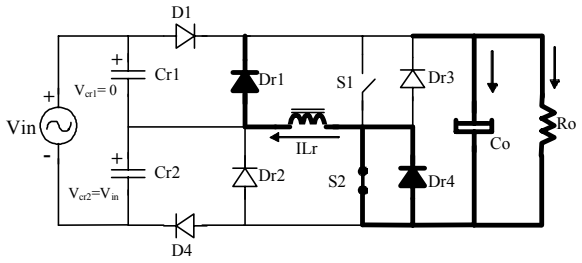


Fig. 9. Sixth stage.

The theoretical inductor current waveform, during a period of commutation, is shown in Fig. 10.

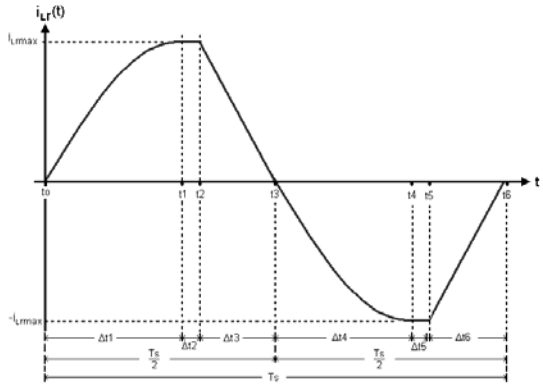


Fig. 10. The theoretical inductor current waveform.

A. Instantaneous Average Input Current

The instantaneous input current i_{in} has the double of the commutation frequency, then its period is $T_S/2$, the value of instantaneous average input current is determined by:

$$\bar{i}_{in}(\theta) = \frac{2}{T_s} \cdot \int_0^{T_s/2} i_{Lr}(t) \cdot dt = \frac{2}{T_s} \cdot \int_{t_0}^{t_1} \frac{v_{in}(\theta) \cdot \sin(\omega_o \cdot (t - t_0))}{2 \cdot Z_o} \cdot dt \tag{10}$$

Resolving (10) it is obtain:

$$\bar{i}_{in}(\theta) = \frac{v_{in}(\theta)}{Z_o \cdot \omega_o} \cdot \frac{1}{T_s} \tag{11}$$

This equation shows that the instantaneous average input current follows the input voltage in natural form if the period T_S is maintained constant. Therefore, the symmetrical charge pump circuit studied behaves like a power factor pre-regulator.

B. Design Equations

The process of transference energy is completely made by L_r, therefore:

$$\mathcal{E} = \frac{1}{2} \cdot (i_{Lr\max})^2 \cdot L_r = \frac{P_{in}}{f_s} \tag{12}$$

Substituting (5) in (12) can be obtained:

$$L_r = \frac{(V_{in})^2 \cdot \eta}{8 \cdot (\pi)^2 \cdot (\beta)^2 \cdot P_{out} \cdot f_S} \quad (13)$$

Where:

$$\beta = \frac{\omega_o}{\omega_s} \quad (14)$$

Replacing (13) in (5) and considering $C_{r1} = C_{r2}$ can be obtained:

$$C_{r1} = C_{r2} = \frac{P_{out}}{(V_{in})^2 \cdot f_S \cdot \eta} \quad (15)$$

The output capacitor design equation [7] is given by:

$$C_o \geq \frac{P_{out}}{\omega_{in} \cdot \Delta V_{out} \cdot V_{out} \cdot \eta} \quad (16)$$

C. Freewheeling Stage

At the second and fifth stages is observed that i_{Lr} is freewheeling through the switches producing losses. A solution to this consists in making these interval zero.

As the circuit is symmetrical can be writing:

$$\Delta t_1 + \Delta t_2 + \Delta t_3 = \frac{T_S}{2} \quad (17)$$

Substituting (6) and (9) in (17) yields:

$$\Delta t_2 = \frac{2 \cdot \pi \cdot \beta \cdot V_{out} - \pi \cdot V_{out} - 2 \cdot V_{in}}{2 \cdot \beta \cdot V_{out} \cdot \omega_S} \quad (18)$$

In order to satisfy $\Delta t_2 = 0$, must be fulfilled that:

$$2 \cdot \pi \cdot \beta \cdot V_{out} - \pi \cdot V_{out} - 2 \cdot V_{in} = 0 \quad (19)$$

Then from (19) β is obtained:

$$\beta = \frac{1}{2} + \frac{V_{in}}{V_{out} \cdot \pi} \quad (20)$$

The former equation was obtained considering maximum input voltage. Only in this voltage value the second and fifth stages are zero, therefore for the design β must be selected a value lower than (20).

IV. Design Example

The charge pump circuit parameters were determined using the design equation obtained in the former section.

The simulated circuit is shown in Fig. 11.

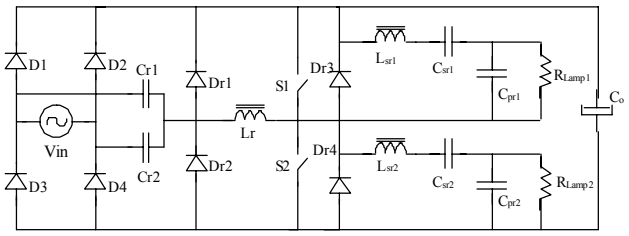


Fig. 11. Simulated circuit.

In Table 1 the input specifications are given.

TABLE 1
DESIGN SPECIFICATIONS

Input Voltage	220 [V_{RMS}] ; 50 [Hz]
Output Voltage (V_{out})	315 [V_{CC}]
Output Power (P_{out})	80 [W]
Switching Frequency (f_s)	50 [KHz]
Output Voltage Ripple	2% de V_{out}
Efficiency (η)	1 [-]
Duty Cycle(D)	0.5 [-]

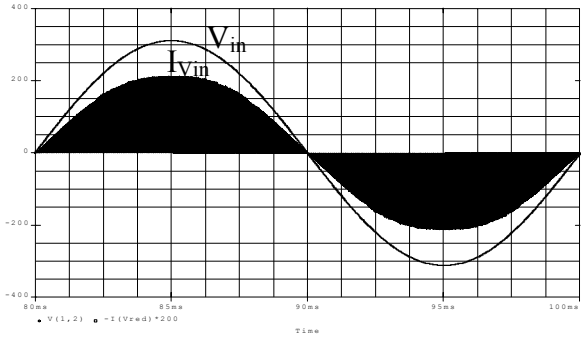
From (20) is determined β = 0.813, then taking β = 0.7, and with former specifications the parameters of circuit were obtained:

$L_r = 621$ [uH]
$C_{r1} = C_{r2} = 16.65$ [nF]
$C_o \geq 128.3$ [uF]

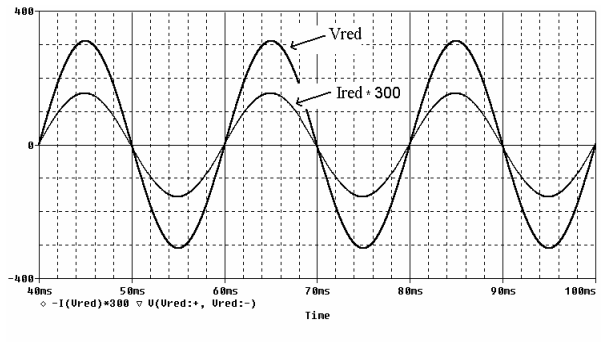
The main waveforms are presented in the following figures.

In Fig. 12(a) the input voltage and input current, without filter, are shown. It can be noticed that the current follows the input voltage, and has a THD of 2.5% and a Power Factor of 0.99.

Fig. 12(b) shows the input voltage and input current waveform, with their components in high frequency filtered.



(a)



(b)

Fig. 12. Input voltage and input current; (a) without filter; (b) with filter, operating in steady state.

Fig. 13 shows the inductor current waveform of a half network period.

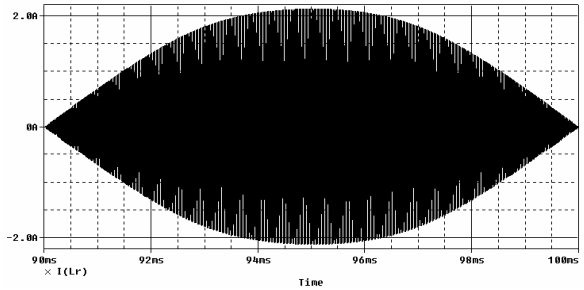


Fig. 13. Inductor current waveform, operating in steady state.

V. EXPERIMENTAL RESULTS

The electronic ballast driving two lamps Philips TLT-40W/54, working with an operation voltage V_{op} equal to 106 [V_{rms}].

In Table 2 the main components of the prototype are listed, specifying the theoretical and real values.

TABLE 2
COMPONENTS OF THE CIRCUIT

Symbol	Description	Theoretical value	Practical value
D_1, D_2, D_3, D_4	Diode bridge (UF4004)	---	---
D_{r1}, D_{r2}	Freewheeling diodes (UF4004)	---	---
C_0	Output capacitor	151 uF	223 uF
S_1, S_2	Mosfet IRF740	---	---
U_1	IC IR2151	---	---
L_{sr1}, L_{sr2}	Resonant inductor of ballast	1.45 mH	1.4 mH
L_r	Charge pump Inductor	528 uH	532.4 uH
C_{r1}, C_{r2}	Charge pump Resonant capacitor	19.6 nF	22 nF
C_{sr1}, C_{sr2}	Ballast Serie-resonant capacitor	20.34 nF	33 nF
C_{pr1}, C_{pr2}	Ballast Parallel-resonant capacitor	2.26 nF	6 nF

In Fig. 14 the experimental input current and voltage line are shown, the power factor obtained is 0.997.

The Fig. 15 shows the voltage across the capacitor C_o that is of approximately 320[V].

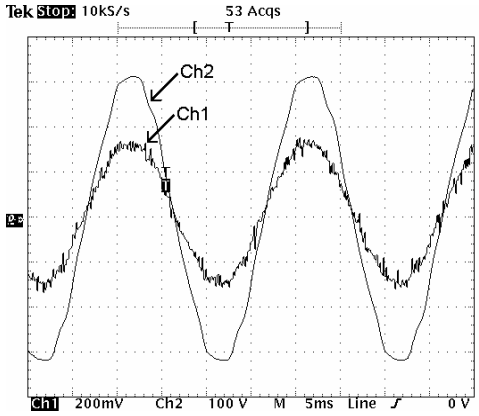


Fig. 14. Input current (Ch1) and input voltage (Ch2). (0.4A/div; 100V/div; 5ms/div)

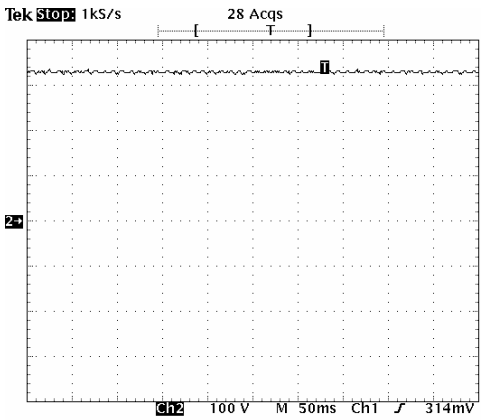
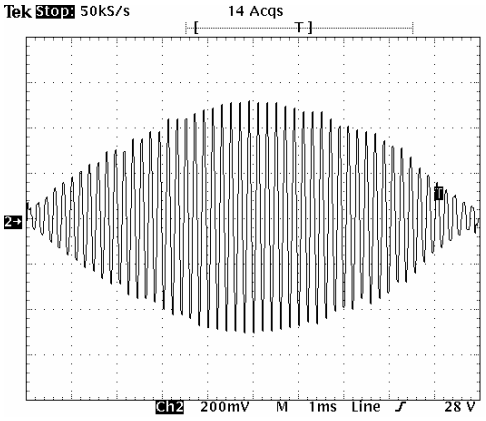


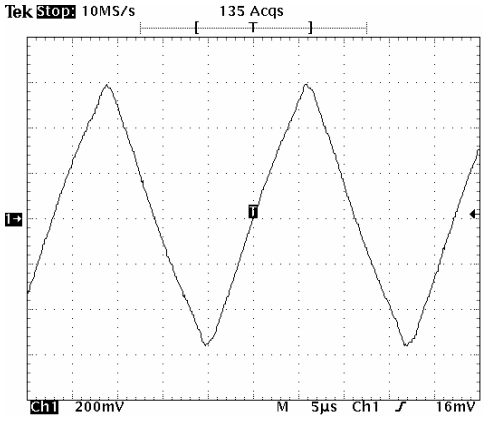
Fig. 15. Voltage across C_o (100V/div; 50 ms/div)

Fig. 16(a) shows the current through the inductor L_r. It can be observed that is formed by two components: one modulated in low frequency (100 Hz) another in high frequency (50 KHz). The Fig. 16(b) shows a detail of the current through inductor L_r when the current reaches its maximum values, being observed that the current does not present flat zones in its peaks, which indicates that the stage of freewheeling was eliminated, however, Fig. 16(c) shows a detail of the current through the inductor L_r when the current reaches its minimum value presenting flat zones in its peaks.

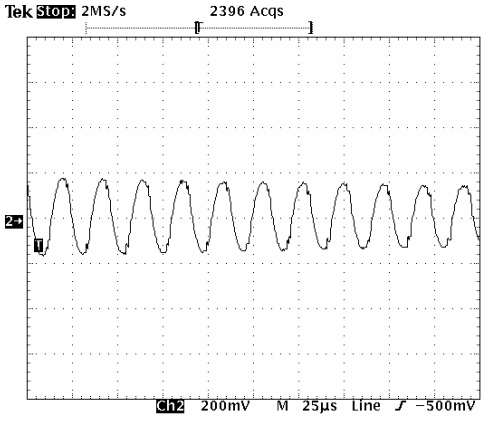
This indicates the stage of freewheeling has not been completely eliminated.



(a)



(b)



(c)

Fig. 16. Inductor current waveform, steady state:
(a) In a period of network (1A/div; 1ms/div)
(b) In its maximum (0.8A/div; 5us/div)
(c) In its minimum (0.3A/div; 25us/div)

Finally Fig. 17 shows the high frequency voltage and current in one of the lamps.

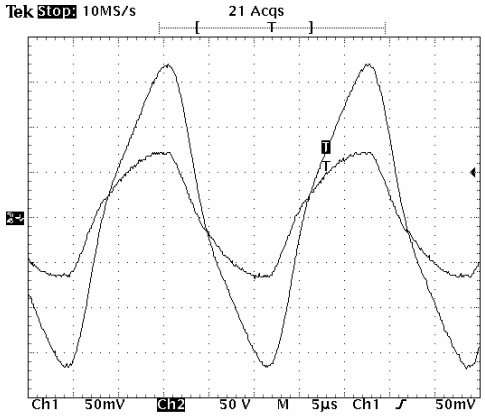


Fig. 17. Lamp voltage and current, operating in steady state.
(50V/div; 0.5A/div; 5us/div)

VI. CONCLUSIONS

A study and design methodology for a power factor pre-regulator based on symmetrical charge pump circuit was presented.

The experimental results obtained verify the validity of the correct design methodology.

The main advantages of the charge pump circuit are that input and output capacitor (C_o) current have the double of the switching frequency, this allows to reduce the size of the input filter and the output capacitor, besides does not increase the number of switches, having a single stage of processing of energy.

A disadvantage of the symmetrical charge pump circuit is that it only operates with nominal power, being necessary to design a circuit of protection against voltages surges when a lamp falls or the reactor is no load.

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