A NEW HIGH-POWER-FACTOR AC VOLTAGE REGULATOR IN HIGH-SWITCHING FREQUENCY OF OPERATION

F. D. Dantas[1] and C. A Canesin[2]

[1] UNIDERP, P.O. Box 2153, Campo Grande/MS, Brazil, e-mail: fausto@dee.feis.unesp.br
[2]DEE, FEIS-UNESP, Paulista State University, P.O. Box 31, Ilha Solteira, Brazil, e-mail : canesin@dee.feis.unesp.br

Abstract— **This paper describes a novel high frequency ac voltage-regulator using a Single Ended Primary Inductance Converter as power stage, and active power factor correction through the use of variable hysteresis control technique. The main advantage of this ac voltage-regulator concerns with the smaller volume, and size than the conventional ones. Nowadays, due to power quality standards, high input power factor is a necessity for power electronic converters to perform that the input current total harmonic distortion (THD) fits into the limits of the standards, like as IEC 61000-3-2 limits. It should be noticed that the input current harmonics content for the novel ac high frequency voltage-regulator are in agreement with the requirements defined in the IEC 61000-3-2 standards. This paper presents a complete analysis, design and simulation results for a prototype rated at 300W, operating with variable switching frequency (30Hz until 90kHz), and 127Vrms of nominal input and output voltages.**

KEYWORDS

AC voltage regulators, active power factor correction, digital control, EPLD devices

I. INTRODUCTION

In the last years researchers have been developed active control techniques to obtain input current THD limitation, and almost unity input power factor for several power electronics converters [1].

On the other hand, the use of high switching frequency operation becomes an option to obtain high power density, resulting in a volume, and size reduction for the converters [2 until 8].

In this context, for the ac voltage regulators, the use of a conventional structure, normally composed by a single-phase autotransformer, or transformer, passive elements, and active semiconductors operating at low frequencies, becomes a problem to obtain agreement with the requirements of the power quality standards.

However, additional problems are the volume and size of these conventional structures that use low frequency control techniques to obtain output voltage regulation [1, 2, 7, and 9].

In spite of the conventional ac voltage-regulators perform high input power factor for linear loads applications, the non-linear loads are increasing in the last decades for several power electronics converters, mainly for electronic information applications. So, the use of the conventional ac voltage regulator does not permit to obtain a high input power factor, and low input current total harmonic distortion for non-linear loads [1, 2, 7, and 9]. Therefore, active power factor correction techniques are appropriated for this application.

The use of a structure that operates at high switching frequency additionally allows an increased in the power density of the converter [9].

The proposed high frequency ac voltage-regulator uses a SEPIC (Single Ended Primary Inductance Converter) structure, allowing conditions to control the input current shape through the sinusoidal hysteresis control technique to ensure that the input current THD satisfies the requirements of IEC 61000-3-2 standards, resulting in a high input power factor for the converter. The load voltage regulation is performed using a feed-forward control technique, and digital control (VHDL) employing an EPLD device.

Therefore, the novel ac voltage-regulator performs high input power factor, and reduced input current THD, independent of the load type.

In this context, this paper presents a new 300W SEPIC ac voltage-regulator, operating with variable switching frequency (30kHz to 90kHz), and 127Vrms of nominal input and output voltages.

II. THE NOVEL AC VOLTAGE-REGULATOR

The power stage diagram of the novel high switching frequency ac voltage-regulator is shown in Figure 1, where the ac switches S_a and S_b are bi-directional switching elements. Each bi-directional switch is composed by two switches implemented with MOSFETs connected in anti-series.

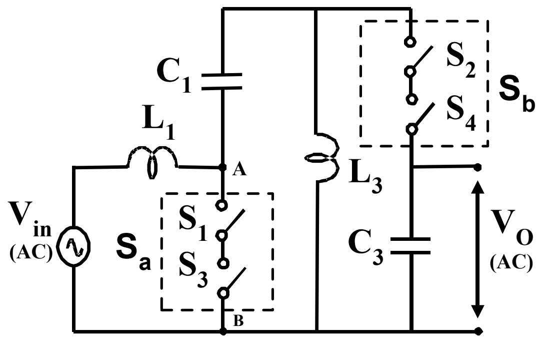


Figure 1- The power stage diagram of the AC/AC SEPIC regulator.

The ac switches are composed by two semiconductor devices (MOSFET), in an arrangement as shown in Figure 2.

In order to describe the operation of the proposed structure, it is assumed that:

- All semiconductor devices are ideal;
- The switching frequency is larger than the ac line frequency;
- During a switching period, the input voltage is constant;
- The input voltage is considered purely sinusoidal;
- The reactive components are ideal.

Through the use of the above simplified conditions, the converter can be analyzed in four stages of operation as shown in Figure 3.

A. VARIABLE HYSTERESIS CONTROL TECHNIQUE

Figure 4 shows the variable hysteresis control technique used to obtain high input power factor for the novel ac voltage-regulator.

The control circuitry uses digital technique, employing VHDL and EPLD devices to compose the signals for all controlled semiconductors. The blocks diagram of this control circuitry is shown in Figure 5.

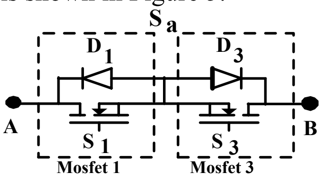
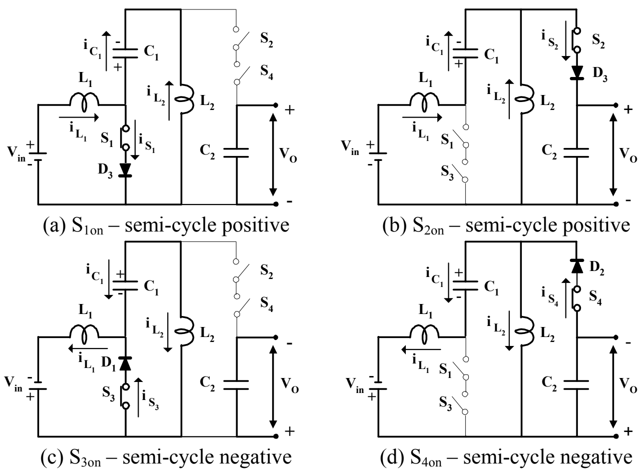


Figure 2 – Main AC switch S_a arrangement, using power MOSFET.



(a) S_{1on} – semi-cycle positive (b) S_{2on} – semi-cycle positive

(c) S_{3on} – semi-cycle negative (d) S_{4on} – semi-cycle negative

Figure 3 – Stages of operation for the novel ac voltage-regulator.

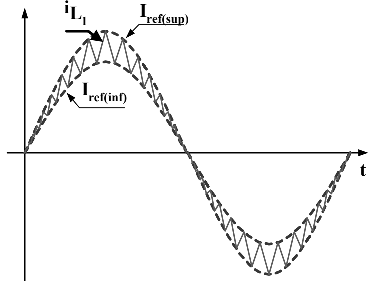


Figure 4 – Variable hysteresis control technique, using VHDL and EPLD devices.

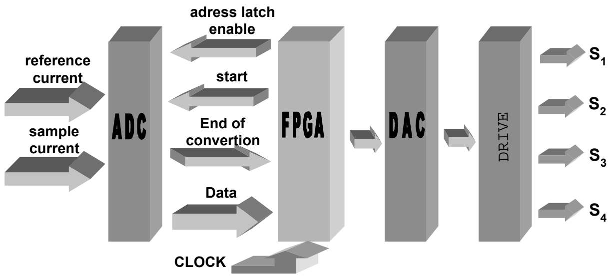


Figure 5 – Blocks diagram of control circuitry.

III. DESIGN PROCEDURE AND EXAMPLE

The input and output data for the novel high frequency ac voltage-regulator proposed are listed as follow:

$V_{in_{rms_{nominal}}} = 127V$; $f_{line} = 60Hz$; $P_{O_{nominal}} = 300W$;

$V_{O_{rms_{nominal}}} = 127V$; $f_{s_{min}} = 30kHz$; $f_{s_{max}} = 90kHz$;

$\Delta I_{L_1} = 0.352A$; $\Delta V_{C_1} = 50V$; $\Delta V_{C_2} = 5V$; $f_{s_{peak}} = 50kHz$.

In the next steps one can verify the proposed design procedure.

Step 1: Inductance values of the input filter (L_1), and accumulation inductor (L_2).

The inductance (L_1) value of the input filter is given by equation (1):

$$L_1 = \frac{V_{in_{max}} . D_{rms}}{f_{s_{peak}} . \Delta I_{L_1}} \tag{1}$$

Where:

$V_{in_{max}} = 179.61V$

$D_{rms} = 0.5$

Thus,

$$L_1 = 5.108mH$$

Therefore, were adopted:

$$L_1 = L_2 = 5.1mH$$

Step 2: Capacitance value (C_1) of the accumulation filter

The capacitance C_1 value of the accumulation filter is given by equation (2):

$$C_1 = \frac{I_{in_{rms}} . \sqrt{2}}{2 . f_{s_{peak}} . \Delta V_{C_1}} \tag{2}$$

Where:

$I_{in_{rms}} = 2.487A$

Thus,

$$C_1 = 703.43nF$$

Therefore, was adopted:

$$C_1 = 680nF$$

Step 3: Capacitance (C_2) value of the output filter

The capacitance (C_2) value of the output filter is given by equation (3):

$$C_2 = \frac{\dfrac{P_{O_{nominal}}.\sqrt{2}}{V_{Orms_{nominal}}}}{2.f_{s_{peak}}.\Delta V_{C_2}} \quad (3)$$

Thus,

$$C_2 = 6uF$$

Therefore, was adopted:

C_2 = 3x2.2uF (in parallel)

Figure 6 shows the designed power circuit used to verify the performance of the proposed ac voltage-regulator, through its simulation results.

IV. SIMULATION RESULTS

The main simulation results for the proposed ac voltage-regulator, supplying linear and non-linear loads, are shown in Figures 7 and 8.

One can verify that the input power factor for both conditions of loads is almost the unity, and the input current THD is reduced, independent of the load type. Therefore, the novel ac voltage-regulator fits into the limits of the IEC61000-3-2 standards.

It should be notice that, using variable hysteresis control technique, the switching frequency will be variable.

Figure 9 shows details of the distortion at input current during the zero-crossing of the references.

Figures 10 and 11 show details of the current through the input inductor for different values of the instantaneous input voltage. It can be observed in Figure 10(a) that the minimum value of switching frequency is 30kHz, and its maximum value is almost 90kHz, according Figure 10(b). Figures 11(a) and 11(b) show that the switching frequency in the maximum and minimum input voltage values is 50 kHz.

In spite of all circuit parameters have been designed for 30kHz, the total volume and size are reduced, in comparison with the conventional ac voltage regulators.

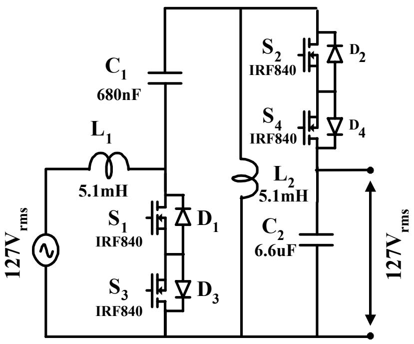


Figure 6 - Novel ac voltage-regulator proposed.

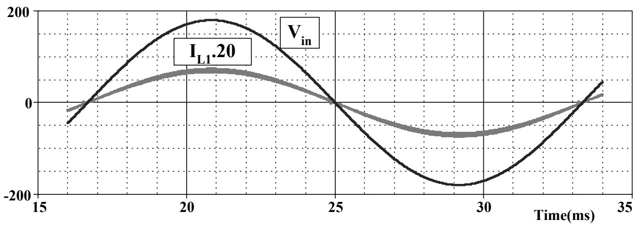


Figure 7 – Input current and voltage for linear load, operating at nominal value.

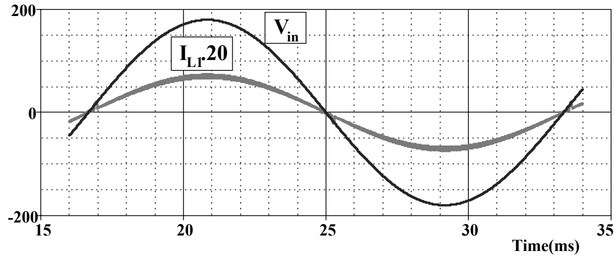
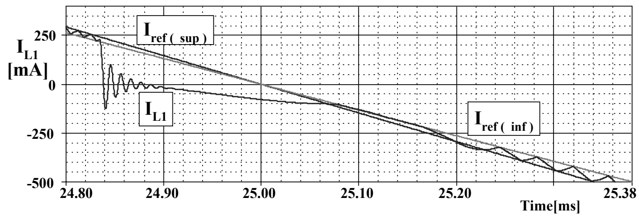
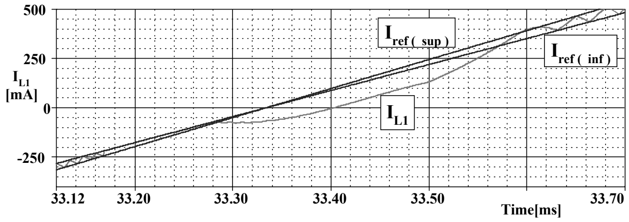


Figure 8 – Input current and voltage for non-linear load (switching-mode power supply), operating at nominal value.

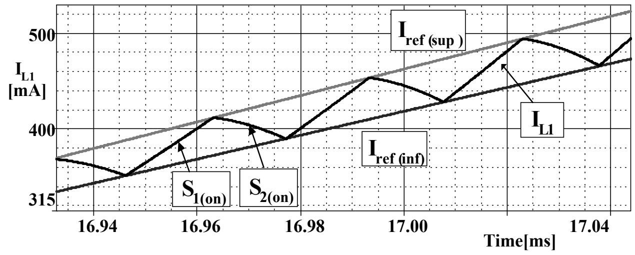


(a) Positive semi-cycle to negative semi-cycle.

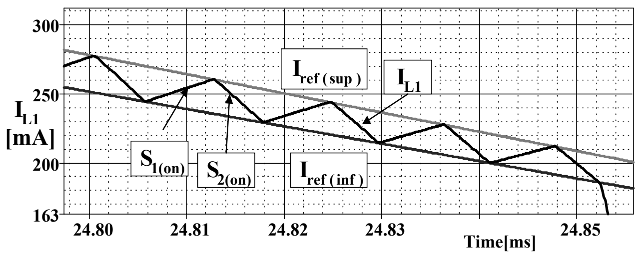


(b) Negative semi-cycle to positive semi-cycle.

Figure 9 - Details of the distortion at input current during the zero-crossing of the references (I_{sup} and I_{inf}).



(a) Vin ≅ 10V; switching frequency ≅ 30kHz (minimum value).

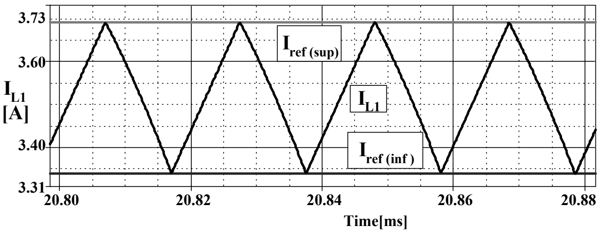


(b) Vin ≅ 10V; switching frequency ≅ 90kHz (maximum value).

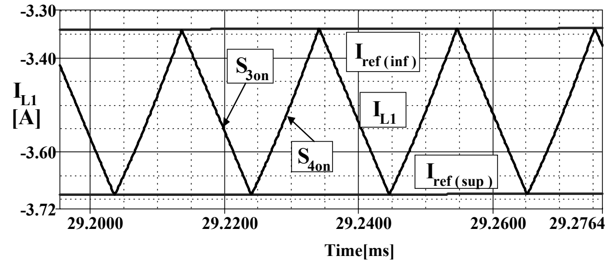
Figure 10 – Details of the current through the input inductor, in the positive semi-cycle.

It is important to note that the controller does not allow that the switches operate for a voltage range of $+10V$ until $-10V$. This leads to a small input current drift, as shown in Figure 9. During this interval, all switches are turned off.

This constraint for the controller is to ensure that the switching frequency (f_s) stays between 30 kHz and 90 kHz.

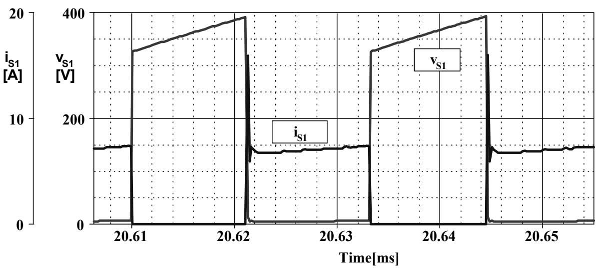


(a) Vin ≅ 180V; switching frequency ≅ 50kHz (fs_{peak}).

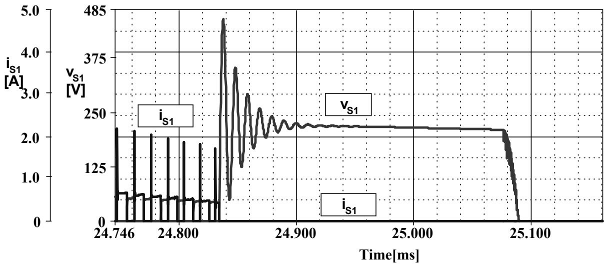


(b) Vin ≅ -180V; switching frequency ≅ 50kHz (fs_{peak}).

Figure 11 – Details of the current through the input inductor, in the positive and negative value peak of the input voltage.



(a) S_1 commutations near maximum input voltage value (V_{in} ≅ 180V).



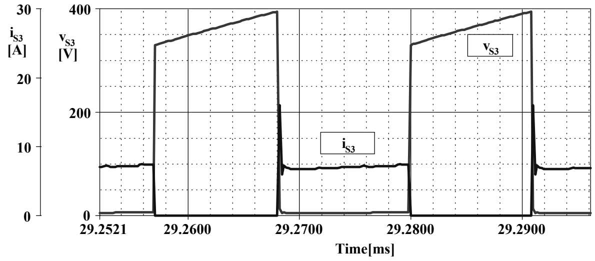
(b) S_1 commutations near zero input voltage value (V_{in} ≅ 0V).

Figure 12 – Details of the S_1 commutations near maximum and near zero input voltage values.

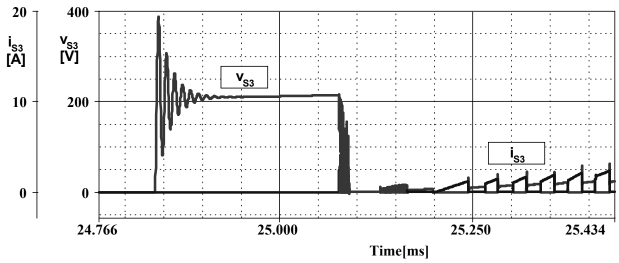
Figures 12 and 13 show details of the S_1 and S_3 commutations near maximum and near zero input voltage values.

The proposed control is in closed-loop operation, in spite of this, an example in open-loop operation, using VHDL (MAXPLUS II), is shown in Figure 14.

Figure 15 shows simulation results for some cases of the S_1 and S_2 commutations. Figure 15(a) shows that the value of sample current is higher than the values of superior reference current and memory current. In addition, the derived of sample current is positive. In this case, the switch S_2 turns on and S_1 turns off. Figure 15(b) shows that the value of sample current is between inferior and superior reference currents, and its derived is negative. In this case, the switch S_2 must continues turned on.



(a) S_3 commutations near maximum input voltage value (V_{in} ≅ 180V).



(b) S_3 commutation near zero input voltage value (V_{in} ≅ 0V).

Figure 13 – Details of the S_3 commutations near maximum and near zero input voltage values.

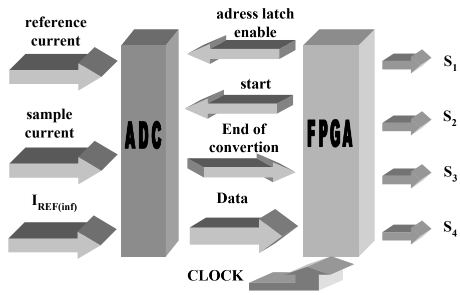


Figure 14 – Blocks diagram of control circuitry, in open-loop operation.

Figure 15(c) shows that the value of sample current is lower than the values of the inferior reference current and memory current. In addition, the derived of sample current is negative. In this case, the switch S_1 turns on and S_2 turns off.

Figure 15(d) shows that the value of sample current is between superior and inferior reference currents. In this case, the switch S_1 must continue turned on.

Figure 16(a) shows that the value (in module) of sample current is higher than the values (in module) of superior reference current and memory current. In addition, the derived of sample current is negative. In this case, the switch S_4 turns on and S_3 turns off. Figure 16(b) shows that the value (in module) of sample current is between superior and inferior reference currents, and its derived is positive. In this case, the switch S_4 must continue turned on. Figure 16(c) shows that the value (in module) of the sample current is lower than the values (in module) of the inferior reference current and memory current. In addition, the derived of sample current is positive. In this case, the switch S_3 turns on and switch S_4 turns off.

Figure 16(d) shows that the value of sample current is between superior and inferior reference currents. In this case, the switch S_3 must continues turned on.

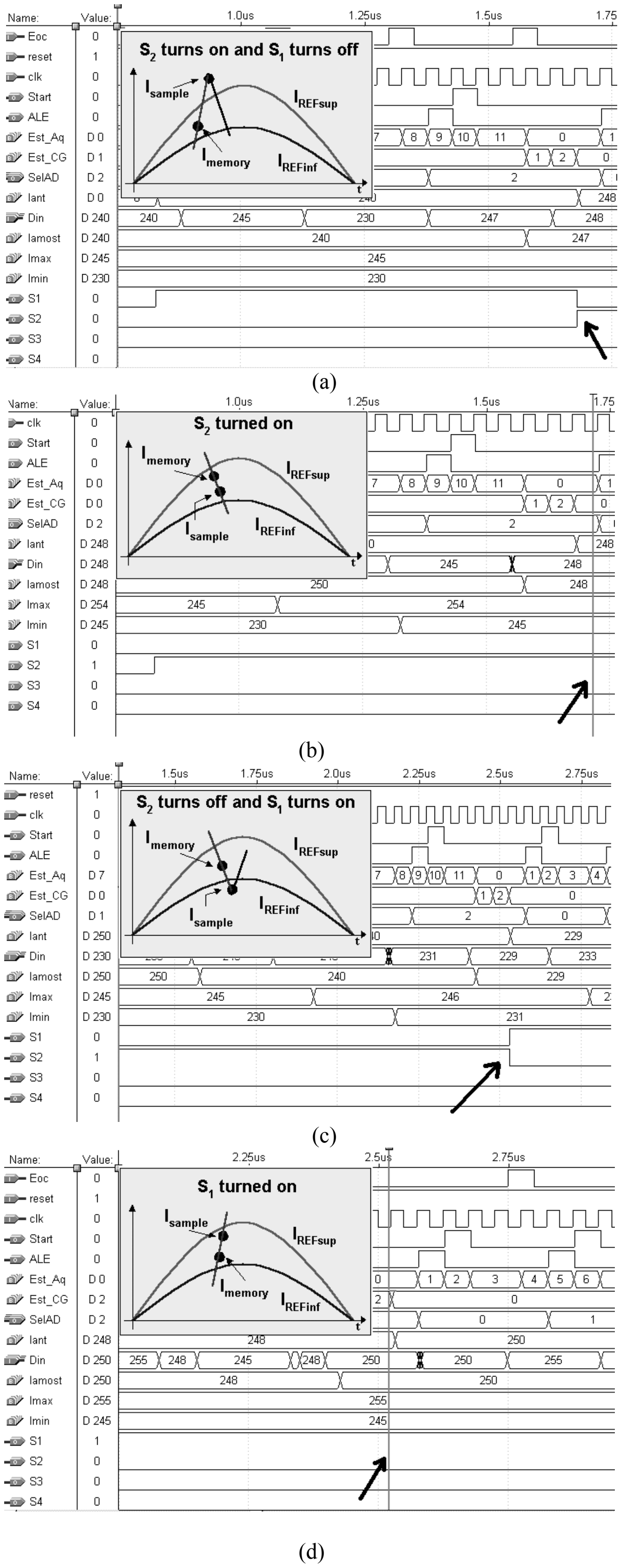


Figure 15 - Details for the S_1 and S_2 commutations, due to the proposed control technique.

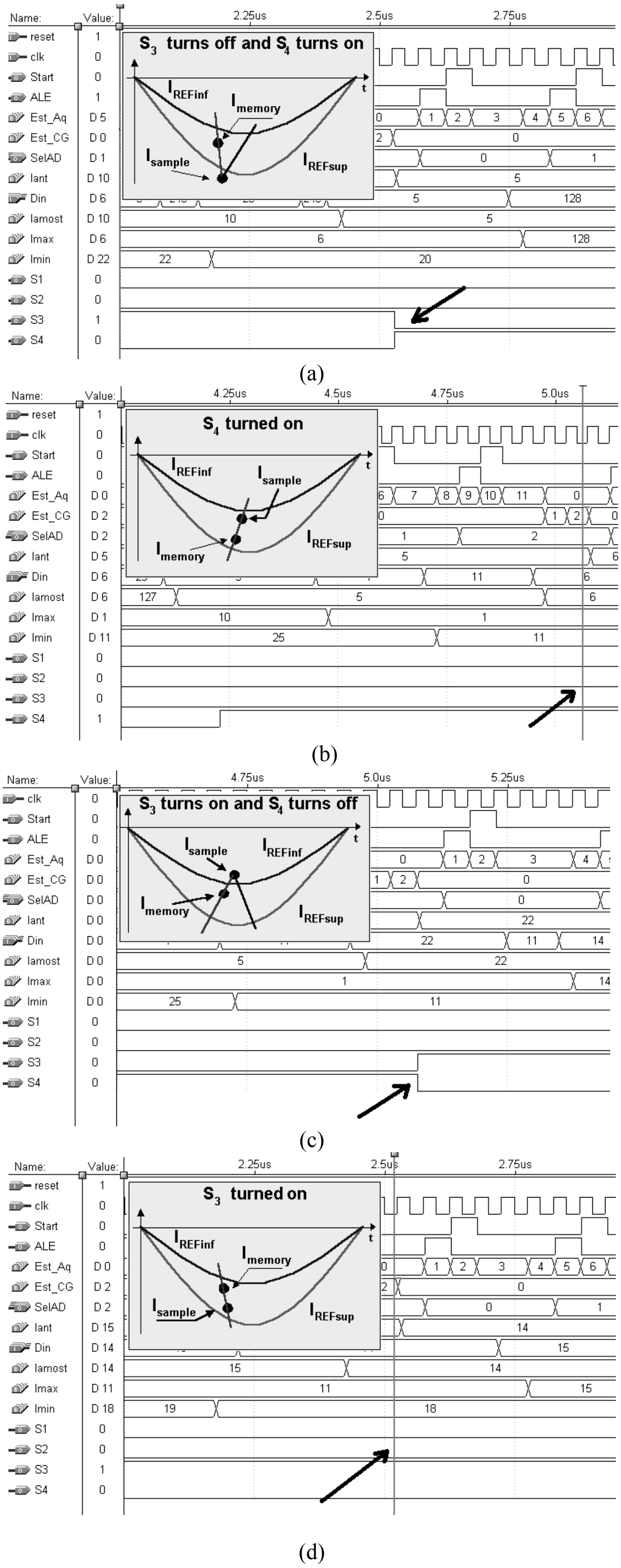
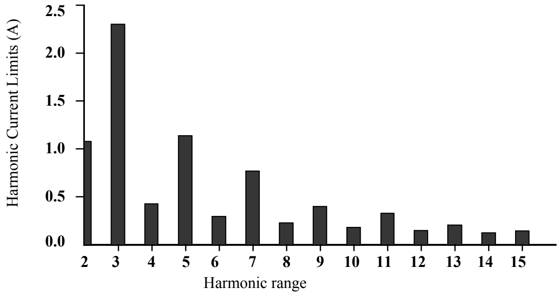
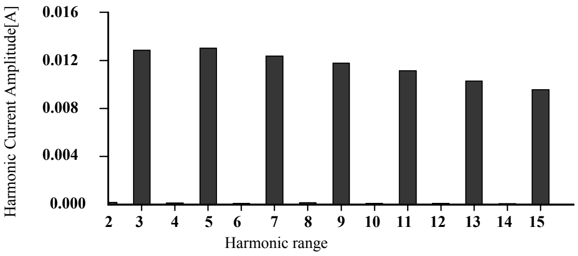


Figure 16 - Details for the S_3 and S_4 commutations, due to the proposed control technique.



(a) Harmonic Current Limits of the IEC 61000-3 –2 standards.



(b) Harmonic current amplitudes from the designed example.

Figure 17 – Harmonic current limits for the IEC 61000-3–2 standards and harmonic current amplitudes from the designed example.

Figure 17 shows the harmonic current limits established by the IEC 61000-3-2 standards, for class **A** equipments, and the harmonic current content from the proposed converter.

From these simulation results, it can be observed that the total harmonic current distortion from the proposed converter satisfies the IEC 61000-3-2 standards.

V. CONCLUSIONS

This paper presented a novel high frequency ac voltage-regulator with high input power factor, through the use of variable hysteresis control technique.

The main advantage of this proposed converter is the low input current THD, independent of the load type (linear, and non-linear loads). In addition, through the use of the SEPIC converter, operated at 30kHz of minimum switching frequency value, the proposed regulator presents high power density (low volume, and size), in comparison with the conventional ones, that operate at low switching frequencies.

Using VHDL and EPLD devices, the control technique and circuitry were simplified, reducing size and costs.

Therefore, through the use of this novel ac voltage-regulator will be possible a compact converter and power quality accomplishment with the requirements of the IEC 61000-3-2 standards.

ACKNOWLEDGMENTS

The authors would like to thanks to CNPq and UNIDERP for supporting this work.

REFERENCES

[1] C. Zhou, R.B. Ridley, F.C. Lee, “Design and analysis of a hysteretic boost power factor correction circuit”, *IEEE-PESC '90 Records*, pp. 800-807, 1990.

[2] S. A. Hamed, “Steady-State Modeling, Analysis, and Performance of Transistor Controlled AC Power Conditioning Systems”, *IEEE Trans. On Power Electronics*, Vol. 5, no 3, pp. 305-313, July, 1990.

[3] D. H. Jang, J. S. Won, G. H. Choe, “Asymmetrical PWM Method for AC Chopper with Improved Input Power Factor”, *IEEE-PESC '91 Records*, pp. 838-845, 1991.

[4] I. Barbi, , J. C. Fagundes and Kassick E. V., “A Compact AC/AC Voltage Regulator Based on an AC/AC High Frequency Flyback Converter”, *IEEE-PESC '91 Records*, pp. 846-852, 1991.

[5] P. N. Enjeti and S. Choi, “An Approach to Realize Higher Power PWM AC Controller”, *Conference Proceedings of IEEE-APEC’93*, pp. 323-327, 1993.

[6] I. Barbi, E. V. Kassick, J. C. Fagundes, “A Novel Family of PWM High Frequency AC Choppers”, *COBEP’93*, pp. 302-307, 1993.

[7] I. Barbi, E. V. Kassick, J. C. Fagundes, “A PWM AC Chopper Without Dead Time and Clamping Circuit”, *COBEP’93*, pp. 297-301, 1993.

[8] D. Y. Huh, G. H. Cho, “Electronic Step Down (220/110V) Transformer Using a New Quantum Series Resonant Converter”, *IEEE Transaction Industrial Electronics*, Vol. 8, No.4, pp. 439-444, October, 1993.

[9] G. F. Moita, E. V. Kassick, I. Barbi, “An AC Voltage Regulator Employing Power Transistors and High Frequency Switching Technique”, *COBEP’93*, pp. 365-370, 1993.

[10] J. C. Oliveira, L. C. Freitas, V. J. Farias, and J. B. Vieira Jr, “A Serial Regulator using s soft switching PWM AC/AC Full Bridge Converter”, *PESC'99*, pp. 193-198 1999.

[11] J. C. Oliveira, L. C. Freitas, V. J. Farias, and E. A. S. Silva, “ Two AC/AC Regulators studied in a comparative way: The serial AC Link Regulator and the Boost/Inverter Converter”, *Conference Proceedings of IEEE-APEC’2000*, pp. 862-874, 2000.