A DIGITAL CONTROL APPLIED TO A SERIES ACTIVE FILTER FOR HARMONIC VOLTAGE REDUCTION

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***Abstract* – This paper proposes a harmonic voltage reduction filtering system, which uses a series active filter under a digital control strategy. The digital control approach is chosen to overwhelm certain unfavorable points, which are common in the analog controllers. The filtering system reduces or even eliminates harmonic voltage content supplied to loads or consumers. It consists of a voltage-fed PWM inverter with a LC filter and is inserted in series between an AC supply and a load. The compensation principle and theoretical analysis are described. Simulation and experimental results of an active filter, applied to a load, are presented which validate its purpose.**

KEYWORDS

Series active filter, digital control, active filtering, harmonic voltage reduction.

I. INTRODUCTION

The growing and widespread use of electronic equipment by different segments of society is perceptible. This equipment presents itself as non-linear impedances to its supplying electrical systems and generates harmonic currents with well-known undesirable effects, such as low power factor, electromagnetic interference, voltage distortions, etc. These disturbances have required researchers and power electronics engineers to present solutions to minimize or eliminate them [1,2]. Hence, the quality of the electrical system is an important matter and, within this context, voltage distortion is the focus of this article. Thus, if a sinusoidal or good quality voltage waveform must be available at a certain point in the electrical system to supply generic or critical loads, consumers or to comply with standards and technical recommendations, a voltage filtering system is required (Fig. 1).

An option is the use of active filters, conceptually established in the 70's. A series active filter is the appropriate choice to improve voltage waveforms. One topology, proposed by [3], describes the use of a series filter requiring a power source (usually a dc link) that is supplied by an auxiliary source. Still regarding series active filters, a second work proposes its use in harmonic current compensation [4] while a third one, combined it with a passive element resulting in a hybrid voltage filter [5]. Different from the concept used in [4] the hybrid filter acts as a controlled voltage source to correct the voltage available to loads. According to [5], the main problem of the hybrid filter is determining its reference signals (current and voltage). The structures pointed at [6, 7] overcome these restrictions. Conversely its strategy control requires the use of a filter system to extract the reference signal to the active filter. Thus, it is necessary to separate the fundamental component from all others harmonic components including those of low order (3^{rd}, 5^{th}, 7^{th},…). This is a hard task and sometimes it requires special circuits to be executed. This situation is an unfavorable aspect of that strategy control.

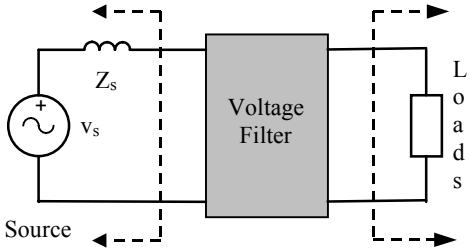

Fig. 1 Voltage filtering system.

An alternative to overwhelm the cited unfavorable aspect is the use of the digital technology. So this paper proposes a series active filter under a digital control strategy, to reduce harmonic voltages without using auxiliary source for the DC bus line. The filter equations were developed to determine, in a direct manner, its parameters and components. In addition, the digital control strategy used for the active filter is quite simple.

II. FILTERING SYSTEM CONFIGURATION AND PROPOSED CONTROL STRATEGY

The control strategy for the series active filter uses average voltage mode control. It is illustrated in Fig. 2. The series active filter is controlled by monitoring the input voltage. A digital sinusoidal voltage $v_{s1}(k)$ is subtracted from the input voltage resulting the signal $v_{sh}(k)$, which contains the harmonics to be compensated.

The $H_1(z)$ compensator is responsible for keeping the average voltage on the DC side of the inverter constant, therefore, the losses of the inverter and capacitor C_a will be compensated. It takes the sample of v_{di} and compares it to the reference $v^*_d(k)$.

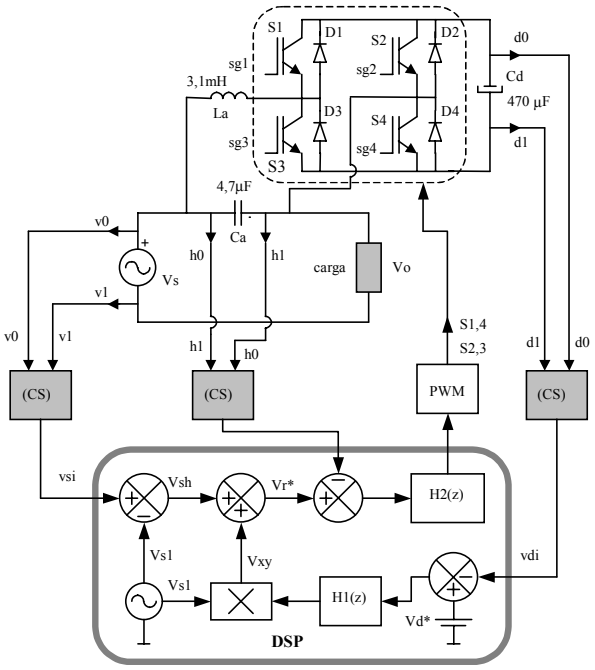

Fig. 2 – Series active filter and its digital control block diagram.

After processing the error between these signals its output multiplies the digital sinusoidal signal $v_{s1}(k)$, which is in phase with and proportional to the fundamental component of the input voltage. This operation produces the sinusoidal signal $v_{xy}(k)$. It is added to the voltage $v_{sh}(k)$ yielding a reference voltage, the signal $v^*_r(k)$, which is to be produced in C_a.

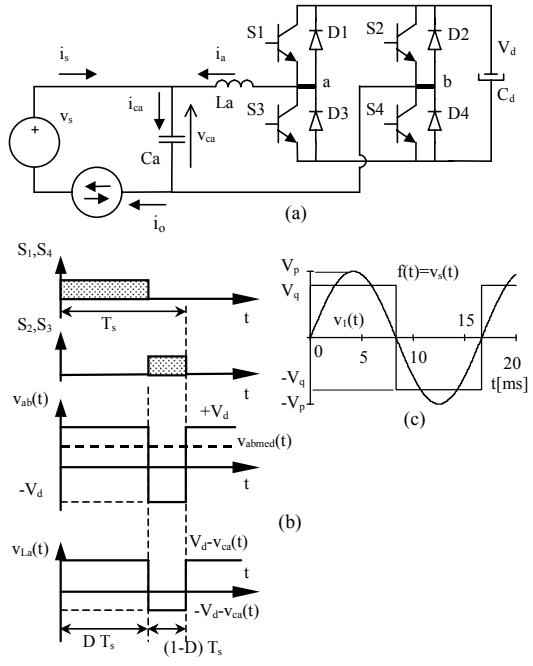

Fig. 3 Series active filter (a); waveforms for a switching period (b); source voltage waveform (c).

This signal and the signal sampled from capacitor C_a are compared one to another and are fed to the compensator $H_2(z)$. The output signal of $H_2(z)$ is fed to the digital PWM module. This module generates command signals for the inverter's switches.

Fig. 3a presents the series active filter being used between a voltage source, a distorted one, and a load, represented by a current source. During operation, the inverter's switches are commanded in a complementary manner. During the interval DT_s, switches S_1 and S_4 are on and S_2 and S_3 are off. During the interval $(1\text{-}D)T_s$, this situation is inverted. This characterizes a two-level modulation of the voltage between terminals **a** and **b**. Fig. 3 is used for the theoretical analysis.

III. THEORETICAL ANALYSIS – PRINCIPAL EQUATIONS

Voltage $v_{ab}(t)$ varies between $-V_d$ and $+V_d$, as shown in Fig 3b. The average value of this voltage, within a switching period, $T_s = 1/f_s$ is defined by equation (1).

$$V_{abmed}(t) = \frac{1}{T_s}\left[\int_0^{D\,Ts} V_d\,dt + \int_0^{(1-D)\,Ts} -V_d\,dt\right] = V_d\,(2D-1) \quad (1)$$

It is determined that during a switching period, T_s, the DC bus line voltage remains constant with an average value of V_d. Duty cycle D is associated with switches S_1 and S_4 and its complement, (1-D), is associated with S_2 and S_3. The value of interval Δt is defined by (2).

$$\Delta t = DT_s \quad (2)$$

Voltage $v_o(t)$ across the load must be sinusoidal and a square waveform, f(t), as presented in Fig. 3c, is used for input voltage $v_s(t)$ - ($v_s(t) = f(t)$). Signal $v_s(t)$ has a maximum amplitude equal to V_q, a period of T = 1/60 s, $\omega = 2\pi/T$ and making $(4/\pi)V_q = V_p$, $v_s(t)$ can be written as in (3).

$$v_s(t) = V_p \sin(\omega t) + V_p\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega t\right]\right] \quad (3)$$
$$= v_1(t) + v_h(t)$$

A. Duty cycle D, current ripple Δi_a and inductor L_a

Voltage $v_{ca}(t)$ across capacitor C_a, which contains the harmonics to be filtered, is defined by (4).

$$v_{ca}(t) = \frac{4V_q}{\pi}\left[\sum_{u=2}^{v}\frac{1}{2u-1}\sin\left[(2u-1)\omega_c t\right]\right] \quad (4)$$

Between terminals **a** and **b** a high frequency waveform is present, composed of a carrier signal and a modulating signal, that is, voltage $v_{ab}(t)$. This voltage is similar to voltage $v_{ca}(t)$. Therefore, voltage $v_{ab}(t)$ is defined by (5).

$$v_{ab}(t) = \frac{4V_q}{\pi}\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega_a t\right]\right] \quad (5)$$

Assuming that the switching frequency, f_s, is by far greater than the frequency of the highest order harmonic, in (5), and combining equations (1), (2), and (5) results in a duty cycle D(t) as shown in (6).

$$D(t) = 0.5\left[1 + \frac{4V_q}{\pi V_d}\left[\sum_{n=2}^{m}\frac{1}{2n-1}\sin\left[(2n-1)\omega_a t\right]\right]\right] \quad (6)$$

Assuming $V_q = V_d$, as more harmonic components are taken into consideration, the excursion of D(t) tends, in some regions, towards the limit values of 1.0 and 0. In this manner, a voltage modulation index, M_v, is defined as in (7).

$$M_v = \frac{V_q}{V_d} \quad (7)$$

During the conduction interval of S_1 and S_4 of the circuit in Fig. 3a, equation (8) in obtained.

$$L_a \frac{\Delta i_a(t)}{\Delta t} = V_d - v_{ca}(t) \tag{8}$$

Equations (2), (6) and (4) are substituted into (8) resulting in equation (9), which represents the parametric variation of the ripple current through inductor L_a of the series active filter.

$$\overline{\Delta i_a(t)} = \left[0.5 - 2\left(\frac{2}{\pi} M_v\right)^2 \left(\sum_{n=2}^{m} \alpha_n \sin(\gamma_n \omega_a t)\right)\right] \left(\sum_{u=2}^{v} \alpha_u \sin(\gamma_u \omega_c t)\right)$$

$$\overline{\Delta i_a(t)} = \frac{L_a \Delta i_a(t)}{V_d T_s} \quad \alpha_n = \frac{1}{2n-1} \quad \gamma_n = 2n-1 \tag{9}$$

$$\alpha_u = \frac{1}{2u-1} \quad \gamma_u = 2u-1$$

The maximum value of equation (9) is equal to 0.5. Therefore, the value of L_a can be determined by (10).

$$L_a = \frac{0.5\, V_d}{f_s\, \Delta i_{a\max}} \tag{10}$$

B. Transfer function $\Delta V_{ca}(s)/\Delta D(s)$

A way of deriving the transfer function $\Delta V_{ca}(s)/\Delta D(s)$ to the series active filter was presented in [7]. It can be noticed that the parasitic elements were neglected in that transfer function. Considering the unfavorable aspects of the digital technology a more complete equation is required to that transfer function.

So using the PWM switch model an equivalent circuit to series active filter was developed as illustrated in Fig. 4. From it several relationships can be derived and among them $\Delta V_{ca}(s)/\Delta D(s)$, i. e., the relationship between voltage and the duty cycle D. It is given by the expression (11).

$$\frac{\Delta V_{ca}(s)}{\Delta D(s)} = \frac{2V_d(sC_a r_{Ca}+1)}{s^2 L_a C_a + sC_a(r_{Ca}+r_{La}+2r_a)+1} \tag{11}$$

C. Transfer function $\Delta V_d(s)/\Delta V_{ca}(s)$

The average voltage at the DC bus line of the inverter must remain constant and this situation demands the use of a controller. In order to select a controller, the variation of voltage $v_d(t)$ as a function of the voltage variation across capacitor C_a must be known.

Again using the circuit of Fig. 4 and after solving its equations, the transfer function $\Delta V_d(s)/\Delta V_{ca}(s)$ is defined as shown by (12).

Equations (11) and (12) can be reduced to more simple expressions when some parasitic elements are neglected. They will be equal to those presented at [7].

$$\frac{\Delta V_d(s)}{\Delta V_{ca}(s)} = \frac{(2D-1)(sC_d r_{Cd}+1)}{s^2 L_a C_d + sC_d\left(r_{La}+r_{Cd}(2D-1)^2+2r_a\right)+(2D-1)^2} \tag{12}$$

D. Coupling capacitor C_a

The value of inductor L_a is determined according to the variation of the current ripple, which flows through it during a commutation period. Capacitor C_a can be calculated using equations (13).

$$v_{cae}(t) = X_{caeq}\, i_{cae}(t) \quad v_{cae}(t) = \frac{V_q}{\pi}\sqrt{(\pi^2-8)}$$

$$X_{caeq} = \sqrt{\frac{\sum_{n=2}^{m}\left(\frac{1}{2n-1}\right)^2}{(m-1)(\omega_1 C_a)^2}} \tag{13}$$

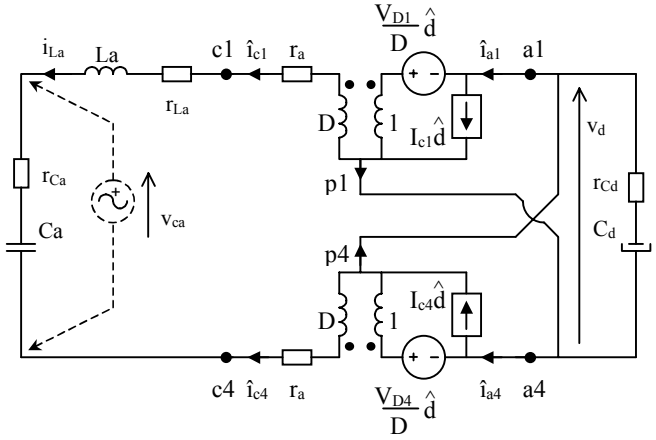

Fig. 4 Series active filter equivalent circuit using the PWM switch model.

E. Capacitor C_d

Admitting for Fig. 3a a linear load with impedance Z_o and after analyzing that circuit an expression to the DC bus line voltage is derived. Expression (14) represents the behavior of the $v_d(t)$ voltage.

$$v_d(t) = \sqrt{\begin{matrix} c_1(1-C) - c_2(-0.5CS+0.5u) + c_3 S \\ +(c_4+c_5-c_7)(C2-1) - c_6 S2 + V_d^2 \end{matrix}} \tag{14}$$

where:

$$C = \cos u \quad C2 = \cos 2u \quad S = \sin u \quad S2 = \sin 2u$$

$$c_1 = \sqrt{2}\frac{2V_q}{\omega C_d} I_1 \quad c_2 = \frac{8}{\pi}\sqrt{2}\frac{V_q}{\omega C_d} I_1 \quad c_3 = 8\frac{C_a}{\pi}\frac{V_q^2}{C_d}$$

$$c_4 = 8\frac{C_a}{\pi^2}\frac{V_q^2}{C_d} \quad c_5 = \frac{L_a}{C_d} I_1^2 \quad c_6 = 4L_a\frac{C_a}{\pi}\frac{V_q}{C_d}\omega\sqrt{2} I_1$$

$$c_7 = 8L_a\frac{C_a^2}{\pi^2}\frac{V_q^2}{C_d}\omega^2 \quad u = \omega t$$

The $v_d(t)$ voltage aspect and values depend on several parameters. Capacitor C_d is one of them. Thus for a given value of C_d, a certain variation of the voltage $v_d(t)$ will be observed.

IV. DESIGN AND NUMERIC SIMULATION RESULTS

A. Active filter design

An example of the project is described as follows, in which the main components of the active filter are determined, with VSI, which is used in the numerical simulations. The filter is projected to compensate for loads up to 1250W and has the following specifications: V_{sp} = 311 V, f = 60 Hz, V_d = 250 V, f_s = 20 kHz, Δi_{amax} = 25% I_{sp} and C_a = 4.7 μF, L_a = 3.11 mH. The transfer function is calculated using equation (11), but taken into consideration the digital approach used and applying the z-transform to (11) equation (15) is achieved.

$$G(z) = \frac{0.04629z + 0.04266}{z^2 - 1.947z + 0.9982} \quad (15)$$

The discrete transfer function of the chosen digital controller is given by (16). Equation (16) was determined using the root locus design.

$$D(z) = \frac{4.0z^2 - 3.2716z + 3.379528}{z^2 - 1.0z} \quad (16)$$

No special design procedure was used in this digital approach. It is recalled that the root locus system is a plot of the roots of the system´s characteristic equation as gain is varied. Thus the character of the transient response of a system is extracted from the root locus and the design procedure is to add poles and zeros via a digital controller so as to shift the roots of the characteristic equation to more adequate locations in the z-plane.

B. Numerical simulation results

A series active filter was prepared and simulated using Matlab® program. A resistive load with R = 30 Ω was connected to the active filter. The active filter could be tested with other types of loads. The inverter's power stage is made of switches S_1 to S_4, which are of MOSFET types. Fig. 5 presents simulation results related to the resistive load. The distorted voltage $v_s(t)$ at the AC mains port and the conditioning voltage $v_{ca}(t)$ are shown. The latter cancels the distortions of the input voltage, yielding a sinusoidal signal $v_o(t)$ over the R load, that is also presented in Fig. 5. The simulation results confirm the ability of the series active filter, under digital control strategy, to generate all required harmonic voltages to cancel the voltage source harmonics content.

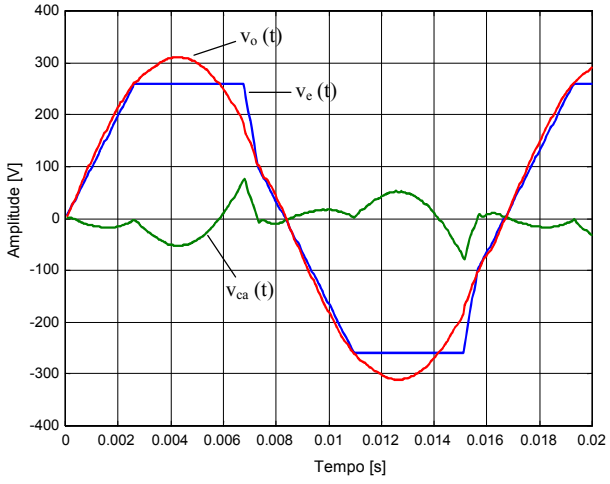

Fig. 5 - Simulation results related to the R-load.

V. EXPERIMENTAL RESULTS

In order to verify the principle of operation and the behavior of the digital control strategy, a 1250 W series active filter has been implemented. Its switching frequency is around 36 kHz. The power stage diagram of the prototype is similar to that shown in Fig. 2. Its parameters and components specifications are the following. V_s = 220 V_{rms}, V_{dc} = 160 V, switches S_1, S_2, S_3, S_4: IGBT modules SKM50GB063D, L_a = 3.17 mH, C_d = 470 µF, C_a = 4.7 µF, r_{La} = 0.09 Ω and r_{Ca} = 0.12 Ω. The digital controller was conceived using the root locus design method (Fig. 6).

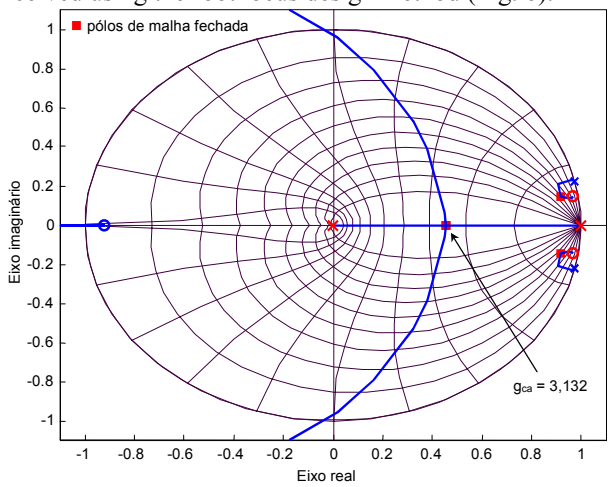

Fig. 6 - The series active filter root locus design.

From this method its equation was derived and it is given by expression (17).

$$D(z) = \frac{u(z)}{e(z)} = \frac{3.132z^2 - 6.0636z + 2.9984}{z^2 - 0.995z - 0.005} \quad (17)$$

To be used in a digital system, expression (17) is written as difference equation as it appears in expression (18).

$$u(k) = 0.995u(k-1) + 0.005u(k-2) + 3.132e(k) - 6.0636e(k-1) + 2.9984e(k-2) \quad (18)$$

The digital control system uses the digital signal processor TMS320F243. Fig. 7 presents the experimental result obtained from a series active filter connected between the AC source and the R load. Input voltage $v_s(t)$ presents a distortion. In the same figure, output voltage $v_o(t)$ and voltage $v_{ca}(t)$, produced by the coupling capacitor C_a, are also shown. The latter is responsible for reducing the harmonics present in the input voltage. The input and output voltages remained in phase. The filter did not introduce phase shifts between them.

According to the graphical aspect of the output voltage (Fig. 7), it can be said this voltage is better than the input voltage. To prove it, the harmonic content of these voltages was analyzed in quantitative terms. The result of this analysis is presented in Fig. 8.

Fig. 8a presents the harmonic spectrum of the input voltage $v_s(t)$. It presents a total harmonic distortion (THD = 2.76%). And the total harmonic distortion of the output voltage $v_o(t)$ (Fig. 8b), compared to the input voltage, is fewer (THD = 2.34%).

A load variation test was performed. The resistive load was suddenly changed from 40 Ω to 30 Ω. Its results are presented in Fig. 9. It shows the input and output voltages and the output current. One can see that the load variation did not cause disturbances on the voltage delivered by the series active filter.

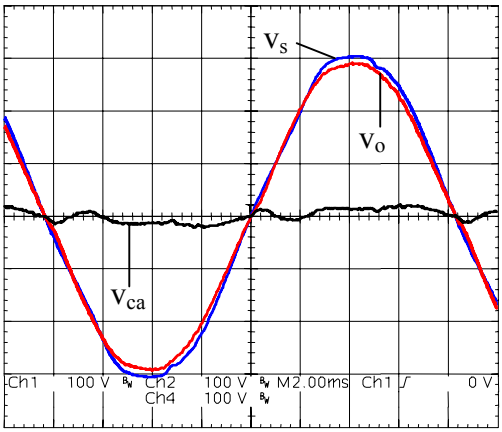

Fig. 7 – The input, output and capacitor Ca voltages (100 V/div., 2 ms/div.).

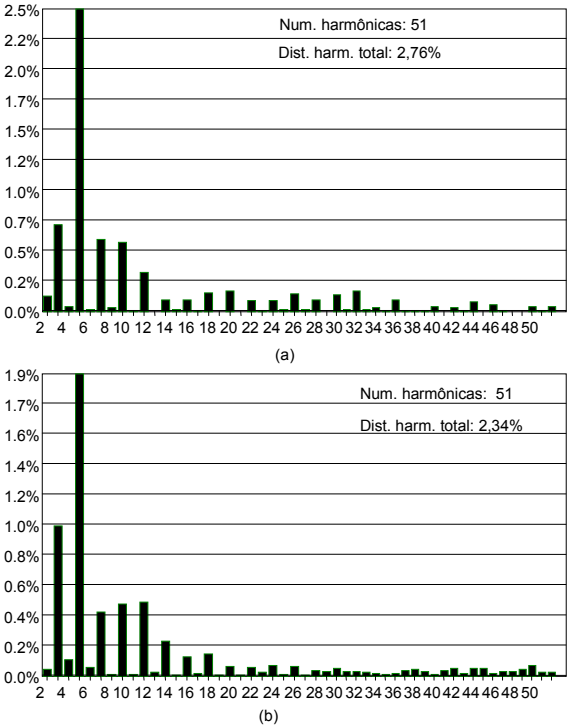

Fig. 8 The input voltage harmonics content (a); the output voltage harmonics content (b).

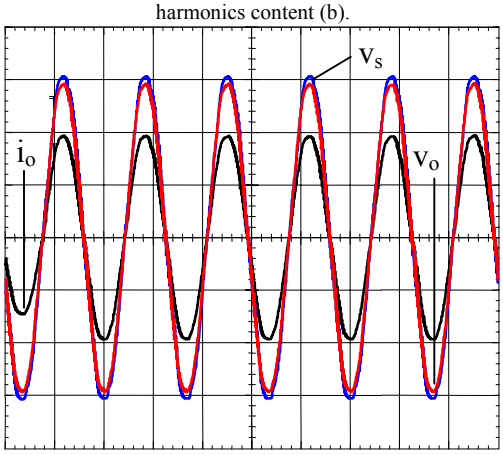

Fig. 9 - The input and output voltages (100 V/div., 10 ms/div.) and the output current (5 A/div., 10 ms/div.)

Fig. 10 presents the experimental result obtained from an active filter connected between the source and a R-L load. Input voltage $v_s(t)$, a distorted signal, is shown in Fig. 10. In the same figure, output voltage $v_o(t)$ and voltage $v_{ca}(t)$, produced by coupling capacitor C_a, are also shown. The latter is responsible for reducing the harmonics present in the input voltage. The input voltage and the output voltage remained in phase. The filter did not introduce phase shifts between these voltages.

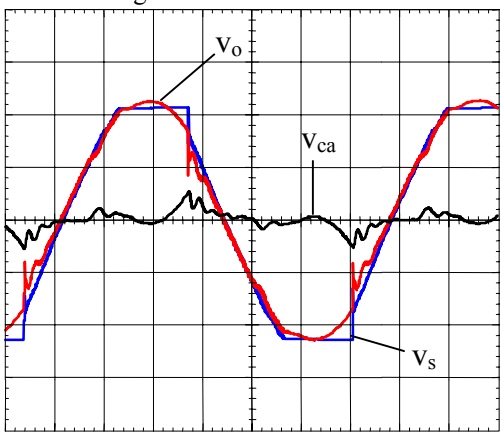

Fig. 10 – The input, output and capacitor Ca voltages (100 V/div., 2.5 ms/div.).

Analyzing the graphical aspect of the output voltage (Fig. 10), it can be said that this voltage is better than the input voltage. The harmonic content of these voltages was analyzed in quantitative terms. The result of this analysis is presented in Fig. 11.

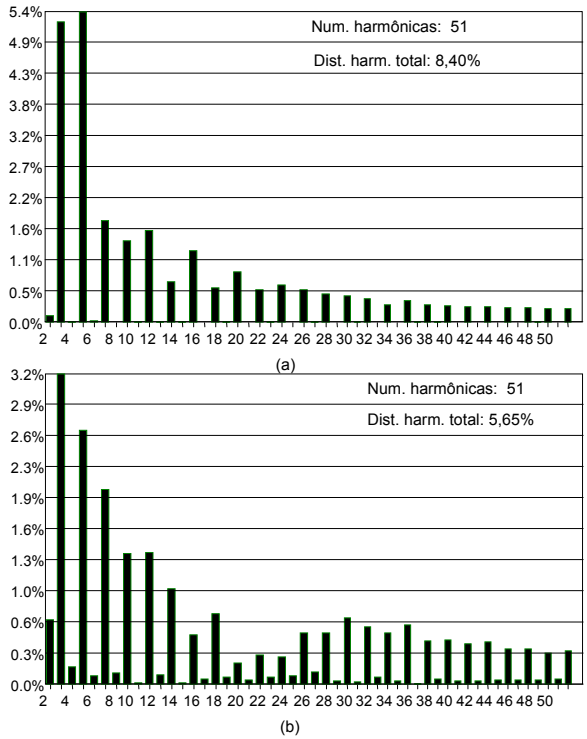

Fig. 11 The input voltage harmonics content (a); the output voltage harmonics content (b).

Fig. 11a presents the harmonic spectrum of the input voltage $v_s(t)$. Notice that this voltage presents a total harmonic distortion of 8.40 % (THD = 8.40%). On the other hand, the total harmonic distortion of the output voltage, $v_o(t)$, presented in Fig. 11b, compared to the input voltage, is smaller (THD = 5.65%). This situation illustrates the

performance of the proposed series active filter.

The input and output voltages ($v_s(t)$ and $v_o(t)$) and the output current, $i_o(t)$, are presented in Fig. 12. The output current, $i_o(t)$, is phase shifted approximately 35° in relation to the input voltage due to the R-L load type. Again a load variation test was performed. The resistive load was suddenly changed from 40 Ω to 30 Ω. Its results are presented in Fig. 13. It shows the input and output voltages and the output current. One can see that the load variation did not cause disturbances on the voltage delivered by the series active filter.

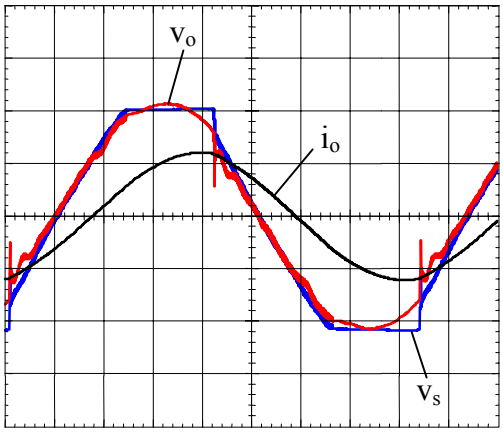

Fig. 12 – The input ($v_s(t)$) and output ($v_o(t)$) voltages (100 V/div., 2 ms/div.) and the output current $i_o(t)$ (2 A/div., 2 ms/div.).

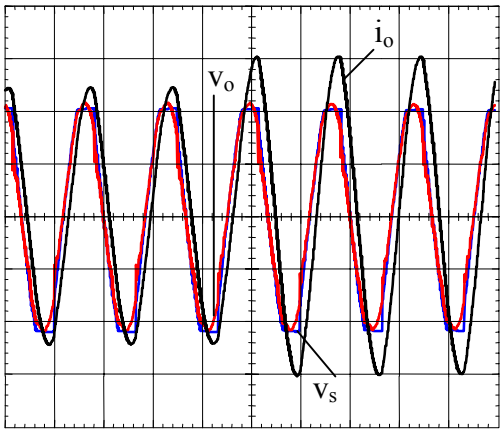

Fig. 13 - The input and output voltages (100 V/div., 10 ms/div.) and the output current (2 A/div., 10 ms/div.)

Fig. 14 shows the input, output and DC bus line voltages ($v_s(t)$, $v_o(t)$ and $v_d(t)$). A constant average voltage is maintained at the DC bus line of the inverter. The voltage $v_d(t)$ has a ripple part designated $v_{d(ca)}(t)$.

The graphical aspect of that voltage is different from that predicted by expression (14). But its amplitude remains around the limits given by (14) for the chosen capacitor C_d. Thus for both experiments the expression (14) gave a good direction to choose the capacitor C_d.

VI. CONCLUSION

The proposed series active filter acting as harmonic voltage compensator, its operating principle and its digital control strategy were presented. A set of its relevant equations was also described. A better waveform, from a distorted voltage source, was delivered to the load after being processed by the filter. The filter topology as well as its digital control strategy is quite simple. Experimental results were obtained and validate the theoretical analysis. The series active filter was tested with R and R-L loads.

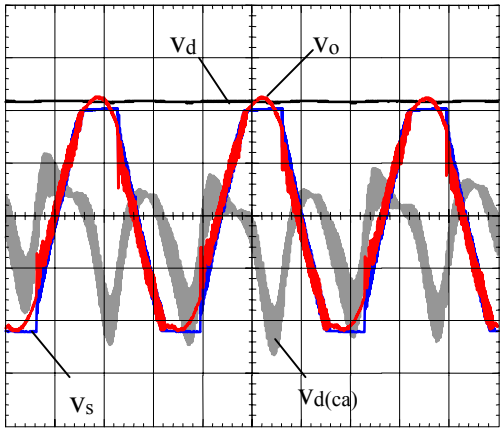

Fig. 14 – The input, output and capacitor C_d voltages: $v_s(t)$, $v_o(t)$ and $v_d(t)$ (100 V/div., 5 ms/div.). The ripple voltage $v_{dca}(t)$ (2 V/div., 5 ms/div.).

The results obtained using the analogue technology [7] are better than those obtained here. The digital approach adopted used so far in this work was the first step among several possibilities offered by the digital technology. Hence using the same hardware and taken into account the flexibility of the digital technology many others attempts will be carried out in order to get better results.

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