

THE IMPROVED ZVS-PWM ACTIVE-CLAMPING BUCK-BOOST CONVERTER

Vitor Mauro Fiori and Cláudio M. C. Duarte
UCPel - Catholic University of Pelotas
Engineering School - Electrical Engineering Course
P.O. Box 402 - FAX: (55) 53 2253105
96010-000 - Pelotas - RS - BRAZIL

vmf@atlas.ucpel.tche.br cmcd@atlas.ucpel.tche.br

Abstract – A new Buck-Boost converter featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches, is proposed to overcome the limitations of Clamped Mode Buck-Boost converter. The new converter is generated from an improved cell of ZVS-PWM active clamping dc-to-dc converters. As the resonant circuits absorb all parasitic reactances, including transistor output capacitance and diode junction capacitance, this converter is suitable for high-frequency operation.

Principle of operation, of the new converter, theoretical analysis, simulation and experimental results are presented, taken from a laboratory prototype rated at 500W, input voltage of 150V, output voltage of 50V, and operating at 100kHz.

KEYWORDS

DC/DC Converters; High Frequency; Soft Switching; Active-Clamping.

I. INTRODUCTION

In order to reduce size and cost of dc-to-dc converters it is necessary to increase the switching frequency. As the switching losses are directly depending on switching frequency it is necessary the use soft-switching techniques.

The Active Clamping technique [1,2] has the advantages of PWM modulation, soft-commutation (ZVS) on main switches and low voltage stresses due to the clamping action. Besides operating at constant frequency and with reduced commutation losses there is no significant increasing on circulating reactive energy that would cause large conduction losses.

The parasitic ringings caused by the interaction of the junction capacitance of the rectifier, in the clamped mode Buck-Boost converter (Fig. 1.a), and the resonant inductor (L_r) are eliminated by the inclusion of an auxiliary clamping diode [3], as shown in Fig 1.b, limiting the voltage stress on the rectifier to the output voltage plus input voltage. Although the voltage stress on the rectifier has been eliminated, by this approach, both D_b and D_c diodes still present hard switching commutation and the voltages across these devices still rise in a high dv/dt rate, which means compatibility electromagnetic problems and switching losses. This paper presents an improved Buck-Boost converter featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches. The

inclusion of capacitor C_D and clamping diode D_c [4], in the Buck-Boost converter, as shown in Fig. 1.b, results in reduced voltage dv/dt and soft-switching conditions for all switching devices, including diodes D_c and D_b . Therefore all parasitic reactances are absorbed, including transistor output capacitance and diode junction capacitance, resulting in high efficiency at high frequency operation without significant increasing in voltage and current stresses on switches.

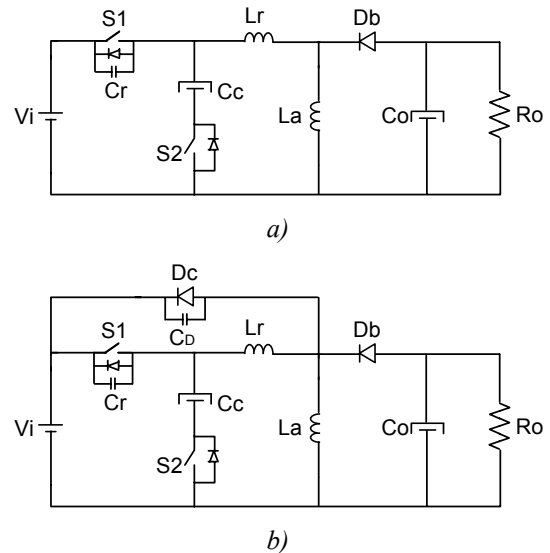


Fig. 1. Clamped mode Buck-Boost converters: - a) without D_c and C_D ; - b) with D_c and C_D .

II. OPERATION AND ANALYSIS OF THE BUCK-BOOST CONVERTER

To simplify the analysis, the output filter capacitance and L_a are assumed large enough to be considered respectively as constant voltage $V(C_o)=V_o$ and current source $I(L_a)=I_L$. The capacitor C_c is selected to have large capacitance so that the voltage $V(c)=V_c$, across these capacitor, could be considered as a constant one. The eight topological stages and key waveforms of the proposed Buck-Boost converter, to one switching cycle, are shown in Fig. 2 and 3 respectively. In those Figures it can be seen that the two switches are switched in a complementary way and soft-switching is achieved for all switches. The main switch S_1 is turned off at $t=t_0$, when the switching cycle starts.

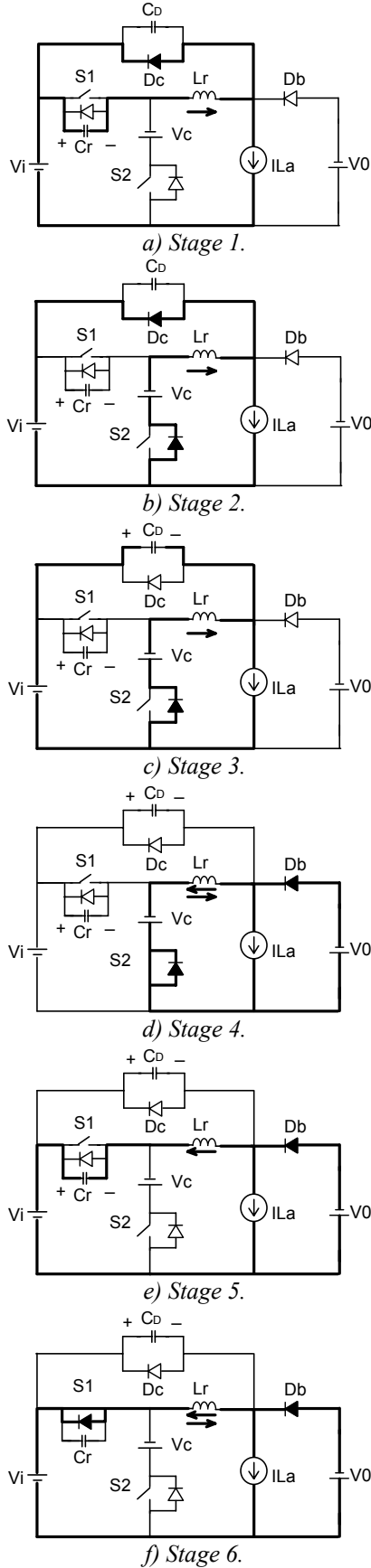
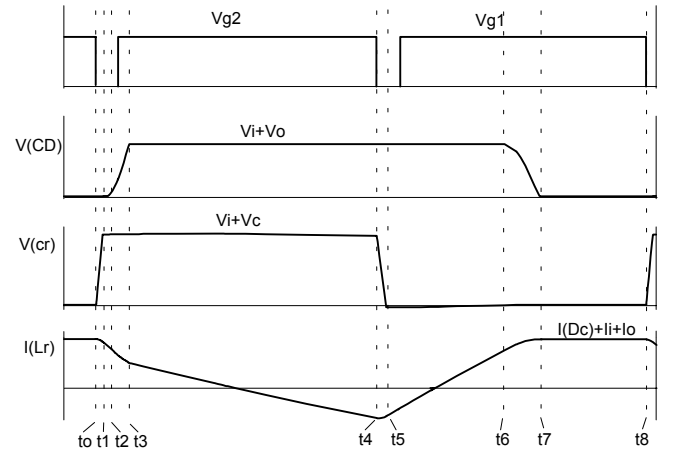


Fig. 2. Topological stages of Buck-Boost converter.



Prior to t_0 , the main switch S_1 is on, the auxiliary switch and diode D_b are off, while diode D_c is on. When S_1 is turned off, at $t=t_0$, the first stage has started, as shown in Fig. 2.a. The capacitor C_r is charged in a resonant way. When $V_{(cr)}$ reaches V_i+V_c , the antiparallel diode of S_2 starts conducting and this stage ends with voltage $V_{(cr)}$ clamped at V_c+V_i . In stage 2, the L_r current ramps down until reaches $I(L_a)=I_i+I_o$, when the clamping diode D_c becomes reversibly biased. When the clamping diode D_c ends conducting, the current through L_r decreases and the capacitor C_D is charged in a resonant way. When $V_{(CD)}$ reaches V_i+V_o , D_b becomes forward biased and starts conducting. In stage 4, the L_r current ramps down, because C_c is considered as a constant voltage source, until it reaches zero, when it change its direction and rises again. When the antiparallel diode of S_2 is conducting, the auxiliary switch S_2 should be switched on to achieve a soft-switching turn-on. This stage ends when S_2 is turned off at $t=t_4$. The voltage across C_r falls, due to the resonance between L_r and C_r , until

it reaches zero at $t=t_5$. This stage ends when $V_{(cr)}$ becomes null and the antiparallel diode of S1 begins conducting. In stage 6, S1 is turned on in a soft-switching way (ZVS), because $V_{(cr)}$ became null. The current through L_r changes its polarity and ramps up to reaches (I_i+I_o) at $t=t_6$. Then the diode D_b becomes reversibly biased and turns off. When diode D_b is turned off, capacitor C_D and inductor L_r begin resonate. The voltage across C_D reduces to zero and current through L_r rises. This stage ends when voltage across C_D becomes null and the clamping diode D_c becomes forward biased. At $t=t_7$, the diode D_c is conducting and the current through L_r is clamped at $I_o+I_i+I_{(DC)}$. The diode D_b is reversibly biased and power is not transferred to the load. This stage ends when S1 is turned off at the end of the switching cycle.

III. THEORETICAL ANALYSIS

As the resonant time intervals of stages 1 and 5 are so small when compared with the duration of stages 2,3,4,6,7 and 8 it is possible to obtain the dc voltage gain from an simplified analysis regardless those resonant time intervals. So, we have:

$$q = \frac{V_o}{V_i} \quad (01)$$

$$\beta = \frac{V_c}{V_i} \quad (02)$$

$$\omega_2 = \frac{1}{\sqrt{L_r C_D}} \quad (03)$$

and,

$$\Delta t_4 = (t_4 - t_3); \quad \Delta t_3 = (t_3 - t_2); \quad \Delta t_2 = (t_2 - t_1) \quad (04)$$

$$\frac{\Delta t_4}{T_s} = (1-D) - \frac{1}{\omega_2 T_s} \left[\frac{1+q}{1+\beta} + \cos^{-1} \left(1 - \frac{1+q}{1+\beta} \right) \right] \quad (05)$$

$$\frac{\Delta t_3}{T_s} = \frac{1}{\omega_2 T_s} \cos^{-1} \left(1 - \frac{1+q}{1+\beta} \right) \quad (06)$$

$$\frac{\Delta t_2}{T_s} = \frac{1}{\omega_2 T_s} \frac{1+q}{1+\beta} \quad (07)$$

$$A = \sqrt{\frac{(1+\beta)^2 - (\beta-q)^2}{(1+q)^2}} \cdot \frac{\Delta t_4}{T_s} \quad (08)$$

$$B = \frac{\omega_2 T_s}{2} \cdot \frac{(\beta-q)}{(1+q)} \left(\frac{\Delta t_4}{T_s} \right)^2 \quad (09)$$

$$C = \frac{1}{\omega_2 T_s} \left[\frac{(1+q)}{2(1+\beta)} - 1 \right] \quad (10)$$

$$L_n = \frac{1}{\omega_2 T_s (1-D)} \{A + B - C\} \quad (11)$$

Where q is the dc voltage gain, D is the duty cycle and L_n is the normalized load current.

$$L_n = \frac{L_r I_o}{V_i T_s} \quad (12)$$

From this simplified analysis it is possible to obtain the normalized clamping voltage (β) as:

$$\beta = \frac{D}{(1-D)} \quad (13)$$

The dc voltage gain and the normalized clamping voltage, as a function of normalized load current are shown in Fig. 4.

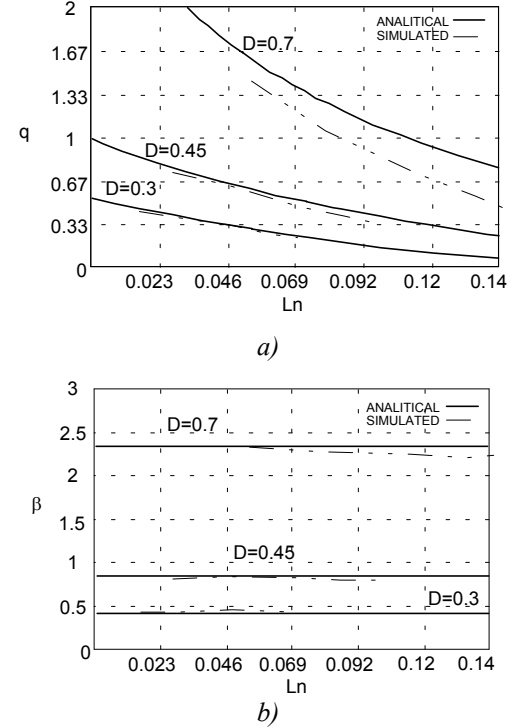


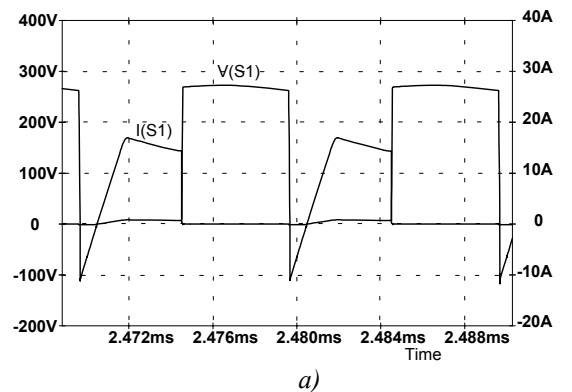
Fig. 4: (a) DC voltage gain; (b) Normalized clamping voltage.

IV. SIMULATION RESULTS OF THE PROPOSAL BUCK-BOOST CONVERTER

The new Buck-Boost converter was simulated with the following specifications: output power $P_o=500W$; input voltage $V_i=150V$; output voltage $V_o=50V$; switching frequency $f_s=100kHz$. The power stage consisted of the following parameters:

$$D = 0.45 \quad \beta = 0.82 \quad L_r = 15\mu H \quad C_r = 2.6nF \\ C_c = 3.6\mu F \quad C_D = 3nF$$

Simulation obtained waveforms of the switches current and voltages can be seen in Fig. 5 a and b.



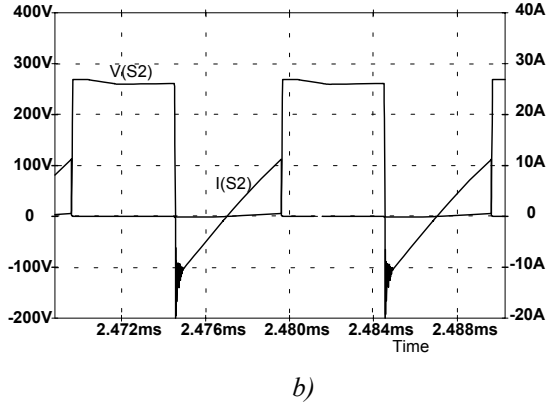


Fig. 5. a) Voltage across S_1 and current through S_1 ; b) Voltage across S_2 and current through S_2 .

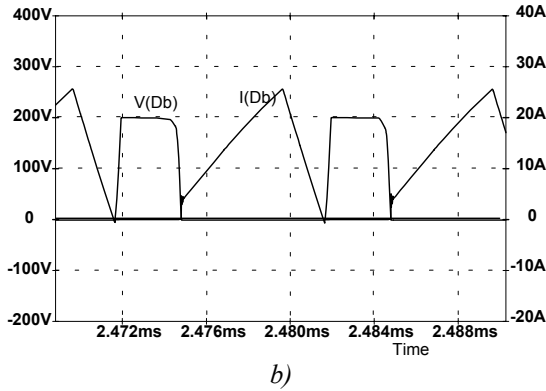
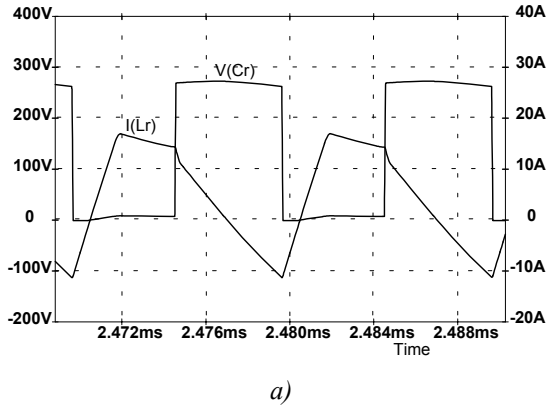


Fig. 6. a) Voltage across C_r and current through L_r ; b) Voltage across D_b and current through D_b .

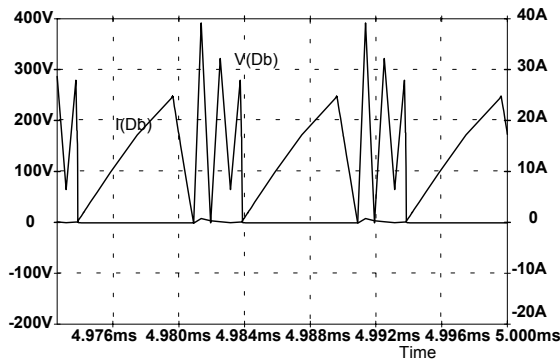


Fig. 7. Voltage across D_b and current through D_b for Buck-Boost converter of Fig. 1.a.

The waveforms of Fig. 5 and 6 agree with those predicted theoretically, and as it can be noted, the main switches (S_1 and S_2) and diodes (D_b and D_c) present ZVS commutation with clamped voltages.

The Buck-Boost converter shown in Fig. 1.a was simulated, under the same conditions of the proposed converter, at Fig. 7 we can see the oscillations in $V(D_b)$. In this case, it is necessary the presence of a dissipative clamping circuit.

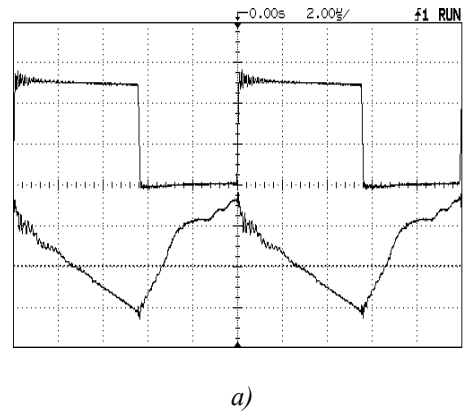
By comparing the waveforms of Fig. 6.b and 7 it is possible to conclude that the new converter has advantages in relation to the conventional Clamped Mode Buck-Boost converter, because, besides it presents less voltage oscillations, it doesn't need a dissipative clamping circuit.

V. EXPERIMENTAL RESULTS

The new Buck-Boost converter was implemented, with the following specifications: output power $P_0=500W$; input voltage $V_S=150V$; output voltage $V_0=50V$; switching frequency $f_s=100kHz$. The power stage consists of the following parameters:

- switches S_1 and S_2 : power MOSFET's IRFP460;- diode D_b : RURP3060;- diode D_c : RURP3060 - extern resonant capacitor C_D : 3000pF/400V- extern resonant capacitor C_{ext} : 3700pF/400V;- capacitor C_C : 100μF/400V;- output filter C_f : 200μF/400V;- resonant inductor L_r : 15μH, core (E-30/7)-Thornton;- inductor L_a : 1000μH, core (E-65/39) Thornton.

Experimentally obtained waveforms of the switches drain-to-source voltages and the resonant inductor current are shown in Fig. 8 and the voltage across diodes D_b and D_c and the current through L_r are shown in Fig. 9. These waveforms agree with those predicted theoretically and, as it can be noted from the waveforms shown in Fig. 8, the main switches (S_1 and S_2) present ZVS commutation with clamped voltages. From Fig. 9, it is possible to note that the diodes present ideal commutation conditions.



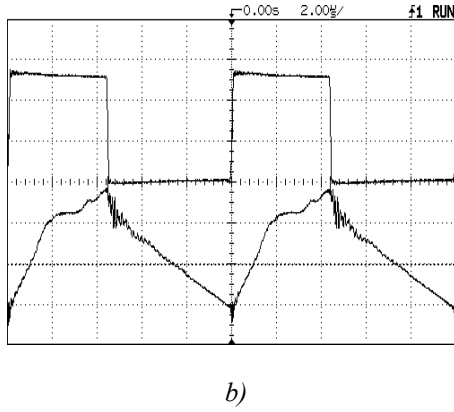


Fig. 8. a) Drain-to-source voltage across main switch S_1 and current through L_r ; b) Drain-to-source voltage across switch S_2 and current through L_r (voltage: 100V/div; current: 10A/div; time scale: 2μs/div).

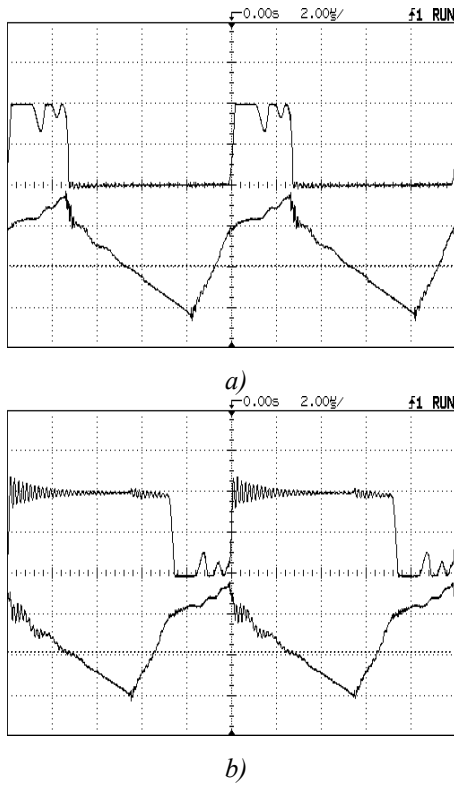


Fig. 9. Voltages across D_b (a) and D_c (b) and current through L_r (a) and (b) (voltage: 100V/div; current: 10A/div; time scale: 2μs/div).

In Fig. 10, the DC voltage gain as a function of output current is shown, for different duty cycles. In Fig. 11, the efficiency measurement, as a function of the output power, of the new Buck-Boost converter is shown in comparison with the ZVS-PWM Active-Clamping Boost converter. The converter's efficiency were measured, at the same input and output data, and the converters operating at the same switching frequency (100kHz). The experimentally obtained efficiency from the new ZVS-PWM boost converter is equal to 92%, and from the ZVS-PWM Active-Clamping Boost converter, it is equal to 90%, for rated load.

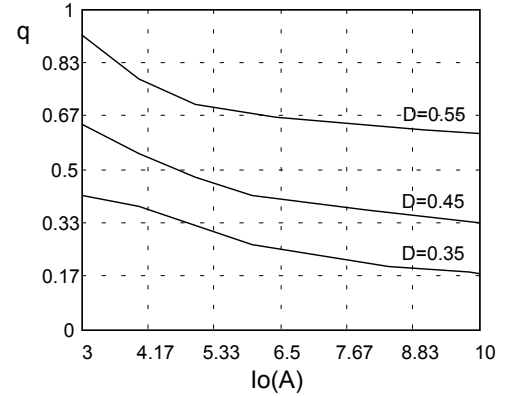


Fig. 10. DC voltage gain with different load conditions and duty cycle.

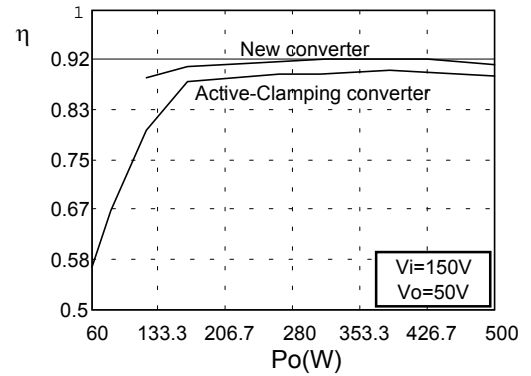


Fig. 11. Experimental efficiency curves with constant output and input voltage.

VI. CONCLUSION

A new Buck-Boost converter featuring clamping action, PWM modulation and soft-switching (ZVS) in both active and passive switches is proposed to overcome the limitations of clamped mode Buck-Boost converter. As the resonant circuits absorb all parasitic reactances, including transistor output capacitance and diode junction capacitance, that new converter operate with favorable switching conditions in all switching devices. Therefore, that converter is suitable for high-frequency operation.

VII. REFERENCES

- [1] C.M.C. Duarte and I. Barbi, "A Family of ZVS-PWM Active-Clamping DC-to-DC Converters: Synthesis, Analysis, Design, and Experimentation," in *Proc. INTELEC*, 1995, pp. 502-509.
- [2] C.M.C. Duarte and I. Barbi, "A New Family of ZVS-PWM Active-Clamping DC-to-DC Boost Converters: Synthesis, Analysis, and Experimentation," in *Proc. INTELEC*, 1996, pp. 305-312.
- [3] M. Jovanovic, "A Technique for Reducing Rectifier Reverse-Recovery-Related Losses in High-Voltage, High-Power Boost Converters," in *Proc. APEC*, 1997, pp. 1000-1007.
- [4] C.M.C. Duarte and I. Barbi, "An Improved Family of ZVS-PWM Active Clamping DC-DC Converters," *IEEE Transactions on Power Electronics*, January 2002.