ASD VOLTAGE SAG RIDE-THROUGH IMPROVEMENTS: COMPUTATIONAL ANALYSIS

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***Abstract*—Amongst the various power quality phenomenons, voltage sag appears to be one of the most relevant types of disturbance. This loss of quality may affect quite a variety of devices, being the Adjustable speed drives (ASD) recognized sensitive equipment to this kind of problem. This device dependence on Power Quality problems can be attributed to the use of a highly sensitivity protection philosophy to prevent the equipment from high cost damages. Typical voltage sag occurrences may cause the frequency converter to completely shutdown with consequent loss of production and other undesired effects. To prevent this, some strategies can be used to improve the overall system/converter/load performance. Some are quite simple while others involve more complex solutions. By using a comprehensive supply and ASD models into the time domain SABER simulator, studies are carried out to illustrate the converter performance under voltage sag conditions with and without the inclusion of two ride-through improvement strategies. Computational results associated with a commercial type of VSI-PWM unit are given to clarify the work and the equipment sensitivity improvement.**

KEYWORDS

ASD, power quality, ride-through capability, computational simulation.

I. INTRODUCTION

The use of Adjustable Speed Drives (ASD's) [1,2] in industrial plants, commercial facilities and even in residences has significantly increased. The voltage source inverters (VSI) with pulse width modulation control (PWM) emerge as the most common type of converter. Despite several advantages, VSI-PWM converters are susceptible to electric power quality disturbances such as voltage sags. This dependence may even lead the equipment to a complete shutdown operation and the corresponding side effects [3]-[6]. As voltage sags express the majority of power system disturbances they can be responsible for the majority of industry process interruptions [7].

On the investigation of drive trip out causes, it is found that the control and the protection unit operation are the main reasons for the equipment shutdown. Usually, the mechanism involved is [8]:

- The drive controller or protection detects a sudden change in operating conditions and trips the drive to prevent damage to the power electronic components. Tripping of the drive is mainly related to the dc-bus undervoltage protection;
- The increased input ac currents during the sag or the post-sag situation may cause overcurrent enough to trip or even blows the fuses;
- The process may not be able to tolerate the motor drop in speed or the torque variations due to the sag.

In order to prevent the above problems, this paper aims to present practical strategies to be used under voltage sag conditions, so that to improve the ride-through capability of ASD performance. Two methods are focused [9]:

- Modifications on existing ASD topologies;
- Boosting the V/Hz Control strategy.

The first utilises an additional capacitor to provide energy to stand the instantaneous voltage drop [10], the second makes use of concepts associated to DC voltage drop compensation by increasing the Volts/Hertz relationship during voltage sag occurrences [11].

Besides the concepts, the investigations are carried out using a comprehensive ASD time domain model implemented into a computer program named as SABER simulator. The overall supply system, frequency converter, ac motor, load performance and the ride-through capability improvement are then fully considered.

II. VSI-PWM FREQUENCY CONVERTER MODEL

Fig. I shows the general VSI frequency converter power units. It can be seen that a non-controlled rectifier, a DC busbar and the inverter itself are the main parts. The input is a three-phase feeder derived from the AC supply. Non-ideal supply conditions such as: voltage sag, swell, distortion, unbalance, amongst others, could be individually or simultaneously represented. The output corresponds to the three-phase voltage applied to the induction motor associated with the load.

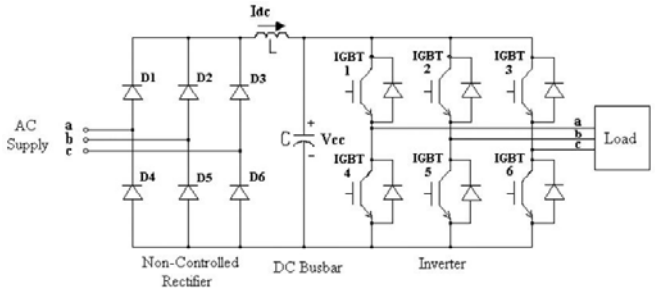

FIGURE I
General power units forming the Supply-Converter-Load

To represent the overall system the following models are used [12]:

- AC supply - This is modelled by three-phase voltage sources behind impedances to represent the local short-circuit level. Any non-ideal condition associated with power quality degradation can be easily included;
- Rectifier - Using the Saber internal components library, a 6-pulse diode rectifier template is obtained. The necessary protection components such as snubber circuits and others were included. The diodes are of commercial type;
- DC busbar - This comprises a combination of inductors and capacitors already available from the software library;
- Inverter - The DC to AC unit is again represented by internal commercial power transistors offered by the software library. The control strategy is included in this unit;
- Load - This is a three-phase induction motor supplying a mechanical load. The motor was fully represented by independent three-phase models in accordance with reference [13].

For simulation purposes, a practical system was considered. The main data set is given in table I.

TABLE I
Simulated system parameters

Type	Characteristics
AC Supply	Ideal three-phase balanced, non-distorted voltage of 380V (RMS phase-phase) with an internal impedance defined by R=0,7Ω and L=0,05mH.
Frequency Converter	Sinusoidal PWM control, with 4,1kVA, switching frequency of 4kHz, with a DC link inductance of 0,1mH and a DC capacitance of 330μF.
Induction Motor	Three-phase, squirrel type, 3HP, 4 poles, 60 Hz, rs=3,31Ω, xs=2,34Ω, rr=2,29Ω, xr=3,50Ω, xm=83,18Ω, load corresponding to 75% of the rated value.

III. ASD PERFORMANCE UNDER VOLTAGE SAG CONDITIONS

Figs. II to VI are related to the drive operation waveforms during three-phase balanced voltage sag occurrence. The phenomenon studied leads to a final voltage level of 80% lasting for 30 cycles. As a balanced disturbance was considered, only a single line-to-line voltage (v_{ab}) and a line current (i_a) are illustrated.

The applied supply voltage and the input current under the above phenomenon are shown in figures II and III.

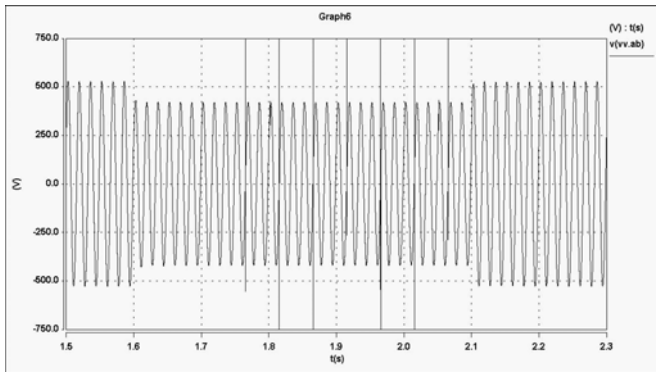

FIGURE II
Voltage Supply Waveform (v_{ab})

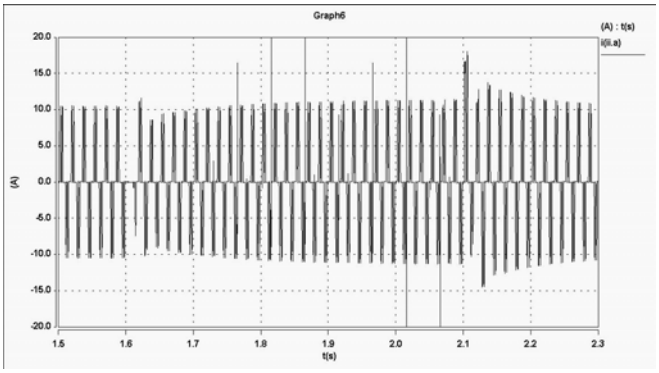

FIGURE III
Input Current (i_a)

At the start of the sag, the current initially drops to zero. This situation is maintained whilst the supply voltage level is less than the capacitor voltage. Under this condition, the diodes of the rectifier are reversed polarised, causing the line current blocking. According to figure IV, this effect carries on up to the time the capacitor voltage is proportional to the ac supply voltage level. For the remaining period, a balance is achieved and this allows the current to be re-established with a higher peak value.

At the end of the sag, high peak currents are again found on the supply. This can damage the rectifier components and/or activate the converter protection. The sudden change on the capacitor voltage is the reason for this occurrence, as seen in figure IV.

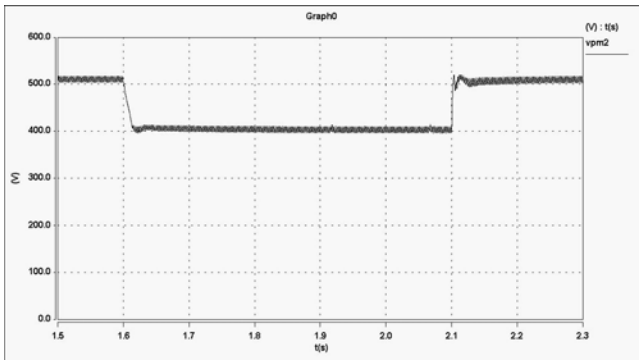

FIGURE IV
DC busbar voltage (v_{DC})

If no ride-through solution is included, figures V and VI show the voltage sag effect transference to the converter output. In figure V the effect upon the converter output voltage is shown. As expected, the relationship between the output RMS voltage after the supply voltage sag and during this disturbance is 80%.

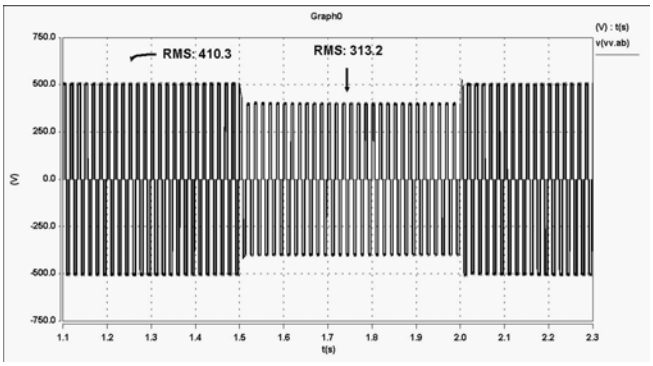

FIGURE V
Output voltage (vab)

Fig. VI shows the motor current waveform. The voltage recovery produces high peak currents, which may damage inverter components and, to prevent this, the protection may trip the equipment.

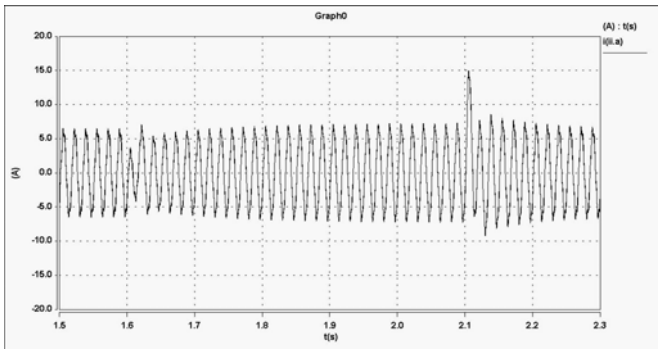

FIGURE VI
Output Current (i_a)

To exemplify the DC busbar protection and the equipment being tripped, results related to voltage sag of 75% lasting for about 10 cycles are presented in figures VII and VIII. Figure VII gives the corresponding DC voltage and figure VIII the associated output voltage.

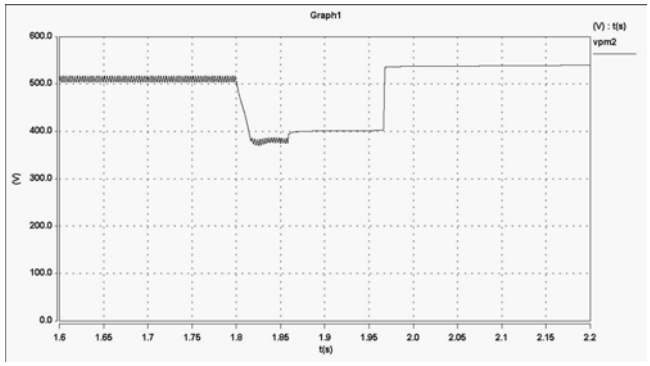

FIGURE VII
DC Busbar Voltage (v_{DC})

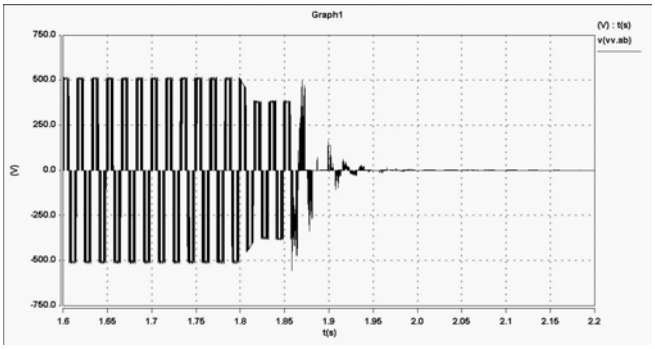

FIGURE VIII
Output Voltage (v_{ab})

In figure VII the trip event can be seen and figure VIII makes clear that the equipment is subjected to a complete shutdown.

IV. ASD RIDE-THROUGH METHODS: CONCEPTS AND COMPUTATIONAL PERFORMANCES

In order to improve the ASD performance, two ride-through strategies are considered:

- DC busbar capacitance reinforcement;
- Boosting the V/Hz Control Strategy with and without transformer tap adjustment.

IV.1. DC busbar capacitance reinforcement

This approach consists of increasing the DC busbar capacitor. According to (I), the required capacitance to overcome the ac voltage sag occurrence during a certain time interval can be obtained by applying equation (I).

$$C_{new} = \frac{2P}{\left[V_{DC}(0)\right]^2 - \left[V_{DC\min}\right]^2} t_{\max} \qquad \text{(I)}$$

Where:

P	-	Motor load power
$V_{DC}(0)$	-	Pre-sag DC voltage
$V_{DC(min)}$	-	Minimum value required for the DC voltage during sag conditions
t_{max}	-	Maximum time interval to reach V_{DCmin}.

Using the previous system data and considering:

P=2280[W], $V_{DC}(0)$=510[V], $V_{DC}(min)$=400[V] and t_{max}=166[ms].

Equation (1) leads to a capacitor of 6.67mF to match the requirements. Figure IX shows the new drive input current under the DC capacitor reinforcement. Comparing figures III and IX, similar transients may be detected at the instant the supply voltage recovers. However, as expected, the larger the capacitor, the higher the transient peak current after voltage sag elimination.

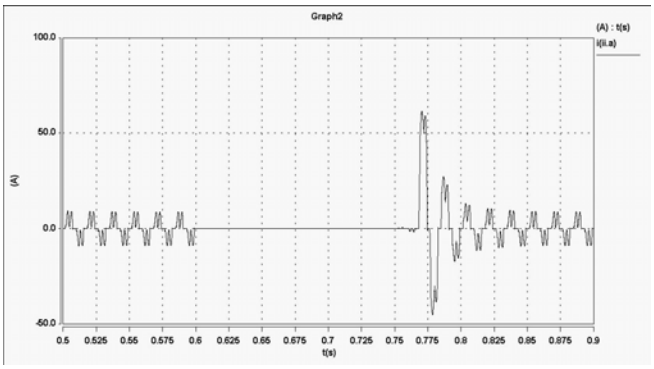

FIGURE IX
Input Current (i_a)

The DC busbar voltage related to the capacitor increase can be seen in Fig. X. The voltage performance is in accordance with the theory, as predicted by equation (I).

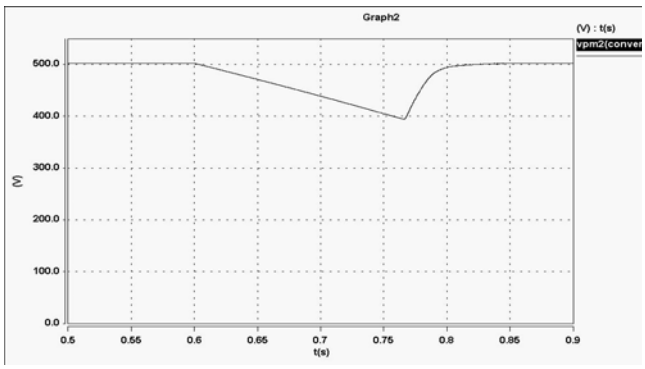

FIGURE X
DC busbar Voltage (v_{DC})

Fig. XI shows the motor supply voltage. Comparing figures VIII and XI the improvement associated with this ride-through strategy becomes quite evident.

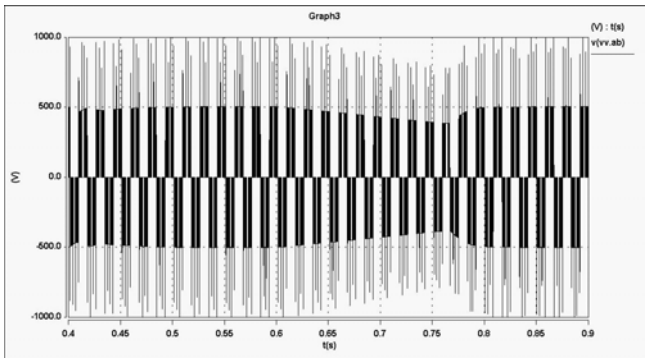

FIGURE XI
Output Voltage (v_{ab})

IV.2. Boosting the V/Hz Control Strategy

Another approach to improve the drive performance utilises an advanced hardware modification. In this study, the additional dc link energy has been utilised without any extra energy supply. Modifications on the Volts per Hertz circuit have been implemented so that during the voltage sag, speed loss has been minimised [11].

Fig. XII shows the circuit to be used. It can be seen that there are two Operational Amplifier stages. The first provides a linear relationship with the DC link voltage. The second corresponds to a comparator circuit used to compare the incoming DC link voltage level to an established voltage. This unit generates the final pulse voltage to compensate for the voltage sag occurrence.

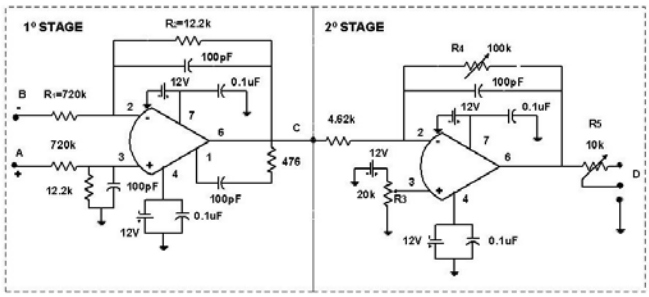

FIGURE XII
Drives Volts/Hertz compensation circuit

This strategy investigation, as given below, will be split into two further possibilities. The first does not take into account the transformer tap adjustment, and the second, includes this alternative.

- *Results without transformer tap adjustment*

Fig. XIII shows the output voltage with the boost circuit effect without considering any previous transformer tap selection. The output voltage during sag conditions was 313V (figure V) and under the boosting action it goes up to 326V (figure XIII). The effectiveness may be considered low. This can be attributed to the small voltage area availability to promote a proper compensation. Neverthless, the effect of the V/Hz circuit can be easily seen.

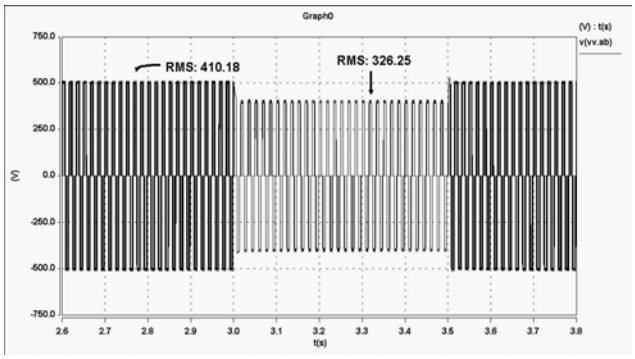

FIGURE XIII
Output Voltage (v_{ab})

To provide a better physical behaviour understanding of the boosting effectiveness, figures XIV and XV represent the output voltage zoom during the boosting. The original voltage (figure XIV) with no compensation is included for comparison purposes.

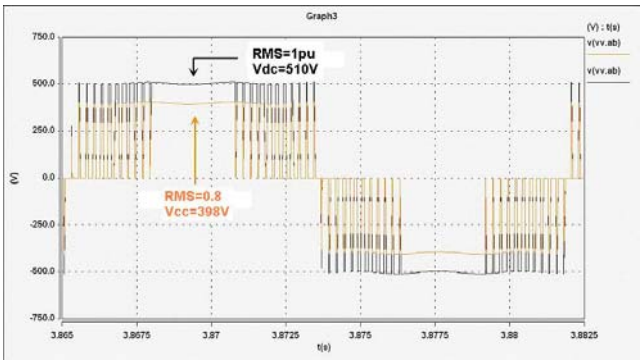

FIGURE XIV
Output voltage with no V/Hz boosting - Zoom

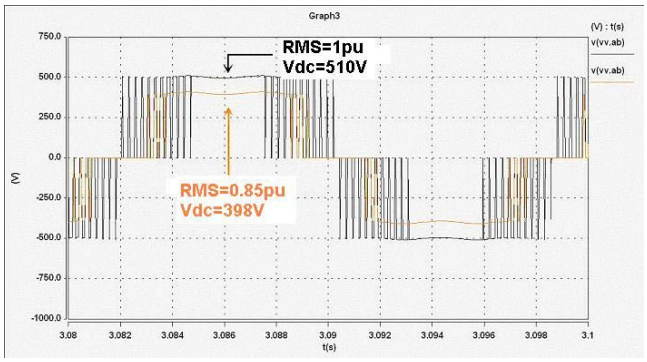

FIGURE XV
Output voltage with V/Hz boosting - Zoom

- *Results with transformer tap adjustment*

In this case, the ASD feeding transformer tap has been previously set so as to produce a higher secondary voltage than the one used before. This selection must be carefully made so as offer the boosting circuit a larger range of voltage compensation for the level of sag that may occur in the supply system. For the given example, the 380V was adjusted to 460V. For normal conditions, the new voltage is compensated by the PWM modulation so as to keep the same previous RMS for the output voltage. This can be seen in figure XVI. After sag occurrence, leading to 80% of rated value, during 30 cycles, it can be noticed the output RMS voltage is now 389V (the previous value was 326V). This clarifies the methodology efficiency.

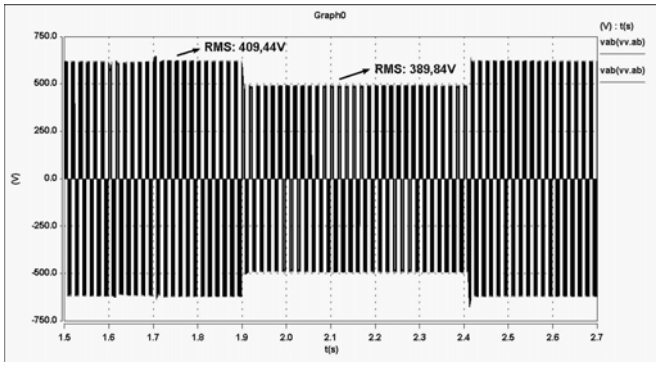

FIGURE XVI
ASD v_{ab} output voltage with boosting and transformer tap selection

Figure XVII gives further details related to the strategy here considered. It is possible to see that the output voltage produces a much better RMS value than before. The new value for 80% of rated voltage is now 0.95 pu (it was 0.8 pu with no tap adjustment).

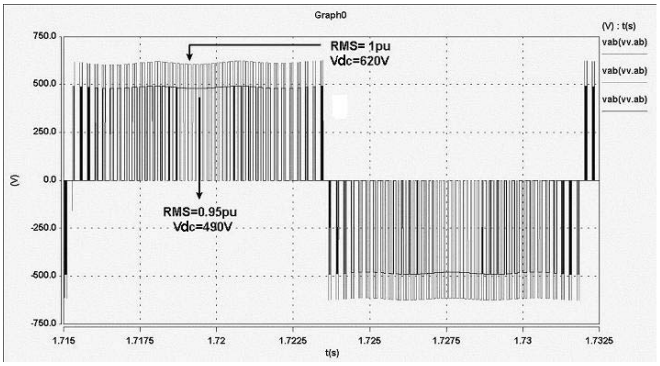

FIGURE XVII
Output voltage with V/Hz boosting and transformer tap selection – Zoom

V. CONCLUSIONS

The potential of the ASD model as well as the power of two methods to improve the equipment performance under voltage sag conditions were fully described throughout computational studies. Thought the converter model efficiency was validated in reference [12], the ride-through approaches require further investigations using laboratory experiments. The authors are carrying this out.

In a general way, it could be stated the strategies showed to be effective. Economical aspects as well as physical area limitations should dictate the more suitable solution for specific needs.

The classical inclusion of additional capacitor on the DC busbar was the first to be considered. This proposal has been

recommended for many applications and appears to be the simplest way of obtaining the required converter immunity improvement to voltage sag. The effectiveness related to this was shown to depend directly on the capacitor bank size.

The use of V/Hz boosting seems quite attractive. However, to achieve better results, it requires normal voltage operation control to be revaluated and appropriated set up. Besides, there is need for additional hardware/software.

The implementation of any solution will naturally be accompanied by extra costs. However, the gain in reliability may largely compensate for this afford.

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