

A Three Level Double-Ended Forward Converter

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ABSTRACT - A new four-switch converter topology is presented. This topology is intended for use in high input voltage (900V-1200V) and low power applications (@ 150W), specially auxiliary power supplies. Its main advantage is the off-voltage stress reduction on the switches at half of the input voltage. It works in a similar way like the classical double-ended forward converter. The four switches can be set on with the same gate pulse, with a small delay time in the off signal of the internal switches after the external ones. This position prevents direct short circuit in the DC link. This reliability and the simplicity of the way it is commanded, makes this converter very suitable for auxiliary power supplies applications. This digest presents the principle of operation of the proposed converter. Each stage with the main characteristics, and the main equations are also presented. Consistent simulation results with a project example are showed. Experimental data shows the suitability of the proposed converter.

I. INTRODUCTION

In telecommunication energy systems, or motor drive applications, the power supply is commonly composed by a power factor correction rectifier (ac-dc converter). To achieve power factor correction (PFC), the topology generally used is the boost rectifier, which presents an output voltage greater than the peak of the AC input voltage. This kind of converters encloses, usually, auxiliary supplies connected at the DC link. These auxiliary sources must start up before anything in the power supply system.

Most of the popular topologies used in auxiliary supplies present as a drawback the off-voltage stress over the main switch [1]. This voltage is twice the input voltage of the converter (e.g. flyback, forward). As one answer to the investigation on reliable converters, that also reduce the off-voltage stress on the switches, and that could be implemented with relative simplicity, the three level forward converter is stated [2, 4, 5, 6].

II. THE DC-DC THREE LEVEL FORWARD CONVERTER

A. Circuit description

The three level forward converter proposed in this paper is shown in Fig. 1. The S1, S2, S3 and S4 MOSFETs indicate the four switches. The input capacitors with the voltages V_{C1} and V_{C2} split the input voltage E . The clamping diodes D_{C1} and D_{C2} certify the voltage on the switches S_1 and S_4 to be half of the input voltage. The diodes D_1 and D_2 permit the core reset on the input supply. L_m indicates the magnetizing inductance.

The output stage is composed by the rectifiers diodes D_{O1} and D_{O2} . The output filter is indicated by L_O and C_O . The resistance R_O represents the load.

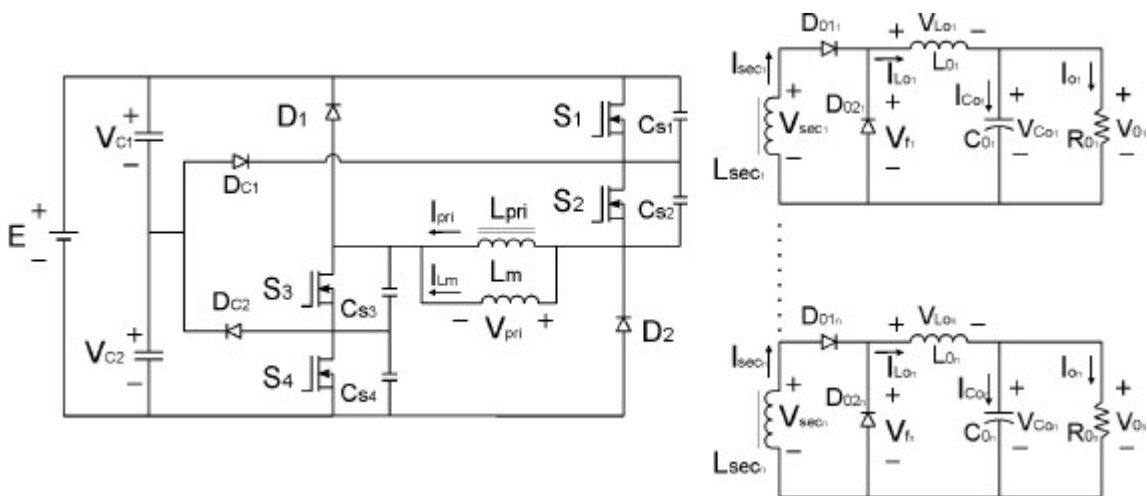


Fig. 1 – Three level forward converter with 'n' outputs.

B. Principle of operation

To simplify the analysis some suppositions are made: 1) the circuit operates in steady state; 2) all power semiconductors are ideal; 3) the intrinsic capacitances of the

MOSFETs are equal and constants, and are indicated by C_{S1} , C_{S2} , C_{S3} and C_{S4} .

The seven stages of operation are presented in Fig. 2. The main waveforms that correspond for each stage can be observed in Fig. 3. The operation is described as follows:

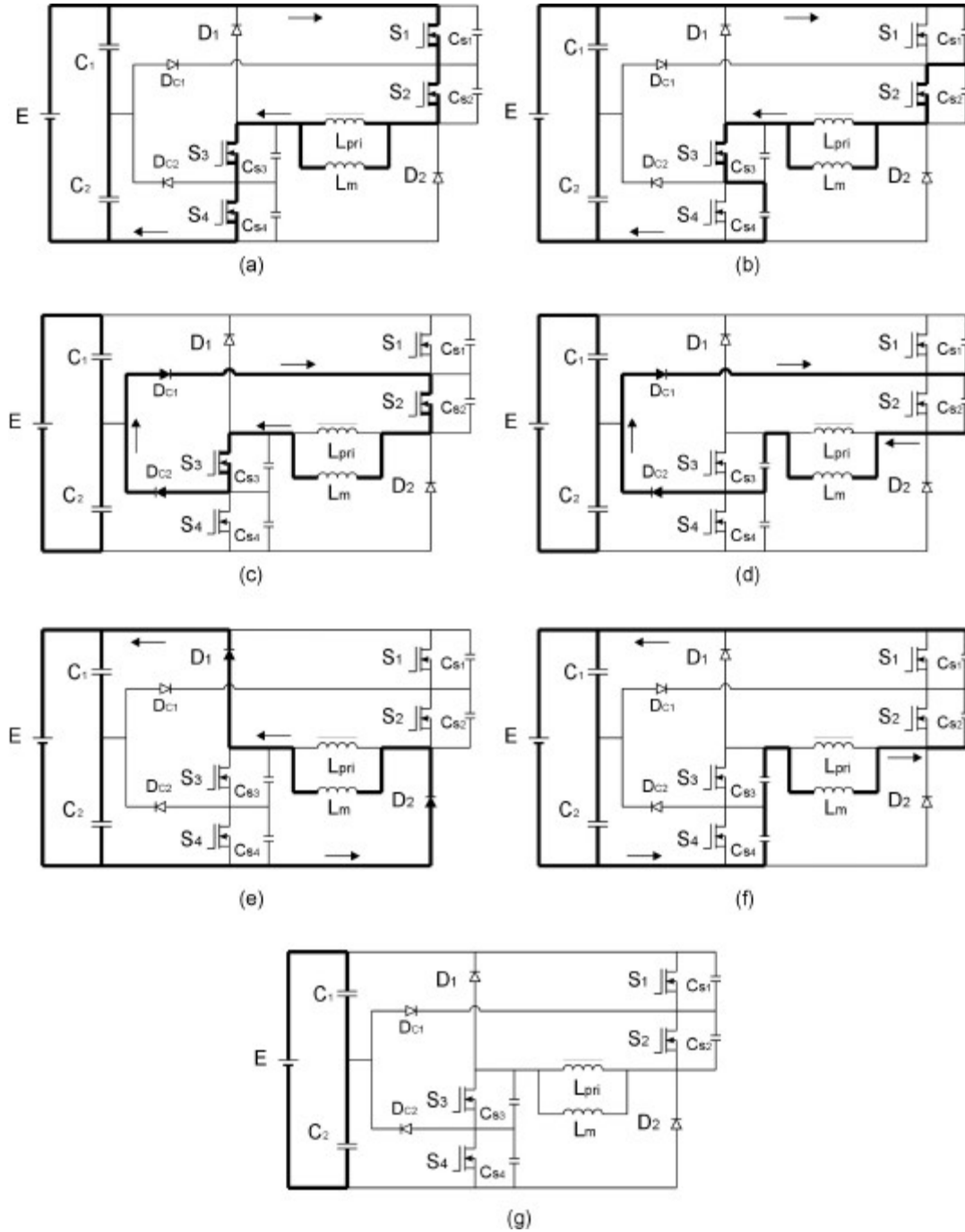


Fig. 2 – The topological stages of operation: (a) first stage; (b) second stage; (c) third stage; (d) fourth stage; (e) fifth stage; (f) sixth stage and (g) seventh stage.

First stage (t_0, t_1): This is the stage when the energy is transferred to the load. The switches S_1, S_2, S_3 and S_4 are allowed to conduct.

Second stage (t_1, t_2): The switches S_1 and S_4 are gated off in t_1 . The capacitors C_{S1} and C_{S4} are charged with the load current I_O . That's why this stage is very short in time.

Third stage (t_2, t_3): At t_2 , the voltage over C_{S1} and C_{S4} reaches $E/2$. Then the diodes D_{C1} and D_{C2} clamp the $E/2$ voltage on the S_1 and S_4 switches. The voltage on the primary side of the transformer is zero. A freewheel path is formed on the secondary side also, with the L_O inductance keeping the output current continuity. This free wheeling mode on the secondary side will be maintained until the last stage.

Fourth stage (t_3, t_4): The switches S_2 and S_3 are gated off in t_3 . The capacitors C_{S2} and C_{S4} are now charged with the storage energy in the magnetizing inductance.

Fifth stage (t_4, t_5): The voltage over C_{S2} and C_{S3} reaches $E/2$. The diodes D_1 and D_2 are willing to conduct, resetting the core magnetizing energy on the input supply E . The voltage on the primary side of the transformer is now $(-E)$.

Sixth stage (t_5, t_6): When the reset stage ends, a small resonant circuit is formed with all the intrinsic capacitor, the magnetizing inductance and the input source. In this stage the voltage of the input will be divided by the four capacitors C_{S1}, C_{S2}, C_{S3} and C_{S4} .

Seventh stage (t_6, t_7): In this stage the voltage over the switches is $E/4$. The voltage on the primary side is zero, as the current. This is a stand by stage, but its importance is legitimate, as the operation of the converter must reach this stage to be stable and guarantee the $E/2$ voltage on all the switches.

C. Output characteristic

The output mean voltage could be calculated using the waveforms in Fig. 3. This voltage is the positive voltage on the secondary winding and can be calculated as follows:

$$V_o = \frac{1}{T} n \int_0^{t_1} E dt + \int_{t_1}^{t_2} E \frac{1}{C_{eq}} (I_{O_{pri}} + I_{Lm}) t dt \div \frac{t}{T} \quad (1)$$

The second integral of the expression above is referent to the second stage, where C_{eq} refers to C_{S1} and C_{S2} in series. This term is very small and can be eliminated. So the output equation is described as:

$$V_o = nE \frac{t_c}{T} = nED \quad (2)$$

Where n denotes the turns rate, t_c is the switching conducted time defined by $(t_1 - t_0)$, T is the switching period, and D is the duty cycle defined as t_c/T .

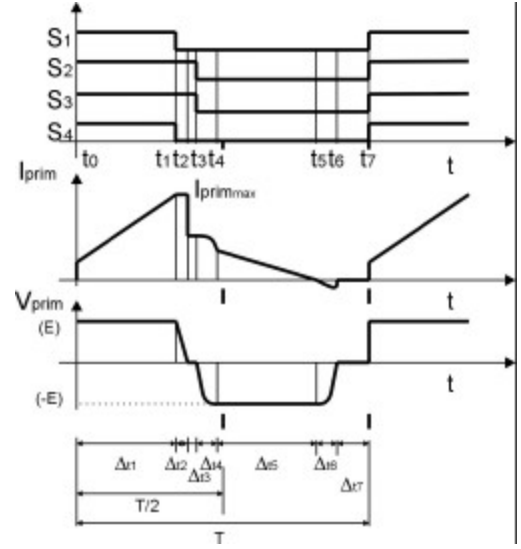


Fig. 3 – Main theoretical waveforms.

III. THE INPUT CAPACITORS EQUILIBRIUM

The input capacitors equilibrium is critical, because any difference in the on-times, or in intrinsic characteristics will lead the split voltage on the input capacitors to an unequal division.

This problem could be turned round splitting the primary side of the transformer in two coupled windings, with a one by one turns rate. This division does not change the converter principle of operation, but turns the equilibrium stable. Some current surge could happen, but this peaks are limited by the series resistance of the primary winding (since it is a high voltage winding with the number of turns in direct proportion with the voltage). Fig. 4 shows this division.

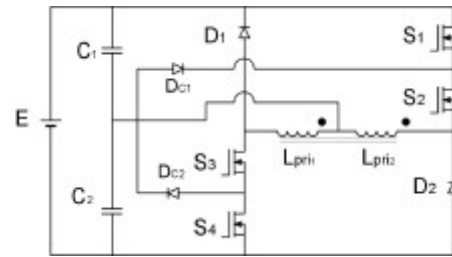


Fig. 4 – The split of the primary side to the equilibrium.

IV. THE MAGNETIZING INDUCTANCE

The magnetizing inductance plays an important role in this converter. Its storage energy has to be delivered back to the input supply. Otherwise, when the switches are turned on again, the voltage over the switches could not be guaranteed at $E/2$. The following equation describes that the sum of all the intervals after the first stage must be less than the half period.

$$t_2 + t_3 + t_4 + t_5 + t_6 + t_7 = \frac{T}{2} \quad (3)$$

When $t_2 = t_2 - t_1$ and so on for t_3, t_4 , etc. Since the third stage and the seventh stage can be considerate as delay times (do not depend on the circuit characteristics), the equation can be write as follow:

$$t_2 + t_4 + t_5 + t_6 = \frac{T}{2} \quad (4)$$

All the intervals on equation (4) can be write in function of L_m . This sum can be compared with the semi-period in one chart. Fig. 5 illustrates this chart. Now, the magnetizing inductance states as a restriction in the project, that is, it must be less than a critical value to guarantee the reset core and the $E/2$ voltage over the switches. This indicate that if the magnetizing inductance is greater than the maximum value, a gap in the core transformer must be provided to reduce this inductance until its maximum value is reached.

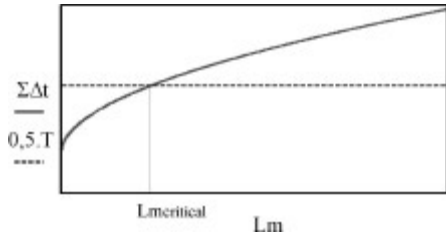


Fig. 5 – The critical value of magnetizing inductance L_m .

V. EXPERIMENTAL RESULTS

To demonstrate the converter principal of operation, a 80W, 300-1200Vdc input prototype was initially construct. This prototype has eight outputs, one 5Vdc, one 24Vdc, another six 15Vdc, and another output working also for self-source and feedback regulation.

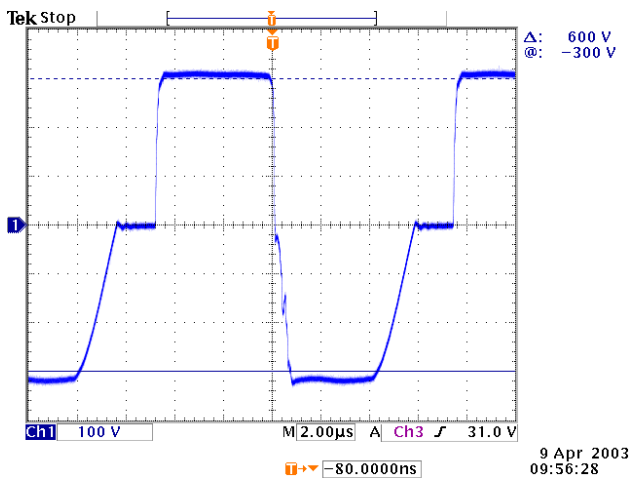


Fig. 6 – Primary winding voltage for 300V input.

The voltage imposed on the primary winding of the transformer is presented in Fig. 6. This is the minimum input voltage for this design. It can be noted that at this input voltage, the time for inverting the primary voltage is higher than the time for this voltage being zero when the external switches are turned off. Also can be noted the resonant stage when the primary voltage goes from minus 300V to zero.

Fig. 7 shows the primary winding waveform for a 1200V input. As the primary currents here are smaller, the input voltage even does not reach the 1200V negative for the core reset. The primary is divided in two halves, as commented in section 3. The two halves voltage could be observed in Fig. 8. It could be seen that this technique really guarantees the voltage balance on the input capacitors.

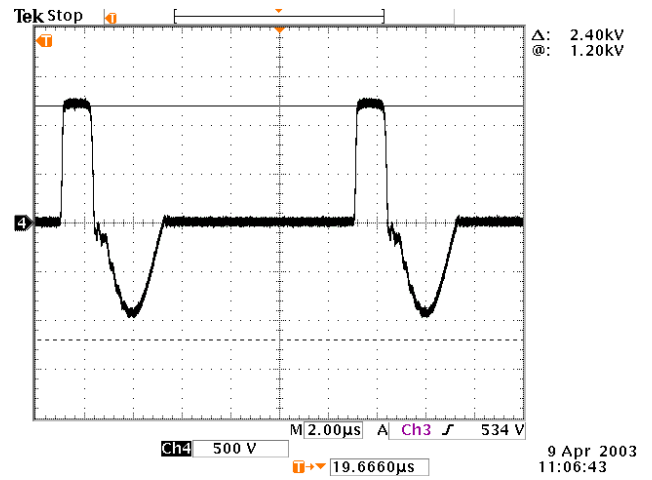


Fig. 7 – Primary winding voltage for 1200V input.

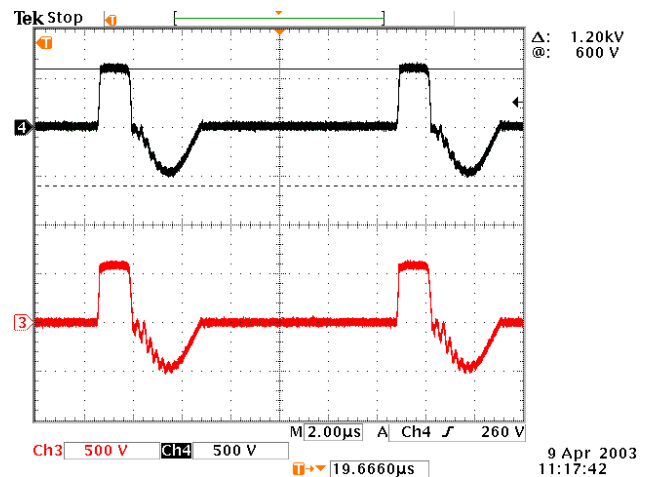


Fig. 8 – The primary winding voltages splitted on the two halves.

Another main characteristic of this converter is presented in Fig. 9 and Fig. 10. These pictures presents the drain to source voltages on the switches. It is showed that these voltages are clamped at 600V, half of the input voltage. The time delay

between the external (S_1 and S_4) and the internal (S_2 and S_3) switches setting off can be identified also.

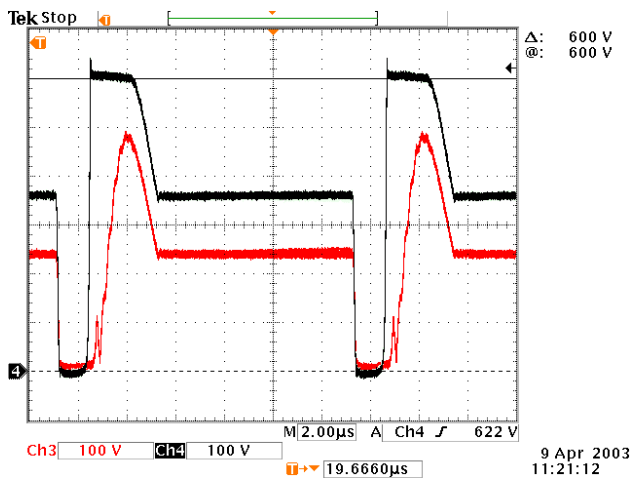


Fig. 9 – Drain to source voltages on S_1 (Ch4) and S_2 (Ch3).

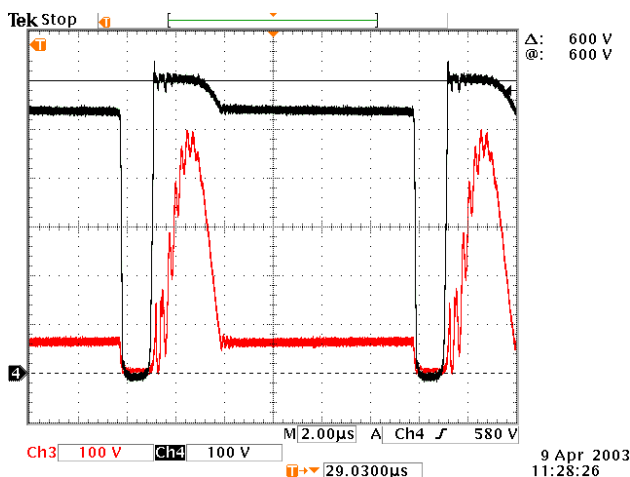


Fig. 10 – Drain to source voltages on S_3 (Ch3) and S_4 (Ch4).

The output current referred to the primary forces the clamping diodes to conduct when the external switches are turned off [3]. So on, depending on how fast these diodes begins to conduct, and depending on the parasitic inductances in the path of this loop, an overshoot voltage will appear on these switches. This overshoot is noted on Fig. 9 and Fig. 10. In Fig. 11 a zoom on the rise time of S_1 switch. In this picture could be observed that the overshoot voltage does not surpass 10% of the clamping voltage. This also demonstrated that some subjects must be take in account to not permit destructive over voltages.

V. CONCLUSION

A new three level forward converter was presented. Its main characteristics, as low off-voltage stress and simplicity, were demonstrated.

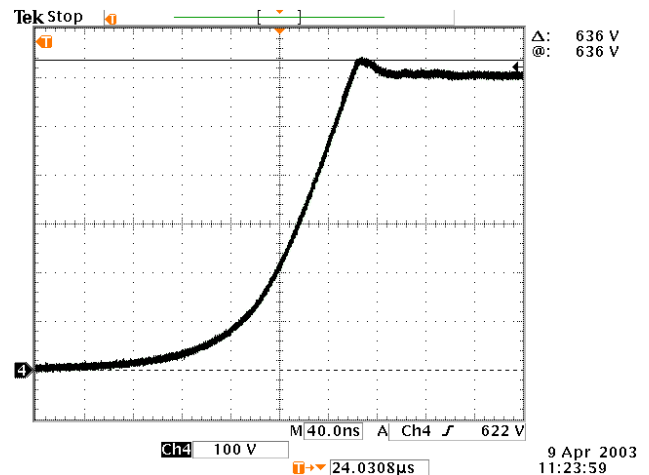


Fig. 11 – Drain to source voltage on S_1 : a zoom on the rising time.

A first laboratory prototype was already constructed to demonstrate the operational principle. This was also intent to reach the objectives of voltage stress reduction on the switches.

The voltage stress on the switches stays clamped at half of the input voltage. Considerations on the overshoot voltage clamping were made, and this overshoot could be limited.

Finally, the gate signal that drives the switches is the same, isolated by a pulse transformer, what represents simplicity in the modulation. Also the natural voltage balance on the input capacitor makes this converter very suitable for auxiliary supplies with a great input voltage range, and high input voltages (300Vdc-1200Vdc).

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