DYNAMIC MODELLING AND REGULATORS DESIGN FOR MULTIPLE INPUT POWER CONVERTERS FOR THE PROPULSION SYSTEM OF ELECTRIC VEHICLES

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Abstract - **This paper deals with the dynamic modeling and regulators design to the DC-DC converters used in an electric vehicle propulsion system that includes fuel cell generator, ultracapacitor tank and batteries. The three on-board power sources supply the vehicle traction drive through three DC-DC power converters that provide the desired management of the power flows. The ultracapacitor converter is used to control the DC link bus and automatically levels the battery load current during transients resulting from either acceleration or braking. The converters dynamic transfer functions are obtained using the state variables average method. A 35 kW prototype is used to conduct laboratory experiments and validate the control strategy.**

KEYWORDS

DC-DC converters, dynamic modeling, Electric vehicle, Bidirectional boost converter, Ultracapacitor, Fuel cell.

I. INTRODUCTION

The present researches concerning electric vehicles (EV) and hybrid-electric vehicles (HEV) concentrate in the search for a compact, lightweight, and efficient energy storage system that is both affordable and has acceptable cycle life. The traction system, composed by electric motor, inverter, and associated control circuitry is not the limiting factor to obtain high performance and to permit large-scale production of such vehicles.

In terms of power sources, the proton exchange membrane fuel cells (FC) are being increasingly accepted as the most appropriate supply for EVs [1,2] because they offer clean and efficient energy without penalizing performance or driving range. A battery storage unit can be combined with the FC stack to achieve the maximum efficiency for the FC system. The batteries deliver the difference between the energy required by the traction drive and the energy supplied by the FC system. In such a system the batteries have to deal with power peaks being on demand during acceleration or braking phases. Such transients result in a hard constraint for batteries, what increases the losses and temperature, and reduces their lifetime. Thereby, it is desirable to minimize these power peaks by introducing an additional auxiliary power device: the ultracapacitors (UCs) [3], which present high power density, obtain regeneration energy at high efficiency during decelerations and supply the stored energy during accelerations. In spite of reaching thousands of Farads, the UCs support very low voltages (1~2.5V). A stack of series-connected UCs can produce an equivalent capacitor of tens of Farads that is able to hold up tens of Volts. The UC stack must supply the power required in excess of the FC–battery system rated power, provided that the UC state of charge (SOC) is greater than a minimum threshold. Whenever the power required to operate the vehicle is lower than the FC-battery rated power, the UCs can be charged with the power in excess. Whenever regenerative braking operations occur, energy is put into the UC tank provided this device is not fully charged yet.

The energy storage arrangement, shown in Fig. 1, includes the FC, that is the main energy source. As the FC has poor efficiency at light load, the batteries supply the power at such situation, in order to save total efficiency. The FC is sized to supply the traction electric drive up to 4/5 of the cruising maximum power, whereas the storage battery should feed at least the additional 1/5 for the time calculated on the basis of selected driving cycles. The UC tank is used to satisfy acceleration and regenerative braking requirements accomplishing the system load transients and improving the on-board battery cycle life. Additionally it is responsible to control the DC link voltage, while the other sources are current controlled in order to limit the current variation ratio and to prevent excessive peaks.

The goal of this paper is to develop dynamic models for the DC-DC converters in order to analyze the influence of the system components, to choose the best feedback variable for each converter and to design the adequate regulators.

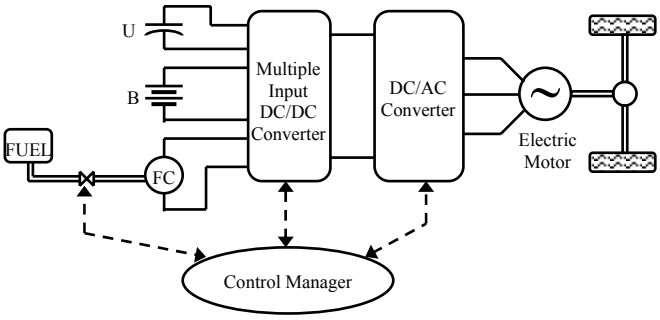


Fig. 1 Basic hybrid drive-train.

II. DC-DC CONVERTERS

Both FC and UC typically present a terminal voltage lower than the DC voltage necessary to feed the inverter. Also for the batteries bank would be of practical interest to use a lower voltage, in order to minimize the series resistance. In such cases it is necessary to use step-up converters for connecting the sources with the common DC bus, as shown in Fig. 1. Additionally, for the batteries and for the UCs it is necessary to have step-down operation in order to recharge them, what means that these converters must be bidirectional in current. A convenient topology is shown in Fig. 2.

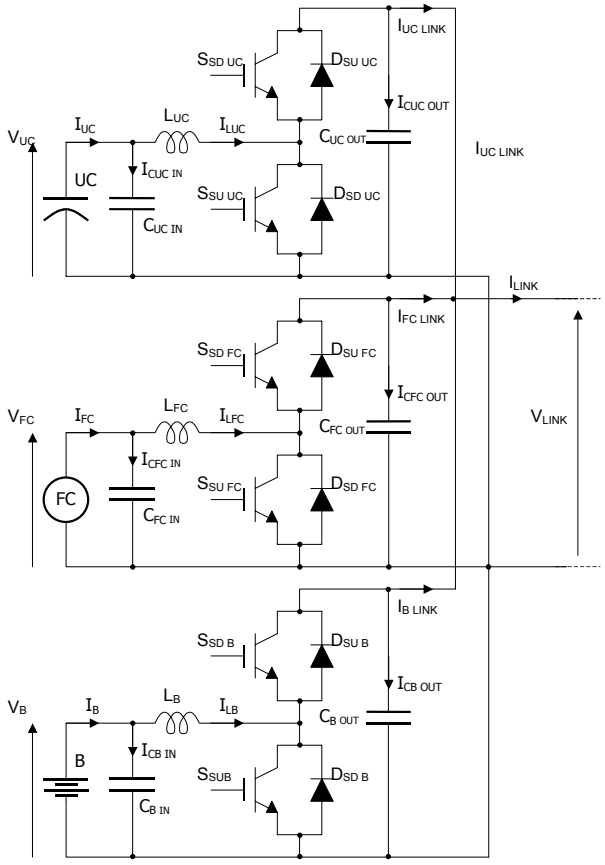


Fig. 2 DC-DC converters.

Each DC-DC converter can be built using a branch of a three-phase DC-AC converter, what means that there are power modules and drives already available in the market.

Considering that the common DC link voltage is the highest, the bottom transistor, together with the top diode, configures a boost converter, while the bottom diode and the top transistor realize the buck converter. For the FC converter the buck action must not occur because this apparatus does not take charge from the DC link.

A filter capacitor is connected at each source terminals in order to minimize the circulation of high-frequency components through the supplies [4]. This filtering is as effective due to the presence of the sources series resistance.

The converters can be voltage or current controlled, depending on the source role in the overall system, and their limitations. For example, it is important to limit the current variation in the FC, as well as in the batteries. As any capacitor, the UC can be controlled in voltage mode, only using a maximum current protection.

The references for the control loops are derived from many parameters: the instantaneous load current, the DC link voltage, the batteries and UC state of charges, the FC output power, etc. [5].

III. DYNAMIC MODELLING

Small signal modelling, considering the average value of the state variables over one switching period, is a well-known method to analyze non-linear systems, like a switched-mode power supply [6,7]. The resulting model is valid in a frequency range sufficiently below the switching frequency. The state equations or the equivalent function transfer can be used to design the regulators in order to achieve a desired system performance.

There are many methods to such design and this article uses the one described in [8]. Fig. 3 shows the single DC-DC converter considered. If the converter works as step-up, the average value of the currents i_p, I_L, and i_o are positive. In the step-down mode (necessary to recharge batteries and UC), the average values are negative. As the dynamic behavior as boost converter imposes more severe restrictions for the control loop design, this case is analyzed at the beginning and, afterwards, the buck operation is verified.

As the power switches operate in complementary way, the converter always operates in continuous conduction mode (CCM). Notice that, in steady state, the duty-cycle depends only on the voltages V_p and V_o (neglecting the source resistance, R). The average current is adjusted during the transients and does not depend on the voltages.

1) State variables averaging method

The state variables, usually the inductors current and the capacitors voltage, are represented in the vector $\mathbf{x}$. The sources are represented in the vector $\mathbf{U_i}$. For the next analyses the sources are supposed of fixed value. For each topologic situation, the differential equations should be obtained and put in the format $\dot{\mathbf{x}} = \mathbf{A_1} \cdot \mathbf{x} + \mathbf{B_1} \cdot \mathbf{U_i}$.

These equations are valid during one topologic combination, for example, while the transistor is on. During the diode conduction, the equations will be $\dot{\mathbf{x}} = \mathbf{A}_2 \cdot \mathbf{x} + \mathbf{B}_2 \cdot \mathbf{U_i}$.

As the circuit operates in CCM, there are only these two cases.

The same procedure is used to obtain the equations that describe the output variable: $v_o = \mathbf{C_1} \cdot \mathbf{x}$, for the first topologic state and $v_o = \mathbf{C_2} \cdot \mathbf{x}$ for the second one.

The system behavior can be obtained averaging each matrix by the duty-cycle, δ, in which it is valid:

$$\dot{\mathbf{x}} = \left[\mathbf{A_1} \cdot \delta + \mathbf{A_2} \cdot (1-\delta)\right] \cdot \mathbf{x} + \left[\mathbf{B_1} \cdot \delta + \mathbf{B_2} \cdot (1-\delta)\right] \cdot \mathbf{U}_i \quad (1)$$

$$v_o = \left[\mathbf{C_1} \cdot \delta + \mathbf{C_2} \cdot (1-\delta)\right] \cdot \mathbf{x} \quad (2)$$

It is possible to split the state variables, the output and the control variable (duty-cycle) in their average value plus a perturbation:

$$\begin{aligned} \mathbf{x} &= \mathbf{X} + \boldsymbol{x} \\ v_o &= Vo + v_o \\ \delta &= D + d \end{aligned} \quad (3)$$

Substituting (3) into (1) and (2), and neglecting the product of two perturbations, it is possible to obtain the desired transfer function:

$$\frac{v_o(s)}{d(s)} = \mathbf{C} \cdot \left[s \cdot \mathbf{I} - \mathbf{A}\right]^{-1} \cdot \left[(\mathbf{A_1} - \mathbf{A_2}) \cdot \mathbf{X} + (\mathbf{B_1} - \mathbf{B_2}) \cdot \mathbf{U_i}\right] \quad (4)$$

$\mathbf{A} = \mathbf{A_1} \cdot D + \mathbf{A_2} \cdot (1-D)$, $\mathbf{B} = \mathbf{B_1} \cdot D + \mathbf{B_2} \cdot (1-D)$ and $\mathbf{C} = \mathbf{C_1} \cdot D + \mathbf{C_2} \cdot (1-D)$

2) Boost converter

Let us consider the boost converter, in the CCM, having a capacitive input filter. The voltage source presents a series resistance R. The load is represented by a current source that, for the dynamic analysis, is an additional input. Figure 3 shows the circuit and figure 4 indicates both equivalent topologies.

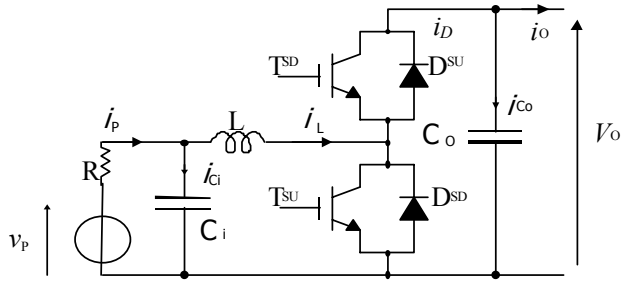
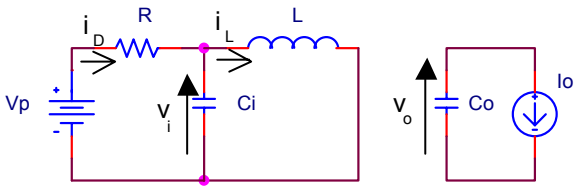
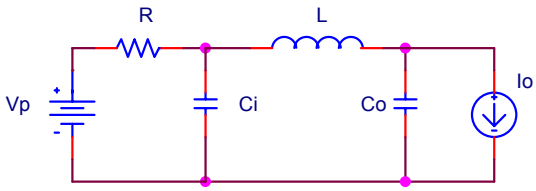


Fig. 3. DC-DC converter for dynamic modeling.



(a)



(b)

Fig. 4: (a) Low-side switch conduction (T_{SU} or D_{SD}); (b) High-side switch conduction (D_{SU} or T_{SD}).

Taking the voltage v_o as the output variable, the transfer function to the duty-cycle, that is the control variable, is calculated using the following equations:

$$\mathbf{x}=\begin{bmatrix} v_o \\ v_i \\ i_L \end{bmatrix},\ \mathbf{U_i}=\begin{bmatrix} i_o \\ V_p \end{bmatrix},\ \mathbf{B_1}=\mathbf{B_2}=\mathbf{B}=\begin{bmatrix} -\frac{1}{C_o} & 0 \\ 0 & \frac{1}{RC_i} \\ 0 & 0 \end{bmatrix},$$

$$\mathbf{C_1}=\mathbf{C_2}=\mathbf{C}=\begin{bmatrix} 1 & 0 & 0 \end{bmatrix},$$

$$\mathbf{A_1}=\begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{RC_i} & -\frac{1}{C_i} \\ 0 & \frac{1}{L} & 0 \end{bmatrix},\ \mathbf{A_2}=\begin{bmatrix} 0 & 0 & \frac{1}{C_o} \\ 0 & -\frac{1}{RC_i} & -\frac{1}{C_i} \\ -\frac{1}{L} & \frac{1}{L} & 0 \end{bmatrix}$$

$$\mathbf{A}=\begin{bmatrix} 0 & 0 & \frac{1-D}{C_o} \\ 0 & -\frac{1}{RC_i} & -\frac{1}{C_i} \\ -\frac{1-D}{L} & \frac{1}{L} & 0 \end{bmatrix}$$

The resulting transfer function is:

$$\frac{v_o(s)}{d(s)}=\frac{-s^2\frac{Io}{(1-D)C_o}+s\left\{\frac{V_p}{LC_o}-\frac{Io}{C_o(1-D)}\left[\frac{R}{L}+\frac{1}{RC_i}\right]\right\}+\frac{1}{LC_iC_o}\left[\frac{V_p}{R}-\frac{2Io}{1-D}\right]}{s^3+\frac{s^2}{RC_i}+\frac{s}{L}\left[\frac{(1-D)^2}{C_o}+\frac{1}{C_i}\right]+\frac{(1-D)^2}{RLC_iC_o}} \quad (5)$$

The poles and zeroes values depend on the operation point (D is the average duty-cycle, and Io is the average load current). One of the zeros is at the right half-plane (RHP) and its value decreases as the current increases, as shown in Fig. 5. For the next simulations, the circuit parameters are: V_p=120V, R=310mΩ, L=52μH, C_i=2mF, C_o=16mF, V_o=250V.

Additional analyses have demonstrated that capacitors series equivalent resistance and the inductor winding resistance does not affect the regulators design because their effects occur in high frequency.

A linear regulator (one zero, two poles, one at the origin) is designed [8] and adjusted to get 100 Hz cut-off frequency and phase margin of 60°. It is difficult to obtain a higher cut-off frequency due to the flat gain behavior below the double pole (around 400 Hz). The time response for a reference voltage step is shown in Fig. 6. The system takes some tens of milliseconds to reach the new reference value. The current assume positive or negative values depending on the power demand.

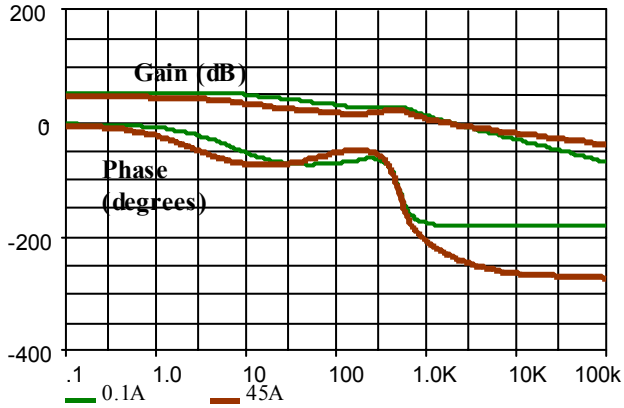


Fig. 5 Bode diagrams for voltage control at different output currents.

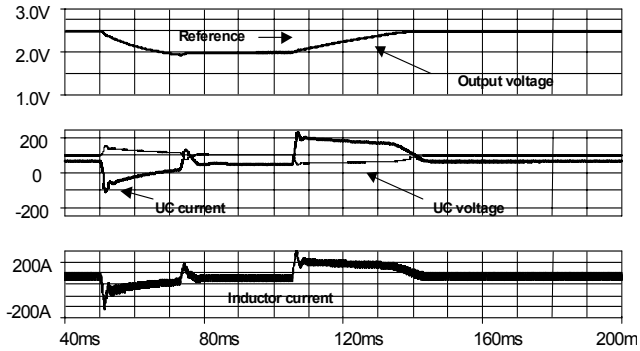


Fig. 6 Time responses for voltage control.

The UC converter operates to control the common DC link voltage, while the other two are controlled in current mode. It is necessary to define in which point the current should be controlled.

The first option is the converter output current, i_D. In this case the reference would be the instantaneous load current that should be provided, within the source limitations, by the FC.

Applying the state variables averaging method, the respective transfer function is:

$$\frac{i_D(s)}{d(s)} = \frac{-\frac{Io}{1-D}s^3 + s^2\left[\frac{Vp}{L} - \frac{Io}{1-D}\left(\frac{R}{L}+\frac{1}{RC_i}\right)\right] + \frac{s}{LC_i}\left(\frac{Vp}{R} - \frac{2Io}{1-D}\right)}{s^3 + \frac{s^2}{RC_i} + \frac{s}{L}\left[\frac{(1-D)^2}{C_o} + \frac{1}{C_i}\right] + \frac{(1-D)^2}{RLC_iC_o}} \quad (6)$$

Besides changing poles and zeros positions according to the load current, the system presents a RHP zero, and also a zero at the origin, whose compensation with an integrator would result in a steady-state error.

The output current is pulsed, since it is the diode current. To obtain its average value it would be necessary to use a low-pass filter in the feedback path, making practically impossible to design a regulator for having wide compensation band with secure phase margin. Consequently this is not the best place to control the current.

Let us consider the inductor current as the controlled variable. For low inductance value the instantaneous current still could have a high ripple, asking for an additional low-pass filter in the feedback. The reference, in this case, should be calculated taking the load current and dividing it by the duty-cycle.

The resulting transfer function is:

$$\frac{i_L(s)}{d(s)} = \frac{s^2\left[\frac{V_p(1-D)-RIo}{L(1-D)^2}\right] + \frac{s}{L}\left[\frac{V_p(1-D)-RIo}{RC_i(1-D)^2} + \frac{Io}{C_o}\right] + \frac{Io}{RLC_iC_o}}{s^3 + \frac{s^2}{RC_i} + \frac{s}{L}\left[\frac{(1-D)^2}{C_o} + \frac{1}{C_i}\right] + \frac{(1-D)^2}{RLC_iC_o}} \quad (7)$$

In this case, all poles and zeroes are at the left half-plane. The system Bode diagrams are shown in figure 7, for a two-zeros, three-poles regulator, calculated to produce a 1kHz cut-off frequency with 60° phase margin. The drawback is the flat gain response below the system's double pole position that results in a very poor response in the range above 10 Hz, even with more complex regulators. As the current ripple is high, a low-pass filter could be necessary in the feedback path.

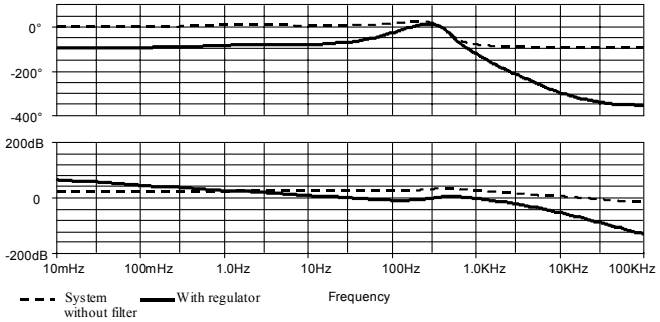


Fig. 7 Bode diagrams for inductance current control.

Another possibility is to control the current in the source, i_p, exploiting the natural filtering introduced by the capacitor. In this case, as the output variable is not a state variable it is necessary to redefine eq. (2) introducing additional terms. The resulting function transfer is:

$$\frac{i_p(s)}{d(s)} = \frac{\frac{1}{RLC_i}\left\{s\left[\frac{Vp}{1-D} - \frac{RIo}{(1-D)^2}\right] + \frac{Io}{C_o}\right\}}{s^3 + \frac{s^2}{RC_i} + \frac{s}{L}\left[\frac{(1-D)^2}{C_o} + \frac{1}{C_i}\right] + \frac{(1-D)^2}{RLC_iC_o}} \quad (8)$$

It is possible to get a 1 kHz cut-off frequency, with 60° phase margin, maintaining an acceptable gain in the low-frequency band. Figure 8 shows the Bode diagrams of the converter and including the designed regulator.

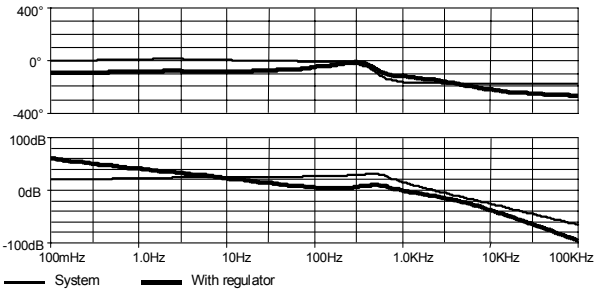


Fig. 8 Frequency response with current source feedback.

Fig. 9 shows the fast time response obtained with a two-zeros, three-poles regulator. In the simulation, the current reference changes from a positive to a negative value, showing that even in the step-down conversion the regulator works properly. Therefore, this variable, with such regulator, seems to be the best option for current control.

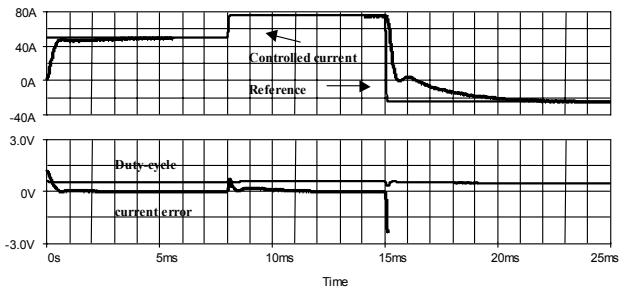


Fig. 9 Time response with source current control.

IV. EXPERIMENTAL WORK

A 35kW prototype of multi-input power electronic converter (MIPEC) has been used to validate results achieved from dynamic modeling investigation. The MIPEC prototype has been accomplished in order to satisfy power/energy requirements for small size HEVs class. Extensive investigation on world-wide used driving cycles allowed sizing of vehicle on-board power source (FC generator) and hybrid storage unit (HSU – UC plus battery). Table I and II show respectively power source – HSU electric characteristics and MIPEC components leading characteristics.

TABLE I. Electric Characteristic of Power Source and HSU

Fuel Cell Generator	
open circuit voltage [V]	220
voltage @ max power [V]	120
current @ max power [A]	160
series resistance [mΩ]	550

Ultracapacitor Tank	
max voltage (@ SOC=1) [V]	140
min. voltage (@ SOC=0.6) [V]	85
max current [A]	200
series resistance [mΩ]	66

Battery System	
rated voltage [V]	168
min. voltage [V]	140
max current [A]	80
series resistance [mΩ]	160

TABLE II. Leading Characteristics of MIPEC Components

Power Semiconductors	PM300DSA060 (IPM 2-pack mod.)
Rated Current [A]	300
Rated Voltage [V]	600

Inductors	L_{FC}	L_{UC}	L_B
Inductance [μH]	130	52	160
Rated Current [A]	160	200	80
Max Current Ripple [A]	32	80	16
Winding resistance [mΩ]	9.6	2.4	9.8

Capacitors	C_{OUT}	C_{FCIN}	C_{UCIN}	C_{BIN}
Capacitance [mF]	15	1	2	1
Rated Voltage [V]	385	385	385	385
Max RMS Current Ripple [A]	195	13	26	13
ESR [mΩ]	5	74	37	74

1) *MIPEC control algorithm description*

Control algorithm of the achieved MIPEC prototype is partitioned in three different sections. First section accomplishes pre-charge of converter input capacitors in order to allow the power system soft start; second section provides HSU constant current charging to values suitable to afford starting and acceleration of the vehicle, as well output voltage is raised to traction drive rated voltage by means of UC converter regulator. As rated output voltage is reached, the whole system is ready to feed the traction drive and third section of the control algorithm commences. FC and B converters are current regulated with the purpose of supplying DC link current requested by the traction drive, however current variation vs. time for both FC generator and B storage unit are limited on the basis of power source and storage unit transient behaviors; whereas UC converter is responsible for DC link voltage control and thus it balances MIPEC output currents when traction drive dynamic asks for DC link current transients faster than FC and B higher performances.

Vehicle regenerative braking is also accomplished by means of MIPEC control system as well diagnostic and protection against over-voltage and over-current. MIPEC control algorithm was implemented on ADSP 21992 from Analog Devices, where standard fixed point configuration was adopted for the whole algorithm except for UC regulator implemented by using the emulated floating point mode of operation.

2) *MIPEC testing*

MIPEC testing was achieved in order to validate previous dynamic modeling investigation, as well to show sharing of requested traction drive power during vehicle simulated acceleration and braking.

Figure 10 shows the DC link voltage control executed by the UC converter using a PI regulator. This result can be compared with Fig. 11, in which, for the same conditions, but using a two-zeros, three-poles regulator, the response is much faster and damped. This last regulator was used in the following.

Figure 12 shows the system operating with two sources: the FC and the UC. Initially the load current is zero. Suddenly a 6Ω load is connected. The DC link voltage is regulated at 170V. The UC delivers the total load current while the FC starts. The control circuit limits the FC current variation.

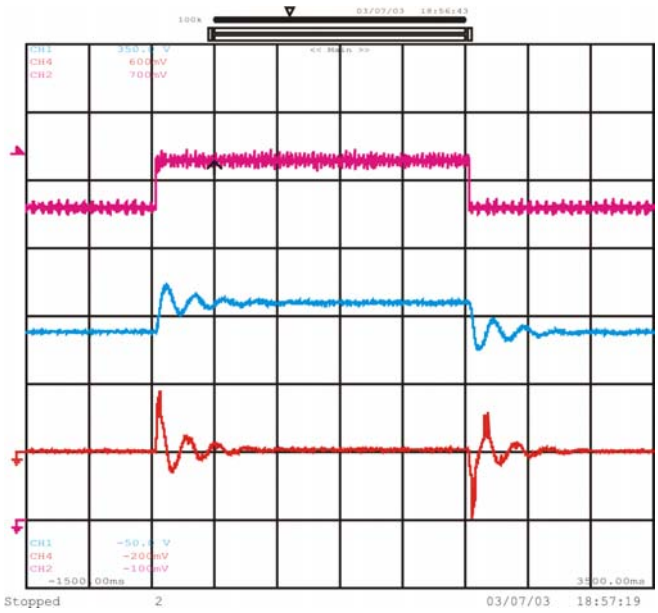


Fig. 10 DC link voltage control with PI regulator. From top to bottom: Voltage reference (100 mV/div. = 30V/div.), DC link voltage (50V/div.) and UC average current (40A/div.). Horiz.: 500ms/div.

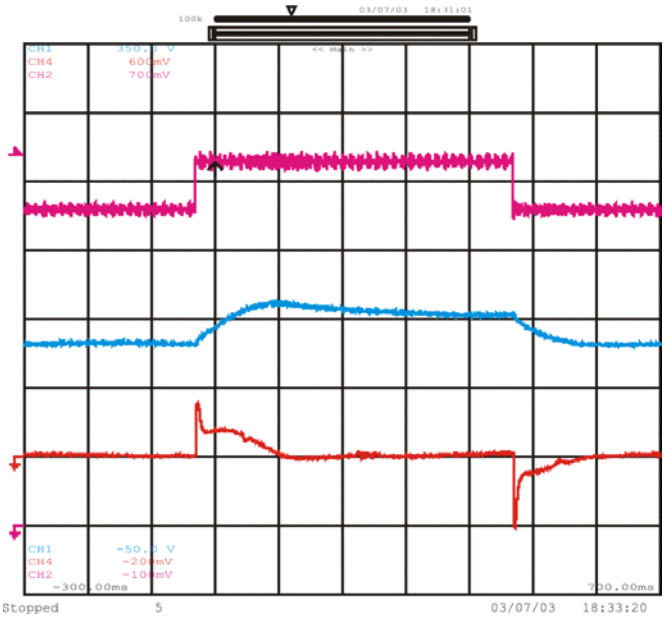


Fig. 11 DC link voltage control with two-zeros/three-poles regulator. From top to bottom: Voltage reference (100mV/div.=30V/div.), DC link voltage (50V/div.) and UC average current (40A/div.). Horiz.: 100ms/div.

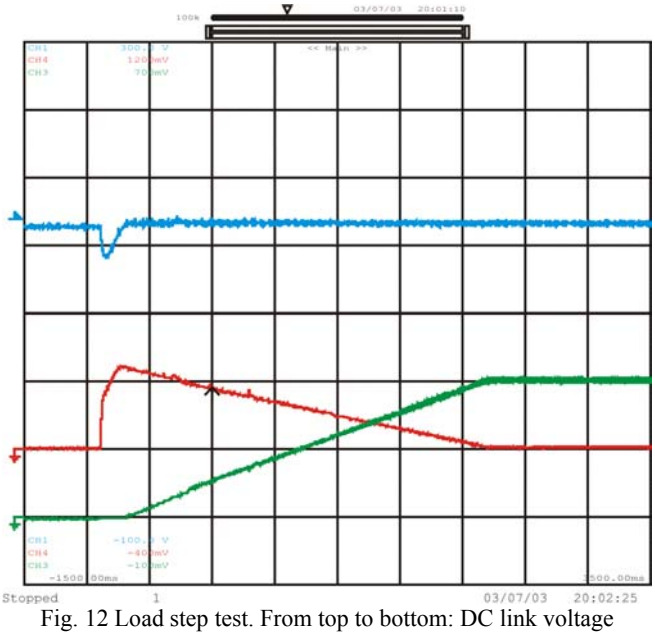


Fig. 12 Load step test. From top to bottom: DC link voltage (50V/div.), UC average current (40A/div.) and FC average current (20A/div) Horiz.: 500ms/div.

V. CONCLUSIONS

The dynamic modeling allows identifying the variable for which it is possible to get the fastest response, as well as to individuate poles and zeros positioning and their effects over the system, allowing to design the regulators for the best overall behavior.

In spite of the modeling has been done for the boost converter, it is valid even for the buck operation, since the duty-cycle is defined for the low-side transistor, and the upper-side one is operated in complement. This complementary mode guarantees operation in the continuous conduction mode and produces a natural transition between step-up and step-down conversions. The same regulator can be used for both conversion modes.

As the transfer functions poles and zeros values can change according to the operation point and load current it is necessary to verify the worst case from the control point of view.

It was shown that for the current-mode controlled converters the source current should be output variable.

A 35kW prototype of multi-input power electronic converter (MIPEC) has been used to validate results achieved from dynamic modeling investigation. MIPEC prototype has been conceived for HEV applications, where fuel cell, battery and ultracapacitor tank are respectively used as on-board generator and storage unit. Experimental results are shown as well a short description of the system control algorithm.

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