IMPLEMENTATION OF A DIGITAL AND A DEADBEAT PLL CIRCUIT BASED ON INSTANTANEOUS POWER THEORY WITH DSP TMS320F243

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***Abstract* - This paper describes mathematical models and digital implementation of two detection phase circuits of three-phase systems (p-PLL and q-PLL) based on the instantaneous real and imaginary power theory. The modeled circuits are analyzed using small signal techniques and by digital simulations. The results are presented showing that the proposed PLLs are able to detect the frequency and the phase of three-phase system voltages or currents, even when they operate in the presence of noise or transitory perturbations. Some experimental results are used to confirm the mathematical models and the computational simulations.**

Keywords – Phase locked loop, DSP, deadbeat controller, instantaneous power theory.

I. INTRODUCTION

During the last decades Static Power Converters (SPCs) have been widely used in power systems as FACTS devices (Flexible AC Transmission Systems), Active Power Filters (APF), High Voltage DC Current Transmission Systems (HVDC) and most recently as switching interface between the utility systems and renewable energy sources such as Photovoltaic Cells and Wind Energy Systems among others [1] and [2]. However, in all these applications, the correct operation of the SPCs is strongly dependent on the accurate measurement of the utility system frequency and its phase angle, which is normally carried out through PLL (Phase Locked Loop) circuits.

The PLL concept is dated from the 1930's, but only in the early 1970's, with the development of large-scale integration of electronic circuits, the interest in the implementation and design of digital PLL increased. Nowadays, as a consequence of the cost reduction and the popularization of microprocessors and microcontrollers, efforts have been done to develop digital software controlled PLL [3] and [4].

This work aims at showing the basic principles and the development steps of digital PLL based on instantaneous power theory using a DSP TMS320F243. The digital PLL samples the system voltages at discrete time intervals. However the detection of the system frequency requires the processing of the sampled signals in a finite amount of time. If the sampled voltages and the processing are not done fast enough, some of the information may be lost and instabilities can occur. Simulated and experimental results will be used to validate the modeled PLL.

II. THE INSTANTANEOUS POWER THEORY PLL CIRCUIT

Fig. 1 (a) and (b) show the block diagram of the modeled PLL circuits. Both circuits use the concept of the instantaneous real and imaginary powers [5] and [6]. In these figures the instantaneous voltages v_a e v_b are obtained applying a Clarke transformation in the set of instantaneous three-phase system voltages as follows:

$$\begin{matrix} v \\ v \end{matrix} = \sqrt{\frac{2}{3}} \begin{matrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{matrix} \begin{matrix} v_a \\ v_b \\ v_c \end{matrix} \quad (1)$$

The currents i'_a and i'_b are fictitious instantaneous currents in - coordinates that are used to calculate the instantaneous real and imaginary powers p' (*W*)and q' (*vai*) as follows:

$$\begin{matrix} p' \\ q' \end{matrix} = \begin{matrix} v & v \\ v & -v \end{matrix} \begin{matrix} i' \\ i' \end{matrix} \quad (2)$$

where *vai* is unit for the instantaneous imaginary power

and means imaginary volt-ampere.

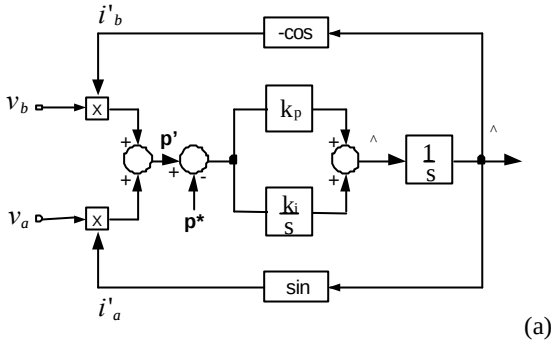

Fig. 1: Block diagrams of the frequency detection circuits: (a) *p*-PLL and (b) *q*-PLL

From Fig. 1, the error between the desired and the measured instantaneous real or imaginary powers feeds the PI controller and its output is the utility system angular frequency ($\hat{}$). The detected angular frequency feeds an integration block used to generate the $\hat{}$. Mathematically there are not differences between the two PLL models, however each PLL name has the prefixes *p* or *q* as a consequence of the instantaneous *real* or *imaginary* power used as feedback signals, respectively [7]. Thus, from this point forward, only the *q*-PLL is going to be analyzed.

III. MATHEMATICAL PLL MODELS

A. Continuous Time Analysis

The dynamic behavior of the q-PLL is strongly dependent on the PI controller gains. From Fig. 1 (b) a small signal model can be derived linearizing the instantaneous imaginary power expression given by:

$$q' = v\ i \quad v \times i = \sqrt{3}V\sin(\quad \hat{}\ ) \tag{3}$$

where, V is the *rms* utility phase voltage in (V), $= (\ t + \ )$, is the utility phase voltage angular frequency in (*rad/s*), is the system voltage phase angle in (*rad*), $\hat{} = \left(\hat{}\ t + \hat{}\right)$, $\hat{}$ is the detected phase voltage angular frequency in (*rad/s*) and $\hat{}$ is the detected voltage phase angle in (*rad*).

The linearizaton of (3) results:

$$q' = \sqrt{3}V_0\cos(\ _0 \quad \hat{}\ _0) \quad + \sqrt{3}V_0\cos(\ _0 \quad \hat{}\ _0)\ \hat{} \quad \sqrt{3}\sin(\ _0 \quad \hat{}\ _0)\ V\ , \tag{4}$$

where the subscript "$_0$" denotes the steady state value of the variables.

Fig. 2 shows the block representation of the *q*-PLL obtained from (4), and (5) shows the state-space model of the *q*-PLL.

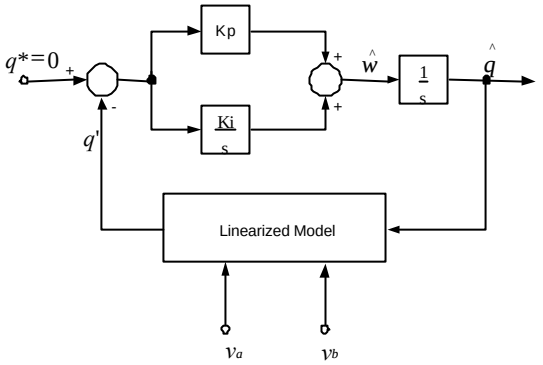

Fig. 2: Linearized block diagram of the *q*-PLL.

$$s\ \begin{matrix}\hat{}(s)\\ \hat{}(s)\end{matrix} = \begin{matrix}0 & 1\\ -k_i k_0 & -k_p k_0\end{matrix}\ \begin{matrix}\hat{}(s)\\ \hat{}(s)\end{matrix} + \begin{matrix}0 & 0 & (s)\\ (k_i k_0/s)+k_p k_0 & -k_i k_1 & s(k_p k_1)\end{matrix}\ \begin{matrix}\\ V(s)\end{matrix} \tag{5}$$

where, $k_0 = \sqrt{3}V_0\cos(\ _0 \quad \hat{}\ _0)$ and $k_1 = \sqrt{3}\sin(\ _0 \quad \hat{}\ _0)$

As shown in [8], the closed loop functions of the *q*-PLL are given by:

$$\frac{\hat{}}{V} = \frac{(\ k_i k_1)s + (\ k_p k_1)s^2}{s^2 + k_p k_o s + k_i k_0} \tag{6}$$

and,

$$\frac{\hat{}}{} = \frac{(k_p k_0)s + k_i k_0}{s^2 + k_p k_o s + k_i k_0}\ . \tag{7}$$

In steady state, for $_0 = \hat{}\ _0$ and assuming that

$V = 1\,pu$, $k_0 = 1.732$ and $k_1 = 0$, it is possible to conclude that variations in the amplitude of the system voltage can not affect the detected angular frequency ($\hat{\ }$).

From (7), choosing the PLL closed loop ( ) damping ratio and the undamped natural frequency ($_n$) equal to 0.707106 and 235.58 rad/s, respectively, the controller gains should be $k_p = 192.257\ rad.s^{-1}/vai$ and $k_i = 32042.94\ rad/vai$ [9].

B. *Discrete Time Analysis*

There are several ways to convert an existing continuous system into a discrete or digital one. However, the conversion from the *s*-domain to *z*-domain causes some distortion on the poles location in the discrete time complex plane [10].

One approach to convert (6) and (7) is the use of the step response of the transfer function, expanding them into partial fractions and using a *z* transform table to find the *z* transforms of each expanded term multiplying them by $(1\text{-}z^{-1})$. Thus, (7) could be rewritten in the *z*-domain as:

$$\frac{\hat{\ }}{} = \frac{A_1 z + A_2}{z^2 + \left[A_1 \quad 2\left(k_p k_0 T_s\right)\right] z + A_2 + \left(k_p k_0 T_s\right)} \tag{8}$$

where, $A_1 = \frac{k_0 T_s}{2} \div \left[T_s k_i + 2\right]$ and

$$A_2 = \frac{k_0 T_s}{2} \div \left[T_s k_i \quad 2\right].$$

Based on (8), if a similar response is desired for digital *q*-PLL model, with a sampling period of $T_S = 0.0002\ s$, the gains should be chosen as $k_p = 192.257\ rad.s^{-1}/vai$ and $k_i = 32042.94\ rad/vai$. Substituting the designed gains in (8) yields:

$$\frac{\hat{\ }}{} = \frac{0.06771z \quad 0.06549}{z^2 \quad 1.932z + 0.9345} \tag{9}$$

Fig. 3 shows the step response of the continuous time and discrete time *q*-PLL models given by (7) and (9), respectively. Fig. 4 shows a detail of the step response of the continuous time and discrete time *q*-PLL. Note that the behavior of both models is too close. Fig. 5 shows the system utility voltage and the detected frequency of the discrete time PLL model when the system voltage is step changed from 60 *Hz* to 120 *Hz* in $t = 50\ ms$.

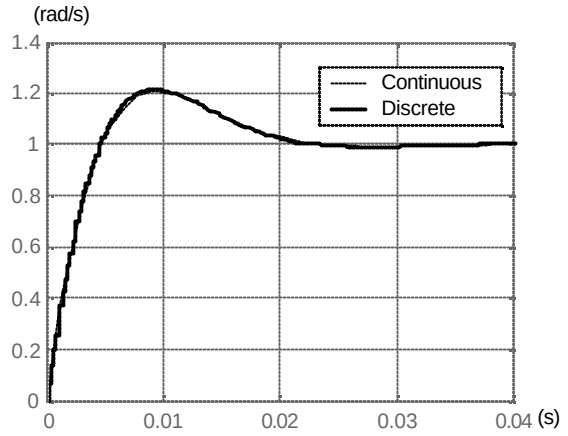

Fig. 3: Step response of the linear and digital models of the *q*-PLL.

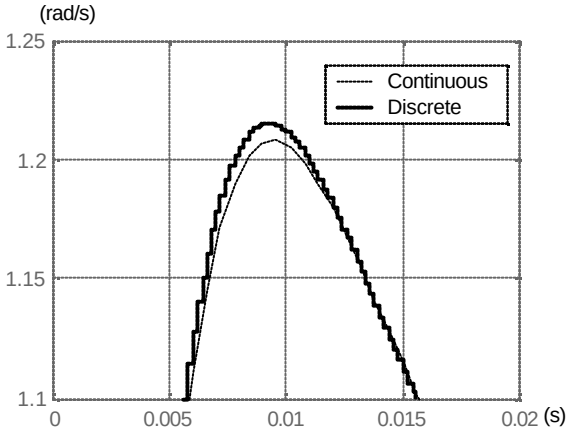

Fig. 4: Detail of the step response of the linear and digital models of the *q*-PLL.

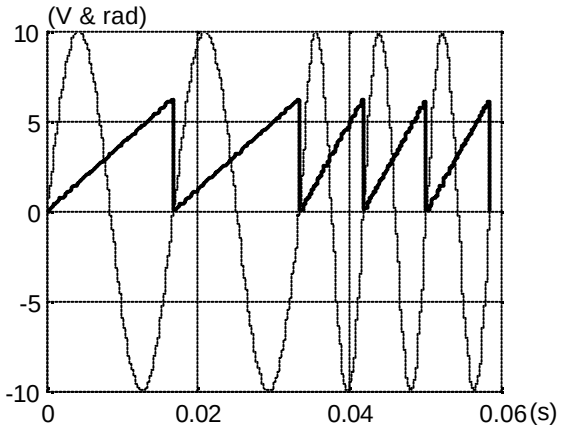

Fig. 5: Utility system voltage and detect phase and frequency of the digital *q*-PLL.

IV. DEADBEAT *q*-PLL MODEL

Ideally, in the analog linearized *q*-PLL model, the output signal (detect frequency) takes an infinite time to settle exactly to the input signal (the utility frequency). A deadbeat algorithm is used when a quick or finite settling time is required. Deadbeat design is carried out entirely in the *z*-domain and the controller replaces the poles of the system by the poles at the origin of the complex *z*-plane.

This strategy has the property to drive all the model states to zero in *n* steps when there is an impulse disturbance in the input. In deadbeat control the sampling period is the only design parameter. Therefore, the sampling period will drastically influence the magnitude of the control signal that increases with the decreasing of the sampling period. This fact leads us to choose the sampling period carefully in the implementation of the deadbeat *q*-PLL model.

From (8), assuming that $(k_p / k_i) = (3/2).T_S$ and $Ts = 0.0002\,s$, the deadbeat *q*-PLL gains should be chosen as $k_p = 2500\sqrt{3}$, $k_i = 8.33.10^6\sqrt{3}$ and its *z*-transfer function is given by:

$$\frac{\hat{}}{} = \frac{2z \quad 1}{z^2} \tag{10}$$

Fig. 6 shows the step response of the digital and the deadbeat *q*-PLL given by (9) and (10), respectively. Note that the deadbeat PLL reaches the steady-state response 2 samples after the instant when the step is applied. Fig. 8 shows the system utility voltage and the detected frequency of the deadbeat *q*-PLL model when the system voltage is step changed from 60 *Hz* to 120 *Hz* in $t = 50\,ms$.

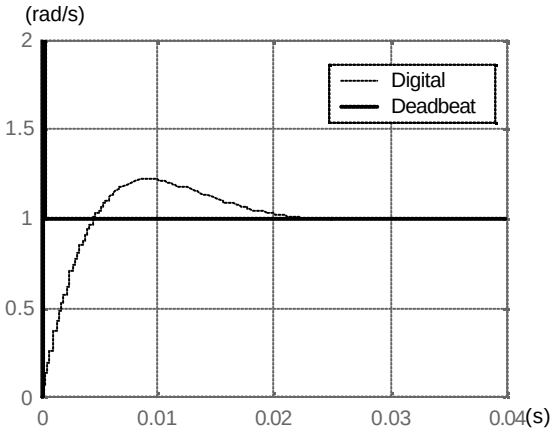

Fig. 6: Step response of the digital and the deadbeat *q*-PLL models.

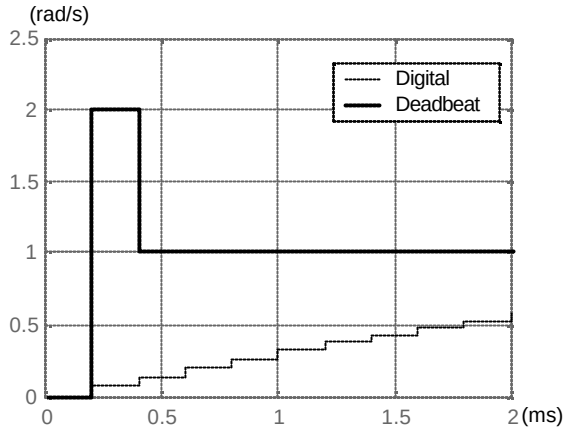

Fig. 7: Detail of the step response of the deadbeat *q*-PLL.

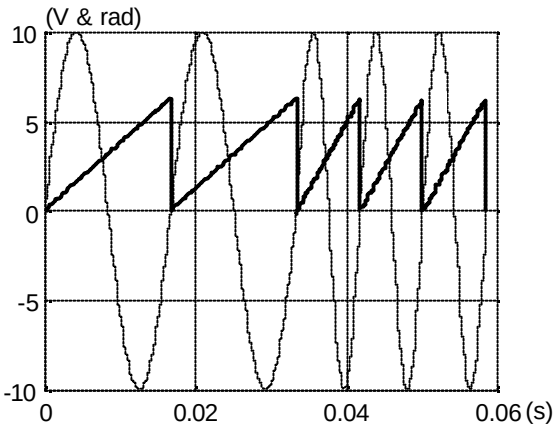

Fig. 8: Utility system voltage and detect phase and frequency of the deadbeat *q*-PLL.

V. EXPERIMENTAL RESULTS

Digital Signal Processors can be divided into two families named as *fixed-point* and *floating-point* arithmetic processors. In most of the cases, the use of a *floating-point* processor results in best technical solutions for digital controllers. However, if the cost is critical, *fixed-point* processors could be a cheaper solution if the performance of the digital controller is not drastically affected [11]. These considerations lead us to implement and to test the digital model of the *q*-PLL into the Texas TMS320F243 *fixed-point* DSP.

On the other hand, there are a lot of problems to implement digital controllers in DSPs. The coefficients of the equations and gains of the controllers have to be represented in limited word-length. In addition, the results of mathematical operations have also to fit in a limited word-length and may lose part of the final result.

These problems are referred to quantization and truncation errors and can cause oscillations and instabilities.

Another problem is the overflow of registers. Successive mathematical operations, in most processors, can make in the result of a calculation go to from the most positive to the least negative.

Therefore, before the practical implementation of the *q*-PLL model, the developed algorithms were tested using in C/C++ program where the variables are integers and they have their length fixed to 16 bits. Fig. 9 shows an example of the sampled AC system voltage and the signal detected by the digital *q*-PLL. Since the obtained results were similar to those presented previously the digital PLL algorithm was implemented into the DSP.

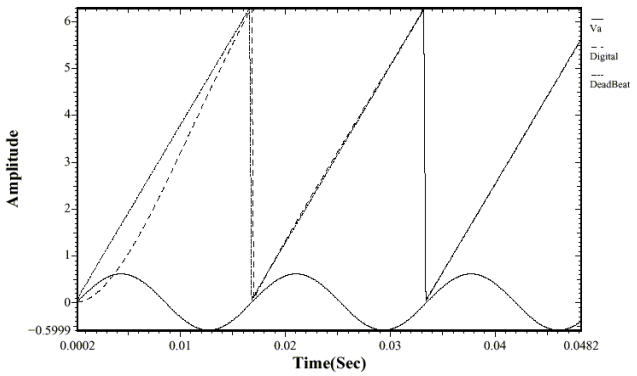

Fig. 9: AC phase voltage and the detected phase angle of the *q*-PLL.

Fig. 10 shows the block diagram of the experimental *q*-PLL implemented into the TMS320F243 DSP with a clock frequency of 20 *MHz* [11]. The proposed PLL algorithm was implemented in assembly to improve the performance of the detected frequency routine. The voltage generator uses the own DSP to synthesize the arbitrary voltages waveforms of the utility system with various conditions to test the performance of the proposed PLL. The three-phase voltages waveforms are sampled with 5 *kHz* and have 10 bits of resolution.

Fig. 11 shows the system utility voltage during the startup process of the digital *q*-PLL and the detected system frequency, respectively. This procedure is equivalent to step change the system voltage from zero to 60 *Hz* in $t = 0\ ms$. The damping ratio ( ) and the undamped natural frequency of the digital *q*-PLL were chosen as 0.707106 and 235.58 *rad/s*. Considering the sampling period of $T_S = (1/f_s) = 0.0002\ s$, the gains were designed to be $k_p = 192.257\ rad.s^{-1}/vai$ and $k_i = 32042.94\ rad/vai$. Note that the *q*-PLL spent less than 4.17 *ms* to track the system frequency.

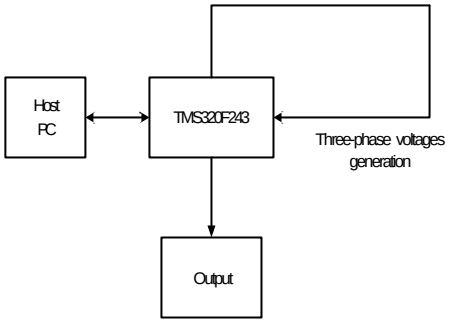

Fig. 10: Block diagram of the implementation *q*-PLL in the DSP

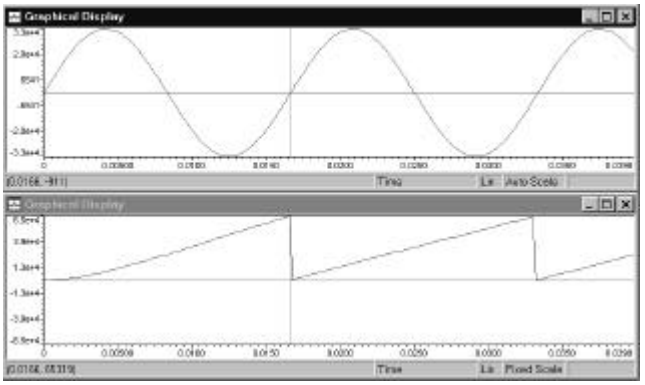

Fig. 11: Utility system voltage (upper trace) and the digital *q*-PLL detected system frequency (lower trace).

Fig. 12 repeats the previous simulation however the phase of the system voltage is - /2 *rad* (-90º). It means that in $t = 0\ ms$, when the *q*-PLL is turned-on, the system voltage is stepped changed from zero to 60 *Hz* but the magnitude of the voltage has its maximum negative value. It is possible to conclude, comparing the lower traces of Fig. 12 and Fig. 11, that in both cases the digital PLL has a good performance.

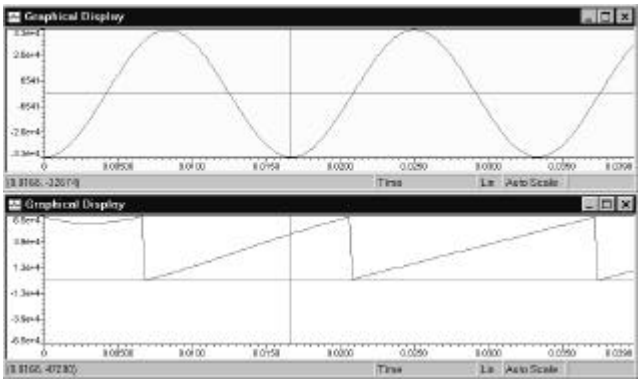

Fig. 12: Utility system voltage (upper trace) and the digital *q*-PLL detected system frequency (lower trace).

Fig. 13 shows the system utility voltage and the detected system frequency for the deadbeat *q*-PLL. In this case, as explained before, the only designed parameter is the sampling period. Thus, choosing $T_S = 0.0002\ s$, the controller gains was designed as $k_p = 2500\sqrt{3}\ \ rad.s^{-1}/vai$ and $k_i = 8.33\ \ 10^6\sqrt{3}\ \ rad/vai$.

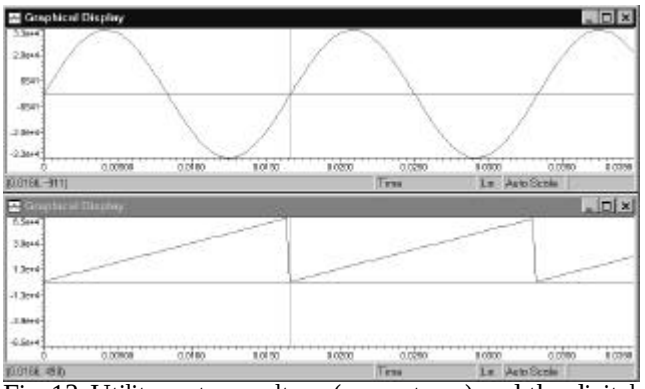

Fig. 13: Utility system voltage (upper trace) and the digital *q*-PLL detected system frequency (lower trace).

The deadbeat *q*-PLL algorithm was also tested using a system voltage phase-shifted by $-\ /2\ rad$ (-90º). In $t = 0\ ms$, the system voltage is stepped changed from zero to 60 Hz but its magnitude has its maximum negative value. As shown in Fig. 14, the deadbeat PLL tracks the system frequency very fast.

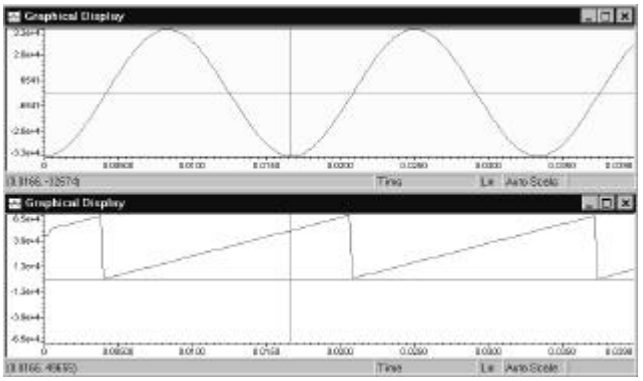

Fig. 14: Utility system voltage (upper trace) and the digital *q*-PLL detected system frequency (lower trace).

Comparing the results presented from Fig. 11 to Fig. 14 it is possible to observe that the deadbeat version of the *q*-PLL is faster than the digital one. In the worst case, while the digital *q*-PLL model spend approximately 8.33 *ms* to track the utility system frequency and phase the deadbeat version of the proposed controller uses two samples only (0.0004 *s*).

VI. CONCLUSIONS

This work presented a PLL model based on the instantaneous power theory. Mathematical models, based on continuous and discrete time, were used to design the PLL gains. Digital simulation and experimental results show that the proposed PLL model could detect the utility system frequency and phase with precision. However, lots of research must be carried on in order to improve the performance of the proposed circuit operating under unbalanced or distorted voltages and currents.

VII. REFERENCES

[1] N.G. Hingorani and L. Gyugyi, "Understanding FACTS – Concepts and Technology of Flexible AC Transmission Systems", IEEE Press, 1999.

[2] R. Ramakumar et al, "Renewable Technologies and Distribution Systems", IEEE Power Engineering Review, Vol. 19, No. 11, Nov. 1999, pp. 5-14.

[3] V. Kaura and V. Blasko, "Operation of a Phase Locked Loop System Under Distorted Utility Conditions", IEEE Transactions on Industry Applications, Vol. 33, No.1, 1997, pp. 58-63.

[4] S.K. Chung, "A Phase Tracking System for Three Phase Utility Interface Inverters". *IEEE Transactions on Power Electronics*, vol. 15, 2000, pp. 431-438.

[5] H. Akagi, Y. Kanazawa and A. Nabae, "Instantaneous Reactive Power Compensator Comprising Switching Devices Without Energy Storage Components", *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, 1984, pp. 625-630.

[6] E. H. Watanabe, R. M. Stephan and M. Aredes, "New Concepts of Instantaneous Active and Reactive Power for Three Phase System and Generic Loads", *IEEE Transactions on Power Delivery*, vol.8, 1993, no. 2.

[7] P.G. Barbosa, "Compensador Série Síncrono Estático Baseado em Conversores VSI Multipulso", *D.Sc. Tese*, COPPE / UFRJ, Rio de Janeiro, RJ, Brasil, 2000.

[8] E.M. Sasso *et al*, "Investigação dos Modelos de Circuitos de Sincronismo Trifásicos Baseados na Teoria das Potências Real e Imaginária Instantâneas (p-PLL e q-PLL)", Anais do Congresso Brasileiro de Automática - 2002, Natal, Brasil.

[9] K. Ogata, "Modern Control Engineering", Prentice Hall, 3rd edition, 1997.

[10] K. Ogata, "Discrete-Time Control Systems", Prentice Hall, 2nd edition, 1994.

[11] TMS320F2x *User's Guide*, Texas Instruments, TX, 1992.