TCSC OPERATION AS SOLID-STATE CURRENT LIMITER

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***Abstract* - This paper describes the use of TCSC (*Thyristor Controlled Series Capacitor*) working as a Solid State Current Limiter. The studied device allows the reduction of a short circuit current in a transmission or distribution network due to the connection of a LC resonant circuit in series with the line. The TCSC with the detection fault current logic controller and the thyristors gate pulse generator were implemented in the ATP/EMTP (*Alternative Transients Program* / *Electromagnetic Transients Program*) simulation package. The digital simulation results showed that the proposed device works very fast.**

Keywords – TCSC, Fault current limiter, electronic circuit breaker.

I. INTRODUCTION

The limitation of short circuit currents in transmission and distribution systems increases the system reliability and safety, prevents equipments breakdown, minimizes switching transients and improves power quality for costumers [1]. Nowadays, there is commercial Fault Current Limiter (FCL) based on reactor that is inserted in series with an ac line when a fault current is detected. However, in high power applications they demand a very large area in the power stations that constitutes a disadvantage [2]. On the other hand, fault current limiters based on resistor technologies are smaller than reactor based FCL, but they could be used only in medium voltages systems ($< 25\ kV$)[3].

Considering the above problems, many electric utility companies are very much interested in the studies involving new solutions to improve the limitation of short circuit current in their networks. In this way, several studies have been testing the usage of fault current limiters based on power electronic semiconductor switches such as Thyristors and GTOs (Gate Turn-off Thyristors). These devices are named in the literature as Solid State Current Limiters (SSCL) and its main function is to reduce the short circuit currents in a transmission or distribution path, as fast as possible, improving the performance and the operation of conventional circuit breakers[4].

Fig. 1 shows the basic diagram of a TCSC that consists of a series capacitor with a parallel TCR (Thyristor Controlled Reactor) [5]. Also connected in parallel, the TCSC has a metal oxide varistor (MOV) for overvoltage protection and a by-pass switch to provide a path for the line current when the TCSC is out of work.

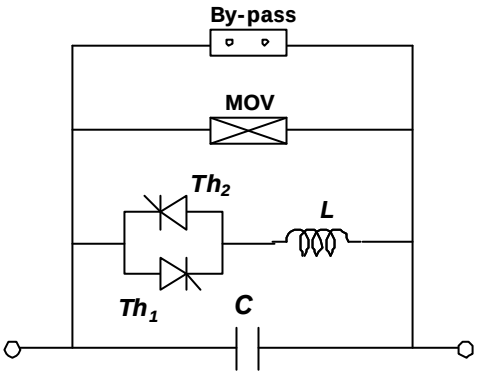


Fig. 1: Basic TCSC configuration.

Since the thyristor technology is well known, this work will focus on Solid State Circuit Limiter based on these switches. Thus, this work aims at presenting the modeling and the analysis of a TCSC (*Thyristor Controlled Series Capacitor*), operating as an electronic fault current limiter. The proposed compensator and its control blocks were implemented in the Alternative Transients Program/Electromagnetic Transients Program (ATP/EMTP) simulation package which was used to test the efficiency of the TCSC in reducing large currents in an ac transmission line.

II. BASIC CONCEPTS

In [6] it was presented a complete mathematical formulation for the steady-state voltages and currents through the TCSC. The developed methodology permits to derive the impedance of the TCSC for any thyristor-firing angle at the fundamental frequency as shown below:

$$X_{TCSC}( ) = \frac{2}{C} \quad \frac{2( )}{C\left({}^{2} \quad {}^{2}_{0}\right)} \quad \frac{4 \ {}^{3}_{0}}{C\left({}^{2} \quad {}^{2}_{0}\right)}.\cos^{2} \quad \tan \frac{{}_{0}}{{}^{2}_{0}\left({}^{2} + {}^{2}_{0}\right)}(\quad) \quad \frac{{}^{2}_{0}\left({}^{2} + {}^{2}_{0}\right)}{C\left({}^{2} \quad {}^{2}_{0}\right)}\sin 2 \qquad (1)$$

where, is the thyristors firing angles in (*rad*); $_0$ is TCSC angular resonance frequency in (*rad/s*); is angular fundamental frequency in (*rad/s*) and C is the fixed capacitance of the TCSC in (*F*).

Fig. 2 shows the TCSC characteristic, obtained from (1), for a sinusoidal current flowing through the AC line and considering L = 15 *mH* and C = 212 F. Modifying the firing angle of the TCR's thyristors [5]-[7], a variable capacitive impedance (series voltage lags of line current) can be synthesized by the TCSC as shown in Fig. 2. The Thyristor Controlled Series Capacitor is a FACTS (Flexible AC Transmission Systems) device that has been proposed initially to control power flow and to damp power oscillation over transmission lines.

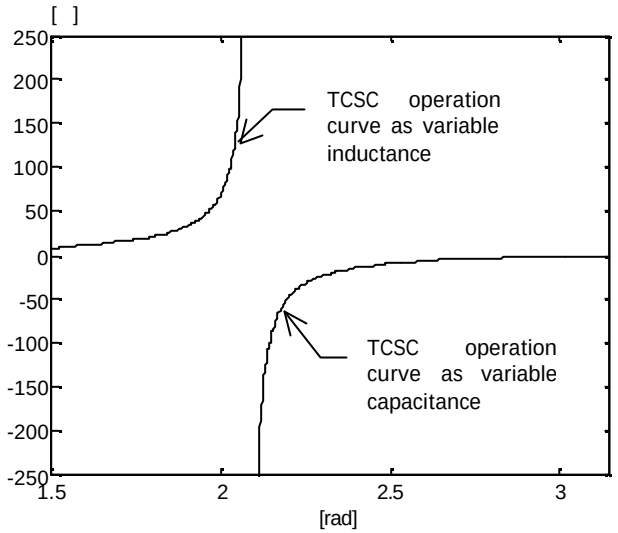


Fig. 2: Characteristic curve of the TCSC x Thyristors firing angles.

The other part of the characteristic curve of Fig. 2, before the resonance frequency, shows that the TCSC could synthesize a variable inductive impedance (series voltage leads of line current). However in both cases, due to the thyristor phase control, harmonics of voltages and currents will appear at the capacitor terminals and flowing through TCR inductance, respectively.

Based on the above discussion, if the TCSC is operated with inductive characteristic and near its resonance frequency, it can emulate large inductive impedance in series with the line. This action allows the TCSC to operate as a Solid-State Current Limiter. However, to avoid generation of harmonics by the TCSC, the inductance and the capacitance are designed to have a resonance in 60 *Hz*.

Fig. 3 shows the TCSC modified characteristic for its operation as SSCL. This figure was obtained, from (1), for L = 454 *mH* and C = 15.5 F. There are different values of L and C that satisfy the condition of resonance frequency equal to 60 *Hz*. However, the capacitance of the TCSC should be designed to present low reactance in series with the protected AC line during the normal operation of the solid-state current limiter.

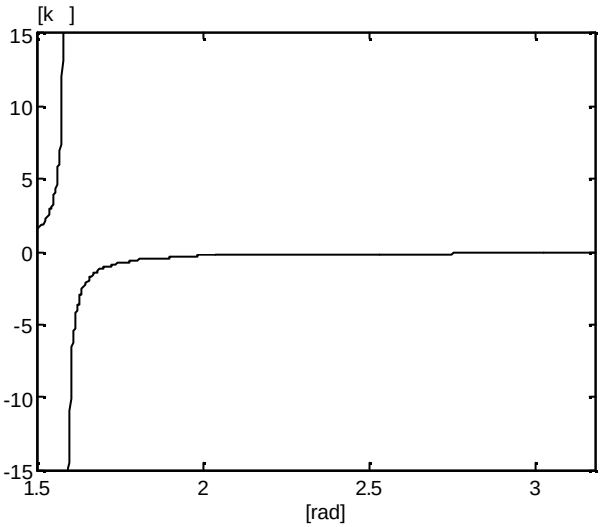


Fig. 3: TCSC characteristic curve for its operation as SSCL.

During the normal operation of the TCSC as SSCL, the thyristors are fired at = 180º (/2 *rad*) and the line current flows only through the series capacitor. Otherwise, when a fault occurs, the thyristors are fired at = 90º (/2 *rad*) to emulate a high impedance in series with the AC line in order to reduce the fault current.

Based on Fig. 3 and assuming that the thyristors are turned on only in 90º (/2 *rad*) or 180º (*rad*), if the AC line current is sinusoidal, the voltage across the TCSC will be always sinusoidal and the equivalent impedance of the TCSC, at the fundamental frequency, is given by [7]:

$$X_{TCR}( ) = \frac{L}{2 \quad 2 \ + sen(2 \ )}, \qquad (2)$$

where, is the thyristors firing angles in (*rad*); is angular fundamental frequency in (*rad/s*) and L is the inductance of the TCR in (*H*).

From (2) and considering the previous approximation, the equivalent impedance of the TCSC operating as SSCL can be calculated considering the connection of the $X_{TCR}(\ )$ and the X_C in parallel, at the fundamental frequency, and it is given by:

$$X_{SSCL}(\ ) = \frac{L}{^2LC \quad 2 \quad +2 \quad sen(2\ )} \qquad (3)$$

Fig. 4 compares the equivalent impedance of the TCSC obtained using (1) and (3) respectively. Since the results for = 90º (/2 *rad*) or 180º (*rad*) are identical, the relation (3) could be easily used to design the components of the SSCL.

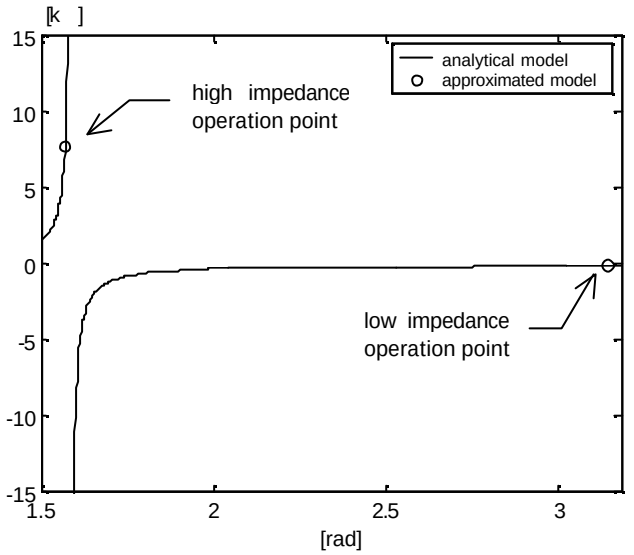


Fig. 4: TCSC characteristic curve for its operation as SSCL.

However in practical applications, errors could make the thyristors turned on with angles a little smaller than 90º. In this case a DC current component will flow into the TCR. It can saturate the inductor causing the shutting-down of the device.

On the other hand, if the thyristors are turned on with an angle little larger than 90º the SSCL will be forced to operate from its maximum inductive to its maximum capacitive characteristic. In this case the equivalent series impedance of the system is reduced, and the fault current will be increased. To avoid these problems the SSCL components are designed to force a resonance between the L and C for an angle a little greater than 91º.

III. Control System and Thyristors Firing Pulses Generators

The main objective of this work is the investigation of the operation of the TCSC limiting short circuit currents. Thus, the detection fault current block was implemented in a very simple way as shown in Fig. 5. Two signals, proportional to the magnitude and to the derivative of the line current respectively, are compared with two threshold values. Then, when a fault current is detected the output signal (CTRL) goes to logic level 1, indicating that the TCR's thyristors should be fired at 90º (/2 *rad*) as explained before. A *Track* block is used to hold the CTRL signal during a pre-established time to avoid the SSCL being switched on and off continuously whenever the fault is not cleaned. Otherwise, the CTRL signal goes to low level and the thyristors are fired at 180º (*rad*) with respect to the voltage at the capacitor terminals.

The synchronization of the thyristors fire pulses uses a double ramp integration scheme as shown in Fig. 6. The controllable voltage V_C is varied from 0 *V* (= 180º) to 0.5 *V* (= 90º) and it is proportional to the thyristor conduction angle. The output of integration block is reset whenever the thyristor firing pulse is generated. The auxiliary signal NC is 1 when the thyristors valves are not conducting and zero otherwise. This method is well explained in [8] and it has the advantage of not requiring the knowledge of the zero crossing instant of the capacitor voltage. Fig. 7 (a), (b), (c) and (d) show the TCR voltage, the TCR current, the double integration ramp and the thyristors firing pulses for = 135º. These curves are obtained considering a sinusoidal voltage across the TCR terminals and are normalized.

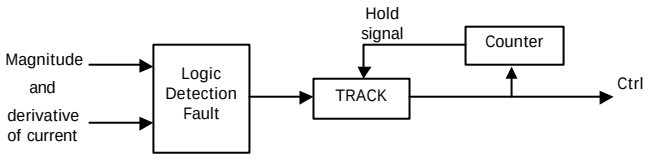


Fig. 5: Simplified detected short circuit current block.

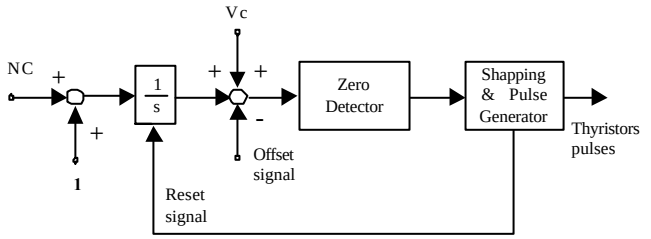


Fig. 6: Fire pulse synchronization block.

IV. Digital Simulation

In order to verify the performance of the TCSC operating as a SSCL, a single-phase limiter was implemented in the ATP/EMTP simulation package as shown in Fig. 8. The FCL was implemented as shown in Fig. 1. The source was modeled as a 132 *kV* phase-to-ground ideal voltage source behind a synchronous

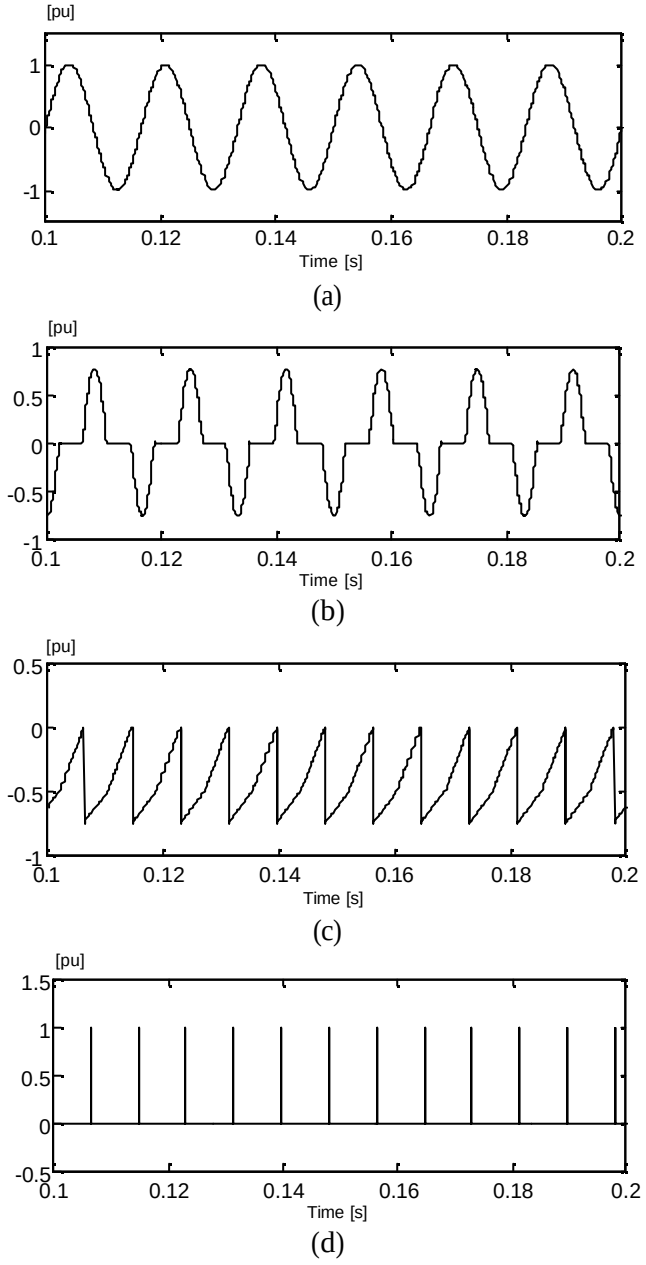


Fig. 7: Thyristor controlled reactor signals: (a) voltage, (b) current, (c) the double integration ramp and (d) firing pulses for = 135º.

reactance. The transmission line length, its series resistance and its inductance are 300 *km*, 0.0216 */ km* and 0.548 *mH / km*, respectively. The load was modeled as constant impedance equal to (1 + *j* 37.7) *k* . The SSCL was designed with the same *L* and *C* showed before, that is 444 *mH* and 15.5 F. The control system and thyristor fire pulse generator blocks were implemented using TACS (*Transient Analysis of Control System*).

Fig. 9 shows the line current of the system when a short circuit occurs at the receiving end line terminals. The system is in steady state with nominal current when in *t* = 50 *ms* a fault is applied at the load terminals. The fault duration is limited to 15 *ms*. Note that the fault current amplitude increases 8 times of the nominal current magnitude approximately.

Fig. 10 (a), (b), (c) and (d) show respectively the line current through AC line, the current flowing into the TCR, the voltage across the series capacitor and the system voltage measured at the sending end terminals when a 15 *ms* duration fault occurs at the load transmission line terminals. The simulation results were obtained for the SSCL connected at the sending end line terminals. From Fig. 10 (a), the peak of the fault current is 2502 *A*. The usage of the SSCL limits the fault current to 5 times of the nominal current.

To test the performance of the SSCL under a more severe condition, a fault is applied at the sending end transmission line terminals. Fig. 11 shows the line current of the system. The system is in steady state with nominal current and a fault is applied in *t* = 50 *ms*. As in the previous case, the fault is limited to 15 *ms*. However, since the system impedance is lower, the fault current first peak increases approximately 36 times of the nominal current magnitude.

Fig. 12 (a), (b), (c) and (d) show respectively the line current through AC line, the current flowing into the TCR, the voltage across the series capacitor and the system voltage measured at the sending end terminals when a 15 *ms* duration fault occurs at the load transmission line terminals. The simulation results were obtained for the SSCL connected at the sending end line terminals. In this case, from Fig. 12 (a), it is possible to conclude that the peak of the fault current is limited by SSCL to 6 times approximately of the nominal line current.

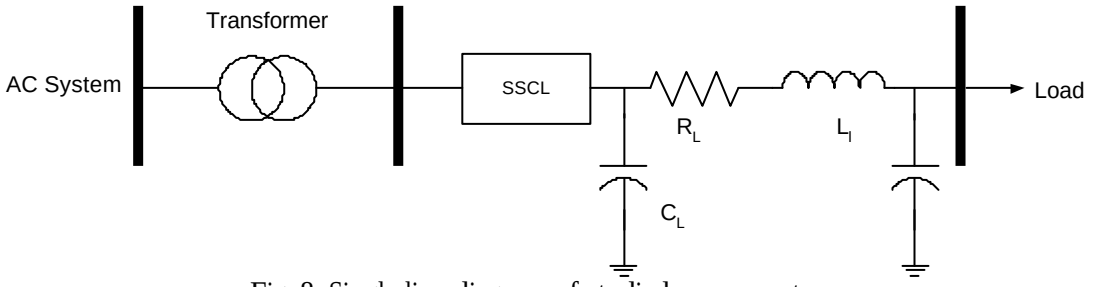


Fig. 8: Single line diagram of studied power system.

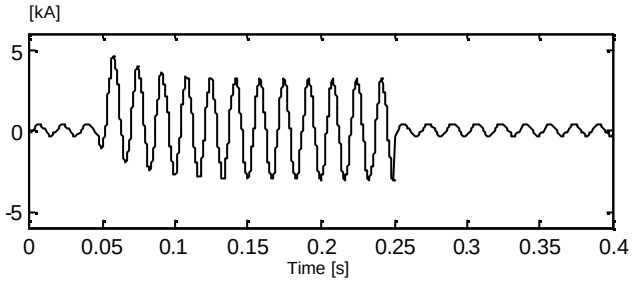


Fig. 9: Current through the system for a short circuit at the load terminals (without SSCL).

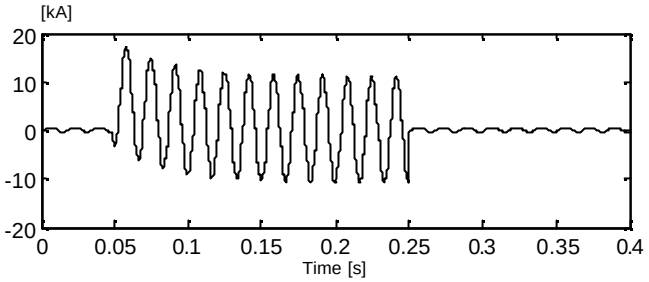
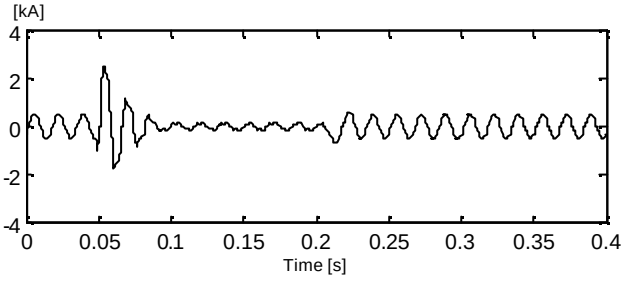
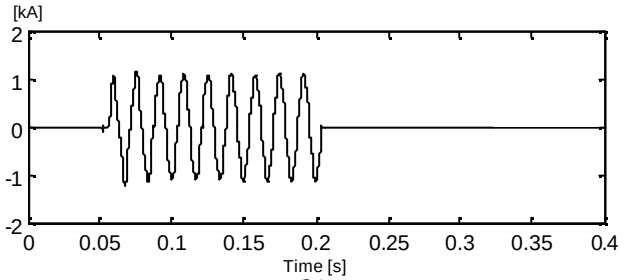


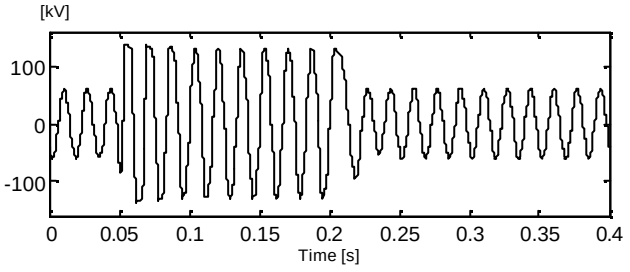
Fig. 11: Current through the system for a short circuit at the sending-end transmission line terminals (without SSCL)



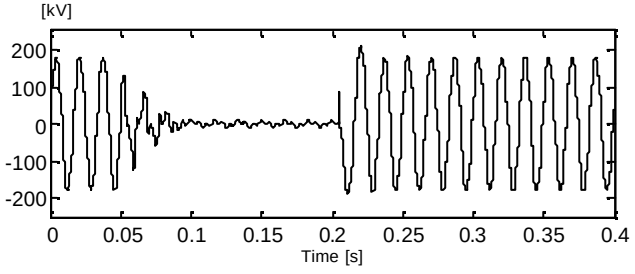
(a)



(b)

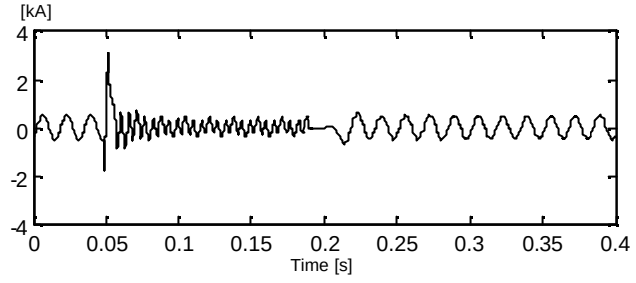


(c)

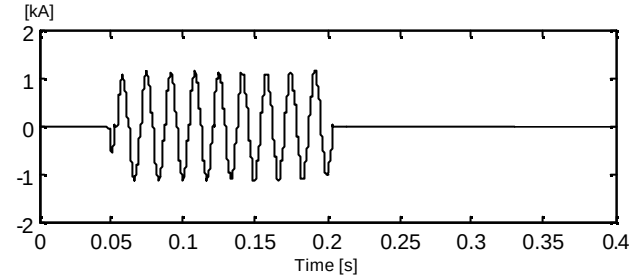


(d)

Fig. 10: Short circuit at the load terminals with the SSCL: (a) line current, (b) TCR current, (c) capacitor voltage and (d) sending end line phase voltage.



(a)



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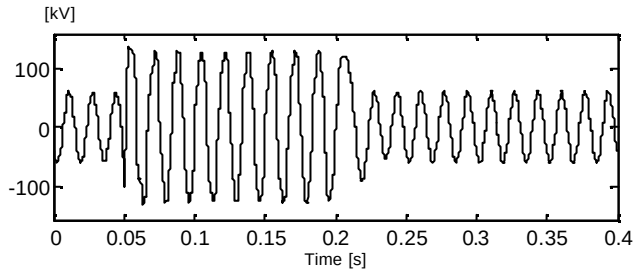
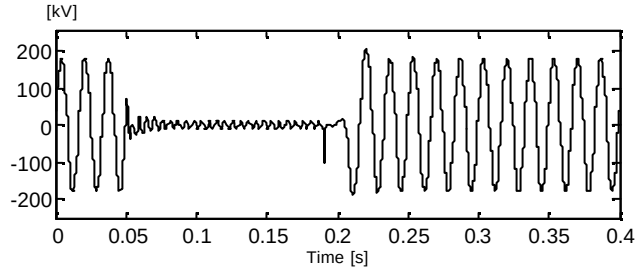


(c)



(d)

Fig. 12: Short circuit at the sending end line terminals with the SSCL: (a) line current, (b) TCR current, (c) capacitor voltage and (d) sending end line phase voltage.

Fig. 10 and Fig. 12 shows that the SSCL have a good performance to limit the fault current through the AC system. However, observing Fig. 10 (b) and Fig. 12 (b), it is possible to see that, during the fault, the current through the TCR has a high magnitude while the line current has its magnitude limited. This characteristic is the main disadvantage of the proposed device since during the fault period the voltage at the capacitor terminals is equal to the system phase voltage. Then, the TCR inductor plus the thyristors valves should be designed to support to block a high voltage and to conduct a high current.

One alternative to overcome this problem is to use SSCL topology where the resonance circuit is formed by a series connection of a thyristor controlled inductor and a fixed capacitor. However, in consequence of lack of space the results of this topology will not be present here.

V. CONCLUSIONS

This work provides an analysis of the TCSC operating as a Solid-State Current limiter. The EMTP was used to model and to illustrate the efficiency of the SSCL to reduce the short circuit currents in a transmission line. The obtained results showed that the fault current could be reduced approximately 90% for a sending end transmission line short circuit. The application of SSCL in transmission and distribution system is an attractive alternative to improve the power system quality and reliability.

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