DIGITAL CONTROL OF THREE-PHASE/SWITCH/LEVEL BOOST RECTIFIER USING ADMC401

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***Abstract*—This article presents the study and implementation of a three-phase three-level pre-regulator rectifier with digital control using a DSP. The structure has a common capacitive center point that allows the three-level operation and a low blocking-voltage stress on the power switches (half of dc-link voltage). The reduction of blocking voltage allows the use of low cost and low losses power devices, increasing the efficiency and the power density with reduced production cost. The control technique used aims to obtain power factor correction (PFC), regulated and balanced output voltages. With the advance of DSP controllers, digital control is increasingly used in power converts systems and offers a number of advantages like more flexibility in modification code and less sensitive to noise. However, sampling time delay, resolution of A/D converter, word length of DSP and instructions cycle time are disadvantages over analog control. Nowadays, control optimized DSP's deliver high performance, great code efficiency and optimal peripheral integration for the digital control with high level on-chip integration to deliver system cost reduction, and powerful computational abilities that enable software innovation then reducing disadvantages of a digital control. The DSP used is the ADMC401 from ANALOG DEVICES.**

KEYWORDS

Three-phase rectifier, digital signal processor, DSP, power factor corrections, ADMC401.

I. INTRODUCTION

The telecommunications rectifiers are normally composed by two stages connected in series: a high power factor preregulator and a dc-dc converter. The development of new topologies of three-phase high power factor switched mode rectifiers, utilized in telecommunications systems, is a very important research topic in order to comply with the standard regulations, which become more and more severe, and to obtain the requirements of low production cost, high power density, high efficiency and reliability.

Recently, three-phase three-level boost rectifier topologies were presented [1, 2,]. These topologies utilize one bi-directional switch per phase, resulting in a lower control and driving effort. The three-level operation allows the obtainance of a lower harmonic RMS value of the mains current than the two-level topology. However, the major advantage of the three level structures is the reduction of the voltage stress on the power switches. Only half of dc-link voltage is applied across the power switches allowing the use of low losses and low cost power devices (IGBT/MOSFET). Besides, the blocking behavior of the diodes is improved resulting in lower switching losses in the active switches. These characteristics make the three-level structures very attractive for a low cost solution with high.

II. DIGITAL CONTROL OF THE THREE-PHASE THREE -LEVEL RECTIFIER

The modulation strategy used is based on the appropriate variation of the duty cycle at a constant frequency. The control technique applied is called control by means of instantaneous average values of the input current [7]. This technique consists of monitoring the input current of the converter, making it follow a sinusoidal reference with the smallest error possible. This imposition is achieved through the appropriate high frequency switching control of the converter's switches. This control automatically regulates the output voltages and keeps them in balance. The control algorithm described was implemented using the ADMC401 – Digital Signal Processor (DSP)

Figure 1 shows, using a block diagram, the digital control circuit used to command and control the rectifier. The topology of PWM rectifier was proposed by J.W. Kolar [1] (VIENNA rectifier). As indicated in Fig.1, eight signals are required to implement the control algorithm. These are, the rectifier input voltages (V_R, V_S and V_T), the inductors currents (I_R, I_S e I_T), and the DC bus capacitors voltages (V_{01} and V_{02}).

The converter is controlled basically by two feedback loops. The inner loop that shapes the input current is a faster loop whereas the average output dc voltage is regulated by a slow response. Each of the output voltages is sensed and the sum of them are regulated in the same designed voltage reference (Vref). The necessary corrections to maintain the total output voltage (V_{01}+V_{02}) in the specified reference are done through the digital voltage controller that increase or decrease the amplitude of current reference waveform signal in each one phases.

The difference between the output voltage on the capacitors (V_{01} and V_{02}) in relation the center point is utilized to insert an offset in the current waveform reference. With this current offset, the charge current of the lower voltage capacitor will increase and the charge current of the higher voltage capacitor will decrease, providing the output voltages balance. Adding a positive or a negative value to the reference currents imposes a positive or negative average value to the center point current, without distorting the input

currents.

The instantaneous signals, input voltages (V_R, V_S and V_T), inductors currents (I_R, I_S and I_T) and the DC bus capacitors voltages (V_{01} and V_{02}) are all sensed and conditioned by the respective interface circuit. The sensed signal are then fed back to the DSP via eight ADC channel Vin0, Vin1, Vin2, Vin3, Vin4, Vin4, Vin5, Vin6, and Vin7.

The digitized sensed V_{01} and V_{02} are summed and compared to the desired reference total bus voltage V_{ref} . The error signal V_{error} is then fed into the digital voltage controller. The output of the voltage loop controller (U_V) is multiplied by the V_{IN} to generate the reference current for the inner current loop. The V_{IN} is result of instantaneous sensed signal of input voltage summed with the difference signal (V_{01}-V_{02} = offset).

In Fig.1, I_{Rref} is the reference current for the current loop, I_{Rref} has the shape of a sinewave and it's amplitude is such that it maintains the total output dc voltage at a reference level V_{ref}, against variation in load and fluctuation in line voltage. The inductor current I_{IN} is compared with the reference current I_{Rref}, the difference between them is passed into the digital current controller. The output of this controller is finally used to generate the PWM duty cycle command for the three – phase rectifier switch.

Figure 1 shows, using a block diagram, the power factor correction (PFC) stage interfaced to an ADMC401 from ANALOG DEVICES. The diagram of Fig. 1 shows the three-phase rectifier control for one phase (R), the other phases are the same way.

A Digital Voltage Controller

This Block is responsible by the converter output voltage regulation. The resultant control action in the output of this regulator will contribute in the reference current composition (I_{Rref}), whose input is a resultant error signal of total voltage sampling in the output voltage (V_{01}+V_{02}) of the converter and a reference voltage (V_{ref}) pre-established in the design.

B. Digital Current Controller

The reference of current is compared with a current sample in the inductor, producing an error signal that is applied to the current regulator. The control action in the output of this block is applied to the PWM modulator (Pulse Width Modulation).

C. PWM

The control action in the output current regulator U_I is compared with a triangular signal in PWM block, resulting the switches command PWM signal. This PWM signal is applied to both switches.

The converter representation with the current and voltage, respective loops controls are shown by means of simplified blocks diagram in Fig.2.

D. Converter model

It is necessary to know the converter model to design adequately the current and voltage regulators with the power factor correction goal, converter output voltage regulation and balance.

For the current loop the converter transfer function must take into consideration the input current *($IL_{R,S,T}$),* related to the control variable, in this case the duty cycle (1). A methodology for modeling was proposed by [14,15]. Thus it arrives to the following transfer function of the converter, taking into consideration the input current and duty cycle (2).

$$Gi(s) = \frac{I_{R,S,T}(s)}{D(s)} \tag{1}$$

$$Gi(s) = \frac{Vo_{1,2}}{s.3.L} \tag{2}$$

By the same way, to design the voltage regulator it is necessary to determine the transfer function that relates the output voltage to the current in the inductor (3):

$$Gv(s) = \frac{Vo_{1,2}(s)}{I_{R,S,T}(s)} \tag{3}$$

Through the output stage analysis [15], the result is given by (4):

$$Gv(s) = 3.\left(\frac{\sqrt{2}.V_{R,S,T}}{Vo_{1,2}.\pi} + \frac{1}{2}\right).\frac{Ro_{1,2}}{s.Co_{1,2}.Ro_{1,2}+1} \tag{4}$$

Where:
$Ro_{1,2}$: Load resistances.
$Co_{1,2}$: Output capacitances.
$Vo_{1,2}$: Output Voltages.
$V_{R,S,}$: Phase Voltages.

The voltage and current regulators, employed in the converter control belong to the Proportional-Integral (PI) kind. The allocation criteria of zero and of integrator gain adjustment of current controller are based in [14], where integrator gain must be fitted to satisfy the gain crossing frequency criterion. It concisely is:

$$fc < fs/4 \tag{5}$$

$$\omega_z = \frac{2.\pi.fs}{20} \tag{6}$$

Where:
fc : Gain crossing frequency.
f_S : Switch frequency.
ω_Z: Zero frequency.

The controllers were determined in the continuous time,

and the discrete transfer function through the bilinear transformation, from the controller knowledge in the domain of Z. Applying the transformed Z^{-1} obtaining the controller under a difference equation form that will be implemented digitally.

The voltage gain of the controller was determined through the direct design by the root locus method by the Z-plane.

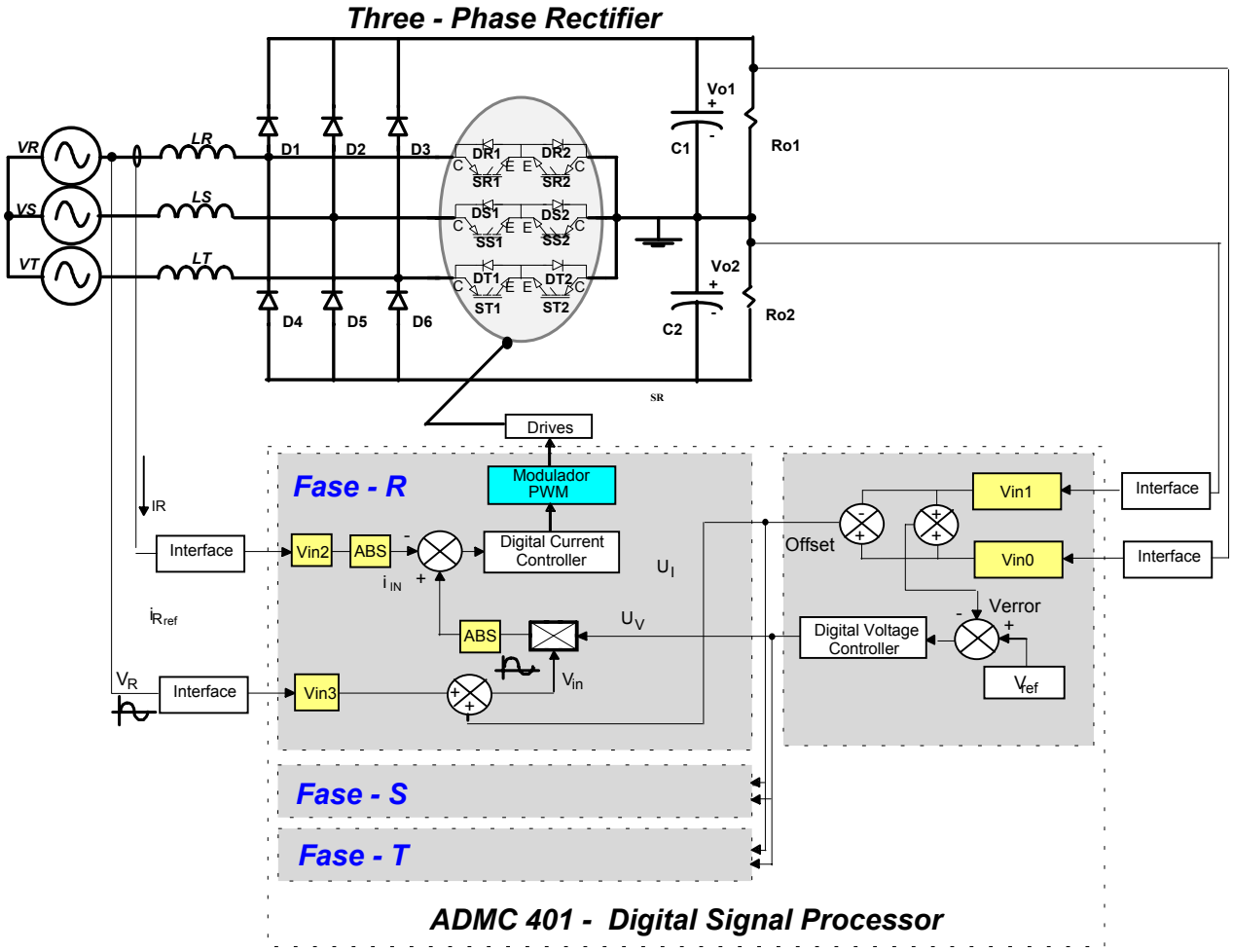

Fig.1 – Control loop block diagram of the DSP controlled PFC rectifier.

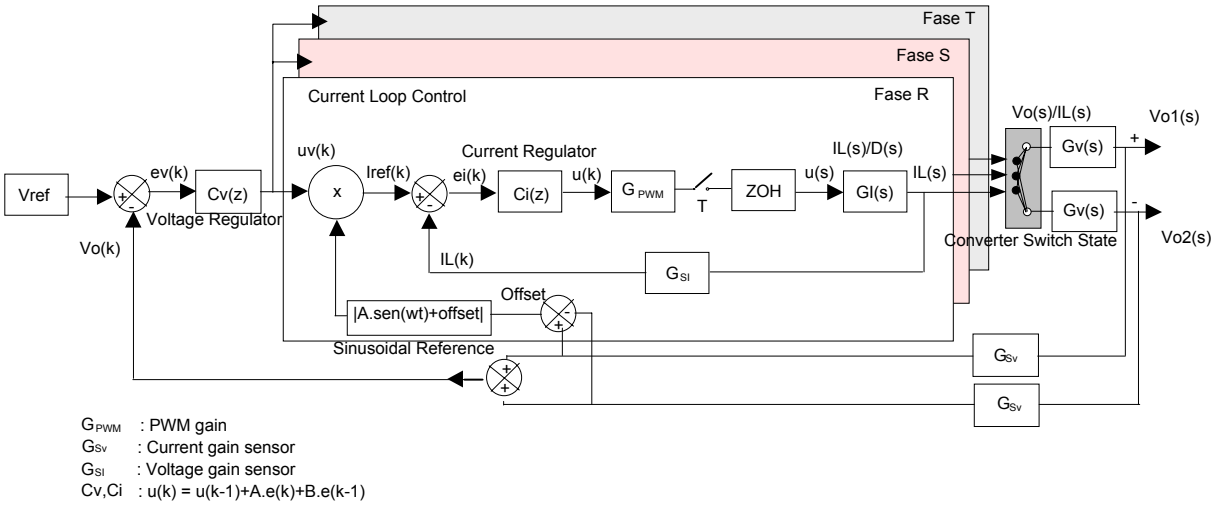

Fig. 2 – Block diagram of the converter control system.

The execution implemented routines sequence blocks diagrams in ADMC401 are exhibited in fig.3.

The control technique described in item II was implemented using DSP ADMC401 of ANALOG DEVICES, whose main characteristic are: 26 MIPS fixed-point DSP core; single cycle instruction execution (38.5 ns); 12-Bit pipeline flash analog-to-digital converter (all eight inputs converted in <2μS) and three-phase 16 bit PWM Generation unit.

The sampling frequency adopted in the voltage variable acquisition and current is 50 kHz. The converter switching frequency is 50 kHz. The PWM controller of the ADMC401 is operating in single update mode, there is a PWMSYNC pulse produced of each PWM period. Consequently, it is possible to produce PWM switching patterns that are symmetrical about de midpoint of the period. With this sampling frequency of 50 KHz, a resolution of about 9 bits PWM of the DSP was achieved. It was used the three-phase 16-bit PWM generation unit of the ADMC401 for the activation of both switches in each on phase, depending on the half-cycle of the AC-mains input voltage, one of the switches will conduct while the other will be blocked.

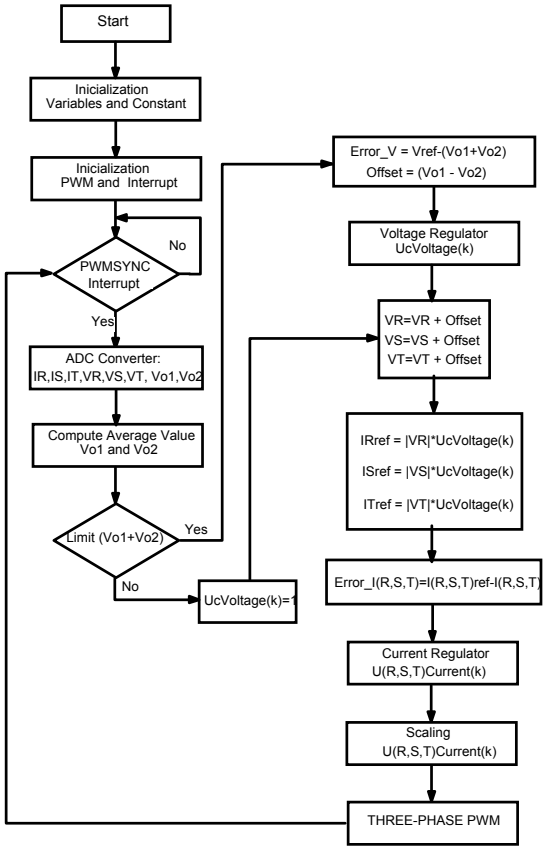

Fig. 3 – Program Blocks diagram.

At the beginning of each PWM period, the control unit of ADMC401 receives a synchronization pulse, change direction an interruption service routine. The ADC conversion process is started on the rising edge of this pulse, them sampling of the output voltages, input voltages and the input phase current are made. From these values the controller calculations (PI) of voltages and the controller (PI) of current. Once the controller control action of current is certain, this value is loaded in the three-phase PWM unit, which itself generates the PWM.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To verify the practical aspects of the digital control proposed by three-phase three-level rectifier, a laboratory prototype was built and tested. The operation specifications are:

Line-to-line Voltage:	V_{RMS} = 220V± 10% (60 Hz)
DC-link Voltage:	V_{DC} = 450V
Switching Frequency:	f_S = 50 kHz
Output power:	P_O = 2.8 kW

Fig.4 shows a converter photo and the environment of ADMC401.

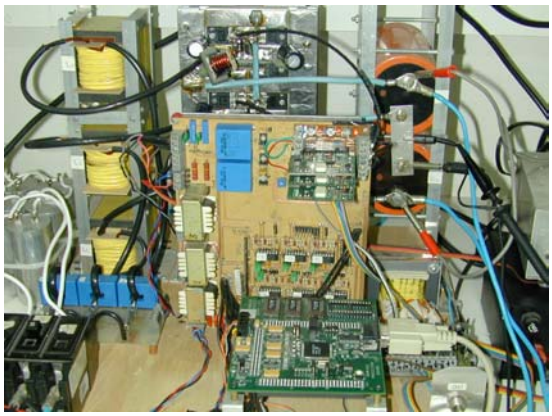

Fig.4 – Implemented prototype photo.

The power circuit of the three-phase three-level pre-regulator implemented is presented in Fig. 5.

The bi-directional switches (S_R, S_S and S_T) are implemented using IGBT's with internal diode. The following components are used in the pre-regulator:

$S_{R1,2}$, $S_{S1,2}$ and $S_{T1,2}$: *IRGPC50UD.*
D_1, D_2, D_3, D_4, D_5 and D_6: *APT30D100K.*
C_1 and C_2: 3300μF/350V
L_R, L_S and L_T: 600μH.

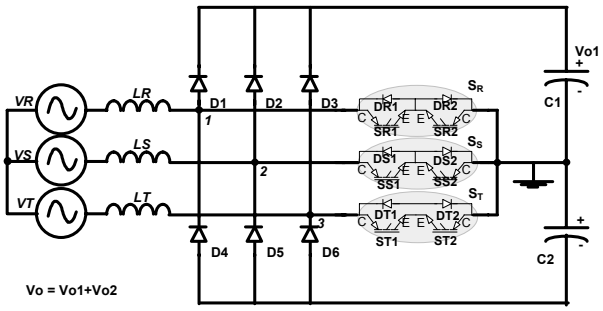

Fig. 5 - Power circuit of the three-phase pre-regulator.

The following figure shows the waveforms of the converter operating at rated power (2800 W). Fig. 6 shows the input current in each phase (I_R, I_S and I_T) and the input phase voltage (V_R) and Fig. 7 shows the input current in each phase (I_R, I_S and I_T) and the total output voltage on the capacitors (Vo_1+Vo_2).

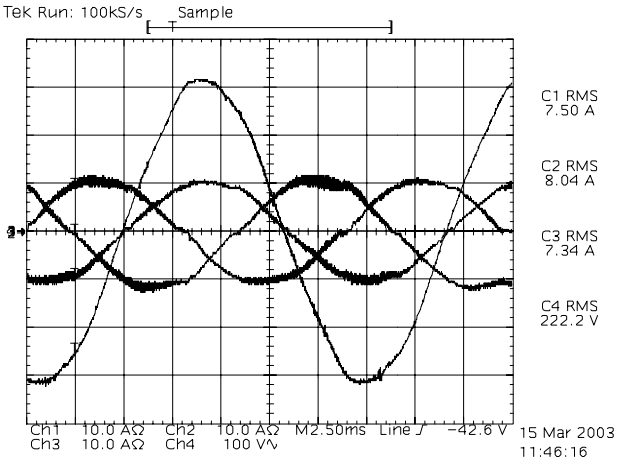

Fig.6 - Input currents (I_R, I_S and I_T), input phase voltage (V_R).

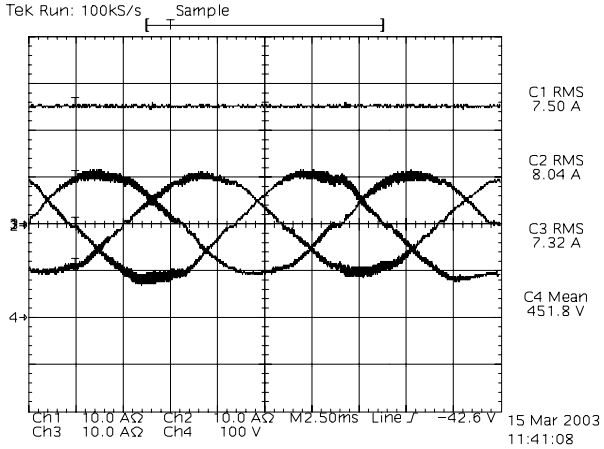

Fig.7 - Input currents (I_R, I_S and I_T), output voltage on the capacitors (Vo_1+Vo_2).

Fig.8, Fig.9 and Fig.10 show the THD diagram of the input current in each phase (I_R, I_S and I_T).

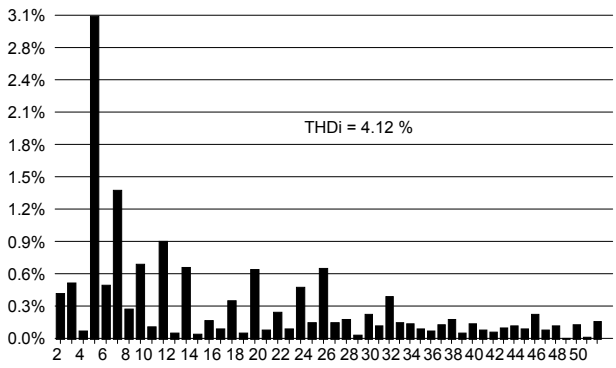

Fig.8 – Harmonic magnitude as a % of the fundamental amplitude of phase R input current.

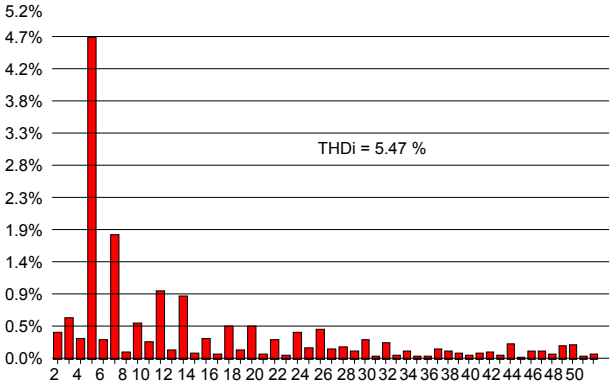

Fig.9 – Harmonic magnitude as a % of the fundamental amplitude of phase S input current

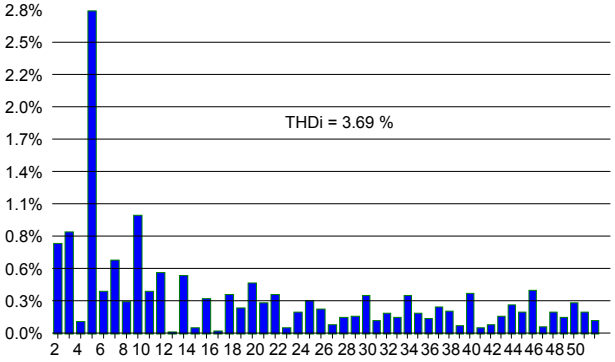

Fig.10 – Harmonic magnitude as a % of the fundamental amplitude of phase T input current

TABLE I

THD of the input current in each phase (I_R, I_S and I_T), THD of the input voltages in each phase (V_R, V_S and V_T) and The Power Factor (PF).

Phases	THD_V	THD_I	PF
R	3.36%	4.12%	0.9985
S	3.49%	5.47%	0.9972
T	3.14%	3.69%	0.9977

Fig. 11 shows the input current in each phase (I_R, I_S and I_T) and the input line voltage (Vin). The converter output Vo_1 are perturbed, it has reductions of 20% in relations of Vo_2. Fig. 12 shows the output voltages on the capacitors Vo_1 and Vo_2 under perturbation.

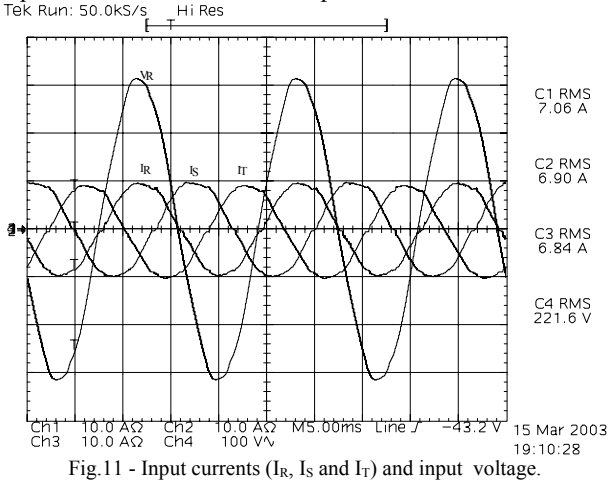

Fig.11 - Input currents (I_R, I_S and I_T) and input voltage.

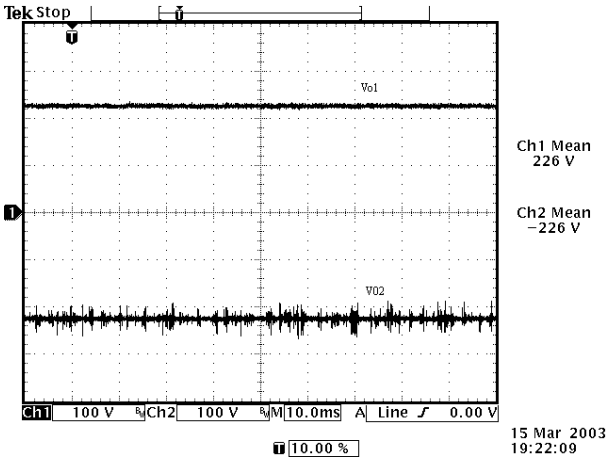

Fig.12 - Output voltage on the capacitors (Vo_1 and Vo_2).

Fig. 13 shows the input current in each phase (I_R, I_S and I_T) and the input line voltage (Vin). The converter output Vo_2 are perturbed, it has reductions of 20% in relations of Vo_1. Fig. 14 shows the output voltage on the capacitors Vo_1 and Vo_2 under perturbation.

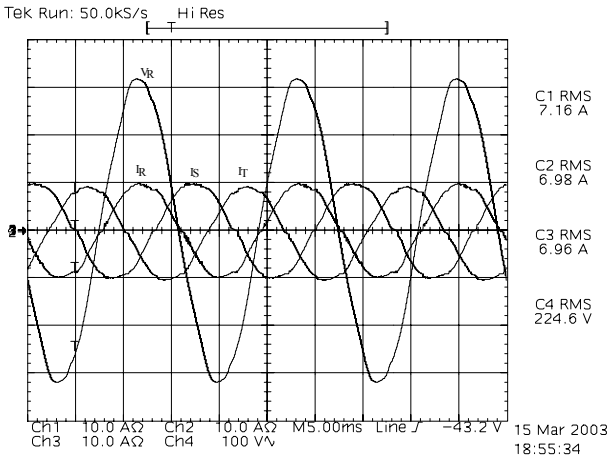

Fig.13 - Input currents (I_R, I_S and I_T) and input voltage.

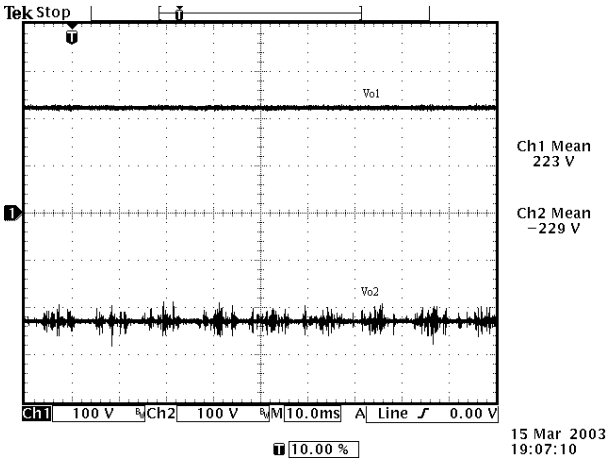

Fig.14 - Output voltage on the capacitors (Vo_1 and Vo_2).

IV. CONCLUSION

This paper proposed the use of digital control and commands a rectifier by using a DSP, looking towards: power factor correction, regulation and balancing of the output voltages. Using digital techniques implemented by a DSP, it is possible to reduce the volume and cost of the command and control circuits; the first is due to the fact that by using the ADMC401, most of the components responsible for implementing the control laws can be eliminated, since these laws are implemented by means of software. As for the cost, these components are becoming more and more accessible and diversified. The final result is a high efficiency, high power factor converter with regulated and balanced output voltages. With the control optimized DSP deliver high performance, great code efficiency and powerful computational abilities, easily we can use more sophisticated and efficient digital control techniques in power electronics converters.

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