AN INTERLEAVED ZCS-FM BOOST RECTIFIER, WITH DIGITAL CONTROL USING A FPGA DEVICE AND VHDL

Carlos A. Canesin [1] and Flávio A. S. Gonçalves [2]
DEE, FEIS-UNESP, São Paulo State University
P.O. Box 31, Ilha Solteira, Brazil
e-mail : (canesin@dee.feis.unesp.br [1], flavio@dee.feis.unesp.br [2])

Abstract – **This paper presents a single-phase high power factor interleaved boost rectifier operating in critical conduction mode employing a soft-switching technique and controlled by Field Programmable Gate Array (FPGA). The soft-switching technique is based on zero-current-switching (ZCS) cells, providing ZC (zero-current) turn-on and ZCZV (zero-current-zero-voltage) turn-off for the active switches, and ZV (zero-voltage) turn-on and ZC (zero-current) turn-off for the boost diodes. The disadvantages related to reverse recovery effects of boost diodes operated in continuous conduction mode (additional losses, and electromagnetic interference (EMI) problems) are minimized, due to the operation in critical conduction mode. In addition, due to the interleaving technique, the rectifier's features include the reduction in the input current ripple, the reduction in the output voltage ripple, the use of low stress devices, low volume for the EMI input filter, high input power factor (PF), and low total harmonic distortion (THD) in the input current, in compliance with the IEC61000-3-2 standards. The digital controller has been developed using a hardware description language (VHDL) and implemented using a XC2S200E-SpartanII-E/Xilinx FPGA, performing a true critical conduction operation mode for a generic number of interleaved cells, and a closed-loop to provide the output voltage regulation, like as a pre-regulator rectifier. Experimental results are presented for a 1kW implemented prototype with two interleaved cells, 400V nominal output voltage and 220Vrms nominal input voltage, in order to verify the feasibility and performance of the proposed digital control through the use of a FPGA device.**

Keywords - **Boost ZCS-FM, critical conduction mode, FPGA control, interleaved techniques and power factor correction.**

I. INTRODUCTION

The power factor correction (PFC) converters have been widely accepted in the power supplies for improving power quality and to achieve the agreement with the international current harmonic standards, like as the IEC61000-3-2 [1-6]. One interesting PFC approach for the boost rectifier is based on operating the boost converter at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In this operation mode the switching frequency is variable, and the reverse recovery related effects are minimized, because there is no stored charge in the boost diode at switch turn on [1, 2].

However, boundary operation requires additional input current filtering and produces peak currents that are at least two times the input current averaged over the switching cycle. This is generally undesirable for high power and power-factor correction applications. Therefore, these disadvantages can be alleviated if two or more converters are interleaved.

Interleaved power conversion refers to the strategic interconnection of multiple switching cells for which the conversion frequency is identical, but for which the internal switching instants are sequentially phased over equal fractions of a switching period. This arrangement lowers the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses. An interleaved system can therefore realize a savings in filtration and energy storage requirements, resulting in greatly improved power conversion densities without sacrificing efficiency [3].

Several low cost commercial integrated circuits are available for implementation of the boundary control mode in a single boost converter. However, there is no available IC capable to provide the ideal operating phase shift among the cells, required by interleaved technique, together with critical conduction mode in the cells. Usually, due to inherent variable switching period, the solution for the determination of the ideal phase-shift lead to a relatively complex analog control circuit [4]. In this context, a digital control can easily incorporate this task by monitoring the switching periods to perform the interleaved technique.

Digital controllers offer advantages over analog controllers such as flexibility, additional processing options, low sensitivity to external influences. Nevertheless, digital control was restricted to relatively high-power applications owing to high cost of devices. On the other hand, in recent years use of digital controllers is increasing even in low-to-medium power applications, due to the advent of fast digital signal processors DSPs with embedding control peripherals such as PWM generation units, A/D converters, etc. However, the main limitation of DSPs is their sequential operation, where the instructions are executed one after the other [5, 6].

On the other hand, the implementation of control systems using programmable logical devices, allows the use of concurrent operations. Thus, in a FPGA, for example, all the control processes are executed continuously and simultaneously, allowing to process algorithms in higher speeds than the provided in a sequential way by the DSPs [3, 8].

A digital control based on programmable logic devices, such as FPGAs, can use the recent advances in digital design methodologies, where hardware description language (VHDL) allows the descriptions of digital systems using their behavior models [9].

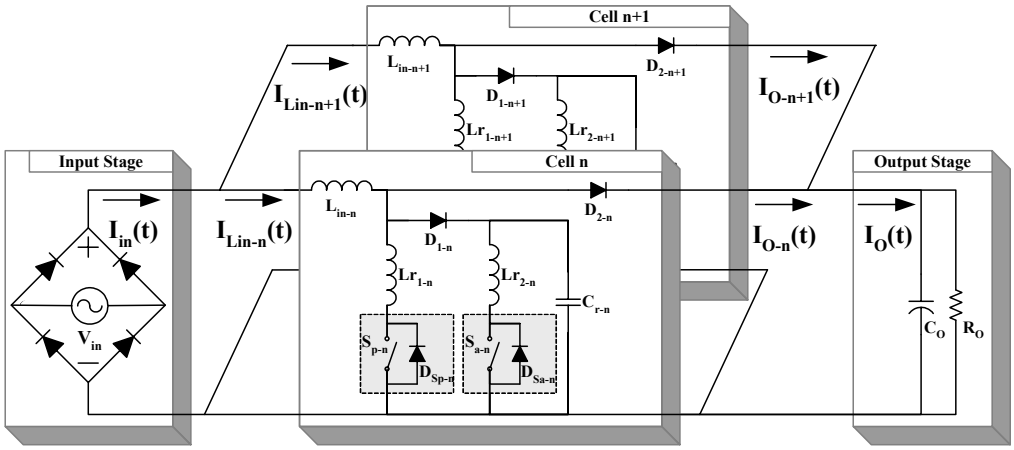


Fig.1 Pre-regulator AC/DC Boost ZCS-FM Interleaved with two cells.

Therefore, this paper presents a complete analysis and description of a digital control technique using a FPGA device and VHDL language, applied to an interleaved ZCS-FM boost rectifier, performing high input power factor with low total harmonic distortion in the input current, and output voltage regulation.

In this context, Fig. 1 shows the Interleaved ZCS-FM boost rectifier with two cells that can reduce the switching losses, including the diode reverse recovery losses, yields higher efficiency, high power density, and lower EMI emission [10].

II. DIGITAL CONTROL STRATEGY

The dynamic modeling of power factor correction converters is difficult due to the fact that the conversion ratio widely changes within each half-line period and the steady state operation point fluctuates at double the line frequency. However, it was shown theoretically and experimentally [11, 12] that the steady state can also be approximated as a linear system which fluctuates around a dc point determined by the rms value of the input voltage. Therefore, the small-signal analysis can be performed similar to that of a dc-dc converter with the input voltage replaced by the rms value of the rectified line voltage.

The statement that a power factor correction converter can be treated as a dc-dc converter with its input voltage equals the rms value of the rectified ac line voltage, simplifies the analytical process and allows most of the well-understood dc-dc converter techniques to apply directly to the power factor correction control applications.

In order to derive the small-signal average model of a converter using a state-space technique, the time averaged values of inductor currents and capacitor voltages are assigned as state variables, while the input voltage and output current are assigned as input variables and input current and output voltage as output variables. However, the control variable is selected as the switch on-time t_{ON} instead of duty cycle.

The resulting small-signal model can be collected in a representation where the input port of a converter is described using Norton equivalent circuit, and the output port using Thevenin equivalent circuit.

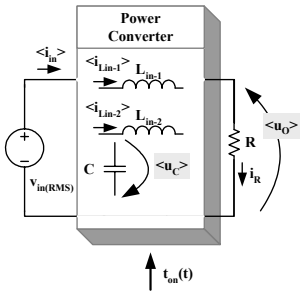


Fig. 2 – Power converter with associated variables for small-signal modeling.

A second order system may be represented as (1) where the upper row defines the Norton equivalent circuit, and the bottom row the Thevenin equivalent circuit.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_{o(RMS)} \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{ji-o} \\ G_{io-o} & -Z_{o-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{Lin-1} + \hat{i}_{Lin-2} \\ \hat{u}_C \end{bmatrix} + \begin{bmatrix} G_{c-in} \\ G_{c-o} \end{bmatrix} \cdot \hat{t}_{ON} \quad (1)$$

In spite of boundary operation mode provides the inductor current $i_L(t)$ to become zero twice in every switching period, the time averaged inductor current $<i_L>$ is a continuous function of time within a switching period as shown in Fig 3. The distribution of charge within the on-time and off-time of a switching period is dependent on the mode of operation. The portion of average inductor current delivered during the on-time (t_{on}) and the off-time is dependent on the mode of operation.

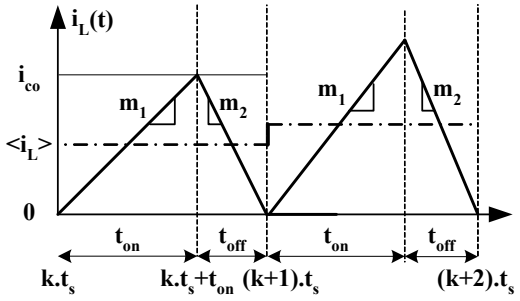


Fig. 3 – Inductor current waveforms in boundary conduction mode.

The variable-frequency operation (boundary conduction mode) is accomplished in such way that the switching period is started when the inductor current reaches zero, and the switch on-time is concluded when the inductor current reaches the control current i_{co} as shown in Fig 3.

The one-zero two-pole PI compensator represented in (2) with one pole at the origin, the other at high frequency and one zero at low frequency is a well-known analog control function for a voltage loop compensator in power converter circuits, where $V_X(s)$ is the compensator output and $V_Y(s)$ is the compensator input.

$$V_X(s) = k\frac{s/\omega_Z + 1}{s\left(s/\omega_P + 1\right)}V_Y(s) \tag{2}$$

The conversion from continuous time domain to discrete time domain can be accomplished by one of the transformation approaches (Euler, Tustin, bilinear). In this case the Euler transformation where, $s = T/(z-1)$, was used in order to obtain the discrete time domain relationship of the compensator where $V_X(n+1)$ is compensator output at time t=kT, and $V_Y(n)$ is compensator input in the discrete domain, as represented in (3).

$$\begin{aligned} V_X(n+1) = {} & \frac{1}{1+\omega_P T}\cdot V_X(n) + \frac{2+\omega_P T}{1+\omega_P T}\cdot V_X(n-1) \\ & + \frac{k\omega_P}{\omega_Z}\frac{T+\omega_Z T^2}{1+\omega_P T}\cdot V_Y(n+1) \\ & + \frac{k\omega_P}{\omega_Z}\frac{T}{1+\omega_P T}\cdot V_Y(n) \end{aligned} \tag{3}$$

The digital controller was implemented in discrete time domain using fixed point arithmetic approach and the facilities provided by the hardware description languages.

Additionally, an anti wind-up control is necessary to prevent integration part leads to instability. Therefore, the anti wind-up scheme which can pull the controller out of the saturate state, quickly provided that the controlled variable is higher than the control reference has to be adopted. In a common PI controller that consists of a proportion part and an integration part separately, it is relatively simple to realize the anti wind-up scheme by putting a limit on the integration part.

In the closed-loop design of the power factor correction converter system the controller should be designed appropriately such that the bandwidth of the voltage loop is considerably lower than the natural 120 Hz ripple frequency in the output to prevent reduction of the converter power factor. The crossover frequency of the loop gain is usually chosen around 10 Hz.

One of the ZCS boost cells is adopted as reference for the phase shifting required in the interleaved technique. It is reasonable to consider that the cells' switching period is almost constant for previous and forward switching periods. So, in order to determine the ideal phase-shift instant regarding the reference cell, information from its previous switching period is used. Particularly, the digital control monitors the rise edge of the gate signal from the main switch of the reference cell.

The digital controller has been implemented using a Field Programmable Gate Array (FPGA), an analog-digital converter and the control algorithm has been developed using a hardware description language VHDL. The FPGA device employed was XC2S200E-pq208-6C by XILINX and mounted in a prototype board D2E by DIGILENT INC.

The subsystems of the digital control system are realized in three separate printed boards. These boards hold the FPGA, where the control logic is executed, the data-acquisition circuits and the circuits for driving the cell switches.

Figure 4 shows the control algorithm developed using VHDL. The developed digital system is fully synchronous using a 50MHz system clock.

The Figs. 5 and 6 show simulations results of digital components developed using VHDL. The Fig. 5 shows the results for the component responsible for the determination of phase-shift instant, it should be noticed that the switching periods variation was exaggerated in order to evaluate the component. The evolution of the gate signals generated by the control for the switches can be verified in Fig. 6, providing the critical conduction mode in the two commutations cells.

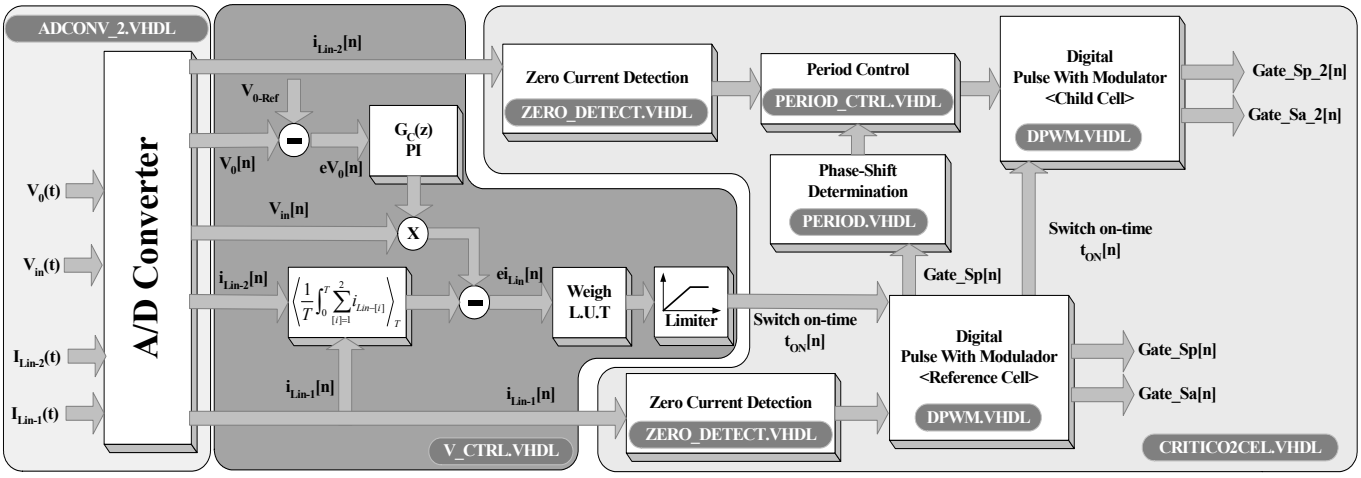


Figure 4 – Block diagram of the control algorithm.

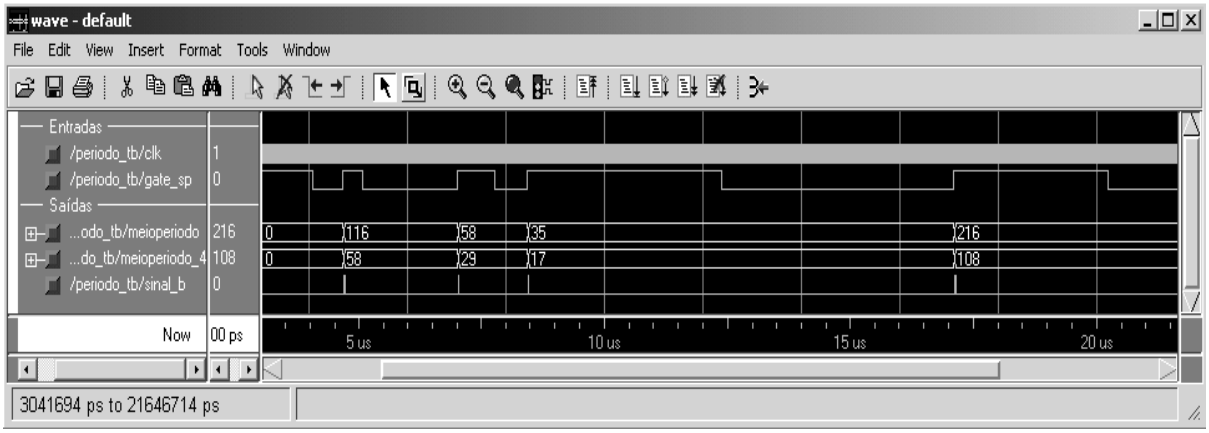


Fig 5 - Simulation results of VHDL behavior, description of component PERIOD.

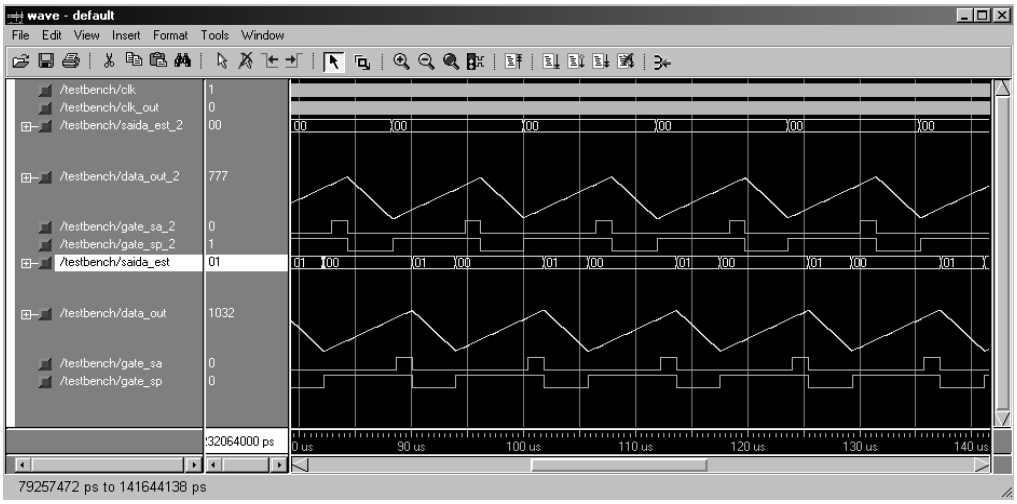


Fig 6 - Simulation results of VHDL behavior, description of component CRITICO2CEL.

TABLE I
CONVERTER PARAMETERS

Input and Output Requirements	
Parameter	**Value**
$V_{in\ [RMS]}$	220 V
V_O	400 V
P_O	1 kW
$f_{s[Quiescent\ Point]}$	50 kHz
Number of Cells (N)	2
Phase-Shift [rad]	π/2

Circuit Parameters	
Parameter	**Value**
S_{P1-i}	HGTP12N60A4D
S_{A1-i}	HGTP7N60A4D
D_{1-i}	RHRP860
D_{2-i}	RHRP8100
L_{in-i}	428.5µH (Litz:7x26 AWG)
L_{r1-i}	28.6µH (Litz:5x26 AWG)
L_{r2-i}	20.0µH (Litz:5x26 AWG)
C_{r-i}	10.0nF
Co	390.0µF

Where: [i] is the number of ZCS boost cell;

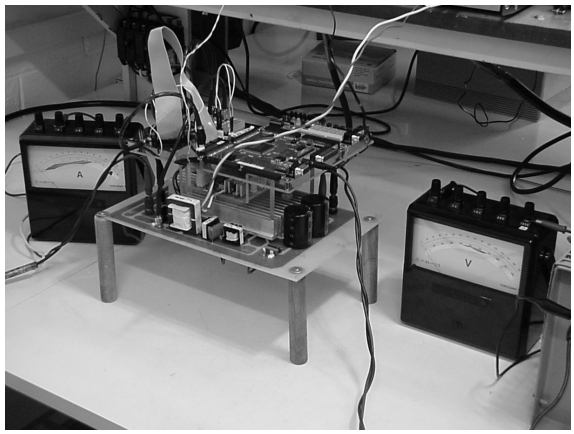
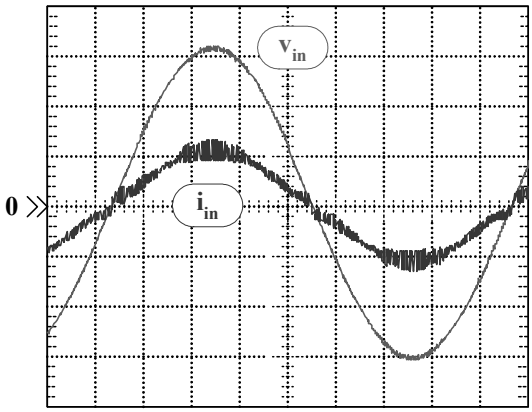


Fig 7 – Implemented prototype for the interleaved ZCS-FM boost rectifier, with digital control using a FPGA device

III. EXPERIMENTAL RESULTS

The proposed converter presented in Fig. 1 has been tested using an experimental prototype shown in Fig. 7. The circuit parameters utilized are described in Table I. These values are based on design methodology previously presented in [10].



v_{in}: 100V/div; i_{in}: 5A/div, 2ms/div.

Fig.8 - Input current and input voltage during one ac period, at full load.

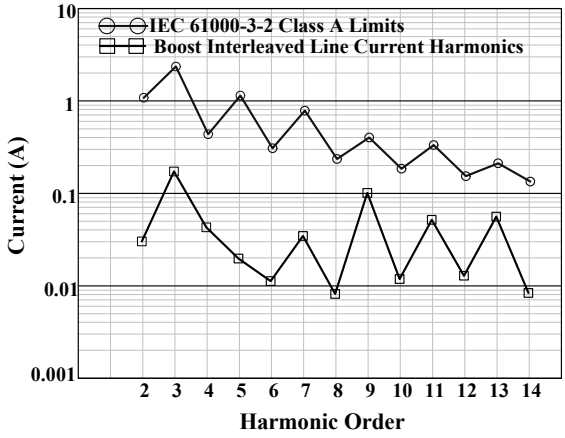
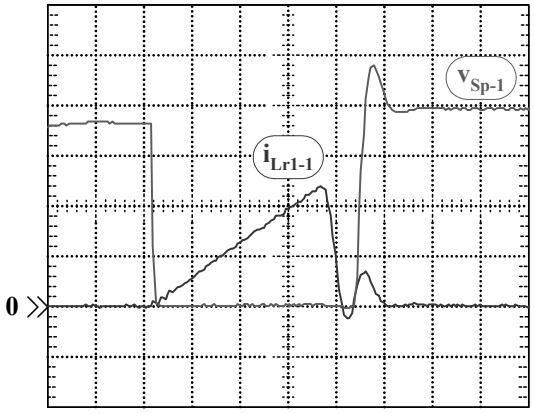
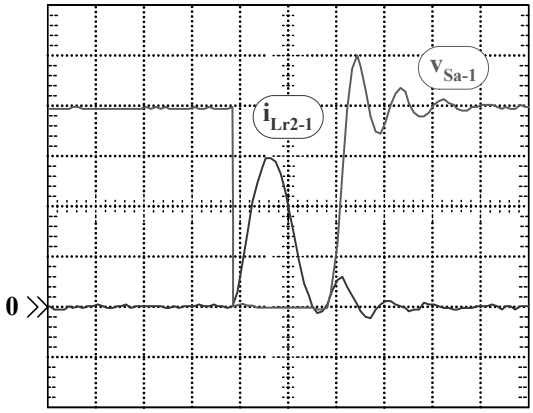


Fig.9 - Harmonic current amplitudes from the proposed pre-regulator converter, and the IEC61000-3-2 Class A Limits.

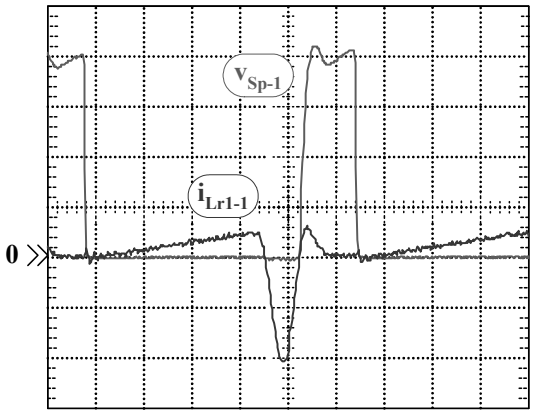


i_{Lr1-1}: 2A/div; v_{Sp-1} : 100V/div, 2μs/div

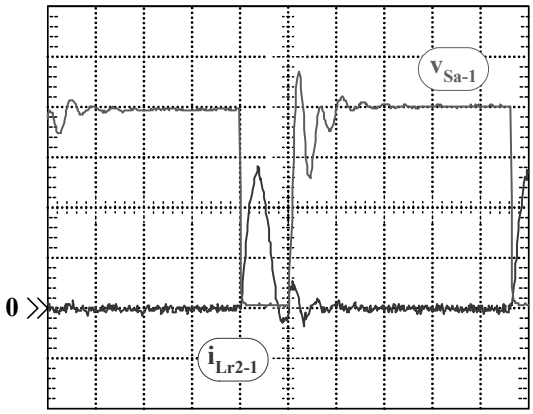


i_{Lr2-1}: 2.5A/div; v_{Sa-1} : 100V/div, 1μs/div

Fig.10 - Commutation details, voltage and current through main switch S_p, and auxiliary switch S_a in the reference cell, where V_{in} is near to its peak value.

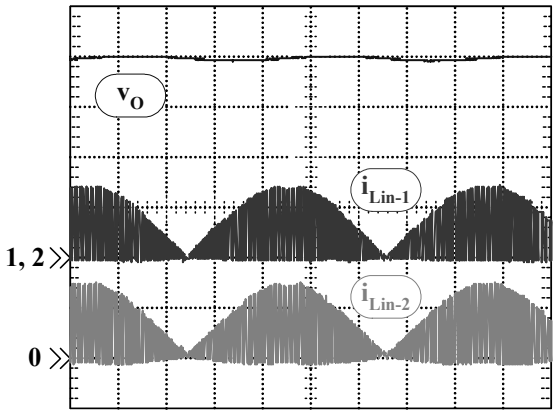


i_{Lr1-1}: 2A/div; v_{Sp-1} : 100V/div, 2μs/div



i_{Lr2-1}: 2.5A/div; v_{Sa-1} : 100V/div, 2μs/div

Fig.11 - Commutation details, voltage and current through main switch S_p, and auxiliary switch S_a in the reference cell, where V_{in} is near to zero value (30V).



V_O: 100V/div; i_{Lin-1} and i_{Lin-2}: 4A/div; 2ms/div

Fig. 12 – Currents through the interleaved boost input inductors and output voltage, at full load.

Figure 8 shows the input current (i_{in}) and input voltage (v_{in}) during one ac line period, at full load. It can be observed in fig. 8 that the interleaved technique eliminates the discontinuity in the input current, and the input current waveform is practically in phase with the input voltage waveform, and the experimental power factor measured for nominal load condition was equal to 0.989.

Moreover, the input current harmonic content resulted in a THD of 5.33%, and in agreement with the limits of Class A - IEC61000-3-2 standard, in accordance with figure 9. It should be noticed that the T.H.D of the input voltage, in the conditions of the results presented in figure 8, was only 0.36%.

All experimental results were acquired with the converter operating without any type of input filter commons in topologies operating in critical conduction mode.

The commutation details for the voltage and current through the main and auxiliary switches, in the reference cell, when the value of the input voltage waveform is near of its peak value and near of its zero crossover, are shown in Figs. 10 and 11, respectively. One can verify in these figures the soft-commutations in the main and auxiliary switches, and these properties are preserved during the entire excursion of the input voltage waveform (ac line period).

Figure 12 shows the currents through the boost input inductors, for each cell, in interleaved operation. One can observe in Figs. 8 and 12 that the interleaved technique eliminates the discontinuity in the input current, providing conditions to reduce the EMI input filter. In addition, Fig. 12 shows the regulated output voltage for nominal load operation.

IV. CONCLUSION

In this paper was investigated an interleaved high input-power-factor pre-regulator boost rectifier operating in critical conduction mode, using a non-dissipative commutation cell and frequency modulation. The interleaved boost ZCS-FM pre-regulator can further reduce the switching losses, including the diode recovery losses. All the semiconductor devices employed in this proposed rectifier perform soft-commutation process. Moreover, these commutations are preserved during the ac system period and load variation. It would be useful for high switching frequency operation and EMI reduction.

The experimental results obtained in this work show that the input power factor is nearly the unity and the harmonic distortions verified in the input current are in compliance to the IEC61000-3-2 standards for class A equipments.

The control logic has been implemented using a programmable logic device FPGA and hardware description language VHDL. All the control processes are executed continuously and simultaneously, in a concurrent way. The functionality of the controller was described using its behavior, performing a true interleaved operation in critical conduction mode, and output voltage regulation.

ACKNOWLEDGEMENT

We would like to thanks FAPESP and CNPq/CT-Energ for the financial support and the TI instruments for the data converters donation.

REFERENCES

[1] T. Ishii and Y. Mizutani, “Power Factor Correction Using Interleaving Technique for Critical Mode Switching Converters”, in Proceedings of the 1994 IEEE Applied Power Electronics Conference, pp. 404-410;

[2] P. Wong and F. C. Lee, “Interleaved to Reduce Reverse Recovery Loss in Power Factor Correction Circuits”, in Proceedings of the 2000 IEEE Industry Applications Society Conference, CD-Rom Folder;

[3] P. Zumel, A. de Castro, O. Garcia, T. Riesgo and J. Uceda, “Concurrent and Simple Digital Controller of an AC/DC converter with Power Factor Correction”, in IEEE Transactions on Power Electronics, Vol. 18, n. 1, January 2003, pp. 334-343;

[4] B. A. Miwa, D. M. Otten and M.F. Schlecht, “High Efficiency Power Factor Correction Using Interleaving Techniques”, in Proceedings of the 1992 IEEE Applied Power Electronics Conference, pp. 557-568;

[5] A. Prodic, C. Jingquan Chen, D. Maksimovic, and R.W. Erickson, “Self-tuning digitally controlled low-harmonic

rectifier having fast dynamic response", in IEEE Transactions on Power Electronics, Vol. 18 , n. 1 , January 2003, pp. 420-428;

[6] G. Spiazzi, P. Mattavelli and L. Rossetto, "Power factor Pre-Regulators with improved dynamic response", in Proceedings of the 1995 IEEE Power Electronics Specialists Conference, vol. 1, pp. 150–156;

[7] R. R. Ramos, D. Biel, E. Fossas and F. Guinjoan, "A Fixed-Frequency Quasi-Sliding Control Algorithm: Application to Power Inverters Design by Means of FPGA Implementation", in IEEE Transactions on Power Electronics, Vol. 18, n. 1, January 2003, pp. 344-355;

[8] Y.Y. Tzou and H-J Hsu, "FPGA Realization of Space-Vector PWM Control IC for Three-Phase PWM Inverters", in IEEE Transactions on Power Electronics, Vol. 12, n. 6, November 1997, pp. 953-963;

[9] T. Riesgo, Y. Torroja and E. De la Torre, "Design Methodologies Based on Hardware Description Languages", in IEEE Transactions on Industrial Electronics, Vol. 46, n. 1, February 1999, pp.3-11;

[10] C. A. Canesin and F. A. S. Gonçalves, "Single-phase High Power-Factor Boost ZCS Pre-regulator Operating in Critical Conduction Mode", in Proceedings of the 2003 International Symposium on Industrial Electronics, CD-ROM Folder.

[11] F. A. Huliehel, F. C. Lee and B. O. Cho, "Small-signal modeling of the single-phase boost high power factor converter with constant frequency control", in Proceedings of the 1992 Power Electronics Specialists Conference, pp. 475-482;

[12] R. Erickson, M. Madigan and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter", in Proceedings of the 1990 IEEE Applied Power Electronics Conference, pp. 792-801.