ANALYSIS AND DYNAMIC MODELLING OF FLYING CAPACITOR MULTILEVEL CONVERTERS

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***Abstract* – A dynamic model of the flying capacitor multilevel converter is presented in this paper. This model presents a time domain approach instead of a frequency domain analysis previously used to characterized the self balancing properties of the capacitor voltage. Through this approach it is possible to obtain a better understanding of the physical properties which governs the self balancing characteristics of the converter. The proposed model is a powerful tool to design the balancing network and the converter itself.**

***Keywords* – Balancing network, dynamic model, high voltage converters, multicell converters.**

I. INTRODUCTION

The number of applications of power converters in the field of the high voltage and high power have increased significantly in recent years. This give rise to the use of new topologies of power converters. Multilevel converters are receiving great attention. The general structure of these converters allows to synthesize a sinusoidal voltage from capacitor voltage sources. There are three types of capacitor voltage synthesis-based multilevel converters: a) diode clamp, b) flying-capacitors, and c) cascaded one phase inverters with separate DC sources [1]-[2]-[3]. One key point in the design of multilevel converters is to obtain a uniform voltage distribution over the different switches of the power converter. Then, it is important to obtain balanced voltage on the different capacitors voltage sources.

In the case of the multicell flying capacitor converter, it has switching redundancy, which can be used to balance the flying capacitors voltages, during steady state operation. More generally, the balance condition is satisfied when all the switches have the same duty cycle and a phase shift equal to $2\pi/n$, with n being the number of cells in the converter. It is more difficult to understand the transient performance of the converter and how the capacitor voltages reach their steady state value. Different frequency analysis, based on the harmonic components of the switching function were developed to understand the transient performance [4]-[5]-[6]. With this analysis it was demonstrated that it is necessary to have some harmonic currents in the cells in order to obtain self-balance of the flying capacitors voltages, and that these components are obtained introducing some dissipative network in the cell. Anyhow, it is not easy to understand the physical phenomena which guarantees the self balance operation of the multicell flying capacitor multilevel converter.

In this paper a time domain analysis of the converter is proposed. The influence of different passive networks (balancing networks) over the capacitor voltage is analyzed. Finally a time domain average model of the basic cell with different balancing networks is obtained. The time domain evolution of the capacitor voltage is calculated with the proposed model. This allows to understand and quantify the effect of the balancing network over the converter performance. It is also a powerful tool to dimension the flying capacitors, the power switches and the passive elements in the balancing network.

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II. DYNAMIC MODEL OF THE MULTILEVEL CONVERTER

In this section, a DC-DC three level buck converter is used to analyze the behavior of the elementary unit of a multilevel voltage source inverter. A time domain analysis is performed to establish the balancing conditions of the capacitor voltages.

A. Self-balance condition.

Fig. 1 shows the DC-DC three level buck converter which is used in the analysis. Here it can be seen that the pair of switches S_k and S_{K+1}, their complements $\overline{S}_k$ and $\overline{S}_{k+1}$ together with capacitor C_k and the voltage source v_e are the basic unit of two cells which form the simplest multilevel converter. Depending on the swithces states, the current through the capacitor (i_k) may be,

a. $i_k = 0$ if S_k and S_{k+1} are ON,
b. $i_k = +\, i_0$ if S_k and $\overline{S}_{k+1}$ are ON,
c. $i_k = -\, i_0$ if $\overline{S}_k$ and S_{k+1} are ON
d. $i_k = 0$ if $\overline{S}_k$ and $\overline{S}_{k+1}$ are ON.

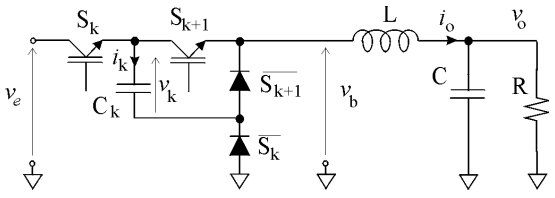


Fig. 1: Three level buck converter

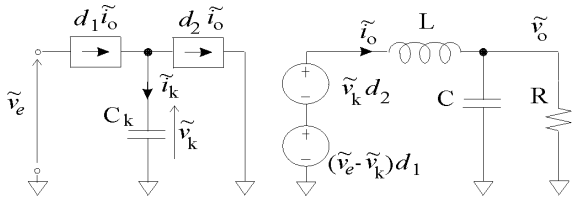


Fig. 2 The average model of the basic unit of multicell converter

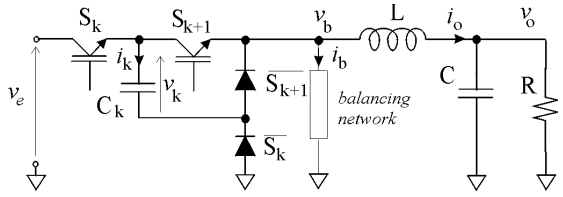


Fig. 3: Three level Buck converter with a balancing network

Then, the balance operation is obtained when conditions b) and c) are applied during the same amount of time in each commutation cycle.

B. Average model

In order to understand the dynamic behavior of the floating capacitor, an average model is used here. The model of the capacitor multilevel converter is obtained following the averaging techniques [7] assuming continuous current operation with low ripple. The switch average model is shown in Fig. 2 and it is characterized with the following equations,

$$\begin{aligned}\frac{d\tilde{i}_o}{dt} &= \frac{1}{L}\left[\tilde{v}_e d_1 - \tilde{v}_O + (d_2 - d_1)\tilde{v}_k\right] \\ \frac{d\tilde{v}_O}{dt} &= \frac{1}{C}\left(\tilde{i}_o - \frac{\tilde{v}_O}{R}\right) \\ \frac{d\tilde{v}_k}{dt} &= \frac{1}{C_k}\tilde{i}_k = \frac{1}{C_k}(d_2 - d_1)\tilde{i}_o\end{aligned} \qquad (1)$$

where d_1 and d_2 are the duty cycles of the power switches S_k and S_{k+1} respectively. They are phase shifted over π rads. From Fig. 2 and the third eq in (1), it can be seen that the current through C_k is the sum of two current generators which depend on the duty cycles of the power switches and the load current. It also shows that the capacitor voltage $\tilde{v}_k$ is constant when d_1 is equal to d_2, regardless of the variation of the load current (i_0).

It is possible to correct the unbalance of $\tilde{v}_k$ by controlling d_1 and d_2. But this requires a control loop and the voltage measure over the flying capacitor. This increases the cost and complexity of the design.

Then, to vary this voltage, without controlling d_1 and d_2, it is necessary to add some kind of DC current over the capacitor, such that,

$$\frac{d\tilde{v}_k}{dt} = \frac{1}{C_k}(d_2 - d_1)\tilde{i}_o + \frac{1}{C_k}\tilde{i}_b \qquad (2)$$

where $\tilde{i}_b$ is the mean value of a current which charges the flying capacitor until it reaches the steady state voltage. Then, $\tilde{i}_b$ varies with $\tilde{v}_k$, and tends to 0 when $\tilde{v}_k$ approaches its steady state (E/2). The way to obtain this current is using a passive network called the balancing network, since it allows obtaining a self balance operation of the converter.

III. CELL MODEL WITH BALANCING NETWORK

Fig. 3 shows the buck converter with the balancing network. The model of the cell is obtained analyzing the voltage variations of v_k and v_b. It is assumed that both duty cycles are equal (d_1=d_2=d) and smaller than 0.5 (although tha analysis is also valid for values of d greater than 0.5) and the output current i_o is constant. Fig. 4 a) shows the instant voltage v_b during the converter start up. When S_k is ON, v_b take the value E-v_k and when S_{k+1} is ON, v_b is equal to v_k. Then, v_b may be separated in a steady state and a transient components. The steady state voltage is a pulse shape with an amplitude of E/2, a duty cycle equal to $2.d$ and a frequency equal to $2.f_S$. The transient voltage is a ac quasi square wave with an amplitude equal to E/2-v_k and frequency equal to f_S, as it is shown in Fig. 4 b). As a consequence, the current in the balancing network (i_b) is the sum of two components produced by the different voltages, the transient component (i_{bt}) and the steady state one (i_{bee}).

The current waveforms (i_{bt} and i_{bee}) strongly depends on the characteristics of the balancing network. Anyhow some operating conditions of the basic cell may be determined independently of the balancing network characteristics.

The current through C_k is,

$i_k = i_o + i_{bee} + i_{bt}$, while S_k is ON and S_{k+1} OFF, and

$i_k = -i_o - i_{bee} - i_{bt}$, while S_{k+1} is ON and S_k OFF.

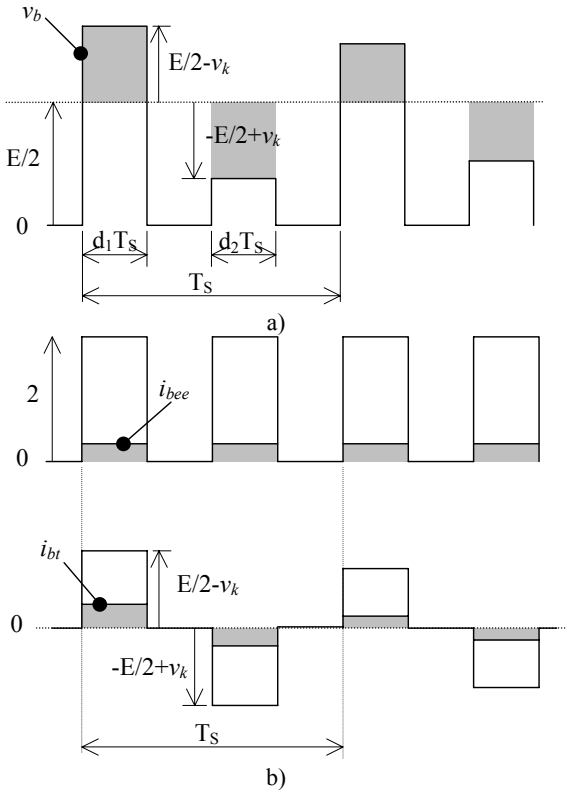


Fig. 4: a) Voltage v_b, b) Steady state and transient components of v_b and i_b

From these equations it is deduced that in order to charge the capacitor, the current of the balancing network should change its polarity. In Fig. 4 b) can be observed that only the transient component change its polarity. On the other hand, the effect of this component results in a single polarity of the corresponding C_k current component. So it is concluded that the balancing network should have some resistive component, then it must be a dissipative circuit.

A. Resistive balancing network

The resistive network is the easiest to start the analysis and modeling of the cell. Fig. 4 b) shows the current components waveforms (i_{bee} and i_{bt}) of the resistive network, together with the voltage components. It is clear that the transient component i_{bt}, changes its sign during every half switching cycle (T_S). Then i_{bt} has always the same sign when it flows through the flying capacitor C_k and charges it to the nominal value. Assuming that $d_1=d_2=d$, the voltage variation over C_k is,

$$\frac{d\tilde{v}_k}{dt} = \frac{\tilde{i}_k}{C_k} = \frac{2.\tilde{i}_{bt}}{C_k} = \frac{2.d.\left(\frac{E}{2} - \tilde{v}_k\right)}{C_k.R_b} \qquad (3)$$

where R_b is the resistance of the balancing network.

The solution of this differential equation indicates that for a pure resistive balancing network, $\tilde{v}_k$ converges exponentially to its steady state value with a time constant equal to $\tau_k = \frac{C_k R_b}{2.d}$.

B. Balancing network with R-C series connection

A R-C series connection balancing network allows to eliminate the DC current component and reduce losses in steady state. The voltage waveforms continue to be those shown in Fig. 4, while the current waveforms are quite different. Following the same analysis of the resistive case, the variation of the flying capacitor voltage is,

$$\frac{d\tilde{v}_k}{dt} = \frac{2\tilde{i}_{bt}}{C_k} = \frac{2C_b}{T_S C_k}\left[1 - e^{\left(-\frac{dT_s}{\tau_b}\right)}\right]\left(E/2 - \tilde{v}_k\right) - \frac{2C_b}{T_S C_k}\left[1 - e^{\left(-\frac{dT_s}{\tau_b}\right)}\right]\tilde{v}_{cb0} \quad (4)$$

where R_b and C_b are the components of the balancing network, $\tau_b = R_b.C_b$ is the time constant of the network and $\tilde{v}_{Cb0}$ represents the time variation of the initial voltage over C_b in each integration interval of the current i_{bt}. If the change of $\tilde{v}_k$ is much slower than the variation of $\tilde{v}_{Cb0}$, then it is possible to find a second differential equation which relates $\tilde{v}_{Cb0}$ with $\tilde{v}_k$,

$$\frac{d\tilde{v}_{Cb0}}{dt} = \frac{1}{R_b C_b}\frac{\left(1 - e^{dT_s/\tau_b}\right)}{\left(1 + e^{\frac{T_S}{2\tau_b}}\right)}\tilde{v}_k - \frac{1}{R_b C_b}\tilde{v}_{cb0} \qquad (5)$$

Eq. (4) and (5) constitute the model of the basic cell with an R-C balancing network.

When the first term in (5) is much smaller than the second one, the characteristic frequencies of the system may be expressed as

$$q1 \cong -\frac{2C_b}{T_S C_k}\left[1 - e^{\left(-\frac{d.T_S}{\tau_b}\right)}\right] \quad \text{and} \quad q2 \cong -\frac{1}{C_b R_b}.$$

It is easy to satisfy also $dT_S << \tau_b$, then $q1$ tends to $q1 \cong -2d/R_b C_k$. Fig. 5 shows the variation of $\tau 1$ ($-1/q_1$) and $\tau 2$ ($-1/q_2$) as a function of the C_b/C_k ratio, for different values of R_b, with d and C_k fixed. Is is clearly seen that as C_b increases, the condition $dT_S << \tau_b$ is fulfilled and $\tau 1$ tends to a constant value. On the other hand, since $\tau 2 \cong \tau_b$, then it increases together with C_b/C_k,. It is clear from Fig. 5 that for the range of values shown in the figure the time evolution of v_k may be approximated by a first order system with a time constant equal to $q1$.

C. Balancing network with R-L-C series connection.

A R_b-C_b-L_b series connection balancing network is a tuned network which allows to eliminate the harmonic components below and above the natural frequency of the network. The voltage waveforms continue to be those shown in Fig. 4, while the current waveforms are quite different. Following the same analysis of the resistive case, the variation of the flying capacitor voltage is,

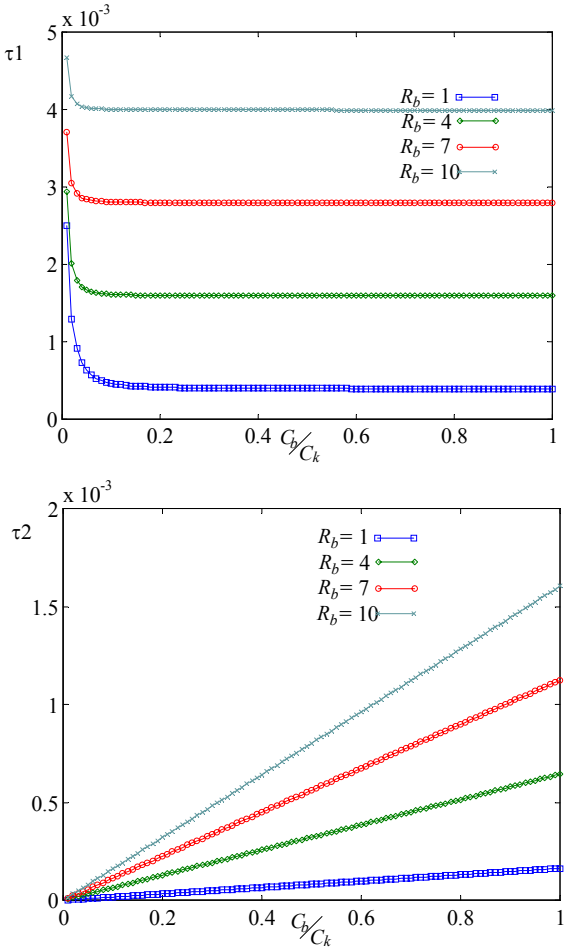


Fig. 5: Roots of the resistive and capacitive balancing network

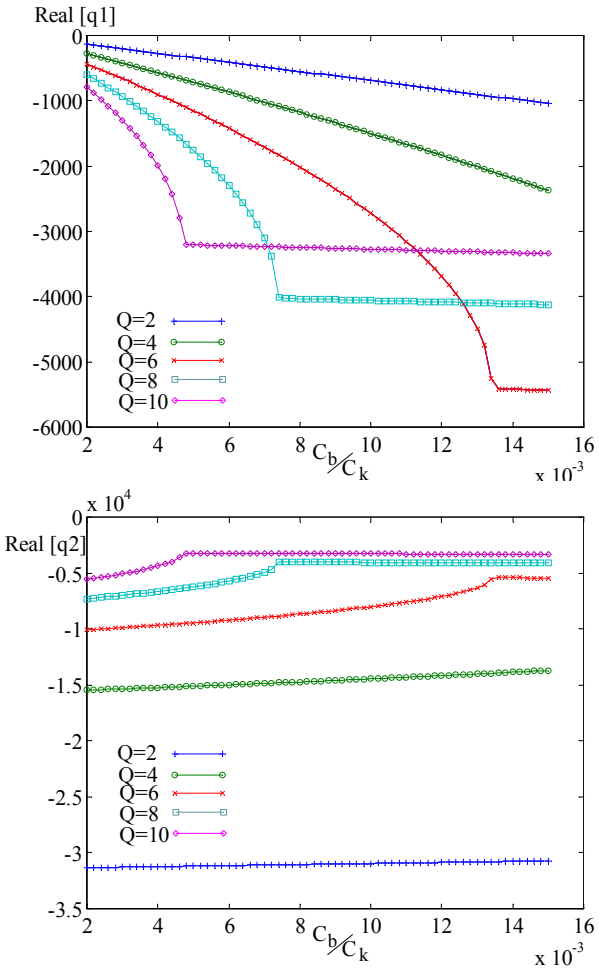


Fig. 6: Roots of the tuned balanced network

$$\frac{d\tilde{v}_k}{dt} = \frac{2C_b}{T_S C_k}\left[1 - e^{-\alpha d T_s}\left(m\sin\theta + \cos\theta\right)\right]\left(E/2 - \tilde{v}_k\right) + \\ + \frac{2\omega_d L_b C_b}{T_S C_k}(1-m)\left[m - e^{-\alpha d T_s}\left(m\cos\theta - \sin\theta\right)\right]\tilde{i}_{cb0} - \\ - \frac{2C_b}{T_S C_k}\left[1 - e^{-\alpha d T_s}\left(m\sin\theta + \cos\theta\right)\right]\tilde{v}_{cb0} \qquad (6)$$

where α and ω_d are the damping coefficient and the damped oscillating frequency of the tuned network respectively, $\theta = \omega_d . d . T_S$ and $m = \alpha/\omega_d$. $\tilde{v}_{Cb0}$ and $\tilde{i}_{Cb0}$ represent the time variations of the initial voltage over C_b and current through L_b in each integration interval of the current i_{bt}. These values depends on the voltage $\tilde{v}_k$, then if the following conditions are fulfilled:

a) change of $\tilde{v}_k$ is slower than variations of $\tilde{v}_{Cb0}$ and $\tilde{i}_{Cb0}$,

b) the merit factor of the tuned network (Q) is higher than 1,

c) the balancing network is tuned at the switching frequency $\omega_S = \frac{1}{\sqrt{L_b C_b}}$,

then it is possible to find two differential equations which relate $\tilde{v}_{Cb0}$ and $\tilde{i}_{Cb0}$ with $\tilde{v}_k$,

$$\frac{d\tilde{i}_{Cb0}}{dt} = -\alpha . \frac{I}{\omega_d . L_b} . \tilde{v}_k - \alpha . \tilde{i}_{Cb0}$$
$$\frac{d\tilde{v}_{Cb0}}{dt} = \alpha . \left(R + \frac{\alpha}{\omega_d} . I\right) . \tilde{v}_k - \alpha . \tilde{v}_{Cb0} \qquad (7)$$

where I and R are constants which depends on α, ω_d, d and T_s.

Eqs. (6) and (7) forms the differential equations system which characterized the dynamical behavior of $\tilde{v}_k$. The system has three roots. One of them is α and it is not important in the modelling. The other roots (*q1* and *q2)* depend on C_b/C_k, Q and d. Fig. 6 shows the real part of *q1* y *q2* as a function of C_b/C_k, for different values of Q, while d and C_k are kept fixed. The time evolution of $\tilde{v}_k$ is determined by the roots *q1* y *q2* only when they are real and different. In this case condition *a)* is fullfilled and the system may be approximated by a second order one. It can be seen in Fig. 6 that for each value of Q as C_b/C_k increases at a certain point the roots become constant. This means that they became a complex conjugated pair. When this happens the model fails to predict the behavior of v_k.

IV. PERFORMANCE EVALUATION

A. Self balance convergence

In this section the models obtained for the different balancing networks are evaluated through SPICE simulation of the power converters. In all the cases the start up of the converter is analyzed since this is the more stringent condition of voltage unbalance. The converter uses a power source E = 50V, a cell capacitor Ck = 160µF. This value was chosen so that the voltage ripple remains below 1% of the nominal voltage. The duty cycle is kept constant and equal to 0.25. The resistive load is so to have a load current of 20A.

1) Resistive balancing network

Fig. 7 shows the variation of v_k during converter start-up for different values of R_b. It can be seen that the model given by (3) follows very well the actual evolution of the voltage over C_k. It can also be concluded that v_k increases faster

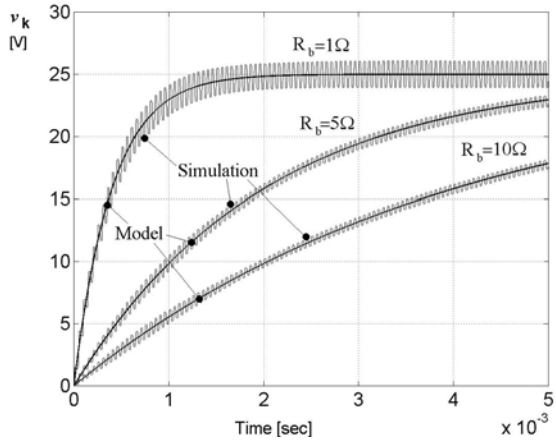


Fig. 7 Simulation and model of the transient voltage v_k for a resistive network at start up (C_k=160uF, E=50V)

when R_b is decreased This is due to the fact that i_{bt} increases its amplitude with a lower resistance.

2) R-C balancing network

Fig. 8 shows the variation of v_k during converter start-up for different combinations of R_b and C_b. It can be seen that the model given by (4) and (5) follows very well the actual evolution of the voltage over C_k. It can also be concluded that v_k increases faster when C_b/C_k is increased regardless of the value of R_b. This is due to the fact that i_{bt} approaches a constant value during dT_S. A lower value of R_b also accelerates the voltage variation. In this case it is related to a higher amplitude of the current i_{bt}.

3) R-L-C balancing network

Fig. 9 shows the variation of v_k for two values of Q, while the ratio C_b/C_K is kept constant. The simulation is compared with the second order model. It can be seen that the model given by (6) and (7) follows very well the actual evolution of the voltage over C_k. As was predicted in Fig. 6 a higher value of Q accelerates the convergence of $\tilde{v}_k$. This is due to the fact that currents at resonance frequency in a high selective tuned network increases with the merit factor Q. This is clearly seen in Fig. 9 where he convergence of v_k is much faster for the balancing network with a Q = 10 than for that with Q = 2. Moreover, also the increase of the ratio C_b/C_k accelerates the convergence of v_k to its nominal value $V_{CC}/2$.

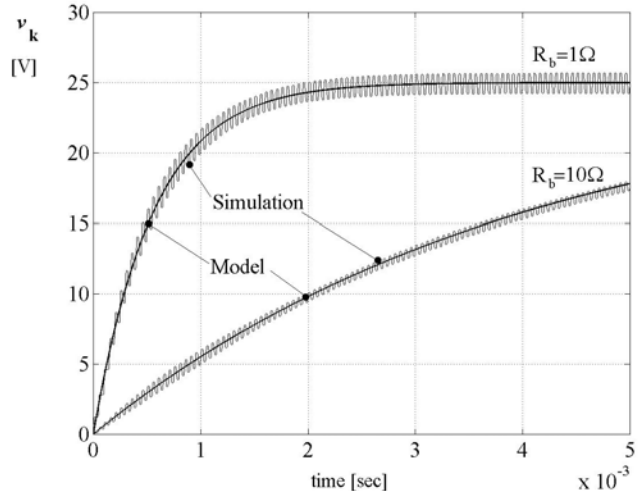
B. Power Losses

Although the balancing networks are an excellent solution to obtain a self balance operation of the power converter they introduce extra power losses that should be considered. In this sub-section the power losses introduced by the different networks are analyzed to have a better understanding in the design of these networks.

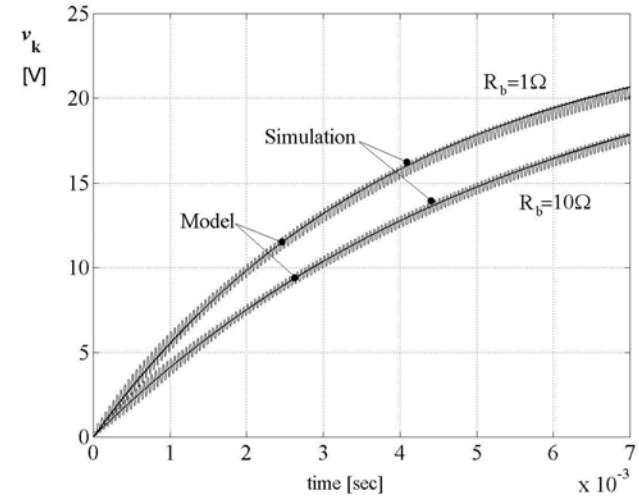
A pure resistive balancing network allows the self balance of the flying capacitor voltage at the cost of introducing extra losses due to the steady state current through the balancing network. In this case the losses are easily calculated as,

$$P_{loss} = d\frac{E^2}{R_b}$$

Nevertheless the R-C balancing network eliminates the DC current through the network, it continue to present extra losses to the power converter. In Fig. 10 the steady state

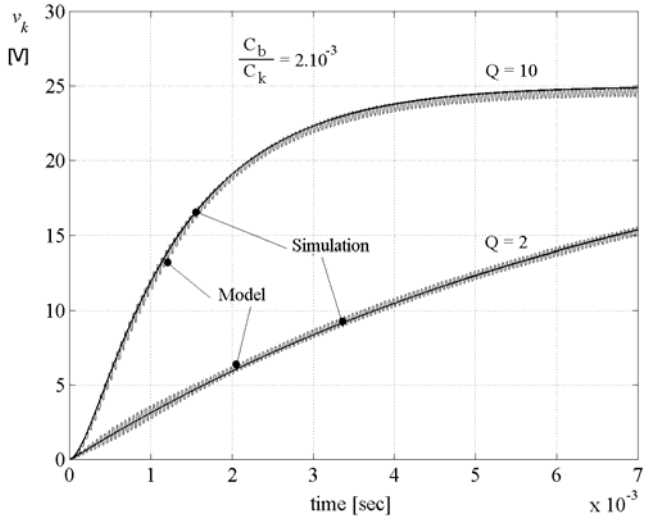


a) C_b=10μF



b) C_b=1μF

Fig. 8: Simulation and model of the transient voltage v_k at start up with R-C network (E=50V, C_k=160μF)



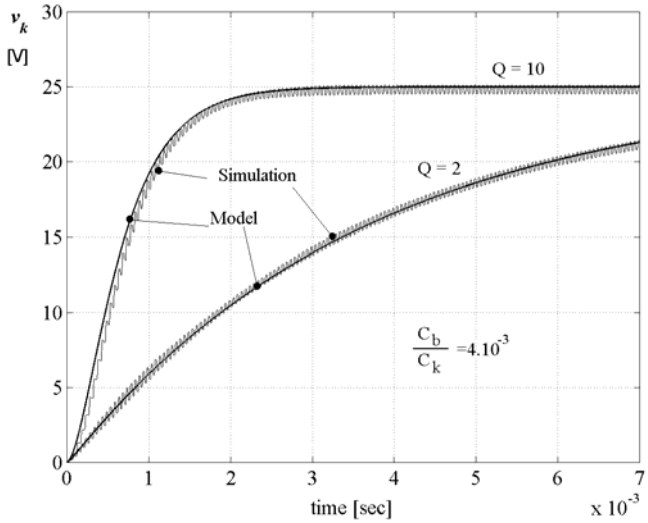


Fig. 9: Simulation and model of the transient voltage v_k for a tuned network at start up (C_k=160μF, V_{CC}=50V).

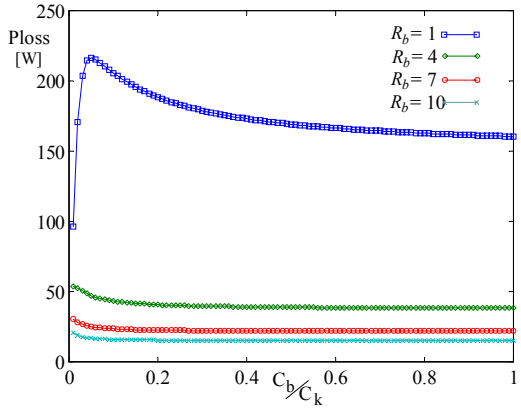


Fig. 10: Steady state power losses on a R_b-C_b balancing network

power losses introduced by the balancing network are presented. It shows how these losses varies with the ratio C_b/C_k and the value of R_b. Power losses increase considerably as R_b decreases. Then there exists a trade off between the power efficiency of the converter and the speed of balance convergence.

The R-L-C tuned network allows a quick convergence of v_k, introducing smaller losses than the other networks. This is mainly due to the fact that the tuned network presents high currents at the resonance frequency (fs) while in steady state the voltage across the network has a frequency equal to $2f_s$. The steady state power losses introduced by the tuned network are presented in Fig. 11. It can be seen that the losses reduce considerably as the network is more selective (higher Q). Moreover this agrees with the convergence speed of the balance. Then, there exist no trade off in the design of this network, making the tuned balancing network the preferred one.

V. CONCLUSIONS

A dynamic model of the flying capacitor multilevel converter was obtained. The proposed time domain analysis allows a better understanding of the self-balance operation of this converter and the role of the balancing network that is necessary for the basic operation of the converter. The time evolution of the flying capacitor voltage towards the balance condition is described precisely with the proposed model. Its performance was evaluated comparing the predicted voltage with the SPICE simulation of the converter presenting an excellent agreement. The proposed model is very useful to design the balancing network with a rapid convergence and minimum extra losses. Different balancing networks were analyzed concluding that the series tuned network is the more attractive regarding its high dynamics and lower losses.

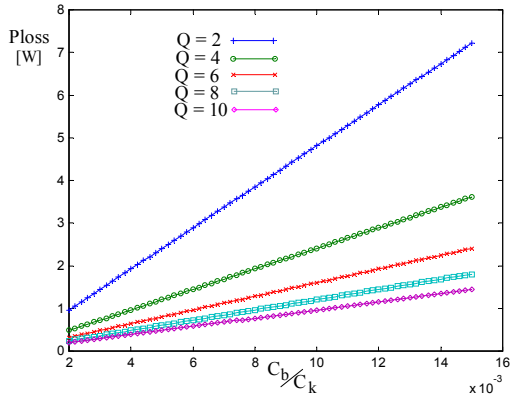


Fig. 11: Stationari power loss on balance tuned network

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