CONTROL STRATEGY BASED ON DFT FOR PFC CONVERTER

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***Abstract* – This article presents the study and implementation of a single-phase pre-regulator rectifier with digital control using a DSP, which can be applied to telecommunications sources. The control technique used aims to obtain Power Factor Correction (PFC) and regulated output voltages. The Discrete Fourier Transform (DFT) was used as a synchronizing circuit. The rectifier is a single-phase voltage doubler with a center tap at the voltage output. The DSP used is the ANALOG DEVICES ADMC401. The greatest advantages of this topology over the standard boost rectifier are: reduction in the number of components, the voltage across the switches that are half of the total output voltage, lower conduction losses and single command for the switches.**

***Keywords* - Digital Signal Processor, DSP, Power Factor Corrected Rectifiers, ADMC401, DFT.**

I. INTRODUCTION

The power supplies for telecommunications are normally composed by two stages connected in series; a rectifier with power factor correction and dc-dc converter. The proposal of this work is the use of a single-phase voltage-doubler PWM boost rectifier with power factor correction whose main characteristics are: high power factor in the input and regulation of the output voltages. The operational basic principle of this converter consists in imposing adequately a sinusoidal reference, which is established through a signal set that brings within itself the necessary characteristics to obtain a high power factor as well as a regulated output voltage. Several control techniques and topologies have been proposed to achieve the requirement of PFC [1,6,7,8,9]. The implemented control of the single-phase rectifiers was based on the average current mode control technique [6], which imposes to each period of commutation the average current value in the inductor. This work presents a control scheme based on the DFT as a synchronism circuit.

II. AVERAGE CURRENT MODE CONTROL TECHNIQUE WITH DFT

The modulation strategy used is based on the appropriate variation of the duty cycle at a constant frequency. The control technique applied is called control by means of instantaneous average values of the input current. It is one of the most used in power factor correction in pre-regulators with high power factor providing an input current with low harmonic distortion [1]. This technique consists of monitoring the input current of the converter making it follow a sinusoidal reference with the smallest possible error. This imposition is achieved through the appropriate high frequency switching control of the of converter switches, this control automatically regulates the output voltages [11].

In this way, is proposed a modification, the general algorithm described here is based on analysis and synthesis of the Discrete Fourier Transform (DFT), we have interest only in fundamental component. The control algorithm described was implemented using the ADMC401 DSP. Fig.1 shows, using a block diagram, the control circuit used.

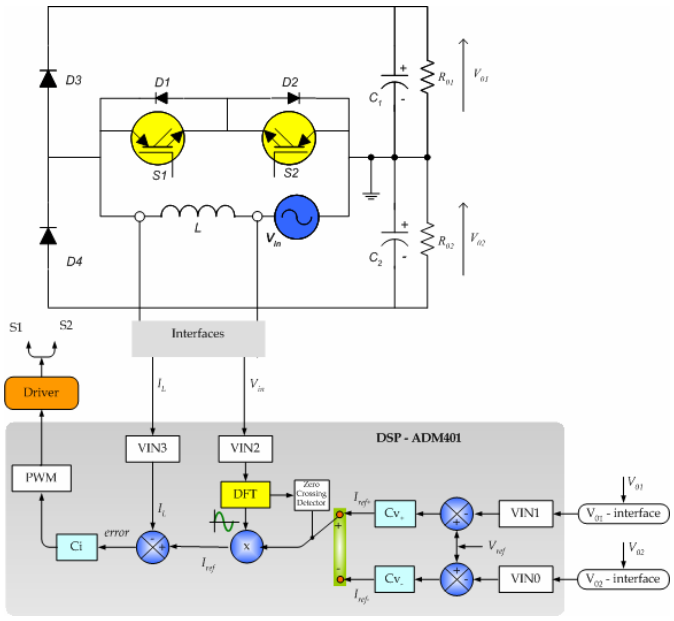

Fig.1 – Block diagram of the control circuit.

A. Digital Current Controller

The reference of current is compared with a current sample in the inductor, producing an error signal that is applied to the current regulator (Ci). The control action in the output of this block is applied to the PWM modulator (Pulse Width Modulation).

B. Modulator PWM

The control action in the output current regulator Ci is compared with a triangular signal in PWM block, the result is the switches command PWM signal. This PWM signal is applied to both switches

C. DFT Algorithm

The reference sign for the current loop will be a sinusoidal sign, calculated point to point for the DSP. Starting from samples of the phase voltage V_{in}, is possible to generate a

sinusoidal sign, without distortion, with the same frequency of one of the phases of the input voltage. In practice it is determined to fundamental component of the input voltage that will serve as reference current loop. The algorithm implemented in this work uses the Discrete Fourier Transform (DFT) for the determination of the current reference.

The frequency of sampling was 50 kHz, and the beginning of the conversion is synchronized with the request of interruption of the module PWM. In that way, every processing of the algorithm of DFT will happen inside of the routine of treatment of the interruption of the PWM. The diagram of blocks of this algorithm is illustrated in Fig. 2.

A generating circuit of ωt was implemented to generate the base of angular position for all functions sine and cosine involved in DFT. That circuit consists basically of the variable ωt, which is increased to each sampling period. The value of the increment is fixed, proportional to the sampling frequency f_s and to the frequency of the ac supply f_r.

The variables are represented in the format 1.15, so that it is compatible with the libraries of the functions sine and cosine. Starting from the samples of the voltage sign V_{in} for the converter A/D, the real and imaginary components are calculated.

By de way, the sign ωt is generated with base in the values of the sampling frequency and of the total number of samples for a period of the ac supply. Starting from the magnitude and phase is synthesized to fundamental component of the input voltage.

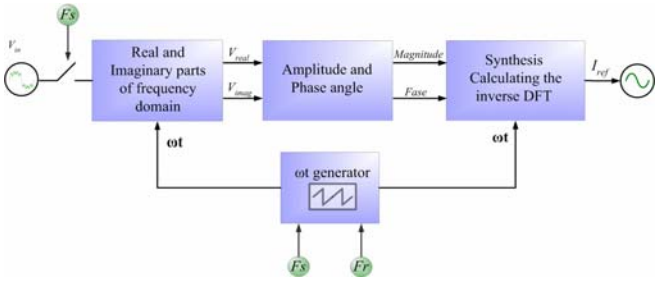

Fig.2 – Block diagram of the DFT algorithm.

D. Converter model

It is necessary to know the converter model to design adequately the current and voltage regulators with the power factor correction goal, converter output voltage regulation and balance.

For the current loop the converter transfer function must take into consideration the input current (I_L), related to the control variable, in this case the duty cycle (1). A method for modeling using the model of PWM switch [5] proposed by [1] was used.

$$G_i(s) = \frac{I_L(s)}{D(s)} \tag{1}$$

An option for the simplified model of the converter operating in continuous conduction mode (CCM) of current was made. This model considers output voltage without ripple and constant input voltage. Thus it arrives to the following transfer function of the converter, taking into consideration the input current and duty cycle (2).

$$G_i(s) = \frac{V_o}{s.L} \tag{2}$$

By the same way, to design the voltage regulator it is necessary to determine the transfer function that relates the output voltage to the current in the inductor (3):

$$G_v(s) = \frac{V_o(s)}{I_L(s)} \tag{3}$$

Through the switch model PWM [5], the result is given by (4):

$$G_v(s) = (1 - D)\frac{R_o}{s \times C_o \times R_o + 1} \tag{4}$$

Where:
R_0 : Load resistance.
C_0 : Output capacitance.

The voltage and current regulators (Cv(z) and Ci(z)), employed in the converter control belong to the Proportional-Integral (PI) kind. The allocation criteria of zero and of integrator gain adjustment of Ci(z) are based in [1], where integrator gain must be fitted to satisfy the gain crossing frequency criterion. It concisely is:

$$fc \le fs/4 \tag{5}$$

$$\omega_z = \frac{2.\pi.fs}{20} \tag{6}$$

Where:
fc : Gain crossing frequency.
f_S : Switch frequency.
ω_Z : Zero frequency.

The voltage gain of the controller Cv(z) was determined through the direct design by the root locus method by the Z-plane. The controllers were determined in the continuous time, and the discrete transfer function through the bilinear transformation, from the controller knowledge in the domain of Z. Applying the transformed Z^{-1} obtaining the controller under a difference equation form that will be implemented digitally.

The converter representation with the current and voltage, respective loops controls are shown by means of simplified blocks diagram in Fig. 3.

Each of the output voltages is sensed and regulated in the same designed voltage reference (V_{ref}). The necessary corrections to maintain the output voltage in the specified reference are done through the converter power flow control for each of the output voltages.

The power flow control is represented through a switch that commutes to each half cycle of the AC-mains voltage period, Fig. 3.

E. Zero Crossing Detector

This module is simply an algorithm that detects the zero cross of the fundamental component of AC supply. With this result it can be determined if the converter is operating in the positive or negative half-cycle. That is part of the strategy of control of the output voltages. More details in [11].

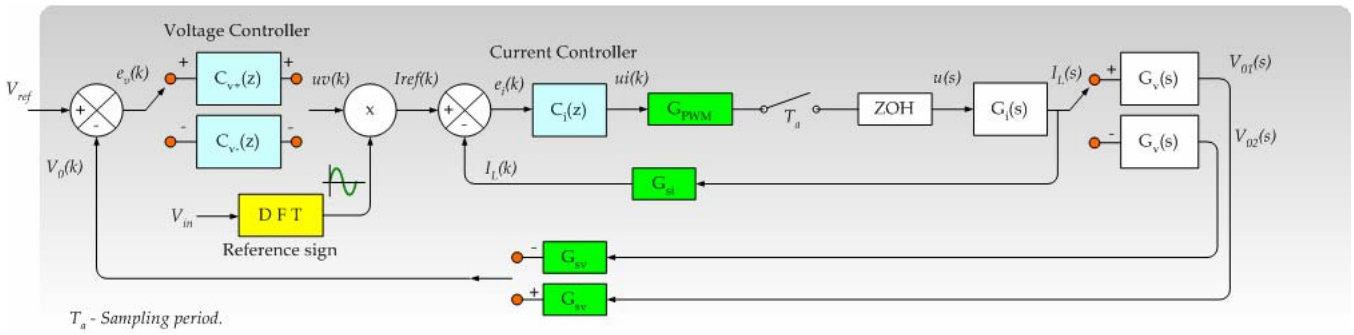

Fig. 3 – Block diagram of the converter control system.

III. DIGITAL COMMAND AND CONTROL

The control technique described in item II was implemented using DSP ADMC401 of ANALOG DEVICES, whose main characteristic are: 26 MIPS Fixed-Point DSP core; Single cycle instruction execution (38.5 ns); 2K x 24 bit – Program memory RAM; 1K x 16 bit - Data memory RAM; Three-Phase 16 bit PWM Generation Unit; 12-Bit Pipeline Flash Analog-to-Digital Converter with all eight inputs converted in <2μS.

The sampling frequency adopted in the voltage variable acquisition and current is 50 kHz. The converter switching frequency is 50 kHz. The PWM controller of the ADMC401 is operating in single update mode, there is a PWMSYNC pulse produced of each PWM period. Consequently, it is possible to produce PWM switching patterns that are symmetrical about de midpoint of the period. With this sampling frequency of 50 KHz, a resolution of about 9 bits PWM of the DSP was achieved. It was used one of the outputs of the three-phase PWM generator of ADMC401 for the activation of both switches, depending on the half-cycle of the AC-mains input voltage, one of the switches will conduct while the other will be blocked.

At the beginning of each PWM period, the control unit of ADMC401 receives a synchronization pulse, change direction an interruption service routine. The ADC conversion process is started on the rising edge of this pulse, where the output voltages and the current in the inductor measures are made. From these values the controller calculations (PI) of voltages, whose output is compared with the input current sample generating an error that is applied to the controller (PI) of current. Once the controller control action of current is certain, this value is loaded in the three-phase PWM unit, which itself generates the PWM. The execution implemented routines sequence blocks diagrams in ADMC401 are exhibited in Fig. 4. The determination of the current reference, through inverse DFT (synthesis), it is made in the end of a period of samples of the input voltage. The data are accumulated in the switching frequency; where some calculations are accomplished with objective of reducing the time spend for the DFT algorithm. The DFT was just used by the easiness in the determination of the fundamental component.

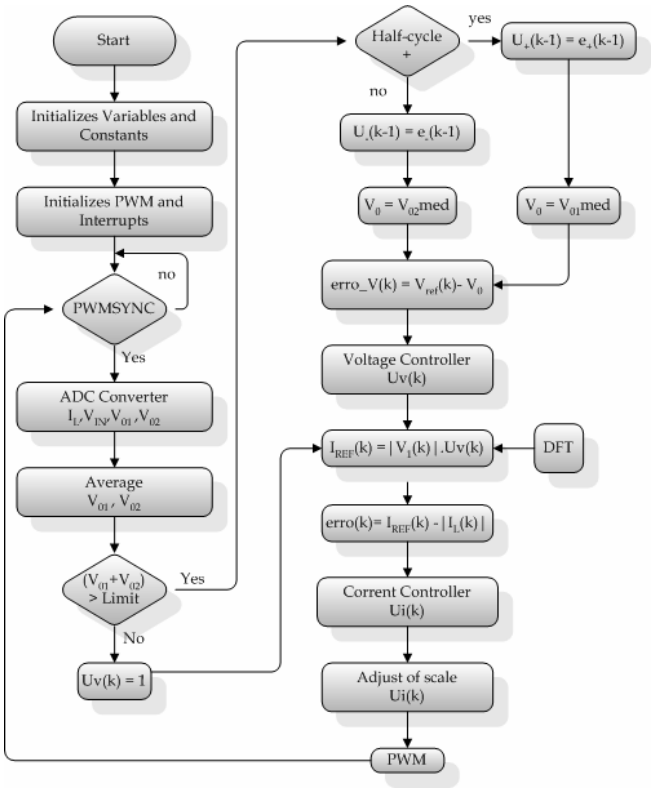

Fig.4 – Program blocks diagram.

IV. EXPERIMENTAL RESULTS

A prototype was planned and implemented using the specifications presented in Table 1.

TABLE I

V_{in}	Input rms voltage	127 V
V_{01},V_{02}	Voltage at each input	225 V
P_o	Total output power	1000 W
f_s	Switching frequency	50 kHz
f_r	AC line frequency	60 Hz

The bi-directional switches are implemented using IGBT's with diode. The following components are used in the pre-regulator:

S1,S2	:	IRG4BC30W.
D1, D2, D3, D4:		HFA15TB60.
C_1 and C_2	:	2X680µF in parallel.
L	:	500µH.

In the Fig.5 we have the graphic representation of the result of operation of the routine DFT, implemented in DSP. Those results show the appropriate operation of the algorithm used in the rectifier's control.

We can notice that a sinusoidal reference (synchronism) was generated in phase with the input voltage (a). The input voltage of the main AC together with to fundamental component resulting for the algorithm DFT can be visualized in the acquisitions. In the same figure, shows the acquisition of the input voltage and of the respective fundamental component (b). Those data were obtained through the use of the converter D/A present in the kit DSP. Those signs were sent of DSP through serial communication for D/A of the development kit. That procedure was just used to verify the operation of the algorithm DFT. The acquisition shows the values of the frequency of the sign of the input voltage and of the fundamental component (b).

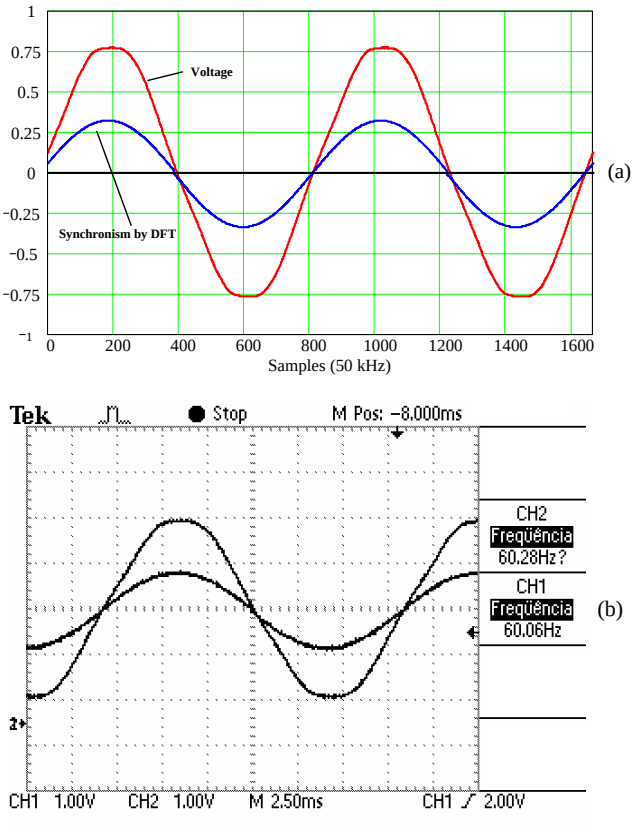

Fig.5 – Input voltage and fundamental component by DFT.

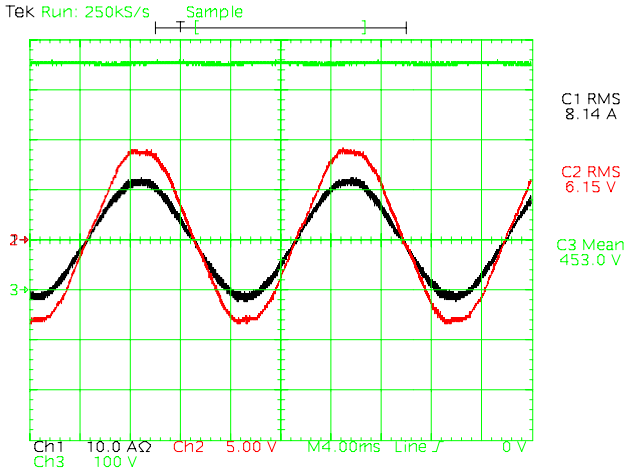

Fig. 6 – Voltage (Vin), inductor current (Iin) and output voltage (V_{01}, V_{02}).

In Fig.6 shows the acquisitions of the input voltage, the input current and of the output voltage. In this experimental test we used as reference just the sign of fundamental component of the input voltage. The converter was operating at rated power (1000 W).

The Fig.7 show the THD diagram of the input current. The input current THD is 2.01 % and the Power Factor (PF) is 0.9965.

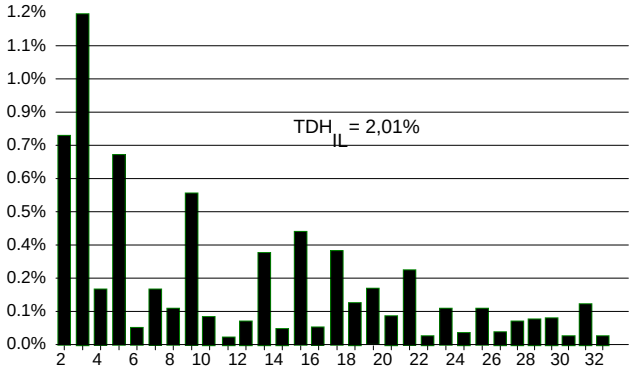

Fig. 7 – Harmonic magnitude as a % of the fundamental amplitude of input current.

More experimental results proving the operation of the converter under load disturbance can be seen in the reference [11]. The output voltage stayed regulated in several tests done with the converter. Only recalling, the objective was to implement and to test the algorithm DFT to be used as strategy of synchronism for the boost PFC.

The objective specifies of this article is to show another more efficient way to determine the reference current. In that way it was just tried to present the experimental results regarding the use of DFT in the control algorithm.

The use of DFT as synchronism strategy, presents a disadvantage regarding the use of the input voltage. The problem is that we needed the samples of a period of the AC voltage to determine the fundamental component. In practice that it represents that the reference for the current loop is updated with it delays of a period of the input voltage.

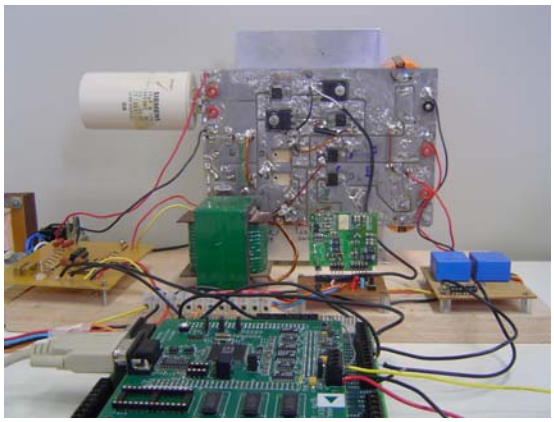

Fig.8 – Implemented prototype photo.

V. CONCLUSIONS

This paper has proposed the use of digital control for a voltage doubler rectifier by using a DSP, taking into consideration: The power factor correction and the regulation of the output voltage. Each of the output voltages is sensed and regulated in the same designed voltage reference (V_{ref}) through the current reference amplitude variation of each half cycle of the AC-mains voltage period. Using digital techniques implemented by a DSP it is possible to reduce the volume and cost of command and control circuits. The reduction of volume is due to the fact that by using the ADMC401 most of the components responsible for implementing the control laws can be eliminated, since these laws are implemented by means of software. As for the cost, these components are becoming more and more accessible and diversified. The final result is a high efficiency, high power factor converter with regulated and balanced output voltages. The Discrete Fourier Transform (DFT) was used as a synchronizing circuit implemented by the ADMC401. This technique presented good results. However, needs the samples of a period of the AC –mains voltage. That causes a delay of a period in the updating of the reference for current loop. In that way, the variations in the width of the fundamental component will be noticed with a period of delay.

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