DESIGN AND IMPLEMENTATION OF AN ASYMMETRICAL MULTILEVEL INVERTER FOR RENEWABLE ENERGY SYSTEMS

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Abstract **- This paper presents the main topics related to the development of an asymmetrical multilevel inverter prototype. The proposed inverter is based on a bi-directional topology that makes use of a low frequency transformer in order to produce several distinct voltages which are combined to produce the stepped output voltage. Design was focused mainly on reliability, efficiency and no-load consumption in order to make it suitable for operating in small renewable energy systems. A 3 kW prototype was implemented and tested. Peak efficiency of 96% was achieved and the prototype showed to be robust.**

Keywords **- Asymmetrical Multilevel Inverter, Power Electronics, Renewable Energy.**

I. INTRODUCTION

The DC/AC converters, namely inverters, play an important role in renewable energy systems. In case of an inverter for stand-alone system installed in a remote region, the most important features to be considered are reliability, efficiency and capability to start heavy loads. Taking into account these features, improved performance can be achieved using multilevel topologies due their inherent low frequency switching operation.

Although multilevel topologies have been mainly used in medium or high power systems [1,2,3], some asymmetrical topologies have showed to be competitive even for small power systems (< 10 kW), where its peculiar advantages justify the required large number of components used in its structure[4, 5].

Some multilevel topologies have been used to implement small asymmetrical inverters, such as those shown in Fig. 1. These topologies are bi-directional (regarding power flow) and are suitable to work with distinct partial voltages (asymmetrical approach). Topology (a) is applicable to systems where independent voltage sources are available and no isolation between input and output is required [5,6,7]. Topology (b) uses several transformers in order to provide isolation and also to produce distinct voltages in each stage [4]. This work makes uses of topology (c), proposed by Schmid [8], which requires only one low frequency transformer.

Due to their inherent low operation frequency, these topologies usually present high efficiency (>90%) and robustness, making then suitable for applications such as renewable energy systems, where high efficiency and high MTBF (Mean Time Between Faults) are of major importance.

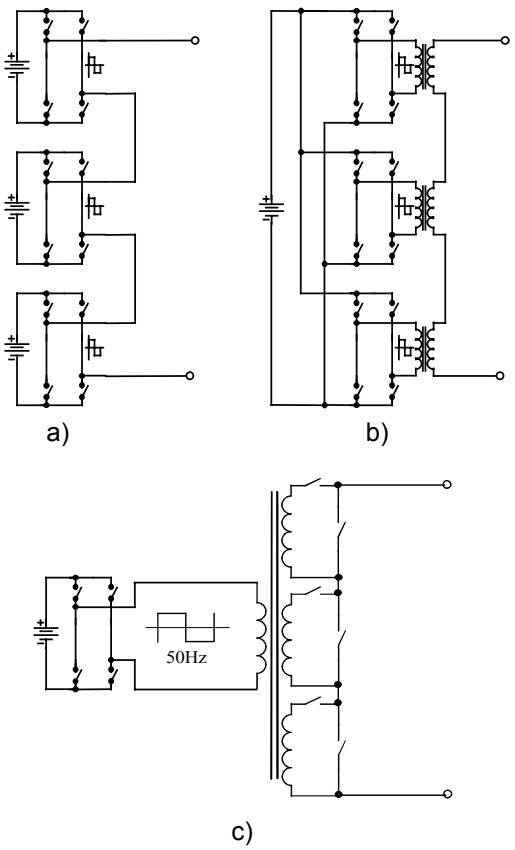

Fig. 1. Some inverter topologies used to implement small asymmetrical multilevel inverters.

II. PRINCIPLE OF OPERATION

With out loss of generality, lets describe operation principle for the two output stage structure showed in Fig. 2. Other bigger structures operate in the same way and only number of components and signals are greater.

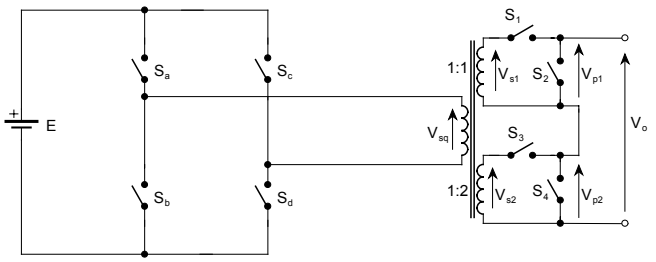

Fig. 2. Structure of a multilevel inverter with two output stages.

Commands of all switches and main voltages are presented in Fig. 3. The full bridge switches operates with

line frequency in order to produce a square waveform (V_{sq}) that is applied to the primary of the transformer. In this example, it is used transformer relation ratios of 1:1 and 1:2, so V_{s1} and V_{s2} are square waves with amplitudes of E and 2.E, respectively.

As can be seen, each output is connected to two switches which operate complementarily (S_1 and S_2 for the first stage and S_3 and S_4 for the second stage). Thus each stage produce partial voltages that can assume only two values: zero and its respective coil voltage. For example, if switch S_1 is closed and switch S_2 is opened, partial voltage V_{p1} is equal to coil voltage V_{s1}. On the other way, if switch S_2 is closed and switch S_1 is open then output voltage is ideally zero.

As all output stages are connected in series, total output voltage is equal to the sum of all partial voltages and can assume distinct values depending on the states of the full bridge and output stages. Table I resumes all possible conditions that can occur.

TABLE I
Output voltage versus switch states.

S3	S4	S1	S2	Vo (V_{sq}=+E)	Vo (V_{sq}=0)	Vo (V_{sq}=-E)
0	1	0	1	0	0	0
0	1	1	0	E	0	-E
1	0	0	1	2E	0	-2E
1	0	1	0	3E	0	-3E

Looking Table 1 one can conclude that it is possible to create a stepped output voltage that can approximate a sinusoidal waveform. It also should be noted that both positive and negative semi-cycles uses same switching patterns (in fact, the only change is the voltage signal).

Different from other topologies, this topology can only sum partial voltages and there is no possibility to subtract partial voltages. This limitation reduces the maximum number of levels for a fixed number of output stages, but this kind of operation do not allows cyclic flow of power which increases losses.

All signals named in Fig. 1 are showed in Fig. 3. It should be noted that switches of the first stage (lowest voltage) operates with higher frequency. In this case, switches S_1 and S_2 operate with 6.f (f = line frequency) while S_3 and S_4 operates only with 2.f. So it is easy to conclude that structures with a greater number of output stages will present switches operating with frequencies even greater. Although the output stage switches operate with frequencies that are multiple of the line frequency, these frequencies can be considered "low" when compared with the value of 20kHz (minimal value typically used by high frequency converters).

For this 2 output stage example, there are 4 distinct output levels per semi-cycle. In general, a structure with n output stages presents a maximum of 2^n levels (if appropriated transformer ratios are used, such as multiples of 2).

Finally, it should be noted that levels widths are not equal, but must be optimized in order to minimize the total harmonic distortion (THD) of the output voltage. Usually this is done using selective harmonic elimination algorithms or minimizing THD contents. This last procedure were adopted in this work, where a numeric algorithm were used in order to calculate widths that minimize the output voltage THD calculated until the 40^{th} harmonic.

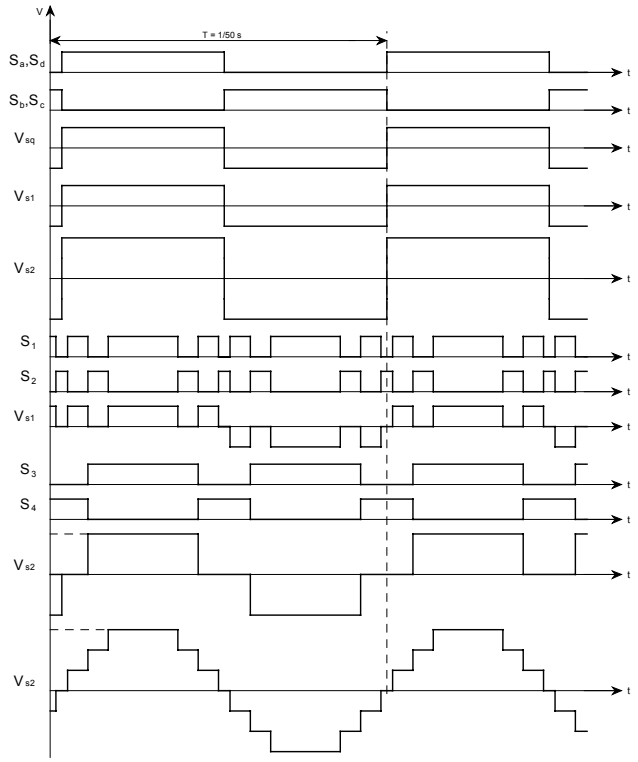

Fig. 3. Typical switches command signals and voltage waveforms for a two output stage stricture.

III. CONVERTER DESIGN

A. Design Guides

The main objective of the proposed inverter is to reach the demand of small stand-alone renewable energy systems. Although converter design was focused in the optimization of efficiency and no-load consumption, other aspects like cost, weight, voltage regulation and audible noise were considered as well. Due to these reasons, the following settings were used in this project:

1. **Output power of 3 kVA**: most small isolated systems requires no more then 1 kW of continuos power. A 3 kVA inverter can supply these consumers and also can start loads such as a refrigerator or a monofase water-pump.
2. **Nominal input voltage of 48 V**: many photovoltaic systems work with this voltage value and it is also suitable for 3 kVA (reasonable value of input current).
3. **Structure with 5 output stages which leads to up of 31 output levels**: With this number of levels it is possible to achieve very good output voltage regulation (aproximatelly 2,6 %). It is important to note that cost difference between structures with 4 or 5 output stages are not significant.
4. **Switches implemented by MOSFET**s: in the full bridge, MOSFETs were chosen (instead of IGBTs) due to its better performance at low voltages. The same occur in the output, because total voltage is divided between the several output stages.
5. **Toroidal Transformer**: toroidal transformers presents low no-load losses and are lighter than

their equivalent conventional transformers. They also saturate very easily but this effect can be minimized controlling properly the full-bridge switching.

B. Selection of a Bi-directional Switch Configuration

Using MOSFETs, a bi-directional switch can be implemented by several configurations, as shown in Fig. 4.

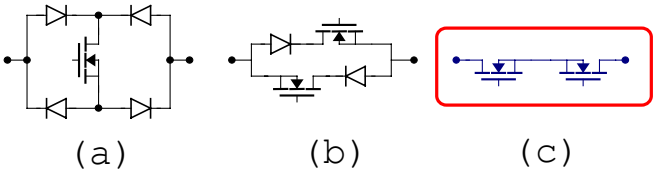

Fig. 4. Different bi-directional switch implementations using MOSFETS.

For the power range of 3 kVA, configuration (c) was chosen because it provides lower losses when compared to (a) and (b), due to the low resistance of modern MOSFETS and its bi-directional channel conduction capability. In this case, when both MOSFETs of configuration (c) are on, it acts as a resistance of 2 times the value of R_{dson} of one MOSFET.

All switches used in the prototype are equipped with a dissipative snnuber of the type shown in Fig. 5. It is important to note that these snnubers increase the reliability while the dissipated total losses do not represent significant value (low frequency switching).

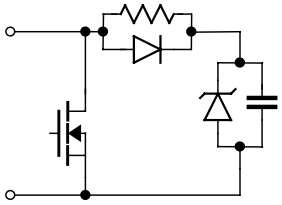

Fig. 5. Dissipative snnuber detail.

C. Operation Mode of each Bi-directional Switch

Ideally, each MOSFET that compose one bi-directional switch should be controlled independently, specially when the converter feed inductive loads. In practice, to achieve lower no-load consumption (lower number of drives) and to decrease costs, both switches are controlled by the same drive. In this case, when the inverter feeds an inductive load, the snubbers must provide a path for the load current during switching transitions (approximately 2 us). Again, low frequency switching allows design simplification.

D. Output filter

Although the proposed converter do not operate with high frequency switching, in practice some high frequency pulses appear at transition of switches stages (switches time delays associated with inductive behavior of the load and transformer dispersion are the causes of these effect). To minimize these undesirable pulses, the filter showed in Fig. 6 was connected between the converter output stage and the load.

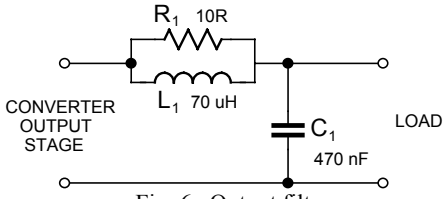

Fig. 6. Output filter.

IV. SIMULATION

In order to validate the proposed topology before implement it, a simulation of the structure shown in fig. 7 was done (using ORCAD 8.3).

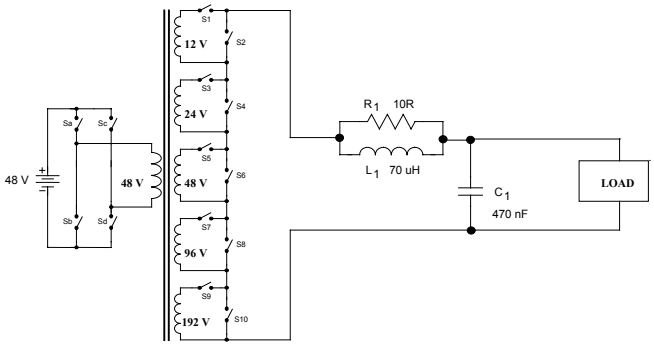

Fig. 7. Simplified schematic used in the simulation.

Simulation of this structure involved some problems regarding signals generation due to the high number of switches at the output stage, which must include time delays also. This problem was solved by creating a "pseudo-language" and a compiler to translate it into signals that could be used by the simulation program. Once this program was done, it was possible to easily make a set of simulations, with different number of output levels, time-delays and so on. List 1 shows the beginning of the code used to generate the signals used in the simulation.

```
I  sa=H sb=L sc=H sd=L
I  1=L 2=H 3=L 4=H;
I  5=L 6=H 7=L 8=H;
I  9=L 10=H;
S 20e-3   2000e-9   100e-9   12.0;

T 0.000200000          sc=b  sd=e;
T 0.000060000          2=e 1=a;
T 0.000160000          1=e 2=a  4=e 3=a;
T 0.000260000          2=e 1=a;
T 0.000380000          1=e 2=a  3=e 4=a   6=e 5=a;
T 0.000480000          2=e 1=a;
...
```

List 1. Piece of program code used to generate simulation signals.

As can be seen in List 1, there are 3 commands used by the compiler:

"I": defines the initial state of each signal (**H**igh or **L**ow);
"S": defines general settings (Period, Time delay, Rise/Falling time, signal level);
"T": defines transitions of signals. The first parameter is the reference time, followed by a list of swicthes that must

be switched around the reference time. ("=e": **e**xact, "=b": **b**efore and "=a": **a**fter). For example, "1=a" means that switch 1 must change it state at the reference time plus the defined time delay.

Once this program (text file) is defined, the compiler is used to produce individual text files for all defined switches. List 2 shows a piece of the text file that defines the command signal for switch S_1.

0.000000000	0
0.000062000	0
0.000062100	12
0.000160000	12
0.000160100	0
0.000262000	0
0.000262100	12
0.000380000	12
0.000380100	0
0.000482000	0
0.000482100	12
...	

List 2. Piece of S_1 command signal text file.

Fig. 8 shows the compiler graphic screen where all defined signals can be observed.

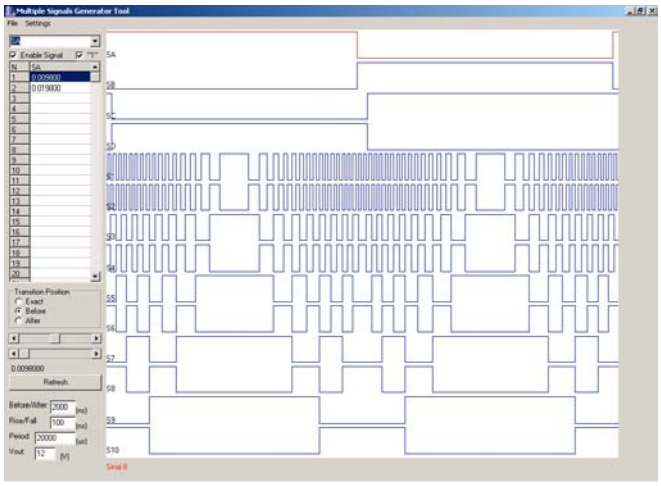

Fig. 8. Compiler screen, showing all signals.

Fig. 9 shows simulation result for the output voltage, before the filter stage. It can be observed a lot of spikes pulses, that occur in the switching instants due to the reasons already explained.

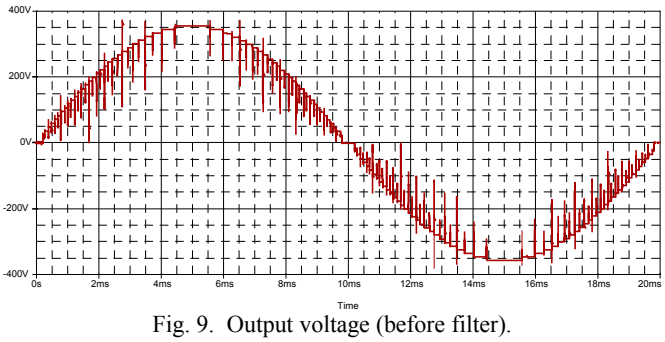

Fig. 9. Output voltage (before filter).

Using the proposed output filter, these spikes almost eliminated, as can be seen in Fig. 10.

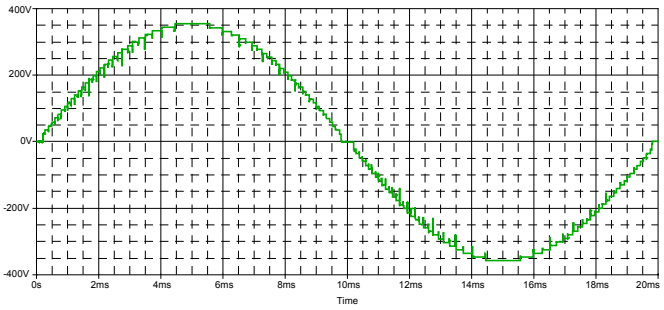

Fig. 10. Output voltage (after filter).

V. IMPLEMENTATION

An inverter of a 3 kVA, 48V/230V-50Hz was implemented and tested. Fig. 7 shows the basic structure of the prototype and Table II presents information about the switches used. When the converter is feeded with nominal voltage of 48V it can produce a maximum peak output voltage of 372 V (263 V_{rms}), allowing the system to always regulate the output voltage around 230 V_{rms}.

Relating to the conduction losses in MOSFETs of the output stage, it is important to note that most are dissipated in the MOSFETs of the higher voltage stages. Conduction losses due to the lower voltage stage represents approximately only 7 % of the total.

TABLE II
Data from all used Switches.

Stage	No. Sw.	Reference	Configuration	Total Rds*
Full Bridge	8	IRFP2907	2 in parallel	4 mΩ
Out. 12V	4	IRFP3205	2 in anti-series	16 mΩ
Out. 24V	4	IRFP3205	2 in anti-series	16 mΩ
Out. 48V	4	IRFP2807	2 in anti-series	26 mΩ
Out. 96V	4	IRFP260N	2 in anti-series	80 mΩ
Out. 192V	4	APT30M40LVR	2 in anti-series	80 mΩ

- Total equivalent R_{dson} due to all switches in the respective stage.

Fig. 11. shows a block diagram including main components of the prototype and Fig. 12 shows the implemented prototype. In order to make a comparison study with other already available inverters, the implemented prototype included all devices needed by a commercial product (aux. power supplies, input/output filters and protections).

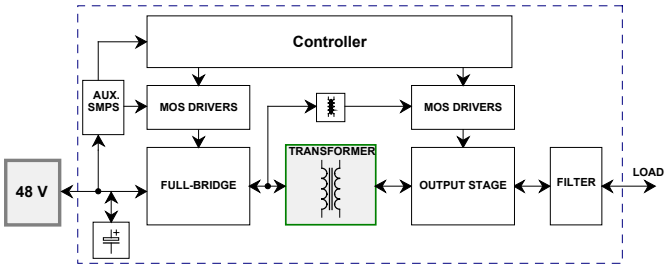

Fig. 11. Block Diagram Showing Main Components.

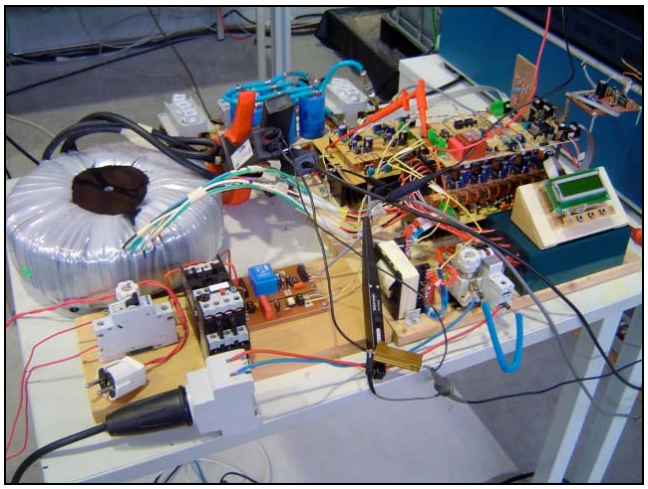

Fig. 12. Prototype overview.

VI. EXPERIMENTAL RESULTS

In order to evaluate the proposed inverter, tests with resistive and indutctive load were conducted. Fig. 13 shows the predicted and measured efficiency. Predicted efficiency was calculated considering the measured no-load losses (19,6 W) and resistances of switches and transformer (at ambient temperature). It is observed good concordance at light loads and above 1 kW increase in discrepancy can be mainly associated to temperature rise. Peak efficiency of 95,9% was achieved at output power of about 860 W.

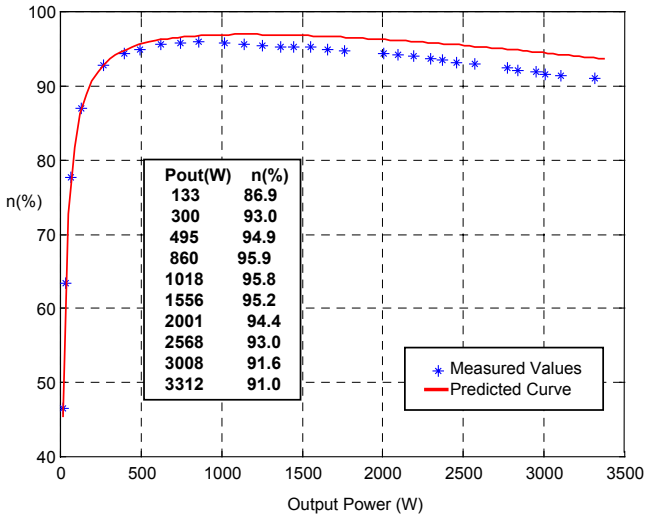

Fig. 13. Predicted and Measured Efficiency x Output Power (V_{in}=48V, V_{out}=230V).

Measured no-load (full functional inverter) is equal to 19,6W, distributed according to Fig. 14. Most of the no-load losses are associated with the power transformer (12W), followed by switching losses at the output stage (2,7W).

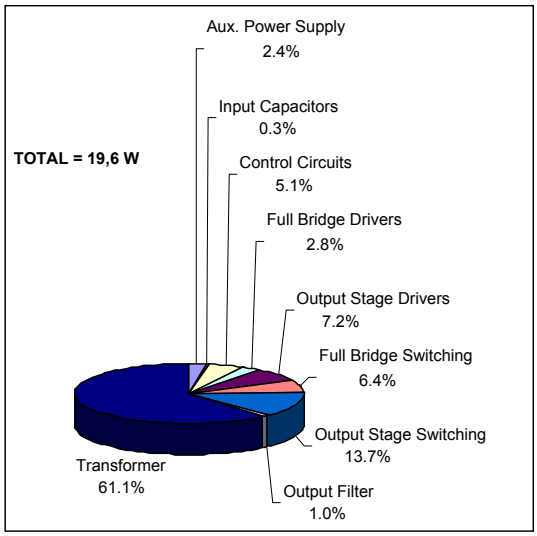

Fig. 14. No load losses Distribuition (V_{in}=48V).

The peak efficiency characteristic of the proposed inverter proved to be superior when compared to some products in the market, as shown in Table III.

TABLE III
Characteristics of some inverters.

Manufacture & Model	Nom Power (VA)	Peak Efficiency	No-Load Consumption (W)
Studer C3548	3500	95%	12
Trace SW3048	3300	95%	16
Phoenix 24/2500	2500	95%	6
Dakar 48/3000/50	3000	90%	4,8
Proposed Inverter	**3000**	**95,9%**	**19,6**

As can be seen no-load consumption still high, but it is expected that it could be optimized even more.

As shown in Fig. 15., total harmonic distortion (calculated until 40th harmonic) is bellow 2% even for the worst case where only 16 levels are used.

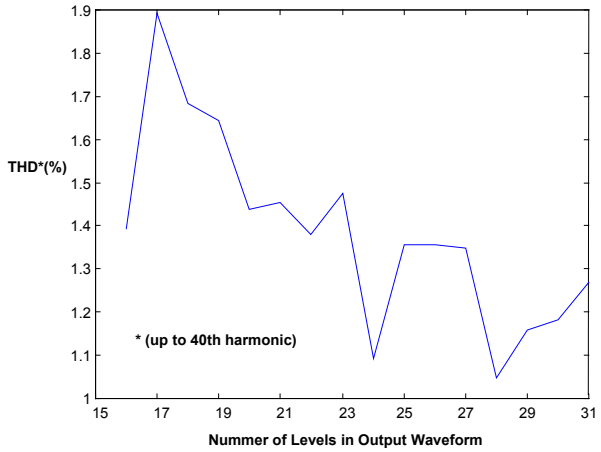

Fig. 15. Total harmonic distortion of measured output voltage versus number of levels.

In fact, output voltage waveform has excellent quality, as shown in Fig. 16. Bi-directional characteristic can be also seen in Fig. 16 where output voltage and current for a very high inductive load are presented. Closed loop output voltage regulation was easily implement in the prototype and good performance were achieved, as can be seen in the example of Fig. 17.

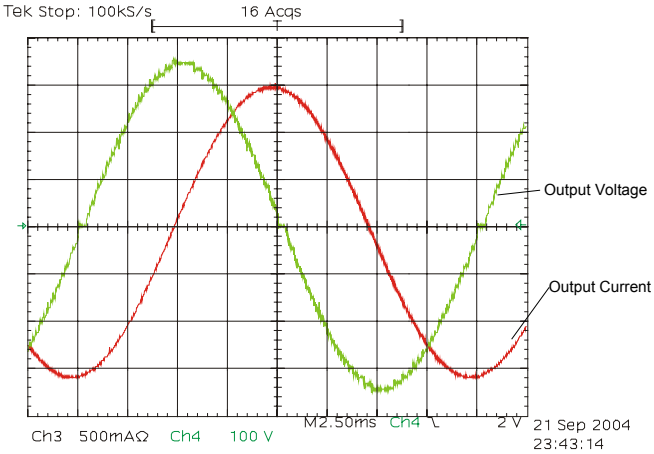

Fig. 16. Inductive load: output voltage and current.

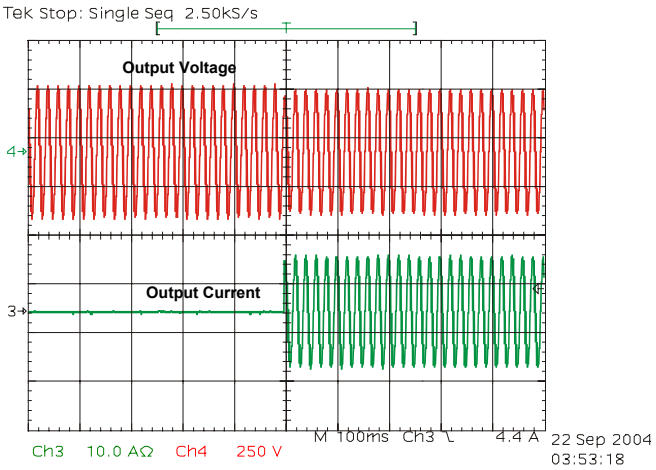

Fig. 17. Output voltage and current for a 2 kW load step.

Some practical tests with a heavy screwdriver under load (1500 VA - universal motor), small refrigerator and a combination of these loads with resistive load of 2 kW were done. The inverter was capable of start and operate all these loads without any problem.

VII. CONCLUSION

The proposed converter has high efficiency and excellent output waveform. It presents good voltage regulation and there is expected to be very reliable. In compare with similar products in the market, it showed to be competitive. Because of all its good features, it is suitable for the use in renewable energy systems.

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