STABILITY ANALYSIS OF A DIGITAL PREDICTIVE CURRENT CONTROLLER FOR PWM CONVERTERS

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***Abstract* – This paper analyzes the stability limits of a digital predictive current controller of a multi-loop control scheme. In particular, a current control technique based on deadbeat response with one sampling period delay for a PWM inverter is modeled and the effects of filter parameters mismatches on stability and robustness of the system under control are analyzed. Simulation results are presented and the algorithm is digitally implemented in a Digital Signal Processor (DSP) in order to verify the validity and drawbacks of the proposed approach.**

***Keywords* - Deadbeat control, pulse width modulation converters, stability analysis.**

I. INTRODUCTION

The use of microcontrollers and digital signal processors (DSPs) has been increasing in industrial applications, since these devices are designed for efficiently optimize real time digital signal processing with low computation times and low power consumption [1],[2]. As a consequence, digital control techniques have become a powerful tool, especially for PWM converters [1],[10].

Among different digital control strategies, predictive controllers with deadbeat response represent more and more an attractive option for practical implementations [5], [6], [9]. As most digital controllers, they have good performance in power converters applications if a reasonable model of the system under control is available. The main advantage of deadbeat response controllers is that they are designed for operation with fixed switching frequency and to have zero tracking error after a defined number of sampling periods. A simple design, implementation and fast dynamic response complement their main characteristics. The drawbacks are essentially sensitivity to parameter mismatches and to noise and the inherent delay due to computation and inverter actuation time [2],[3],[4].

In recent implementations [7],[8], this inherent delay is reduced to one sampling period by executing control and sampling routines twice in a modulation period. Another approach is presented in [6],[9], where the current controller is designed with a two-sampling period delay and the sampling period is equal to the modulation period. This paper presents a deadbeat current control strategy for a simplified converter model, in which a one sampling period delay is considered in the control law and the sampling period is equal to the modulation period. The control technique was developed considering a multi-loop configuration for the PWM inverter of a Dynamic Voltage Restorer (DVR) [11].

A stability analysis of the current loop is made by mapping the closed-loop poles in discrete-time domain and investigating the effect of filter parameters mismatches and DC link voltage limitation. The control algorithm is verified by means of simulation and is implemented on the DSP controller of a reduced-scale single-phase power converter to evaluate the controller performance and to extend the stability analysis of [5], [6], [7] and [9], which are the main contributions of this paper.

II. SYSTEM MODELING

A. Inverter Modeling

The power converter is represented by an averaged model (fig.1), in which the inverter averaged voltage $v_C(k)$ is a controlled voltage source with a zero-order hold (ZOH) sampling of the PWM reference voltage $v_{REF}(t)$. Indeed, this averaged model is effective only if the sampling frequency is much higher than the natural frequencies of the controlled system [6].

The output filter is a LC-type whose second-order dynamics is neglected in order to simplify the analysis. Thus, a first order model which takes into account only the inductive filter is considered. This assumption is correct only if the sampling frequency is much higher than the resonance frequency of the output filter, i.e., the inductor impedance is much higher than the capacitor impedance in the control frequency. Consequently, the output averaged voltage $v(k)$ is independent from the injected inverter current [5], [6], [9]. As this represents a model mismatch that may affect the dynamic response, a well known solution in these cases is to slightly oversize the capacitor filter to obtain desired responses [6].

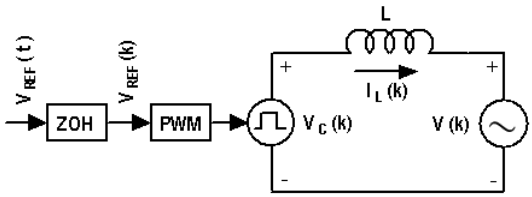

Fig.1 – Averaged model of the converter

For the purpose of stability analysis, the resistance of the inductor filter is neglected, since it represents a damping factor. Also, according to [8], digital predictive controllers are not sensitive to this parameter mismatch, but may become unstable when the inductance varies only ± 7%. The single-phase converter model can be derived from the inductor voltage drop:

$$\frac{di_L(t)}{dt} = \frac{1}{L}\cdot\left[v(t) - v_c(t)\right] \quad (1)$$

where $i_L(t)$ is the inductor averaged current. Discretizing (1) with sampling period Δ and using a trapezoidal approximation for the inverter voltage integral, the inverter dynamic equation is given by:

$$i_L(k+1) = i_L(k) + \frac{\Delta}{L}\cdot v(k) + \frac{1}{L}\int_{t_k}^{t_{k+1}} v_c(t)dt \Rightarrow$$

$$\Rightarrow i_L(k+1) = i_L(k) + \frac{\Delta}{L}\cdot v_c(k) + \frac{\Delta}{L}\cdot\frac{\left[v(k)+v(k+1)\right]}{2} \quad (2)$$

B. Control Algorithm

The multi-loop configuration in the control system block diagram of fig. 2 is particularly interesting for DVRs, since it provides overcurrent protection in the current loop [9]. The external voltage loop is responsible for output voltage compensation algorithm and load disturbances cancelation. Thus, in the current loop, there are two control cases that will be next described.

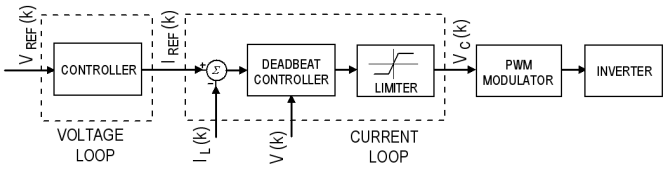

Fig.2 – Control system block diagram

1) Ideal case - The adopted deadbeat control technique consists in making the phase current error equal to zero by the end of the following modulation period (fig.3). In the ideal case, there is no delay in the control law, that is:

$$i_L(k+1) = i_L(k) + \frac{\Delta}{L}\cdot\left[v_{cref}(k) - v(k)\right] \quad (3)$$

To achieve deadbeat response, the inverter voltage $v_{cref}(k)$ calculated in the algorithm must be imposed and the reference current becomes:

$$i_L(k+1) = i_{ref}(k) \quad (4)$$

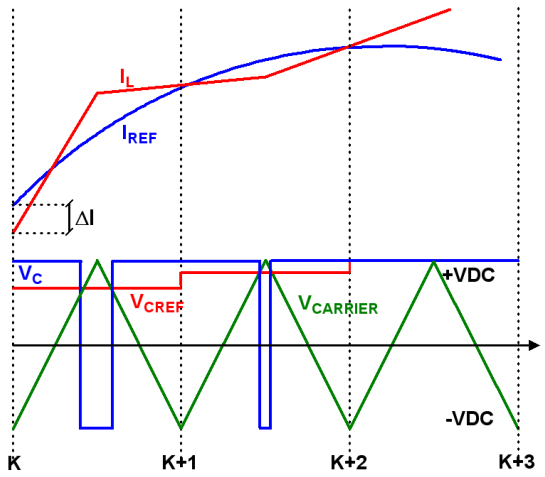

Fig.3 – Deadbeat Control - timing diagram

2) Real case- In practical implementations, there is an inherent delay due to computation time which is included in the control law as a multiple number of the sampling period. In the same way, in sampled carrier-based PWM modulators, the minimum actuation delay is equal to one modulation period. In the proposed controller, the sampling period is equal to the modulation period and the minimum delay adopted for the current loop is one sampling period.

Substituting (4) into (3) and now considering one sampling period delay:

$$i_{ref}(k) = i_L(k) + \frac{\Delta}{L}\cdot\left[v_{cref}(k+1) - v(k)\right] \quad (5)$$

As the inverter averaged voltage reference at sampling time $(k+1)$ is unknown, equation (5) shall be based on previous samples of control variables in order to make the control system causal:

$$v_{cref}(k) = \left[i_{ref}(k-1) - i_L(k-1)\right]\cdot\frac{L}{\Delta} + v(k-1) \quad (6)$$

In other words, at instant $k\Delta$ the inductor averaged current $i_L(k)$ and output averaged voltage $v(k)$ are sampled and the averaged voltage $v_{cref}(k+1)$ to be synthesized by the inverter is calculated by (6). This voltage reference, which makes the current error equal to zero at instant $(k+1)\Delta$, can be seen in fig.3. From the point of view of stability analysis due to inductor filter mismatches, (6) is better expressed as:

$$v_{cref}(k) = \left[i_{ref}(k-1) - i_L(k-1)\right]\cdot\frac{\alpha\cdot L}{\Delta} + v(k-1) \quad (7)$$

where α is a constant that models inductor filter mismatches.

III. STABILITY ANALYSIS

In real systems the actual inductance is slightly different from the modeled one, in which consists the stability analysis performed in this paper. Substituting (7) into (2):

$$i_L(k) = \alpha\cdot i_{ref}(k-2) + i_L(k-1) - \alpha\cdot i_L(k-2) + \\ + \frac{\Delta}{2L}\left[2v(k-2) - v(k-1) - v(k)\right] \quad (8)$$

The term of (8) which involves output voltage samplings at instants $(k-2)\Delta$, $(k-1)\Delta$, $k\Delta$, may be interpreted as disturbances in the current loop equation. If the sampling frequency is high, these disturbance terms may be neglected, since the output voltages are almost constant during two sampling periods. Applying the z-transform to (8) without disturbances terms, the closed loop poles of the resultant discrete transfer function are:

$$z_{1,2} = \frac{1}{2} \pm \frac{j}{2}\sqrt{4\alpha - 1} \quad (9)$$

In fact, the initial aim of the adopted control strategy was to obtain a deadbeat response of the predictive controller, but equation (9) shows that the response is not exactly deadbeat since the poles are not in the origin. If deadbeat response has to be assured, the algorithm must be modified according to [7],[8] or [6],[9] to achieve one or two sampling periods delay, respectively.

Figure 4 shows the closed loop poles on z-plane for $0 \le \alpha \le 2$. As it is well known, a control system is considered stable if the poles magnitudes in the z-plane are less than unity (within the circle in fig.4). According to (9),

for $\alpha > 1$ the system is unstable, for $\alpha < 1$ it becomes stable and if $\alpha = 1$, the system is critically stable (oscillatory), since $|z_{1,2}| = \sqrt{\alpha} = 1$.

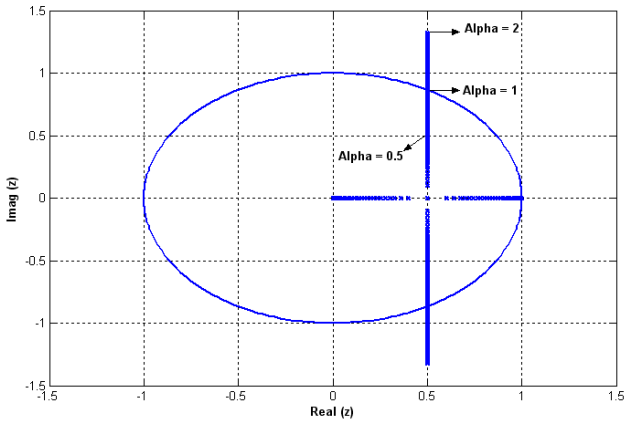

Fig.4 – Closed loop poles for $0 \le \alpha \le 2$

The relationship between the damped ω_d and sampling frequency ω_s is:

$$\frac{\omega_d}{\omega_s} = \frac{arctan\left(\sqrt{4\alpha - 1}\right)}{2\pi} \qquad (10)$$

Figure 5 plots the normalized oscillation frequency of equation (10) for $0 \le \alpha \le 10$. When the modeled inductance is equal to the real inductance ($\alpha = 1$), the relationship between the damped and sampling frequency is $\omega_d / \omega_s = 1/6$. As α tends to infinity, $\omega_d / \omega_s \to 0.25$ and for $\alpha \le 0.25$, the low-order oscillation frequency is not present. The performance of the current controller with respect to α will be discussed in section V.

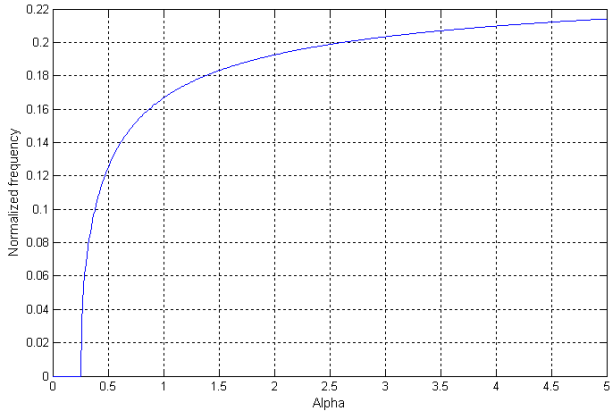

Fig.5 – Normalized frequency (ω_d / ω_s) for $0 \le \alpha \le 5$

In the previous presented derivation all control variables are measured and sampled. In fact, the output averaged voltage $v(k)$ can be estimated and one sensor may be eliminated. However, as stated in [5],[6],[7],[8], the stability limit is augmented when the actual control variable is used instead of the estimated (predicted) one. In [7], the maximum mismatch of the modeled inductance before the control system becomes unstable is 50% for measured values and 10% for estimated values. In [6], these values are 100% and 20%, respectively. Moreover, if the predictor is improved by adopting high order interpolations, the computation time increase and the poles may become more oscillatory[8]. In the case of the proposed approach, a stability analysis of this current controller with estimated variables is not justifiable, since the system is critically unstable without the inclusion of predictors.

IV. SIMULATION RESULTS

The system described in fig.1 has been simulated in PSIMCAD v.5.0.1 and MATLAB with the parameters of table I, for a low inductive load.

Figures 6 shows the simulation of equation (8) as a discrete time model applying ZOH sampling of the control variables. The disturbance terms are sampled from a 60Hz sinusoidal voltage source. Fig. 6 shows the inductor current and its reference for $\alpha = 1$. In order to obtain the harmonic content of the inductor current, a Fast Fourier Transform (FFT) algorithm with Hamming windowing was made and the result is presented in Fig 6 (bottom), where the amplitude is in percent of the fundamental component. As can be observed, the inherent $\omega_s/6$ low-order frequency oscillation (eq.10) is present with approximately 20% of peak value.

TABLE I
Current controller simulation parameters

Switching (sampling) frequency	10kHz
DC-Link Voltage	25V
Output filter inductance	12mH
Output filter capacitance	4.4μF
Load parameters	R_L=25Ω, L_L=12mH
Sinusoidal reference current, 60Hz	0.74A (peak)

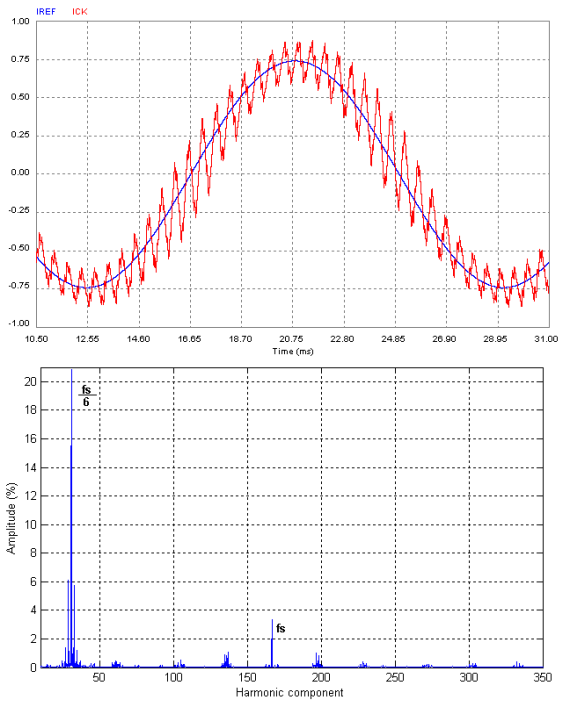

Fig.6 – $\alpha = 1$. Reference current (top blue) and inductor current (top red), simulated. Inductor current spectrum (bottom), fundamental not shown

Figure 7 (top) shows that for a normally acceptable filter inductance variation of only 5% *(α = 1.05)*, the system becomes unstable, which clearly means that the controller is highly sensitive to mismatches, as expected. In fig.7 (bottom) the same simulation is performed, but the inverter is now simulated as a voltage-controlled voltage source and the PWM-block is modeled as a comparator whose inputs are the inverter voltage reference and a 10kHz centered triangular-voltage source. In reality, as the output of a physical system is always bounded, the controlled system becomes critically stable due to DC-link voltage limitation effect in equation (8) and the stability limit is higher than expected from equations (8) and (9).

V. EXPERIMENTAL RESULTS

The control algorithm has been tested in a reduced-scale inverter for the simulation parameters of table I in a 16-bit fixed point ADSP-21992 Analog Devices Digital Signal Processor. The inverter pulses are generated by a sampled symmetrical PWM and the synchronization of sampling control variables is assured by the DSP. Fig. 8 (top) shows the inductor current and its sinusoidal reference for $\alpha = 1$ and the inductor current spectrum (bottom). The low-order frequency $(f_s/6)$ amplitude, when compared to simulation results, is attenuated due to the presence of resistances that were not included in the model, as discussed in section II.A.

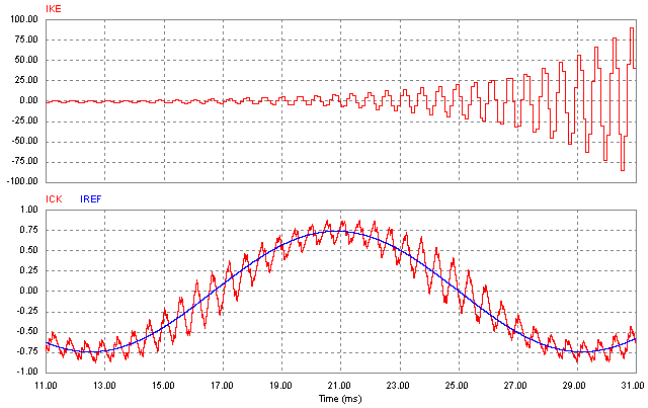

Fig.7 – α = 1.05 . Inductor current (top) applying equation (8), simulated. Reference current (bottom blue) and inductor current (bottom red), DC-Link voltage limitation, simulated.

For $\alpha = 2.0$ (fig. 9), the system is not unstable, as stated before. However, the inductor current ripple increases and the tracking response of the controller gets worse, what can be confirmed by comparing figures 8 and 9. Figure 10 shows the response of the controller for $\alpha = 0.5$. The system is not unstable, but the tracking response is affected.

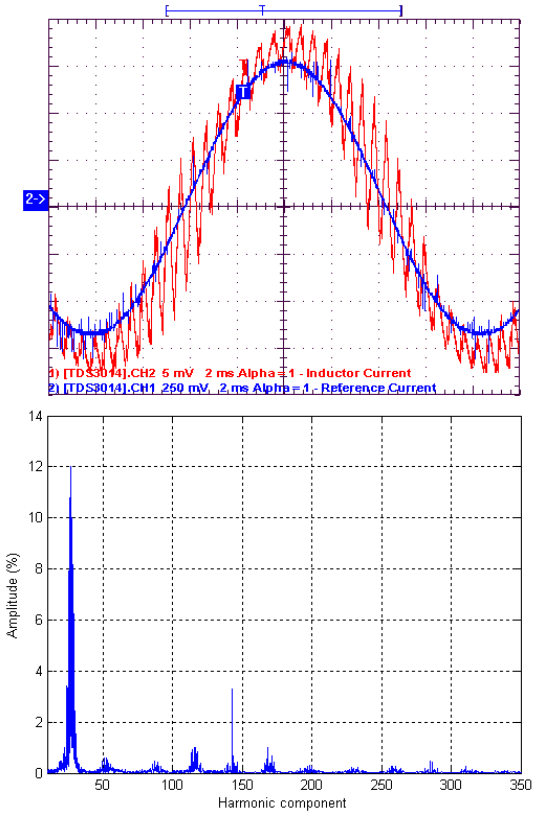

Fig.8 – α = 1. Reference current (top blue) and inductor current (top red), measured. Inductor current spectrum (bottom), fundamental not shown.

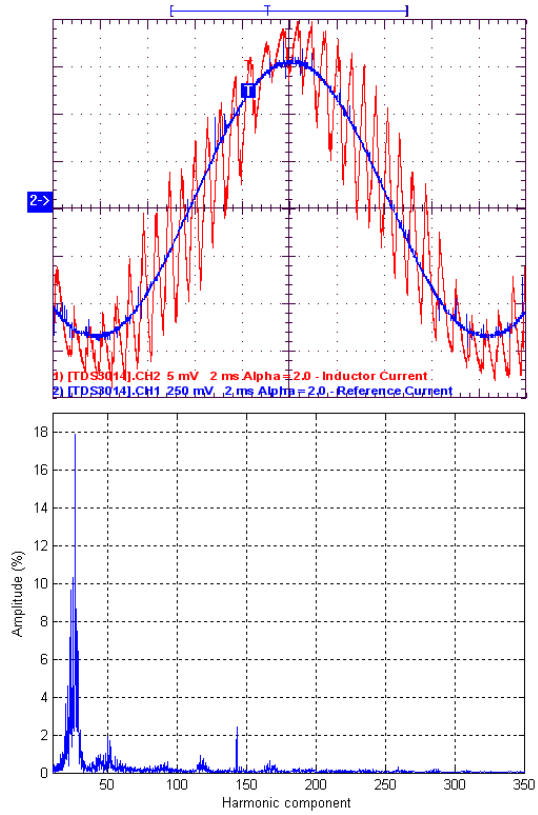

Fig.9 – α = 2. Reference current (top blue) and inductor current (top red), measured. Inductor current spectrum (bottom), fundamental not shown.

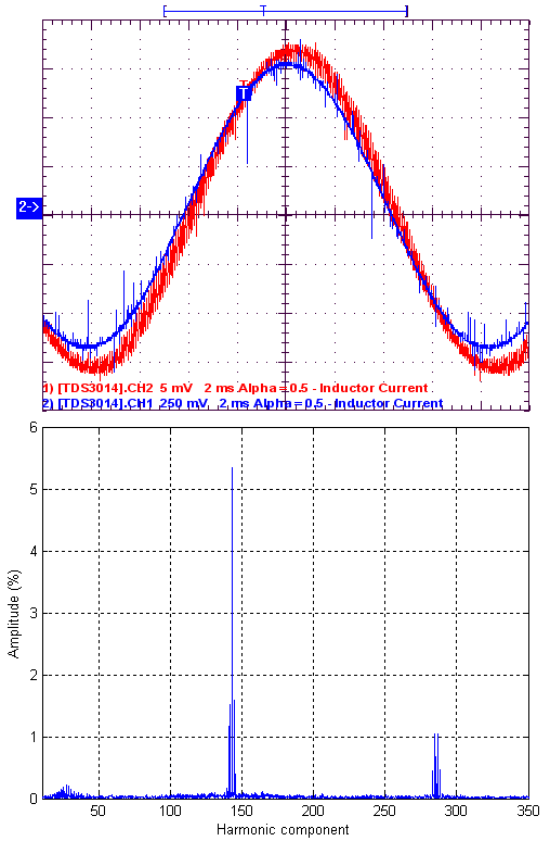

Fig.10 – α = 0.5. Reference current (top blue) and inductor current (top red), measured. Inductor current spectrum (bottom), fundamental not shown.

As can be seen in figs. 8, 9 and 10, in practice α could be increased indefinitely and the system would still have low-order oscillations, but would not be unstable, due to DC link voltage limitation. However, as α increases, the inductor current ripple and the tracking error increase, affecting the controller performance. Moreover, in order to avoid permanent damages to hardware devices, acceptable current ripple values must be considered. These two constraints will represent a practical limit for α.. In cases where a low-order oscillation frequency is unacceptable, the proposed controller is not recommended.

VI. CONCLUSION

This paper has presented a current control technique based on a simplified first-order model of the inverter and a predictive strategy with one sampling period delay and one control actuation per sampling period. The effects of the converter DC link voltage physical limitation and of the filter parameters mismatches on stability and robustness of the system under control were analyzed, simulated and experimentally verified on a reduced-scale implementation. The derivation of the stability analysis, which is in general ommited in the references, was detailed. The control system response is not exactly deadbeat as initially considered and as a consequence low-order harmonics are present in the inductor current. Finally, it was shown that if the model includes the DC-link voltage limitation, the stability limit of the system increases, but the controller performance is degenerated, especially if the filter inductance mismatch is high.

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