A MATRIX CONVERTER DESIGN

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Abstract – **A matrix converter to directly connect a three-phase load to a three-phase power source needs nine ideal bidirectional power semiconductor switches. Since these switches are not available yet, eighteen IGBTs and eighteen fast diodes may be used to construct the bidirectional switches. This high number of switches increases the complexity of the control of the matrix converter. This paper presents some design and implementation details of a 2 kW three-phase to three-phase matrix converter prototype. The input filter is designed so as to maximize the power factor.**

I. INTRODUCTION

The voltage source inverter (VSI) is widely used as a power converter for variable speed drives. However in recent years the matrix converter has been receiving considerable attention as a suitable alternative to the traditional VSI inverter.

The matrix converter is a forced commutated converter which can perform the power conversion directly from an AC power source to the load without any intermediate DC link. The matrix converter consists of an array of bidirectional power switches arranged in a matrix manner so that any of the *m* outputs of the converter can be connected to any of the *n* input voltage sources.

The idea of the matrix converter was first presented in [1] but the growing interest on this subject began with Venturini's paper [2] where a pulse width modulation method known as the direct transfer function method was presented. The direct transfer function method presents the only disadvantage of limiting the matrix converter rms output voltage to 50% of the rms input voltage.

In addition to the lack of an expensive DC link, which makes the matrix converter a compact power electronics circuit, other desirable features like sinusoidal input and output currents, regeneration capability and high power factor are considered to improve performance of the converter. Many papers have been published showing different types of pulse width modulation schemes designed to increase the input to output voltage gain of the matrix converter [3]-[6].

This paper deals with the design and the implementation of a 2 kW matrix converter prototype built in the laboratory with the objective of driving a three-phase induction motor. This converter is driven with space vector pulse width modulation algorithms [3] which allow the operation of the converter with unitary power factor and guarantee a converter voltage gain of 0.866.

II. MATRIX CONVERTER TOPOLOGY

The simplified three-phase to three-phase matrix converter topology is shown in Fig. 1, where $v_{i1}(t)$, $v_{i2}(t)$ and $v_{i3}(t)$ are the input voltage sources and $v_{o1}(t)$, $v_{o2}(t)$ and $v_{o3}(t)$ are the desired output voltages. The matrix converter bidirectional switches must be able to block voltage and conduct current in both directions. However, as there are no such switches commercially avaliable, a practical bidirectional switch can be constructed by using insulated gate bipolar transistors (IGBT) and diodes.

Since the input terminals of the matrix converter are connected to the input voltage supplies they cannot be short-circuited. And due to the inductive nature of most of industrial loads the output terminals cannot be ever left open.

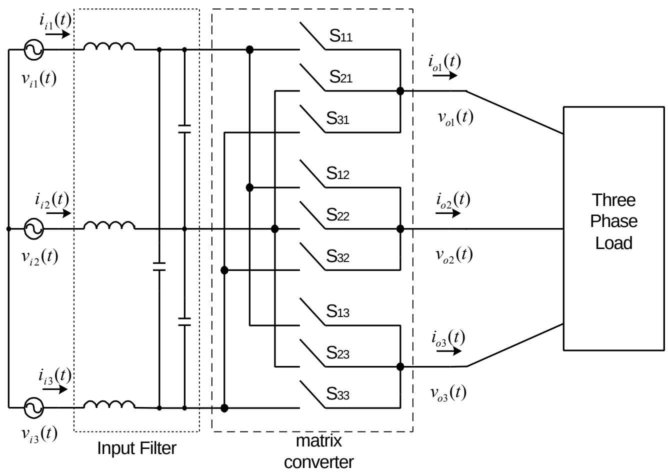


Fig. 1. Three-phase to three-phase matrix converter.

Let us consider S_{ij} a bidirectional switch of the matrix converter. The operating states of the switches are:

$$S_{ij} = \begin{cases} 1, & \text{if the switch is closed} \\ 0, & \text{if the switch is open} \end{cases} \tag{1}$$

Proper switch commutation in the matrix converter requires that (2) is satisfied:

$$\sum_{i=1}^{3} S_{ij} = 1 \quad for \quad any \quad j, j = 1,2,3 \tag{2}$$

Restrictions imposed by (2) mean that to provide safe operation or safe commutation two different input lines cannot be connected to the same output line and no output line can be disconnected to avoid overvoltages. These constraints result in only 27 possible switch combinations which can be divided into three groups. (i) The first one is composed of 6 possibilities with only one switch per input line conducting connected to different input lines (S_{11}, S_{32} and S_{23} for instance). (ii) The second group is composed of 18 possibilities of only one switch per input line conducting but two of them can be connected to the same input line (S_{21}, S_{32} and S_{33} for instance). (iii) The third group is composed of only 3 possibilities of the 3 switches connected to the same input line (S_{11}, S_{12} and S_{13} for instance). Due to the instantaneous power transfer of the matrix converter the electrical variables (voltage and current) on one side may be reconstructed from the corresponding variables on the other side at any time instant. For the space vector modulated matrix converter only groups ii and iii are used.

III. BIDIRECTIONAL SWITCH REALIZATION AND PROTECTION

Fig. 2 shows three possible manners to obtain a bidirectional switch by using unidirectional IGBTs and fast diodes available in the market.

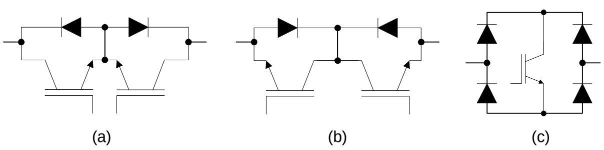


Fig. 2. Possible implementations of bidirectional power switches using IGBTs and diodes: (a) common emitter, (b) common collector and (c) diode bridge.

The common collector and common emitter configurations are preferred to the diode bridge. The technical literature shows that the diode bridge configuration causes higher conduction losses. The two topologies based on common emitter or collector connection of two IGBTs allow lower conduction losses and are the most used ones. The choice of bidirectional switch implementation will influence the hardware requirements of the matrix converter [7]. The common emitter configuration was chosen in this work due to the possibility of building the matrix converter in separate modules (as shown in Fig. 3) without external connection between modules. This approach facilitates tests of the matrix converter. The drawback of this configuration is the need of nine isolated power supplies. Each bidirectional switch is built (as shown in Fig. 4) by using the HCPL3140 gate drive optcoupler [8]. The IRGB15B60KD IGBT [9] with built-in fast diodes manufactured by International Rectifier was chosen due to its 10 μs short-circuit capability. This characteristic is essential in the design of the short circuit protection circuit since the protection circuit presents a delayed actuation. A line-to-line short circuit can occur if both bidirectional switches in the same arm (S_{11} and S_{21} for instance) are momentarily turned on due to any fault resulting from noise or control/drive malfunction. In the case of faults (using the example of S_{11} and S_{21}) the shoot through is detected by two Hall sensors placed in phases V_{i1} and V_{i3}. The protection circuit is implemented by using two standard comparators. The outputs of these comparators are received by a CPLD (Complex Programmable Logic Device). The CPLD sends a shutdown command to turn off all switches whenever a short circuit is detected.

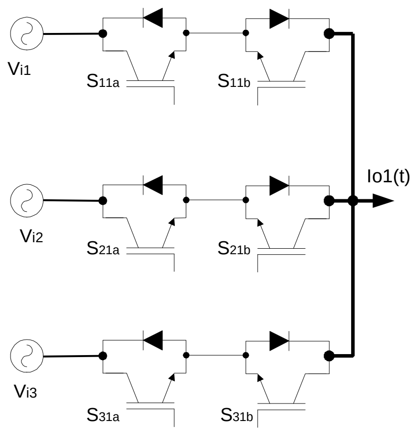


Fig. 3. One module of the matrix converter.

Since the IGBT turns off very quickly in the occurrence of a shutdown command the collector-emitter voltage rises due to the presence of inductive load and the IGBT may be destroyed by overvoltage. Besides this, overvoltage may be produced by line disturbance in the input of the matrix converter. To avoid these problems the switches of the matrix converter must be protected against overvoltage on both sides. The traditional clamp circuit is a common solution to protect the matrix converter but it would require twelve fast diodes and one capacitor. The number of diodes may be reduced to at least six in a new clamp circuit [10]. An alternative low cost solution (used in this work) for low power matrix converters is to use varistors to protect the converter [11].

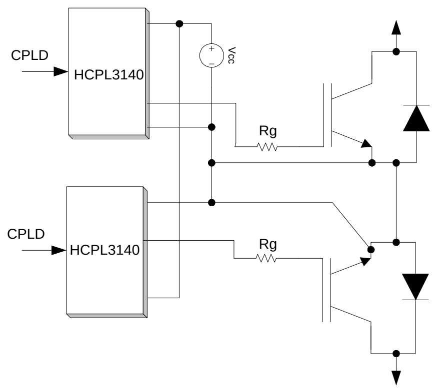


Fig. 4. Bidirectional switch implementation.

IV. SAFE COMMUTATION CIRCUIT

The strategy adopted here to get safe commutation of the matrix converter bidirectional switches is the four-step commutation [12]. This commutation scheme takes in account the current sign. It is shown in Fig. 5 and Table I regarding the module shown in Fig. 3. Let us consider for example that the bidirectional switch S_{11} (formed by IGBTs S_{11a} and S_{11b}) is conducting a current flowing from the source V_{i1} to the load (i > 0) and the matrix converter must commute to the source V_{i3}. The safe commutation that takes place is given by the state sequence $S_{aa} \rightarrow S_1 \rightarrow S_9 \rightarrow S_{10} \rightarrow S_{cc}$ and Table I gives the corresponding gate signal commands for the IGBTs.

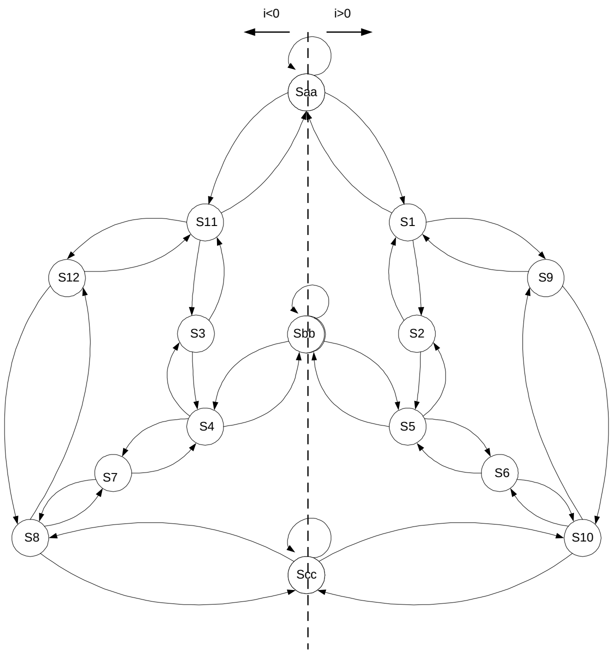


Fig. 5. State machine of safe commutation.

TABLE I
Possible states of the IGBTs

IGBTs						
S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	State
1	**1**	**0**	**0**	**0**	**0**	**Saa**
0	**0**	**1**	**1**	**0**	**0**	**Sbb**
0	**0**	**0**	**0**	**1**	**1**	**Scc**
1	0	0	0	0	0	S1
1	0	1	0	0	0	S2
0	1	0	1	0	0	S3
0	0	0	1	0	0	S4
0	0	1	0	0	0	S5
0	0	1	0	1	0	S6
0	0	0	1	0	1	S7
0	0	0	0	0	1	S8
1	0	0	0	1	0	S9
0	0	0	0	1	0	S10
0	1	0	0	0	0	S11
0	1	0	0	0	1	S12

The implementation of the state machine shown in Fig. 5 is realized with three CPLDs (Complex Programmable Logic Device) programmed with VHDL (Very High Speed Integrated Circuit Hardware Description Language) [13]. One CPLD is used for each of the three matrix converter modules. VHDL is a high-level language used to describe the behavior and the structure of digital systems. The XC9536 CPLD from Xilinx was chosen for this work [14]. It is an in-system programmable device and its I/O pins can be configured for 3.3 V or 5 V operation. They also provide up to 24 mA output currents that are sufficient for driving the HCPL 3140 optocouplers. The CPLD receives signals from three sources: one overcurrent bit from the protection circuit described in section III, one bit with information about the signal current of the load and three bits from the DSP (two bits carry information about the input voltage source to be connected and one bit is the start command).

The current signal of the load is obtained through a current signal detector composed of a Hall sensor, a second order Butterworth low pass filter with 5.2 kHz cutoff frequency and a comparator. This cutoff frequency was chosen to suppress the switching noise without significant time delay. The detector circuit is assembled on the same board of the module shown in Fig. 3. The information about the input voltage source which the bidirectional switch must be connected to is sent from the DSP to the CPLD with a two-bit coding: “00” represents input from the voltage source V_{i1}, “01” represents input from the voltage source V_{i2} and “11” represents input form the voltage source V_{i3}. Six ports of the CPLD are configured as outputs and are used to command the HCPL3140. Another port is configured as output to indicate an overcurrent occurrence through a LED. The CPLD was set to operate with 2 MHz clock frequency, which provides a safe operation margin to drive the IGBT since the turn-off delay time of the IGBT is about 230 ns.

V. PROGRAMMING OF THE SPACE VECTOR MODULATION ALGORITHM

In this paper the space vector modulation method [3] is used due to its simplicity to perform the duty cycle calculation and due to the fact that it provides a voltage gain of 0.866. In [6] it was proved that for a three-phase to three-phase matrix converter the upper limit on the voltage ratio is 0.866 for any modulation method.

In order to apply this technique the matrix converter is modeled as two distinct converters. The first converter behaves as an input rectifier with current link and the second one as an output voltage source inverter, as Fig. 6 shows. This approach permits to use the well-known space vector modulation method in both converters.

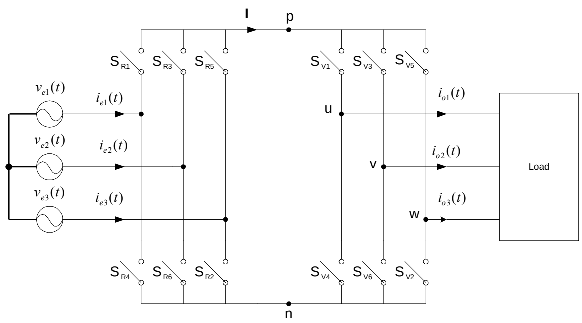
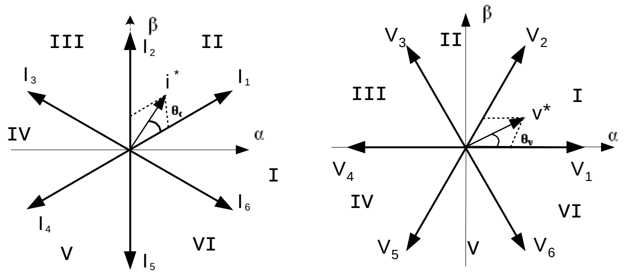


Fig. 6. Matrix converter model.

On the rectifier side there are nine possible combinations that correspond to six active space vectors (I_1-I_6) and three zero vectors (I_7-I_9), as Fig. 7a shows. On the inverter side there are eight possible combinations which produce six active vectors (V_1-V_6) and two zero vectors (V_7, V_8), as shown in Fig. 7b.



(a) (b)

Fig. 7. Space vectors: (a) rectification side, (b) inversion side.

Any bidirectional switch of the matrix converter must perform both rectification and inversion simultaneously resulting in thirty-six combinations of vectors $\mathbf{V}^*$ and $\mathbf{I}^*$. Using the subscripts *a* and *b* for the active input current vector that precedes and succeeds respectively the desirable input current vector $\mathbf{I}^*$ and the subscripts *c* and *d* for the active output voltage vectors that precedes and succeeds respectively the desirable output voltage vector $\mathbf{V}^*$, the switching times are given by the following set of equations [3], where T_s is the sampling time and *m* is the modulation index.

$$\begin{aligned} t_{ac} &= T_s.m.sin\left(60^0 - q_c\right).sin\left(60^0 - q_v\right) \\ t_{ad} &= T_s.m.sin\left(60^0 - q_c\right).sin\left(q_v\right) \\ t_{bd} &= T_s.m.sin\left(q_c\right).sin\left(q_v\right) \\ t_{bc} &= T_s.m.sin\left(q_c\right).sin\left(60^0 - q_v\right) \\ t_0 &= T_s - t_{ac} - t_{ad} - t_{bd} - t_{bc} \end{aligned} \tag{3}$$

The angle q_c is obtained by means of a PLL. The input current vector is synchronized with the input voltage and unity power factor can be achieved. The angle q_v and the voltage sectors are found by integration of the output voltage frequency and time product. Five registers from the timer 1 of the TMS320F2812 DSP [15] are loaded with the switching times from equations (3) and generate the switching sequence shown in Fig. 8.

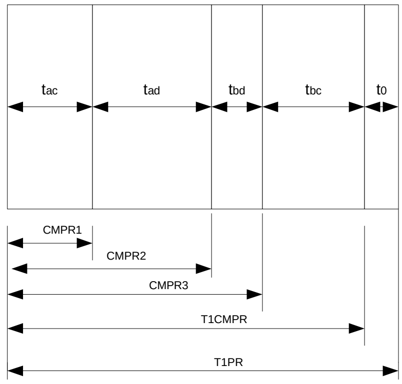


Fig. 8. Switching sequence scheme.

VI INPUT FILTER DESIGN

Because the matrix converter acts as a current source converter for the electrical power source an input filter is necessary to filter the high frequency ripple of the input currents. Considering Fig. 6 where the input of the matrix converter is modeled as a rectifier with current link, the input filter may be modeled using the harmonic equivalent circuit shown in Fig. 9.

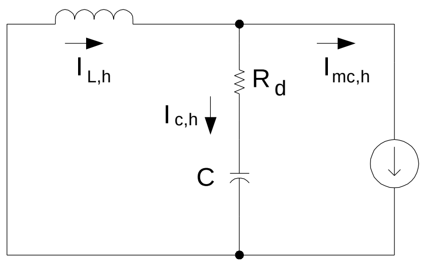


Fig. 9. Input filter model.

The transfer function G(s) of the input filter is:

$$G(s) = \frac{I_{L,h}}{I_{mc,h}} = \frac{1 + sR_dC}{s^2LC + sR_dC + 1} = \frac{1/LC + R_ds/L}{s^2 + R_ds/L + 1/LC} \tag{4}$$

The damping ratio and the natural angular frequency of *G(s)* are given by equations (5) and (6).

$$x = \frac{R_d}{2w_nL} = \frac{R_d}{2}\sqrt{\frac{C}{L}} \tag{5}$$

$$w_n = \frac{1}{\sqrt{LC}} \tag{6}$$

The design of the input filter described here aims to maximize the input displacement factor (IDF) as suggested in [16]. With this design criterion the upper limit of the filter capacitor value is given by equation (7), where I_m is the maximum input current, V_m is the maximum input voltage and w is the angular frequency of the input voltage [17].

$$C_{max} = \frac{I_m}{wV_m} tan(cos^{-1} IDF) \tag{7}$$

As shown in [16], the IDF depends on the modulation index *m* so that decreasing the modulation index *m* the IDF decreases. In this work the input filter was designed so that a desired IDF of 0.98 is achieved when the matrix converter operates with *m*=0.80. With an input phase rms voltage of

127 V the maximum input current I_m will be 5.6 A with m=0.85. This yields a maximum capacitance C of approximately 15 μF. With delta-connected capacitors this value decreases to 5 μF. According to [18] polypropylene film capacitors must be used to comply with this application.

The inductance L is calculated with equation (6). In order to minimize the inductor size a cut-off frequency of 2.9 kHz was chosen and the result is L=250 μH. A toroidal inductor of iron powder core was used. The damping resistor R_d was calculated according to equation (5) with dumping ratio x=0.25. With this dumping one finds R_d=2.5 Ω. With delta connection connection this value is increased to 7.5 Ω. Fig. 10 shows the attenuation characteristic of the designed filter.

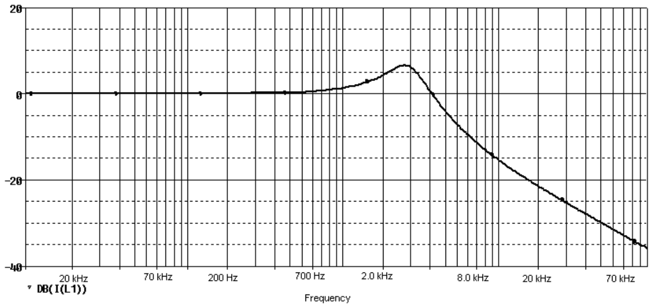


Fig. 10. Attenuation characteristic of the input filter.

VII RESULTS

A three-phase to three-phase matrix converter feeding a RL load with R=15 Ω and L=2 mH was simulated with Simulink. The input phase rms voltage was 127V and the modulation index was set at m=0.80. The filtered input current and the input voltage are shown in Fig. 11 and the IDF is shown in Fig. 12. The total harmonic distortion (THD) of the input current is about 12%.

Fig. 13 shows experimental results obtained with a low power and low voltage converter built with 74HC4316 CMOS bilateral analog switches. As the power matrix converter is under construction at the time this paper is being written it was only possible to test the space vector modulation algorithm implemented on DSP with low voltage and low power circuits. Fig. 13 shows the waveforms of the output voltage of the matrix converter.

VIII CONCLUSION

Some design aspects of the matrix converter were shown in this paper. The bidirectional switch implementation, the safe commutation circuit and the filter design are covered in this work. The power matrix converter is now being finalized and its results will be shown in a future paper.

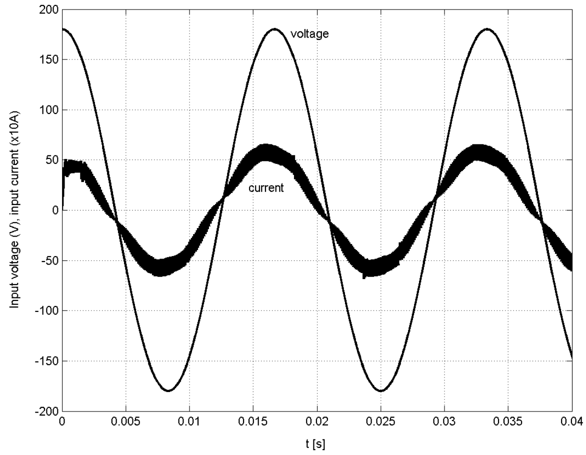


Fig. 11. Input voltage and current of the matrix converter (simulation result).

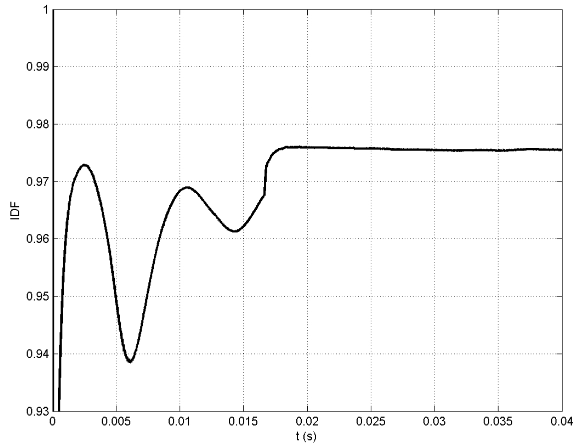


Fig. 12. Input displacement factor caused by input filter (simulation result).

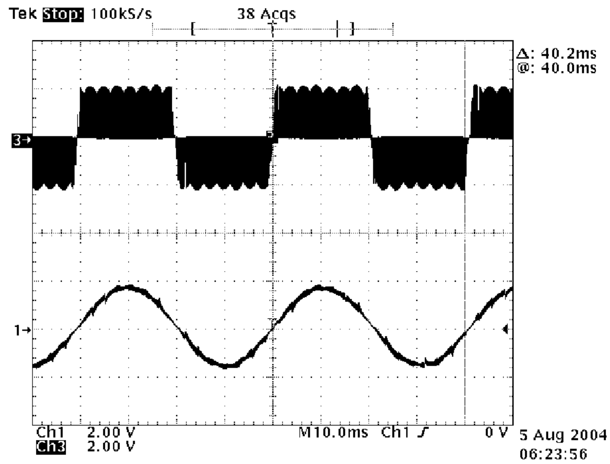


Fig. 13. Channel 3: Output line voltage. Channel 1: Filtered output line voltage.

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