AN IMPROVED NEUTRAL-POINT VOLTAGE BALANCING IN A HYBRID PWM STRATEGY FOR MULTILEVEL VOLTAGE SOURCE INVERTERS

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***Abstract* – This paper proposes an algorithm that allows for improving the balance of neutral-point voltage in three-level inverters. The techniques takes advantage of the concept of a "broad sense" distribution ratio, which includes employing zero and small voltage vectors. A technique with control loop is introduced for balance as a function of the mid-point voltage and the phase current signal. In addition it is shown that under certain conditions there is no need of feedback signals for balance. Simulated and experimental results verify the validity of the proposed technique.**

***Keywords* – Distribution Ratio, Inverter, Multilevel, PWM, Voltage Balancing.**

I. INTRODUCTION

Different from other works on multi-level inverters [1], some papers used PWM strategies based on the correlation between three-level carrier-based PWM (CB-PWM) and Space vector PWM (SV-PWM) methods [2]-[4], similarly to the correlation developed for two-level inverters to obtain results identical to SV-PWM when an appropriate zero sequence component is injected into the carrier system references [5]-[8]. Using such correlation the concept of "distribution ratio" was extended to three-level inverters in [2], which includes the use of either a zero vector or a small vector, differently from two-level case.

Very recently, using the idea of small hexagons introduced in [2] - which allows to reduce the PWM strategy employed in a higher level inverter to that of the two-level inverter - Refs. [9] and [10] extended the concept of "broad sense" distribution ratio to levels higher than 3 without any of the complication in its derivation.

One inherent problem that occurs in the diode clamped inverter topology (Fig. 1) is the input capacitor voltage unbalance caused by small and medium vectors and the direction of load current as discussed in other papers [3][10][11]. This paper proposes an algorithm that allows for improving the balance of the neutral-point voltage in diode clamped inverters. A technique with control loop is introduced for balance as a function of the mid-point voltage and the phase current signal. In addition it is shown that under certain conditions there is no need of feedback signals for balance. Simulated and experimental results validate the theoretical studies.

II. THE PROPOSED METHOD

In the representation of three-level space voltage vectors in Fig. 2 (27 space vectors), the triangle formed by $\mathbf{V_0}$, $\mathbf{V_7}$, and $\mathbf{V_9}$ (Sector 1) can be divided into 4 small triangles A, B, C, and D. So it is for the other Sectors. Such space vector diagram can be reduced into six two-level diagrams [3]. Each two-level diagram is centered in a vector belonging to the group of small vectors ($\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_4}$, $\mathbf{V_5}$, and $\mathbf{V_6}$) in Fig. 2, also used to shift the center of the three-level hexagon to the center of a two-level hexagon on dependence of the region in which is situated the reference vector $\mathbf{V_S}$, given by

$$\mathbf{V_S} = \mathbf{V_M} + \mathbf{V_i} \quad \text{with } i = 1, 2, \ldots 6 \tag{1}$$

Vectors $\mathbf{V_i}$ depend on which small hexagon is being considered [9][10].

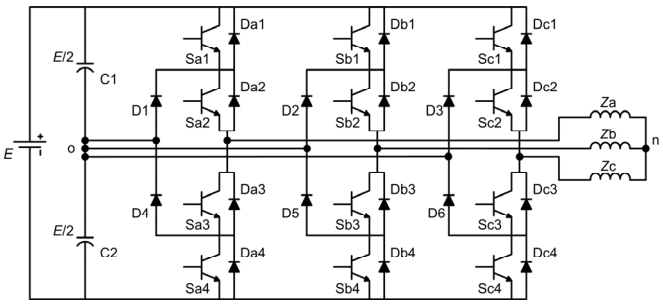


Fig. 1. Diode-clamped three-level inverter.

For Sector 1 and small triangle D in Fig. 2, $\mathbf{V_M}$ (reproduced with the help of vectors $\mathbf{V_7}$ and $\mathbf{V_8}$) is determined from $\mathbf{V_S}T_S = \mathbf{V_1}\, t_1 + \mathbf{V_7}\, t_7 + \mathbf{V_8}\, t_8$, that is,

$$\mathbf{V_M} = V_{Md} + jV_{Mq} = (\mathbf{V_7} - \mathbf{V_1})\frac{t_7}{T_S} + (\mathbf{V_8} - \mathbf{V_1})\frac{t_8}{T_S} \tag{2}$$

Considering that t_1, t_7, and t_8 are the corresponding time of application of vectors $\mathbf{V_1}$, $\mathbf{V_7}$, and $\mathbf{V_8}$ and that

$$T_S = t_1 + t_7 + t_8 \tag{3}$$

Different approaches can be used for determining t_7 and t_8.

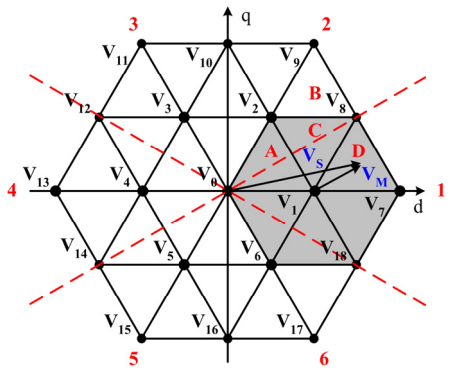


Fig. 2. Three-level inverter: space-vector diagram.

Consider the arbitrary sampling period of Fig. 3 when the CB-PWM technique applied to a three-level inverter uses

two triangle carriers of same amplitude and frequency. Superscripts *i* and *f* refer to the initial and final values at the modulation interval. Consider now the "broad sense" distribution ratio concept as introduced in [2], that is, the relation μ between the duration of $\mathbf{V_1}$ at the beginning (or at the end) of the modulation interval relatively to the duration of that interval. This relation μ involves the use of either a zero vector (for smaller amplitude modulation ratio) or a small vector (as for the modulation ratio in the case) for the three-level inverter.

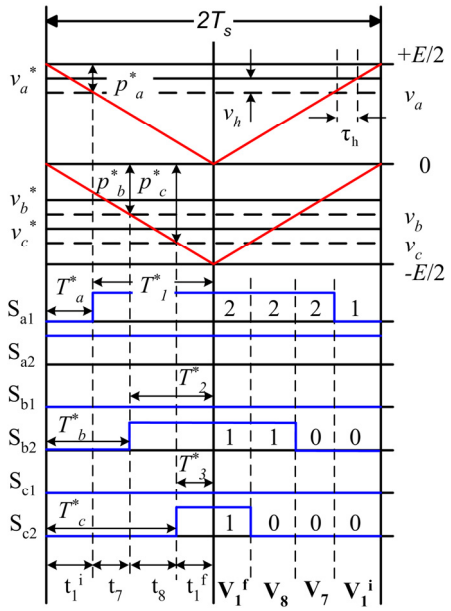


Fig. 3. Three-level inverter: correlation between CBPWM and SVPWM.

From that figure, it can be shown that

$$t_1^i = (1-\mu)t_1,\ t_1^f = \mu t_1 \tag{4}$$

With , $0 \le \mu \le 1$ being the distribution ratio.

From Fig. 2

$$v_x^* = v_x + v_h \quad \text{with } x = a, b, \text{ or } c \tag{5}$$

It can be shown that

$$v_h = -\left\{(1-2\mu)\frac{E}{2} + \mu v_{max} + (1-\mu)v_{min}\right\} \tag{6}$$

With v_{min} = min $\{v_a, v_b, v_c\}$ and v_{max} = max $\{v_a, v_b, v_c\}$ for a given sector.

Equation (6) only applies to two-level inverters. Similar equations for higher level inverters can be obtained by same approach at the expenses of additional complication in its derivation. Such complication can be avoided after a simple mathematical manipulation. Replacing $v_{max} = v_a$ and $v_{min} = v_c$ into equation (6) - for Sector 1 - gives

$$v_h = -(1-\mu)\frac{E}{2} + \mu\left(\frac{E}{2} - v_a\right) + (1-\mu)(0 - v_c) \tag{7}$$

By considering that each of the levels of a N-level inverter level is represented by a horizontal axis that limits the graphics region of the sinusoidal references, v_a, v_b and v_c, as shown in Fig. 4, for N=3. Note that in Fig. 4 values P_a, P_b and P_c measures the differences between the levels and the corresponding sinusoidal reference voltages at a certain modulation instant. Also, P_c and P_a correspond to the maximum and minimum values, respectively, among the values of P_a, P_b and P_c, determined by:

If ($Axis$(k) ≥ v_x ≥ $Axis$(k+1)), then

$$P_x = Axis(k) - v_x \quad \text{with } x = a, b, \text{ or } c \tag{8}$$

Extension of results to any sector of operation and to any number of levels (N ≥ 2) gives [9][10]

$$v_h = \mu p_{min} - (1-\mu)\left(\frac{E}{N-1} - p_{max}\right) \tag{9}$$

With P_{min} = min $\{P_a, P_b, P_c\}$ and P_{max} = max $\{P_a, P_b, P_c\}$ for a given sector.

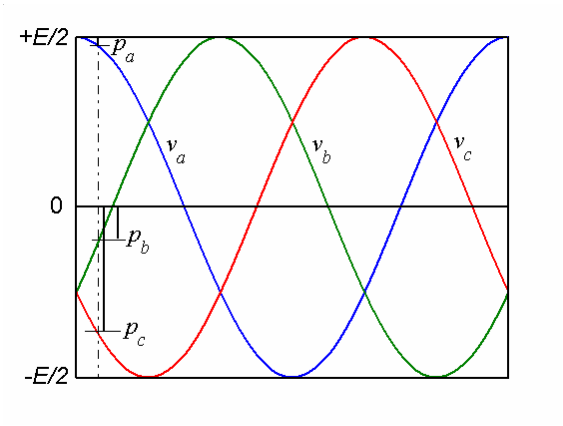


Fig. 4. dc levels in the three-level inverter.

A. Original algorithm [9][10]

The algorithm described next dispenses with the complicated derivation of v_h for N>3:

Step 1 - Consider the N levels of a N-level inverter level as represented by an axis limiting the sinusoidal references, v_a, v_b and v_c. The values of these levels are given by

$$Axis(k) = \left(\frac{1}{2} - \frac{(k-1)}{(N-1)}\right)E \tag{10}$$

With k = 1, 2, ..., N (see Fig. 4 for N=3).

Step 2 - After determining in which sector the reference vector is, calculate the values P_a, P_b and P_c, as shown in Fig. 4, using (8).

Step 3 - Calculate the distorted control signals v_x^* using (5).

Step 4 - Utilize signals v_a^*, v_b^* and v_c^*, obtained from Step 3, to calculate the new values P_a^*, P_b^* and P_c^*. Time intervals T_a^*, T_b^* and T_c^* (see Fig. 3) are given by

$$T_x^* = \frac{p_x^*}{\left(\frac{E}{N-1}\right)}T_s \quad \text{with } x = a, b, \text{ or } c \tag{11}$$

Step 5 - Calculate the signals width to command the inverter switches (T_1^*, T_2^* and T_3^*) using

$$T_y^* = T_S - T_x^* \quad \text{with } x = a, b, \text{ or } c \text{ and } y = 1, 2, \text{ or } 3 \tag{12}$$

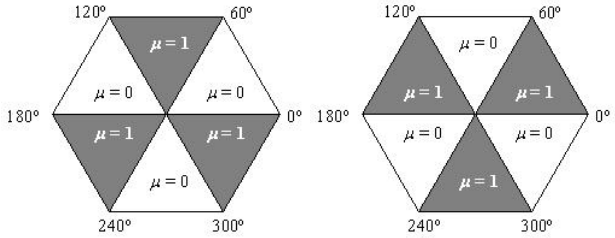
Step 6 - Determine the voltages v_{ao}, v_{bo} and v_{co}:

$$\text{If } (t < T_x^*) \text{ or } (t > 2\ T_y^*),\ v_{xo} = \text{value of } Axis(k+1) \tag{13}$$
$$\text{If } (T_x^* \le t \le 2\ T_y^*),\ v_{xo} = \text{value of } Axis(k)$$

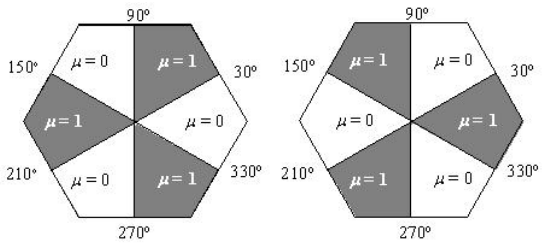
Where k = 1, 2, ..., (N-1) and y = 1,2, 3.

Ratio μ can assume either constant values among 0 and 1 of which μ = 0.5 corresponds to the symmetric modulation. It can also assume alternate values of 1 and 0. In addition, this change of values from 1 to zero or vice versa can occur - but

not restricted to - every 60 degrees as shown in Fig. 5, starting either at 0 degrees - as graphically represented Figs. 5 (a) and 5 (b) - or at 30 degrees - Figs. 5 (c) and 5 (d). These possibilities are referred in this paper as Variations 1 to 4, which result in clamping one of the phases during 60 degrees, while the other two continue to be modulated. This corresponds to a reduction of switching losses, with additional reduction if the clamping interval is placed in the neighborhood of the phase current peak for a given load phase angle. This technique is algebraic and can be used with any of the methods applied to two level converters.



(a) Variation 1 (b) Variation 2

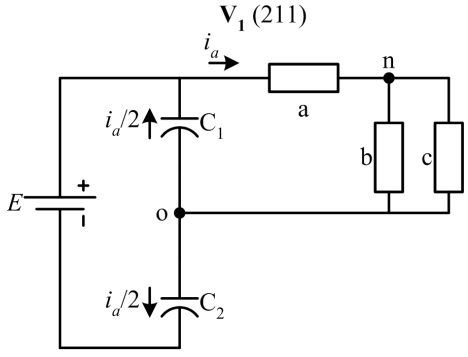


(c) Variation 3 (d) Variation 4

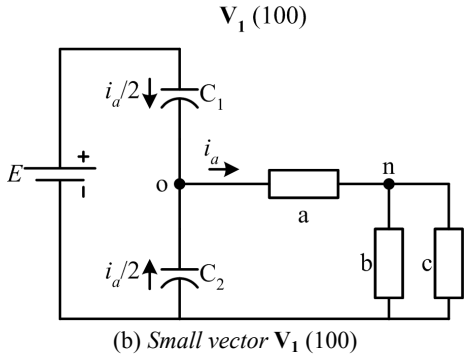
Fig. 5. Multilevel PWM: variations of μ.

B. Voltage Balance and Modified Algorithm

In the diode clamped inverter topology an input capacitor voltage unbalance does occur caused by *small vectors*, $\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_4}$, $\mathbf{V_5}$, and $\mathbf{V_6}$, and *medium vectors,* $\mathbf{V_8}$, $\mathbf{V_{10}}$, $\mathbf{V_{12}}$, $\mathbf{V_{14}}$, $\mathbf{V_{16}}$, and $\mathbf{V_{18}}$ (see the diagram in Fig. 2) and the direction of load current as discussed in other papers [2][11]. This is shown by the examples in Fig. 6 and Fig. 7, respectively. *Zero vectors*, $\mathbf{V_0}$, and *large vectors,* $\mathbf{V_7}$, $\mathbf{V_9}$, $\mathbf{V_{11}}$, $\mathbf{V_{13}}$, $\mathbf{V_{15}}$, and $\mathbf{V_{17}}$, they do not affect the capacitor voltage balance, as show in examples of Fig. 8.



(a) *Small vector* $\mathbf{V_1}$ (211)



(b) *Small vector* $\mathbf{V_1}$ (100)

Fig. 6. Capacitor voltage balance: *small vector* $\mathbf{V_1}$.

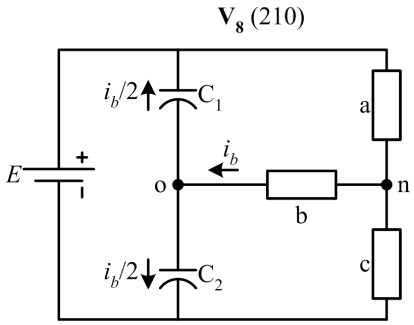
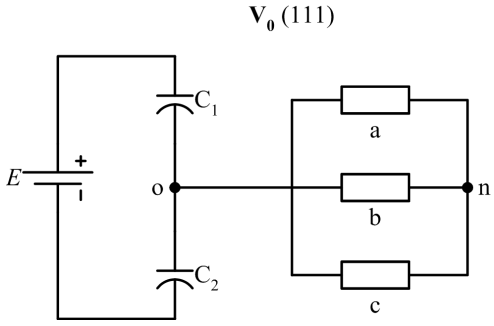
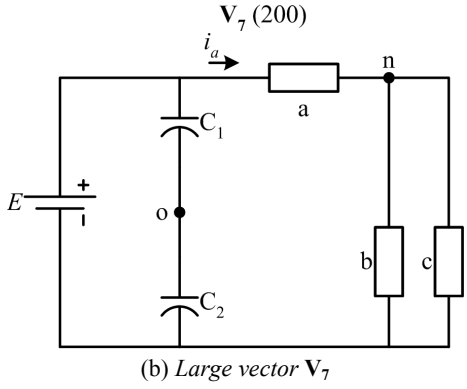


Fig. 7. Capacitor voltage balance: *medium vector* $\mathbf{V_8}$.



(a) *Zero vector* $\mathbf{V_0}$



(b) *Large vector* $\mathbf{V_7}$

Fig. 8. Capacitor voltage balance.

For the small vectors group, one of the possible configurations that realize a given small vector charges one capacitor, while discharges the other (or vice versa,

depending on the phase current direction). The other configuration has the opposite behavior. It is easy to conclude that voltage balance can be obtained by alternately using these two configurations. Since there is just one configuration for each vector of the medium vectors group, it is impossible to compensate the unbalance inside the group.

Now consider Fig. 3. In order to maintain equal capacitor voltages inside the modulation interval T_S, the duration of application of vector $\mathbf{V_1}$ (100), t_1^i, must equal the duration of application of vector $\mathbf{V_8}$ (211), t_1^f, added to the duration of application of vector $\mathbf{V_8}$ (210), that is,

$$t_1^i = t_1^f + t_8 \tag{14}$$

Also, the duration of application of vector $\mathbf{V_1}$ can be made null either at the beginning or at the end of the interval. This technique modifies the charge capacitors during each modulation interval. This can be seen. It can be implemented from the concept of distribution ratio. Figure 9 (a) shows the effect of μ in the capacitor neutral point balance. The neutral point voltage increases for $\mu = 1$ ($t_1^i = 0$) because of the elimination of vector $\mathbf{V_1}$ (100) from the switching pattern and decreases for $\mu = 0$ ($t_1^f = 0$) because eliminates $\mathbf{V_1}$ (211) from the switching pattern. These effects suggest that Variations 1 to 4, that is the variation of μ from 0 to 1, or vice versa, periodically, can be used to balance the capacitor neutral point voltage. However, results in Fig. 9 (b) shows that such balance is only obtained when some control loop is used.

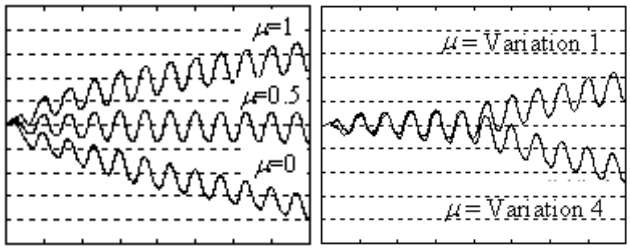


Fig. 9. Simulated results: capacitor neutral point voltage in a three level inverter (a) with different μ and (b) by alternating $\mu = 0$ and $\mu = 1$ (Vert.: 20V/div; Hor.: 50ms/div).

The use of $\mu = 0.5$ also does not eliminate unbalance, since this value allows for equal duration (and compensation) for the two small vectors at the beginning and at the end of the interval but does not compensate the medium vector $\mathbf{V_8}$ (210), which also affects the capacitor voltage balance. How to compensate the effect of the medium vector?

Since the approach in the algorithm reduces the analysis of a N-level converter to a that of a two-level converter lets consider the calculation of v_h for N = 2, even though N = 3. It can be shown that the variation in the pulse width, τ_h due to v_h for a three-level inverter, is given by

$$\tau_h = \frac{v_h}{\left(\frac{E}{2}\right)} T_s \tag{15}$$

Consider the generalized duration of application of the vectors during the modulation interval, that is, t_u^i, t_v, t_w, and t_u^f. It can be shown that for $\mu = 1$, because

$$T_x^* = T_x - \tau_h \quad \text{with } x = a, b, \text{ or } c \tag{16}$$

The modified pulse width in each phase is

$$\begin{aligned} T_a^* &= T_a - \tau_h = t_u^i - t_u^i = 0 \\ T_b^* &= T_b - \tau_h = t_u^i + t_v - t_u^i = t_v \\ T_c^* &= T_c - \tau_h = t_u^i + t_v + t_w - t_u^i = t_v + t_w \end{aligned} \tag{17}$$

Similarly, for $\mu = 0$

$$\begin{aligned} T_a^* &= t_u^i + (T_S + t_u^f) = t_u + T_S \\ T_b^* &= t_u^i + t_v + (T_S + t_u^f) = t_u + t_v + T_S \\ T_c^* &= t_u^i + t_v + t_w + (T_S + t_u^f) = t_u + t_v + t_w + T_S = 2T_S \end{aligned} \tag{18}$$

Note that for $\mu = 0$ the modified pulse width depends on T_S, of which the effect can be important at lower frequencies. Although for $\mu = 1$ the modified pulse width is independent of T_S, it eliminate the vector at the beginning, as mentioned before. Therefore, balance can be achieved by alternating between $\mu = 0$ and $\mu = 1$ at high frequency (small T_S) or by employing a control loop.

For $\mu = 0.5$,

$$\begin{aligned} T_a^* &= t_u^i - \frac{t_u^i}{2} + \frac{t_u^f}{2} + \frac{T_S}{2} = \frac{t_u}{2} + \frac{T_S}{2} \\ T_b^* &= t_u^i + t_v - \frac{t_u^i}{2} + \frac{t_u^f}{2} + \frac{T_S}{2} = \frac{t_u}{2} + t_v + \frac{T_S}{2} \\ T_c^* &= t_u^i + t_v + t_w - \frac{t_u^i}{2} + \frac{t_u^f}{2} + \frac{T_S}{2} = \frac{t_u}{2} + t_v + t_w + \frac{T_S}{2} \end{aligned} \tag{19}$$

After some mathematical manipulation, it can be shown that

$$T_a^* = t_u^{i*} = t_u^i + \left(t_u^f + \frac{t_v + t_w}{2} \right) \tag{20}$$

Similar results can be obtained for T_b^* and T_c^*. In this case, for each of these values of μ, the new value for the time of application of vector V_u^i is equivalent to the time of application of all other vectors so that the capacitor voltages are balanced.

Therefore, the use of N =2 with $\mu = 0.5$ in equations (8), (9), and (10) - and N = 3 from step 4 to step 6 - results in balance of the capacitor voltages for any frequency.

A technique that can be used to control the dc-link voltage employs an on-off controller (Fig. 10). A variable is made 1 or -1, modifying the modulation so that only one of the configurations among the small vectors is utilized inside one modulation interval. The error signal resulting of the comparison between the desired value for the mid-point voltage and the actual value determines which of the capacitors must be charged or discharged. Next, the product of the comparator output signal and the current signal determines which configuration among the small vectors should be chosen.

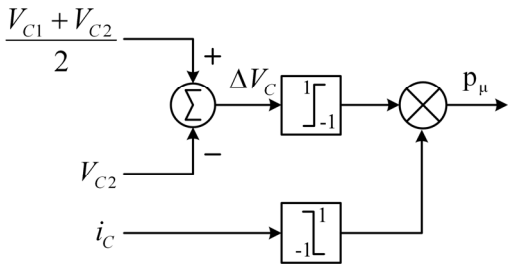


Fig. 10. Block diagram of the on-off controller.

III. SIMULATED AND EXPERIMENTAL RESULTS

The technique was digitally implemented with the help of a DSP, the algorithm being written in C^{++} [10]. Implementation of μ is accomplished with the help of the logic presented in Fig. 11 [6]. Signal $\mu = d$, corresponding to Variation 3, is obtained from b_j with the help of or-exclusive operations. b_j, in turn, is the output of comparators of which the inputs are the reference signals V_{xref} (x = a,b,c). Other Variations can be obtained by simply shifting of an adequate angle the signal corresponding to $\mu = d$. To take into account the phase angle, the signal $\mu = d$ is shifted as a function of ϕ, as in [6] and [12].

An experimental implementation was carried out to validate the technique in the case of three-level inverters, the load being constituted by a 4 poles, 5 hp three-phase motor, 220/380 V, connected in Y. Fig. 12 shows the experimental waveform for the line voltage when $\mu = 0.5$ and the switching frequency is 2 kHz for the modified algorithm. The capacitor voltages are balanced. The modified algorithm was then used for μ as a function of the phase angle - from 1 to 0 and from 0 to 1 - with a modulation index m = 0.9, cos ϕ = 0.95, a switching frequency of 10 kHz, and a three-phase RL load, for dc voltage E = 200V (Fig. 13). Note that the capacitor voltage is balanced. For a frequency of 750 Hz, the results in Fig. 14 show that the capacitor voltages unbalances. For $\mu = 0.5$, even for f_s = 750 Hz, the capacitor voltage is kept balanced (Fig. 15).

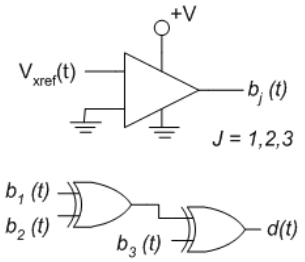


Fig. 11. Generation of signal *d* (Variation 3).

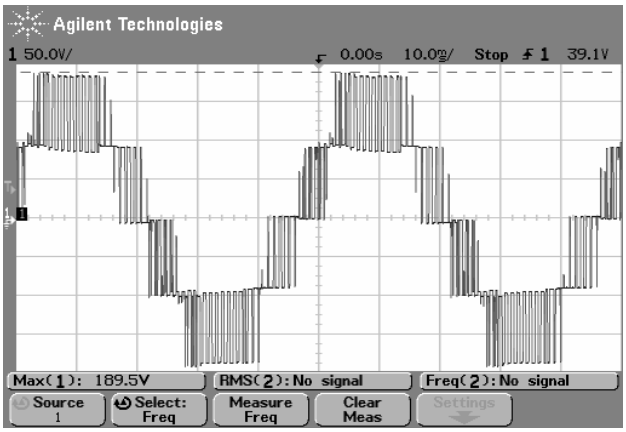


Fig. 12. Three-level inverter: experimental output line voltage with $\mu = 0.5$ and m = 0.9 (Vert.: 50V/div; Hor.: 10ms/div).

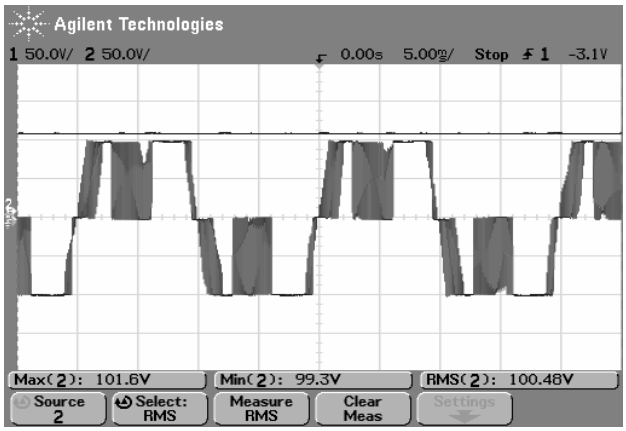


Fig. 13. Three-level inverter: experimental output pole voltage and capacitor voltage with $\mu = 0$ or 1 and m = 0.9 (Vert.: 50V/div; Hor.: 5ms/div).

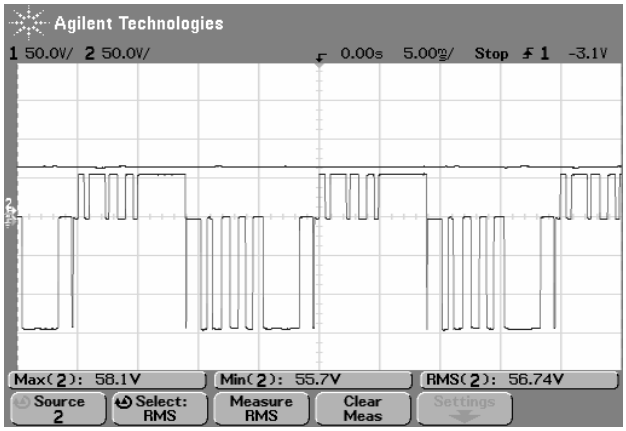


Fig. 14. Three-level inverter: experimental output pole voltage and capacitor voltage with $\mu = 0$ or 1 and m = 0.9 (Vert.: 50V/div; Hor.: 5ms/div).

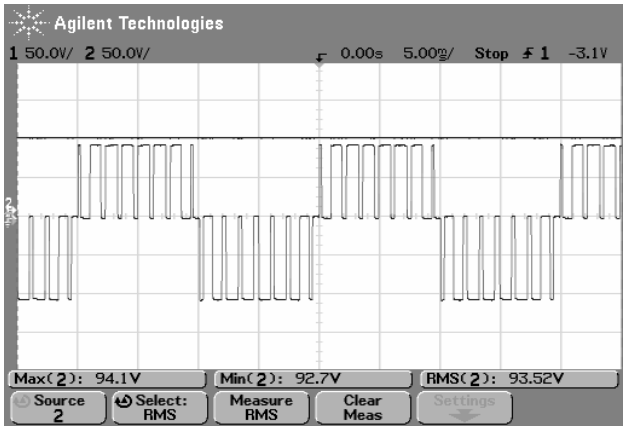


Fig. 15. Three-level inverter: experimental output pole voltage and capacitor voltage with $\mu = 0.5$ and m = 0.9 (Vert.: 50V/div; Hor.: 5ms/div).

Fig. 16 shows the experimental result for the line current when μ is a function of the phase angle - from 1 to 0 and from 0 to 1 and the switching frequency is 750 Hz, with a modulation index m = 0.9, cos ϕ = 0.95 and a three-phase RL. For $\mu = 0.5$, the line current is showed in Fig. 17.

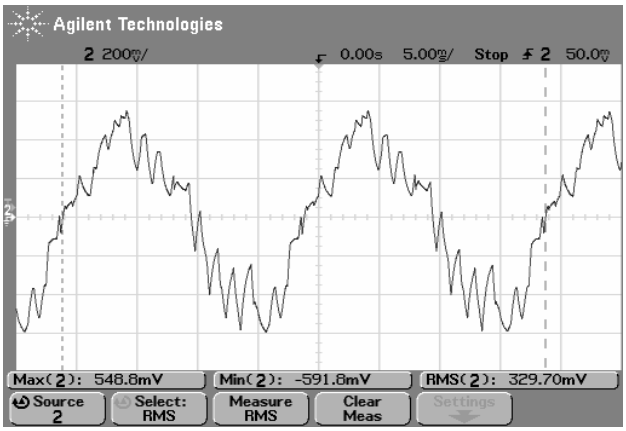


Fig. 16. Three-level inverter: experimental output line current with μ = 0 or 1 and m = 0.9 (Vert.: 2A/div; Hor.: 5ms/div).

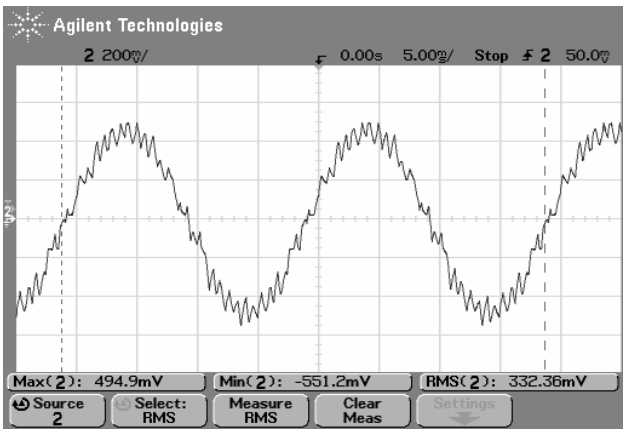


Fig. 17. Three-level inverter: experimental output line current with μ = 0.5 and m = 0.9 (Vert.: 2A/div; Hor.: 5ms/div).

Fig. 18 shows the simulated results when the on-off control is used for 750 Hz with μ varying between 0 and 1 (capacitor voltage ripple is limited in 5% of the E/2, E = 200V). The capacitor voltages are maintained balanced.

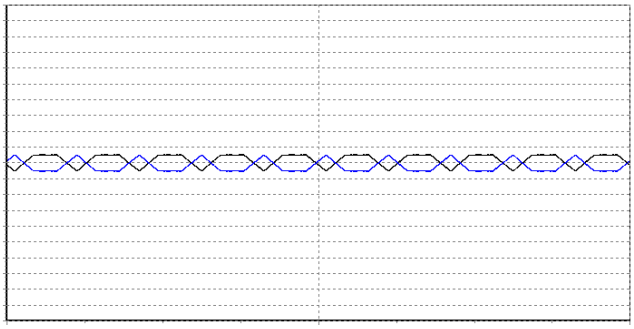


Fig. 18. Three-level inverter: simulated capacitor voltages with μ = 0 or 1 and m = 0.9 (Vert.: 10V/div; Hor.: 1s/div).

Results are coherent with the theoretical analysis.

IV. CONCLUSION

A modified algorithm is used to balance the neutral point voltage of a diode clamped three-level inverter, which guarantees balanced input capacitor voltages for any frequency under symmetrical condition. Under conditions different from the symmetrical one, such balance is achieved only at high frequencies (10 kHz). For low frequencies (750 Hz) an on-off controller is proposed to be included in control. Simulation and experimental results validate the theoretical analysis.

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