SELECTION OF DC SOURCES FOR THREE CELLS CASCADED H-BRIDGE HYBRID MULTILEVEL INVERTER APPLIED TO MEDIUM VOLTAGE INDUCTION MOTORS

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Abstract **- This paper proposes the definition of appropriate values of DC voltage sources for a three-cell cascaded H-bridge multilevel inverter. A set of possible configurations is obtained from a generalized design methodology for asymmetrical hybrid multilevel inverters. Several indexes will be used to define the appropriate configuration, such as: total harmonic distortion, first order distortion factor and analysis of conduction and switching losses for one phase of the hybrid multilevel inverter. This multilevel inverter will be used as a variable-speed drive for a 4.16kV/500hp three-phase induction motor.**

Keywords **- Hybrid Multilevel inverter, medium-voltage, variable-speed drive.**

I. INTRODUCTION

Multilevel inverters have been widely used in last years for high-power applications [1]. Variable-speed drives have reached a wide range of standard applications such as pumps, fans and others. Many of these applications use medium-voltage motors (2300, 3300, 4160 or 6600V), due to their lower current ratings in higher power levels [2]. Static VAr compensators and active filters are other applications that use multilevel converters [3].

Several topologies of multilevel inverters have been studied and presented. Diode-clamped inverters, flying-capacitors inverters and cascaded-inverters with separate DC sources are some examples of candidate topologies [4]. The industry often has used the neutral-point-clamped inverter, presented in [5]. However, the topology that uses cascaded-inverters presents some advantages, as smaller voltage rate (*dv*/*dt*), due to existence of higher number levels, producing less common-mode voltage across motor windings [6]. Also, if use the asymmetric hybrid cascaded inverter, a wide range of different semiconductor power devices, as IGBTs, IGCTs, GTOs and SCRs, can be used in different cells.

Applications, modulation strategies and control of multilevel inverters using H-bridge series-connected cells are presented in [6], [7], [8], [9] and [10]. A generalized design methodology for hybrid multilevel inverter is proposed in [11], and the analysis and comparison of hybrid multilevel voltage source inverters is presented in [12]. The study of the input rectifier stage for all H-bridge cells is discussed in [6], [7], [8], and [13].

This paper will apply the design methodology developed in [11] for a 4.16kV/500hp three-phase induction motor. It will be demonstrated the impact of this methodology in the number of possible configurations and number of levels reached in the inverter output. After to apply this methodology, it is possible to verify that a set of possible configurations can be used. Among these configurations, several indexes , such as the total harmonic distortion (THD), first order distortion factor (DF1) and conduction and switching losses in the multilevel inverter, are used to point which of the configurations is the most adequate candidate for this application.

II. THREE CELLS CASCADED INVERTER

Three cells cascaded H-bridge multilevel inverter is shown in Fig. 1. The output phase voltage ($v_a(t)$) is the sum of the output voltages of each cell ($v_{a,1}(t)$, $v_{a,2}(t)$, $v_{a,3}(t)$), (1), which $v_{a,1}(t)$ is the output of the cell with the lowest voltage and $v_{a,3}(t)$ with the highest voltage.

$$v_a(t) = v_{a,1}(t) + v_{a,2}(t) + v_{a,3}(t) \quad (1)$$

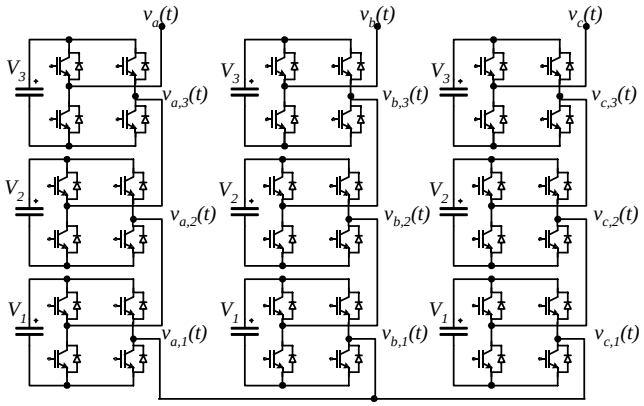

Fig. 1. Cascaded H-bridge hybrid multilevel inverter.

Three-phase induction motor that is driven presents the RMS line voltage of 4160V. Therefore, the peak value of the phase voltage is 3400V.

III. RESTRICTIONS TO DEFINE THE DC VOLTAGE SOURCES

To define the amplitude values of the DC voltage sources, the following restrictions should be respected:

i. DC voltage sources should be arranged so that the second source is equal or higher than first, and so on;
ii. DC voltage source values must be normalized in function of the lowest source voltage, and normalized values must be natural numbers;
iii. Adjacent levels must be equally spaced;
iv. Adjacent levels must be modulated at high frequency;
v. The highest voltage cell must process power levels equal or lower than the load;
vi. Any cell cannot regenerate power.

IV. CHOOSING THE APPROPRIATE CONFIGURATION

The steps presented in the previous section will be performed here after.

The restriction (*i*) considers that the DC voltage sources are arranged in an increasing way, and are given by (2), [14].

$$V_1 \le V_2 \le V_3 \tag{2}$$

The restriction (*ii*) guarantees that every DC voltage sources are multiples of V_1, and its normalized values are given by (3), [8], being $V_{base} = V_1$.

$$V_j = \frac{V_{cc,j}}{V_{base}} \quad and \quad V_j \in \mathbb{N}, \quad j = 1,2,...,n \tag{3}$$

The restriction (*iii*) is given by (4). The conditions (*iii*) and (*iv*) guarantee that every output inverter voltage levels are equally spaced [12].

$$V_j = 1 + 2\sum_{k=1}^{j-1} V_k, \quad j = 2,3,...,n \tag{4}$$

The sum of normalized values of DC sources by phase is σ_n, (5), and the number of levels is given by m (6), [12].

$$\sigma_n = \sum_{j=1}^{n} V_k \tag{5}$$

$$m = 1 + 2\sigma_n \tag{6}$$

Respecting the restrictions (*i*), (*ii*) and (*iii*), three sets of possible DC voltage sources obtained. The first is: $V_1 = 1$, $V_2 = 1$, $V_3 \le 5$. The second is $V_1 = 1$, $V_2 = 2$, $2 \le V_3 \le 7$. And the third set is $V_1 = 1$, $V_2 = 3$, $3 \le V_3 \le 9$. It presents a total of eighteen combinations that can be utilized, which are shown in Table I. The symmetric topology presents the lowest number of levels, 7, while the configuration 1-3-9 will present the maximum number of levels, 27.

TABLE I
Configurations for uniform adjacent levels

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	1	5	15
6	1	2	2	11
7	1	2	3	13
8	1	2	4	15
9	1	2	5	17
10	1	2	6	19
11	1	2	7	21
12	1	3	3	15
13	1	3	4	17
14	1	3	5	19
15	1	3	6	21
16	1	3	7	23
17	1	3	8	25
18	1	3	9	27

The restriction (*iv*) is employed to guarantee that all levels are modulated at high frequency, (7). With this the output voltage harmonic content will be concentrated around of the switching frequency of the inverter with lowest DC voltage source [7].

$$V_j = 2\sum_{k=1}^{j-1} V_k, \quad j = 2,3,...,n \tag{7}$$

After to apply this restriction, the possibilities decrease from eighteen to nine alternatives, that will be divided in two subsets: first, $V_1 = 1, V_2 = 1$, $V_3 \le 4$ and second, $V_1 = 1$, $V_2 = 2$, $2 \le V_3 \le 6$, Table II. Providing a maximum of 19 levels for the configuration 1-2-6.

TABLE II
Configurations for uniform adjacent levels and all levels modulated at high frequency

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	2	2	11
6	1	2	3	13
7	1	2	4	15
8	1	2	5	17
9	1	2	6	19

For the next analysis, the frequency (m_f) and amplitude (m_a) modulation indexes are given by (8) and (9), [12]. Being, f_s is the switching frequency of the lowest power inverter, f_r is the frequency of the reference signal and V_{refp} is the normalized peak value of the fundamental component of the reference signal:

$$m_f = \frac{f_s}{f_r} \tag{8}$$

$$m_a = \frac{V_{refp}}{\sigma_n} \tag{9}$$

Based on restriction (*v*), it is guaranteed that the highest power cell doesn't process a fundamental voltage higher than the load, for all values of m_a, (10), which V_n must be a natural number smaller or equal than has been found (7), [11].

$$V_n \le \frac{\pi}{2} \cdot \sum_{k=1}^{n-1} V_k \quad \in \quad \mathbb{N} \tag{10}$$

The restriction (*v*) determines that the maximum normalized value reached for the highest DC voltage source is four, and consequently now there are seven possibilities, Table III.

TABLE III
Possible Configurations for: uniform adjacent levels, all levels modulated at high frequency, and V_3 does not process a voltage higher than load voltage

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	2	2	11
6	1	2	3	13
7	1	2	4	15

The restriction (*vi*) establishes that none of cell can synthesize negative fundamental voltage for all excursion of m_a. Thus, uncontrolled rectifiers can be employed as front-end converter. With this requirement only two configurations can be implemented, and they are presented in Table IV.

TABLE IV
Possible Configuration for: uniform adjacent levels, all levels modulated at high frequency, V_3 does not process a voltage higher than load voltage and it utilizes only uncontrolled unidirectional rectifier

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9

V. MODULATION STRATEGY

The hybrid modulation strategy used was presented in [11], [12], and associates the stepped voltage waveform synthesis in higher power cell with high-frequency PWM modulation for the lowest power.

In this modulation strategy the reference signal of multilevel inverter is the same used with reference for the higher cell (cell 3), that is compared with two levels DC voltage ($+\sigma_2$ and $-\sigma_2$). The difference between the reference signal and output voltage of cell 3 is the reference for the cell 2, that is compared with ($+\sigma_1$ and $-\sigma_1$). The difference between de reference signal and the output voltage of cell 2 is the reference of cell 1, which is compared with a high frequency triangle carrier signal.

The output phase voltage results are presented in Fig.2 (a) for type 1-1-1 with seven levels and in Fig.2 (b) for type 1-1-2 with nine levels.

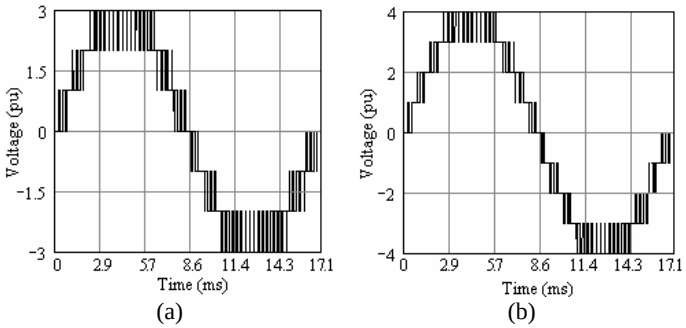

Fig.2. Phase-to-neutral voltage (a) Type 1-1-1 (b) Type 1-1-2

VI. ANALISIS OF TYPES 1-1-1 AND 1-1-2

Fig. 3 (a) and Fig. 3 (b) presents, respectively, the total harmonic distortion and the first-order distortion factor for the configurations 1-1-1 and 1-1-2. THD and DF1 of output phase-to-neutral voltage obtained with type 1-1-1 (THD = 18.8 % and DF1 = 0.26 %) are higher than the THD and DF1 obtained with type 1-1-2 (THD = 14.2 % and DF1 = 0.20 %), considering the amplitude modulation index (ma) equal to 1 and frequency modulation (mf) equal to 61. For this analysis the type 1-1-2 presents an improved performance.

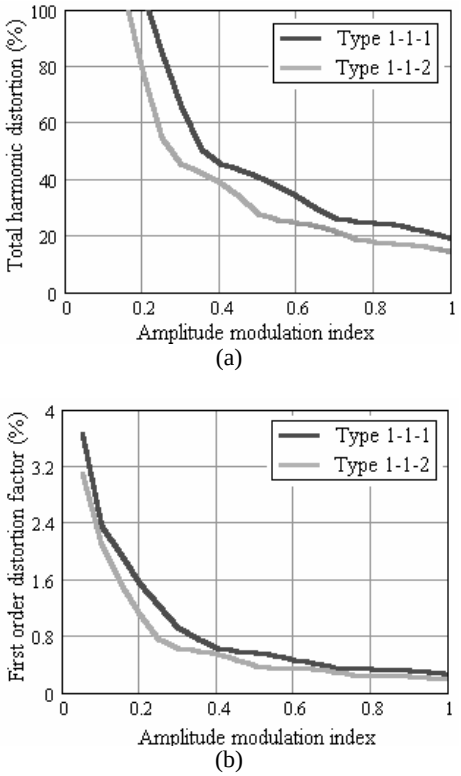

Fig. 3. Indexes for type 1-1-1 and 1-1-2, mf=61 (a) THD (b) DF1.

VII. POWER LOSSES ANALYSIS

The analysis of losses for cascaded H-bridge hybrid multilevel inverter is a complex process, due to the wide number of operation states of this converter. Moreover, this analysis becomes more difficult by using a hybrid modulation technique, because the semiconductor devices command signals and the switching frequencies are different for every cells.

To derivate the losses analysis is need the semiconductors devices information provides by the manufactures in its datasheets. Therefore, this analysis strongly depends on the power devices used. The use of components of different manufacturers can point to distinct results.

The methodology to determine the conduction and switching losses is discussed hereinafter, where total losses is the sum of all losses (11).

$$P_{TOTAI} = P_{cond_{TOTAL}} + P_{switch_{TOTAL}} \quad (11)$$

A. Conduction Losses

Conduction losses are those that occur while the semiconductor device is conducting current. A simplified model of the solid-state device is used to determinate the conduction losses. These models are given in (12) and (13) for an IGBT and a diode, respectively [6], [16] and [17].

$$v_{ce}(\theta) = V_{ce} + R_{ce}.\left|i_{load}(\theta)\right| \quad (12)$$

$$v_F(\theta) = V_F + R_F.\left|i_{load}(\theta)\right| \quad (13)$$

Where, $v_{ce}(\theta)$ and $v_F(\theta)$ are the on-state saturation voltage of the IGBT and diode, respectively, V_{ce} and V_F are the voltage drop for zero current of the IGBT and diode, respectively, R_{ce} and R_F are the equivalent resistance of the resistive components of voltage drop across the power device. $i_{load}(\theta)$ is the load current, given in (14)

$$i_{load}(\theta) = m_a.I_{max}(\theta - \phi) \quad (14)$$

Here, ϕ is the load power factor angle.

To determine the conduction losses of the IGBT and diode the load current sense must be observed. If $i_{load}(\theta) \geq 0$, then the IGBT is conducting (15), otherwise the diode is conducting (16).

$$P_{cond_{SW}} = \frac{1}{2.\pi}\int_0^{2.\pi} v_{ce}(\theta).i_{load}(\theta).v_{cmd_{SW_X}}(\theta)d\theta \quad (15)$$

$$P_{cond_D} = \frac{1}{2.\pi}\int_0^{2.\pi} v_F(\theta).i_{load}(\theta).v_{cmd_{SW_X}}(\theta)d\theta \quad (16)$$

Where, $v_{cmd_{SW_X}}(\theta)$ is the command signal of the switch SW*x*.

The total conduction losses are obtained from (17).

$$P_{cond_{TOTAL}} = P_{cond_{SW}} + P_{cond_D} \quad (17)$$

B. Switching Losses

The most accurate method of determining switching losses is to plot the current and voltage waveform in the controllable switch during the switching transition and multiplies the waveform point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy at turn-on or turn-off [15]. However, in this paper, the turn-on, turn-off and recovery losses are calculated based on the information of the manufacturer (data sheet), turn-on energy losses per pulse ($E_{on}(i_{load}(\theta))$), turn-off energy losses per pulse ($E_{off}(i_{load}(\theta))$) and reverse recovery energy ($E_{rec}(i_{load}(\theta))$).

The switching losses are obtained by identification of every instant of commutation, as at turn-on instant as turn-off instant during all reference period. Therefore, the turn-on losses, turn-off losses and reverse recovery losses are given by (18), (19) and (20), respectively.

$$P_{turn\ on} = \frac{1}{2.\pi}\sum E_{on}(i_{load}(\theta)) \quad (18)$$

$$P_{turn\ off} = \frac{1}{2.\pi}\sum E_{off}(i_{load}(\theta)) \quad (19)$$

$$P_{recovery} = \frac{1}{2.\pi}\sum E_{rec}(i_{load}(\theta)) \quad (20)$$

The total switching losses will be the summation of turn-on, turn-off and recovery reverse losses, given by (21).

$$P_{switch_{TOTAL}} = P_{turn\ on} + P_{turn\ off} + P_{recovery} \quad (21)$$

C. Example of conduction, switching and total losses determination

To conclude the analysis indicating the recommend configuration of DC sources of cascaded hybrid multilevel inverter, one example to calculate losses is presented based on software developed by MathCad®.

The maximum output phase voltage for the induction motor 500hp/4.16kV, is 3400V. Then, by configuration 1-1-1, each isolated source is equal to 1134V. Therefore, it is used a power device of the WESTCODE, IGBT TO360NA25, that subjects 2500V/360A. The functions of $v_{ce}(i_{load}(\theta))$, $v_F(i_{load}(\theta))$, $E_{on}(i_{load}(\theta))$ and $E_{off}(i_{load}(\theta))$ are obtained from the respective data sheet.

The configuration 1-1-2 has one DC source of 1700V and other two DC sources of 850V. In the cell 3 is used the EUPEC IGBT FF200R33KF2C (3300V/200A). However, in the cells 1 and 2 is used the EUPEC IGBT BSM200GB170DLC (1700V/200A).

In Fig. 5 (a) is shown the conduction losses for configuration 1-1-1, and in (b) for 1-1-2. The conduction losses for every IGBTs of cell 3 are represented by SW3 and the reverse recovery losses for every diodes of cell 3 are represented by D3. In the same way, SW2 and D2 for cell 2 and SW1 and D1 for cell 1. It can be observed that in both types the conduction losses of IGBTs decrease by increasing of the power factor angle, while the conduction losses of diode increase.

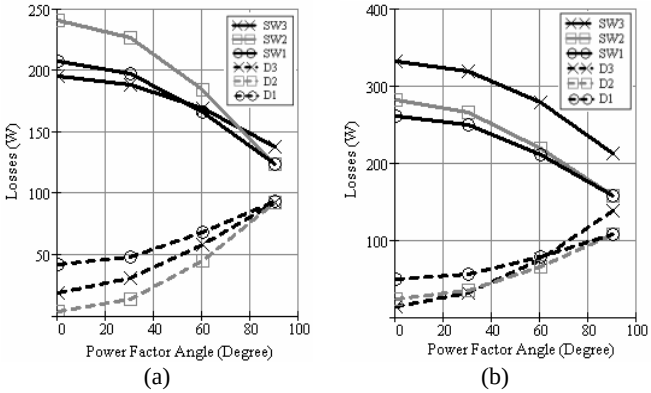

Fig. 5. Conduction Losses (a) Type 1-1-1 (b) Type 1-1-2

Fig. 6 (a) presents the switching losses for the cell 3, (b) for the cell 2 and in (c) for cell 1. These plots show that the switching losses in the cells 3 and 2 are very small in comparison with the cell 1. This fact is due to the effect of the hybrid modulation strategy, because the cell 3 is commutated at the fundamental frequency of output, the cell 2 also at low frequency and only cell 1 operates at high frequency. On the other hand, if a conventional PWM technique had been used for all cells, they would present similar switching losses to that illustrated in Fig. 6 (c) for cell 1.

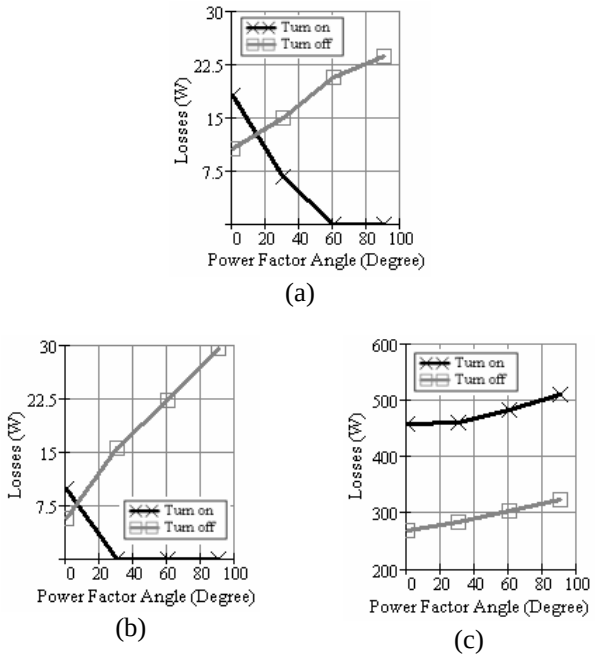

Fig. 6. Switching Losses 1-1-1 (a) cell 3 (b) cell 2 (c) cell 1

Fig. 7 presents the switching losses for configuration 1-1-2. It can be observed the turn-on, turn-off and reverse recovery for all cells, in (a) for cell 3, in (b) for cell 2 and in (c) for cell 1. The same considerations mentioned before in Fig. 6 also are valid for this case.

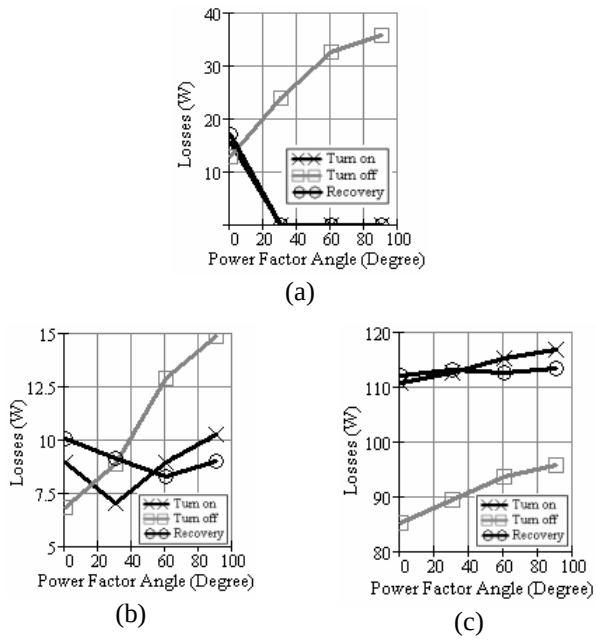

Fig. 7. Switching Losses 1-1-2 (a) cell 3 (b) cell 2 (c) cell 1

Fig. 8 shows the total conduction losses in (a), the total switching losses in (b) and the total losses in (c) for the configuration 1-1-1 per phase.

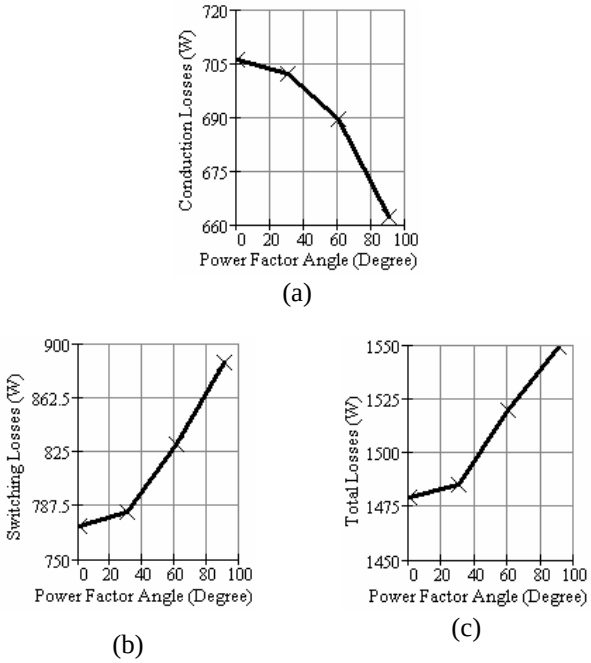

Fig. 8. Losses 1-1-1 (a) conduction (b) switching (c) final

Fig. 9 illustrates the total conduction losses in (a), the total switching losses in (b) and the total losses in (c) for the configuration 1-1-2 per phase.

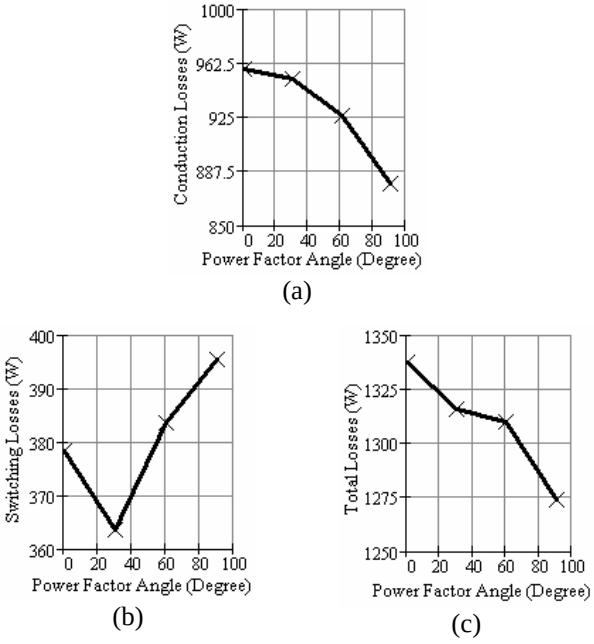

Fig. 9. Losses 1-1-2 (a) conduction (b) switching (c) total

The results of losses presented in Fig.8 and Fig. 9 represent the differences among the semiconductors devices used. In the topology 1-1-1 (Fig. 8) the most significant loss is the switching losses, while in the topology 1-1-2 the conduction losses are the most significant.

For the semiconductors chosen for this analysis of losses the recommended topology is the 1-1-2.

VIII. CONCLUSION

This paper applies a generalized design methodology to determine the DC voltage sources of a hybrid multilevel inverter. For three cells cascaded H-bridge multilevel inverter was possible to reduce the number of configurations for only two, 1-1-1 and 1-1-2. Both configurations will present uniform high-frequency modulated adjacent levels, the highest DC voltage cell does not process voltage higher than load and it is possible to utilize only uncontrolled rectifiers for all range operation.

The configuration 1-1-2 synthesizes nine levels, while the type 1-1-1 only seven levels on output phase voltage. This difference guarantees to configuration 1-1-2 the Total Harmonic Distortion and First Order Distortion Factor approximately 4.6% and 0.06% smaller than configuration 1-1-1, this will reduce the volume of the output filter, when it is necessary.

It was presented a methodology to calculate the conduction and switching losses when a hybrid modulation strategy is used. One example to determinate losses was shown, and in this analysis the configuration 1-1-2 obtained has presented smaller losses than 1-1-1.

Based on every restriction presented, on level numbers, Total Harmonic Distortion, First Order Distortion Factor and the converter power losses, for the semiconductors devices used, conclude that the configuration 1-1-2 is the recommended topology for drive one 500hp/4160V induction motor, among the topologies Three Cells Cascaded H-Bridge Hybrid Multilevel Inverter.

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