CONTROL CONSIDERATIONS ON SINGLE-PHASE BOOST POWER FACTOR CORRECTORS

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Abstract **- This paper presents a systematic review of PF control strategies used with unidirectional boost converter. It also analyses the control possibilities for bi-directional converters with emphasis in the half-bridge boost converter and full-bridge boost converter. In addition to these possibilities, a scheme with an interleaved two-cell boost converter with ac capacitors is also considered. Simulated and experimental results are reported.**

Keywords - **Boost converters; Power factor correction; Power electronics.**

I. INTRODUCTION

Reference [1] classifies the single-phase power factor correctors (PFC) as boost, buck, buck-boost and multilevel with unidirectional and bi-directional power flow in a topology-based classification. Three configurations of unidirectional boost converters, employ a *dc inductor* (that is, the *unidirectional boost converter*, the *interleaved two-cell boost converter*, and the *unidirectional boost converter with high frequency active EMI filter*); other employ an *ac inductor* (that is, the *symmetrical two-device boost converter* and the *asymmetrical two-device boost converter*).

Unidirectional single-phase power factor correction converters with dc inductor are reviewed in [2], which according to Garcia et al. [3] can be classified into two groups: *sinusoidal line current* and *non-sinusoidal line current*. On the other hand, bi-directional converters are classified as *half-bridge boost converter*, *VSI full-bridge boost converter*, *bridge boost converter with dc ripple compensation using ac capacitors and a third leg*, and *bridge boost converter with dc ripple compensation using an inductor and a third leg* [1].

This paper presents a systematic review of PF control strategies used with unidirectional boost converter mainly with sinusoidal line current. It also analyses control possibilities for bi-directional converters with emphasis in the half-bridge boost converter and VSI full-bridge boost converter. In addition to these possibilities, a scheme with an *interleaved two-cell boost converter with ac capacitors* (not considered in previous classifications) is also considered. Simulated and experimental results are reported.

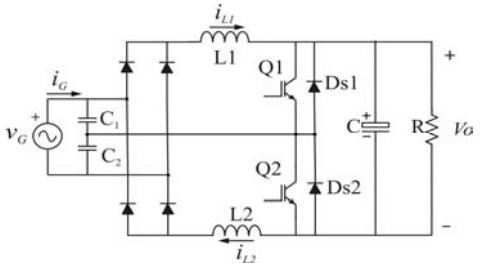
II. UNIDIRECTIONAL BOOST CONVERTERS WITH SINUSOIDAL LINE CURRENT

In this study, non-sinusoidal current, voltage follower, and current waveshaping approaches [4] are considered.

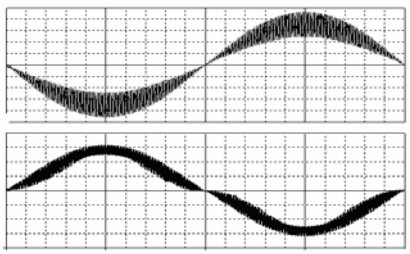
A. Voltage follower approach

In general, the boost converter can operate in continuous (CCM), discontinuous (DCM) or borderline (critical) current mode. The voltage follower approach utilizes DCM operation. It needs only the output voltage control to accomplish almost input unity power factor operation. Borderline control can also use such a scheme [2], this solution will not be considered in this paper.

When the output voltage control is not needed, the *interleaved two-cell boost converter with ac capacitors* can be used. It has been introduced by Nabae in [5] and for this reason it will referred in this paper as *Nabae's converter* (see Fig. 1). Even though the inductor currents are discontinuous, the input current is continuous and its ripple and the size of the inductor L are far decreased as compared to that of the discontinuous inductor current in conventional boost converters. Its control is very simple. The simulated results in Fig. 1(b) indicate its input capacitor voltage $v_{C1,2}$ and input current i_G. They were obtained for a relation between the output voltage and the input voltage $M = V_O/V_G = 1{,}1$ (140V/154V), a switching frequency f_S of 10kHz, and on an output power P_O of 80W. A THD of 12,7% was calculated for the input current.



(a) Converter.



(b) Simulated results: capacitor voltage, v_{C1} (top, 20V/div) and input current, i_G (bottom, 0,5A/div). Hor. 1ms/div.

Fig. 1. Interleaved two-cell boost converter with ac capacitors (Nabae´s converter).

B. Current waveshaping

There are three different possibilities of detecting the current in the various control strategies used with PFC based on boost topology, that is, detection of the: a) input current; b) switch current; c) output (diode) current. Also, switching can be considered as of constant frequency, constant on-time, constant off-time or variable time. Two options will be considered in this paper: control with the use of template and control without the use of template.

a) Control with template

A general scheme for this case is shown in Fig. 2, in which a diode rectifier, formed by diodes D_1 to D_4, is followed by a boost converter, composed by the inductor L, the switch Q, the diode D, and the output capacitor C. In order to control the power factor, the input current is synchronized with the mains voltage. In fig. 2 this synchronization is obtained inside of Block A by multiplying the rectifier input voltage $|v_G|$ by the output voltage error represented by voltage signal v_C.

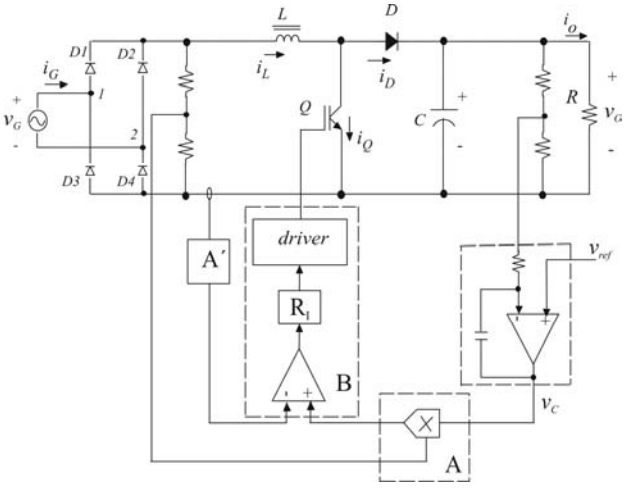


Fig. 2. General scheme for control with template.

The technique is applied to either continuous or borderline control and the constitution of blocks A' and B depends on which type of control is chosen. The techniques the most employed will be discussed next.

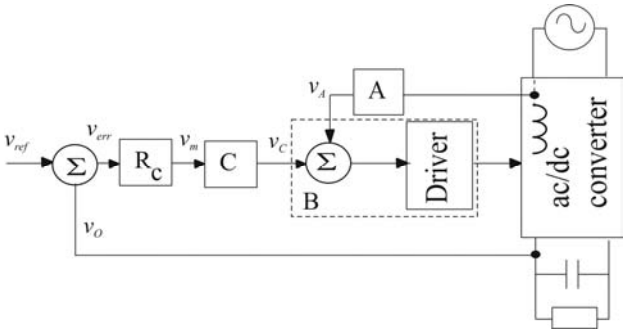
C*urrent peak control* usually limits the inductor or the switch current peak. Different approaches have been developed to reduce the existing line-current distortion under certain conditions. Distortion reduction are obtained by or (i) adding a variable dc offset to the sinusoidal reference, or (ii) pre-distorting the sinusoidal reference with a nonlinear circuit, or (iii) converting the peak-current-control scheme into a simplified average-current-control scheme [6].

Hysteresis control consists in using both an upper and a lower current reference. The solution introduced in [7] to solve the problem of a very high switching frequency associated with the variable hysteresis control was to introduce a certain delay at the start of the rectified cycle at the expenses of an increase in the harmonic distortion with the dead angle increase. The use of an imaginary hysteresis window [8] keeps the frequency constant but also may cause a band of discontinuous current mode of operation around each zero crossing of the line current. The use of a dc biased hysteresis allows for constant switching frequency operation and continuous operation [9]. In the critical mode or *borderline cont*rol, the switch on-time is kept constant during the line cycle and the switch is turned on the current reaches zero, so that the circuit operates at the boundary between CCM and DCM of inductor current. It can be considered as a special case of hysteresis in which the lower control is considered to be zero [10].

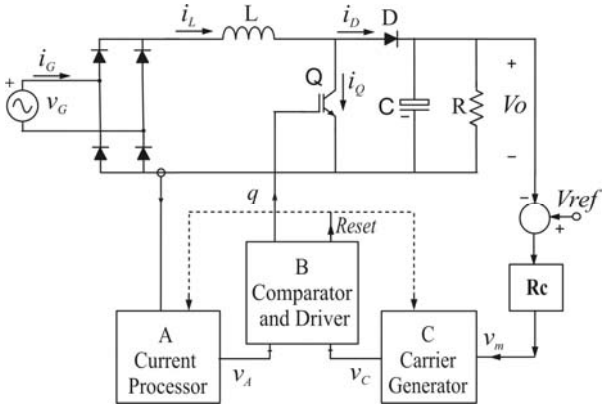
Average current control is a primary choice for many medium power applications. With this control the current is sensed and filtered by a current error amplifier which is used to drive the converter.

b) Control without template

In this approach the dc-link voltage is set up to the reference value by block R_c, which defines the reference current amplitude as shown in the block diagram of Fig. 3 (a). Block B depends on the type of control employed. The multiplier in the previous schemes is eliminated. Instead, synchronization is obtained via reset signal in the block B of Fig. 3(b), which indicates how to realize the technique [11]. However, other alternatives can be used for synchronization and although Fig. 3(b) only considers the detection of the inductance current, either the switch current or the diode current can be also detected, as it will be shown later.



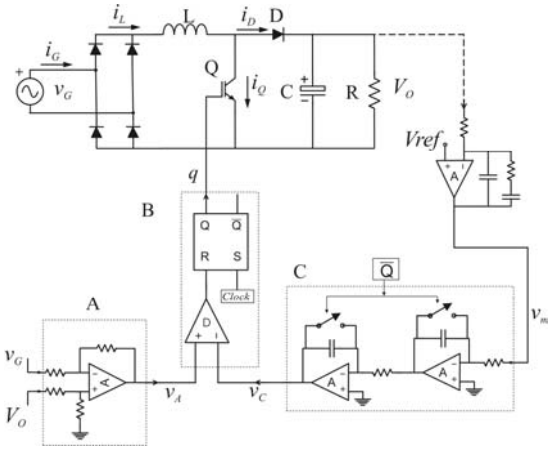
(a) Block diagram.



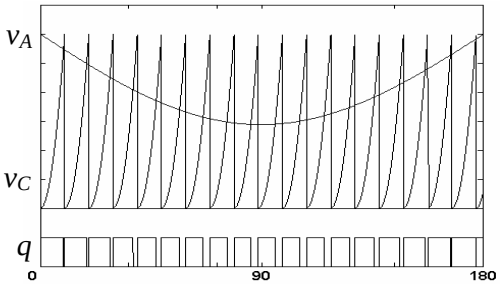
(b) General scheme.

Fig. 3. Control without template.

Different techniques have been introduced providing *average current control* without the multiplier. A well-known nonlinear control approach without any current-loop blocks is the *one-cycle-control* [12], shown in Fig. 4(a), which was conceived for constant frequency, constant *on*-time, constant *off*-time, and variable time switching converter.



(a) One-cycle control for DCM.



(b) One-cycle control principle.

Fig. 4. One-cycle control.

A PFC requires from the mains a current, i_G, that is proportional to the source voltage, v_G. It looks like the PFC emulating a resistance of value

$$R_e = \frac{v_G}{i_G} \tag{1}$$

Consider, now, the average current in the inductor L,

$$\bar{i}_L = \frac{1}{T_S}\int_0^{T_S} i_L(\tau)d\tau \tag{2}$$

It can be shown, for *boost* DCM operation, that

$$\bar{i}_L = \frac{T_S}{2L} v_G \frac{V_O}{(V_O - v_G)} d^2 \tag{3}$$

where V_O is the output average voltage, and $d = t_{ON}/T_S$ is the duty cycle, with t_{ON} being the on-time and T_S the switching interval.

It follows that, for the trailing-edge control and DCM operation, the voltage signal (proportional to the integral of the inductance current) can be achieved if t_{ON} is accomplished by

$$(V_{OS} - v_{GS}) = V_{OS}\frac{R_e}{2LT_S} t_{ON}^{\ 2} \tag{4}$$

where v_{GS} and V_{OS} are the sampled input and output voltage, respectively.

Expression (4) means that when the difference between output and input voltage $v_A = V_{OS} - v_{GS}$ equals the periodic carrier waveform $v_C = V_{OS}(R_e/2LT_S)t_{ON}^2$ the current integrator is reset and the switch turned off (see Fig. 4b) [13]. Simulated results for the input current show a THD of 0,64% for $V_O/V_G = 2.4$, where V_G is the peak value of the input voltage.

For CCM operation a current loop is used and block B depends on whether trailing-edge or leading-edge modulation is employed. Block A depends on which current is detected. Considering the equation for *boost* CCM operation

$$\frac{V_O}{v_G} = \frac{1}{(1-d)} \tag{5}$$

There are, then, three possibilities:

1) *Trailing-edge control of the average value of the input (inductance) current* [14][15] - the voltage signal is compared with the periodic carrier waveform $V_C(t)$, which is achieved in block F by

$$\bar{i}_L = \frac{V_O}{R_e}(1-d) \quad \text{with} \quad v_C(t) = \frac{V_O}{R_e}(1-\frac{t}{T_S}) \tag{6}$$

2) *Trailing-edge control of the average value of the diode current* [14] with

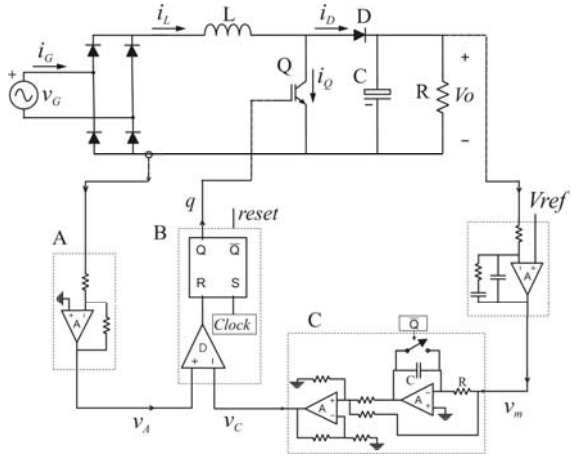
$$\bar{i}_D = \frac{V_O}{R_e}(1-d)^2 \quad \text{with} \quad v_C(t) = \frac{V_O}{R_e}(1-\frac{t}{T_S})^2 \tag{7}$$

3) *Trailing-edge control of the average value of the switch current* - this control corresponds to the nonlinear-carrier control introduced in [16] with

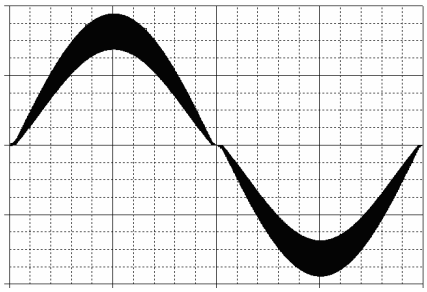
$$\bar{i}_Q = \frac{V_O}{R_e}(1-d)d \quad \text{with} \quad v_C(t) = \frac{V_O}{R_e}(1-\frac{t}{T_S})\frac{t}{T_S} \tag{8}$$

Therefore, the input current - or switch or diode current - is integrated and compared with a ramp that is the realization of $v_C(t)$ in (6) - or the realization of v_C in (7) or (8) - of which the amplitude is defined by the voltage v_m (modulator voltage). Detailed circuits are given in [14] and [15].

This technique without template can be also employed for *current peak control* [14]. It is illustrated in Fig. 5 and is named *input-current shaping technique*. In this case the instantaneous inductor current is detected and feeds block A, while synchronization is achieved in block B. The simulated result for the input current is presented in Fig. 5(b) which has a THD of 2.86% for $M = 2.5$. Note that there exist a distortion at the zero crossing.



(a) Scheme.



(b) Input current. Vert.: 0,5A/div; hor.: 1ms/div.

Fig. 5 . Input current shaping technique.

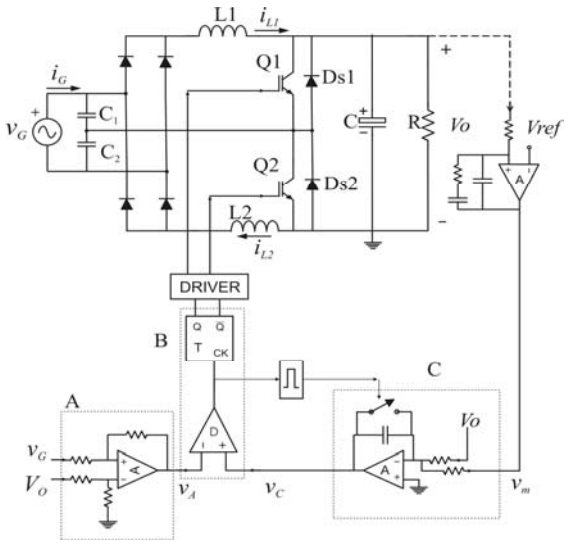
c) Application to Nabae's converter - As mentioned previously, Nabae's converter basic control scheme can only be used for fixed loads. However, the dc-link control, in the case of a variable load, can be obtained by using a modification of the one cycle control witch is based on realizing

$$V_{OS} - v_{GS}/2 = V_{OS}\frac{R_e}{16L}T_S \qquad (9)$$

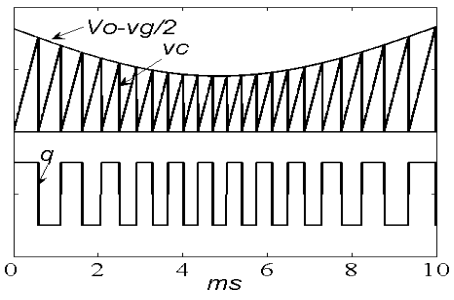
When $v_A = V_{OS} - v_{GS}/2$ equals $v_C = V_{OS}\,T_S R_e/16L$ block C is reset so that the operation is frequency modulated. The scheme in Fig. 6 is simpler than that in Fig. 4. The main controller waveforms are presented in Fig. 6(b). The regulation action while maintaining the power factor near unity was confirmed by simulated results not shown, for $M = V_O / V_G = 2$ (V_G=155 V), f_S = 10 kHz, and a variation of output power from P_{O1} = 60 W to P_{O1} = 120 W. A THD of 3,2%, was found, which is much smaller than that found with Nabae´s basic control mentioned in Section II. Experimental results for the capacitor voltage $v_{C1,2}$, and input current i_G are depicted in Fig. 7 for M = 1.1 (V_G = 155V), switching frequency range from 7.7 kHz to 11.1 kHz, and output power, P_O, of 76 W.

III. UNIDIRECTIONAL BOOST CONVERTER WITH NON-SINUSOIDAL LINE CURRENT

An example of such technique is the *clamped current control*, without reset signal and with C = 1 as shown in Fig. 8 [17]. In this case, the peak current in the switch or in the inductor is clamped at a constant value during the input voltage line cycle. The circuit operates in three different modes of operation, two of which DCM and the other in CCM. It is a simple scheme and with relatively low component stresses but operates at the expenses of a somewhat higher THD. Compensation of harmonics can be achieved with the

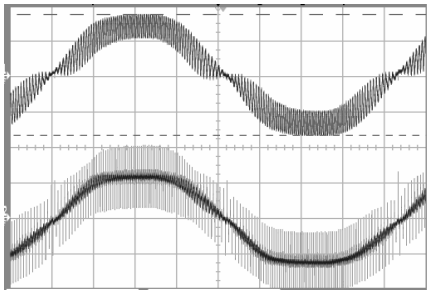


(a) Scheme for modified one-cycle control.

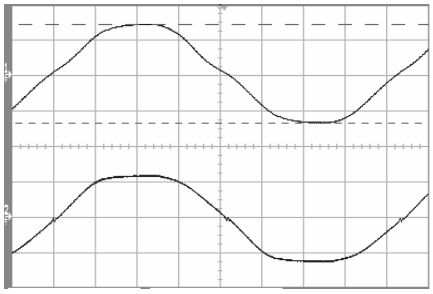


(b) Waveform for Block A and drivers output.

Fig. 6. Nabae´s converter with modified one-cycle control.



(a) Voltage over capacitor C_1 (top, 50V/div) and input current i_G (bottom, 1A/div). f_S: from 7.7 to 11.1kHz.



(b) Filtered waveforms.

Fig. 7 . Experimental results for Nabae´s converter with modified one-cycle control.

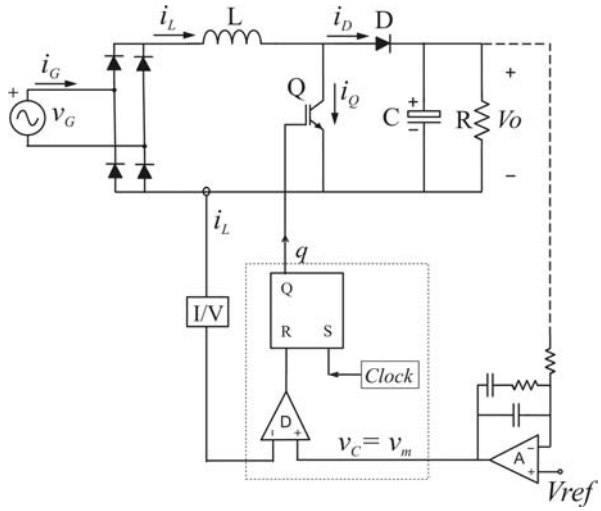


Fig. 8. Clamped current control.

introduction of a slope compensation as in [18], which claims to obtain better results when compared to a conventional average current control.

IV. BI-DIRECTIONAL AC INDUCTOR BOOST CONVERTER

The *half-bridge boost converter* is shown in Fig. 9 and the *VSI full-bridge boost converter* is shown in Fig. 10 [1]. It can be shown that in implementation of these circuits the parasitic resistances must be minimized to favor a power factor control near unity.

A. Control with template

Consider that in Fig. 9 and Fig. 10 the current in inductor L and its power factor angle is determined by the difference between the source voltage v_G and the rectifier input voltage v_r, as indicated in the figures.

For any of those converters, the power factor can be expressed by

$$PF = \cos\phi = \frac{V_r sen\theta}{\sqrt{V_r^2 + V_G^2 - 2V_r V_G \cos\theta}} \qquad (10)$$

where v_r is defined in those figures for each one of the converters. This leads to a first possibility of dc-link and power factor control for both half-bridge boost and the full-bridge boost converters, including current control, indicated by the block diagram in Fig. 11. The dc-link voltage is set up to the reference value by block R_C, which defines the reference current amplitude. In order to control the power factor, the reference current i_{Gref} is synchronized to the source voltage, v_G, by template.

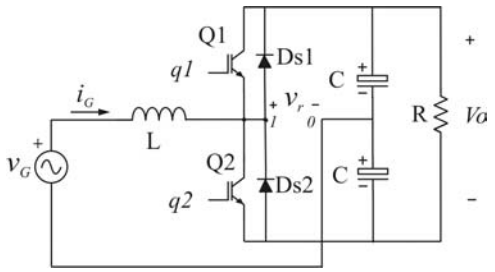


Fig. 9. Bi-directional half-bridge boost converter.

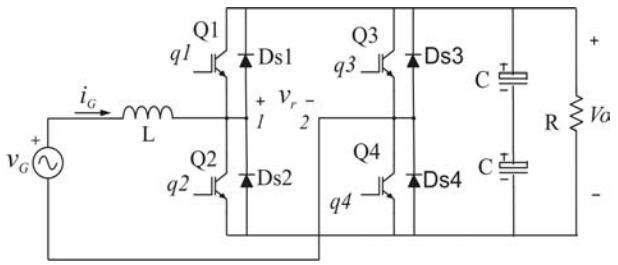


Fig. 10. Bi-directional full-bridge boost converter.

The capacitor voltage controller is of type PI and the current controller can be either a stationary PI (open loop gain equal to infinite at zero frequency, here named *Controller I*) or a controller of positive and negative sequences. This last controller can either exactly cancel of the system pole (*Controller II*) or realize the additional low frequency harmonics compensation (*Controller III*). simulated results indicated a THD of 7.76% for a half-bridge

and a THD of 4.33% for a full bridge when Controller I was employed.

In the case of the VSI full-bridge boost converter, the voltage reference is given by $v_{rref} = v_{1ref} - v_{2ref}$. Therefore, different combinations of v_{1ref} and v_{2ref} generate v_{rref}.

Experimental results for both the bi-directional half-bridge boost converter and the bi-directional full-bridge boost converter operating with the current Controller I are presented in Fig. 12 and Fig. 13, respectively. In the half-bridge converter, Controller I eliminates the half-bridge capacitors unbalance. These are results for an output frequency of 60 Hz. Results not shown indicate that Controller III gives better results than Controller I but leads to tuning problems.

B. Control without template

The multiplier in the previous possibilities can be eliminated by the voltage angle control without current control or by the one-cycle control.

a) Voltage angle control - The principle of this control is represented by the bock diagram in Fig. 14. A PI controller (block R_C) is used to set the angle δ_{ref} to the reference voltage. The phase angle at the rectifier terminals, θ, is then $\theta = \angle v_G - \delta_{ref}$, $\angle v_G$ being the source voltage phase angle. This control is simpler than that in Fig. 11 but its action is sensitive to variations in the system parameters. A THD of 7.89% was found for a half-bridge.

b) One-cycle control - Its block diagram used with the bi-directional half-bridge boost converter and the bi-directional full-bridge boost converter is shown in Fig. 15.

The average current control law

$$\bar{i}_L = \frac{V_O}{2R_e}(1-2d) \qquad (11)$$

for the half-bridge boost converter can be realized as indicated in Fig. 16.

The simulated results presented in Fig. 16 for voltage and input current were obtained for the half-bridge boost with parameters $M = V_O/V_G = 2.6$ (155V / 400V), f_S = 10 kHz, L=4 mH, P_O =567 W. It was found a THD of 2.35%.

In the case of the full-bridge, for $M = V_O/V_G = 2.6$ (155V/400V), f_S = 10kHz, L = 4mH, P_O = 580 W, it was found a THD of 2.57% (Fig. 17).

The difference between these two THD can be explained by the fact that a higher voltage is applied to the inductor, in the case of the full-bridge. However, they are smaller than the two last previous cases.

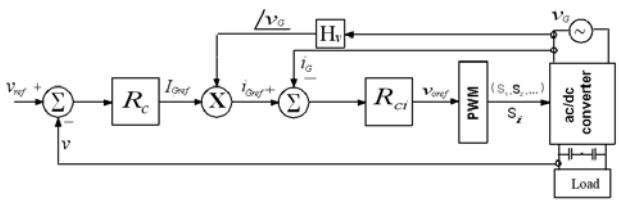


Fig. 11. Block diagram for the current control.

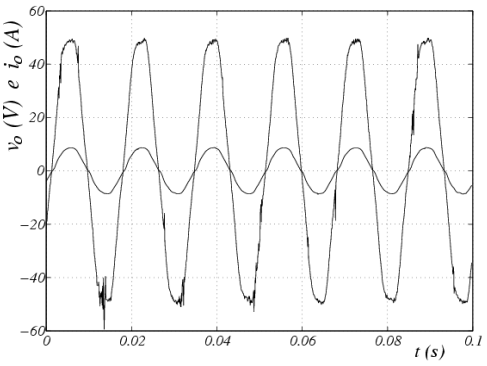


Fig. 12. Experimental results for controller I (half-bridge).

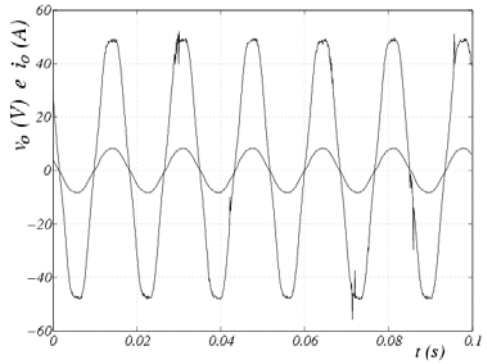


Fig. 13. Experimental results for controller I (full-bridge).

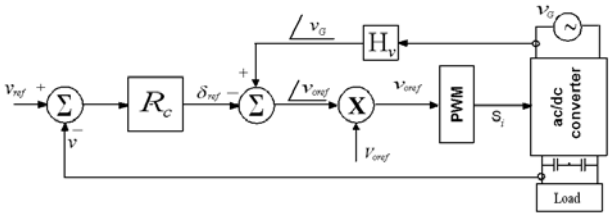


Fig. 14. Block diagram for voltage angle control.

IV. CONCLUSION

This paper presented a systematic review of a systematic review of PF control strategies used for unidirectional boost converter with sinusoidal line current. Emphasis was given to recent possibilities of control techniques without current template. It has been shown that the use of the one-cycle control improves the input current DHT. The implementation of such technique for bi-directional is very simple when compared to more traditional techniques, which also presented higher THD.

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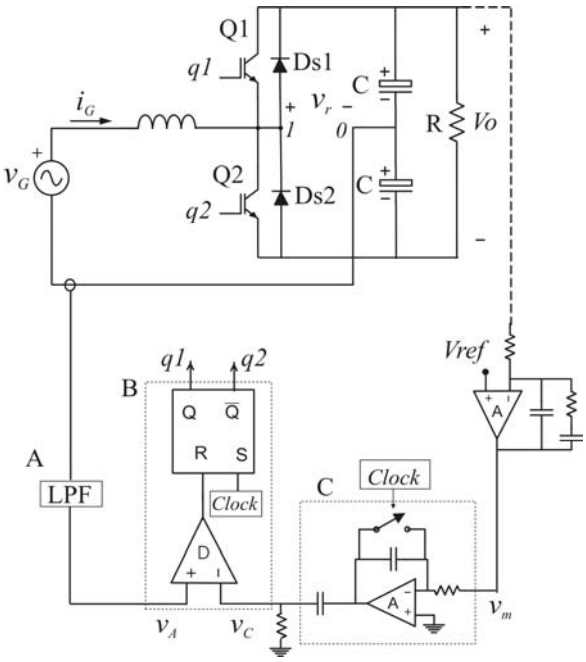

Fig. 15. Implementation of equation (11).

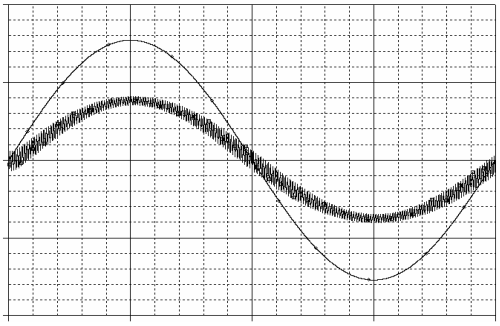

Fig. 16. Simulated results: comparison of input voltage v_G (top, 20V/div) and input current , i_G (bottom, 2A/div) for half-bridge converter (M=2.5, f_S=10 kHz, source freq. = 50Hz). Hor. 1ms/div.

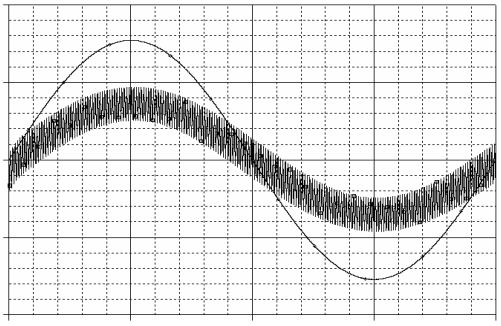

Fig. 17. Simulated results: comparison of input voltage v_G (top, 20V/div) and input current , i_G (bottom, 2A/div) for full-bridge converter (M=2.5, f_S=10 kHz, source freq. = 50Hz). Hor. 1ms/div.

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