QUALITATIVE ANALYSIS OF HYBRID MULTILEVEL INVERTERS IN CLOSED-LOOP SYSTEMS

Cassiano Rech
Universidade Regional do Noroeste do
Estado do Rio Grande do Sul – UNIJUI
Ijuí, RS, Brazil
cassiano@ieee.org

José Renes Pinheiro
Power Electronics and Control Research Group – GEPOC
Federal University of Santa Maria – UFSM
Santa Maria, RS, Brazil
renes@ctlab.ufsm.br

***Abstract* – Hybrid multilevel inverters can adequately use distinct semiconductor technologies, because series-connected cells have different power, voltage and frequency ratings. Nevertheless, in closed-loop systems, the control action that should be synthesized by the hybrid multilevel inverter can present high-frequency components to compensate disturbances with fast transient response. In these cases, it can be necessary to limit the switching frequency of the slow high-voltage switching devices used in the higher power cells, which can deteriorate the dynamic performance of the system. Therefore, the main objectives of this paper is to clearly illustrate the limitations of hybrid multilevel inverters operating as actuators in closed-loop systems, to propose alternatives to overcome them and to investigate the impact of these alternatives on the synthesis of the desired control signal.**

***Keywords* – Actuators, high-power applications, hybrid multilevel inverters**

I. INTRODUCTION

More restrictive specifications have been leading to the development of high-performance closed-loop systems. In these systems, the states and output variables are estimated and/or measured through sensors, and processed by a compensator, which generates a control signal that should be synthesized by an actuator, as depicted in Fig. 1. Several compensator types have been investigated for a large number of applications to meet the specifications imposed to the system, such as: zero steady-state error, insensitive to parametric variations, high disturbance rejection and fast transient response.

These compensators are usually designed from linear plant models using some linear control technique. However, a real actuator presents physical limitations that can introduce nonlinearities to the feedback control system. For instance, in power electronics systems, the actuator can be a static power converter, which has voltage, power and/or frequency limitations. These limitations difficult the control system operation, mainly during startup, shutdown and large disturbances, when these nonlinearities are not included in the analysis [1]. Due to this fact, some alternatives have been developed for distinct power electronics applications to reduce the impact of these limitations [2], [3].

Moreover, many applications use multiple converters/ subsystems, instead of a single converter, to increase the reliability or the voltage/power capability of the entire system. These converters also present voltage, power and/or frequency limitations, but the restrictions of one converter can be different from another, as occurs with asymmetrical and hybrid multilevel inverters [4]–[12].

From the load point of view, asymmetrical multilevel inverters are particularly interesting for high-power applications, because they synthesize voltage waveforms with a higher number of levels, using the same number of switching devices of a conventional multilevel inverter. This advantage is achieved by using distinct voltage levels in the different cells, being able to create more levels in the output voltage and minimizing the output voltage THD (Total Harmonic Distortion) [4]–[8]. Low-frequency modulation strategies can be applied to asymmetrical multilevel inverters, but the output voltages will present low-order harmonics. On the other hand, conventional pulse width modulation (PWM) techniques can be used to move the harmonics to higher frequencies. However, conventional PWM strategies typically are not suitable for asymmetrical multilevel inverters, because the switching devices of the higher voltage cells would have to operate at high frequency during some time intervals [9], [10]. Then, a hybrid modulation strategy has been proposed in [4], [5], using stepped waveform synthesis in the higher voltage cells in conjunction with high-frequency PWM in the lowest voltage cell. With this hybrid strategy, it is possible to use slow semiconductor devices in the higher voltage cells, and also to employ fast semiconductor devices in the cells that operate with reduced voltage levels, taking advantage of the different semiconductors technologies. Then, hybrid multilevel inverters can be defined as those systems composed of several series-connected cells, which present distinct voltage levels, modulation strategies, topologies and/or semiconductor technologies operating in synergism. Consequently, each cell could present different voltage, power and frequency limitations that must be respected in any operating point.

Several papers have been published in recent years to analyze the operating principles of hybrid multilevel inverters, but mainly with sinusoidal command signals. However, a detailed analysis about the performance and the limitations of hybrid multilevel inverters operating as actuators in closed-loop systems, where the command signals are typically nonsinusoidal, was not still presented.

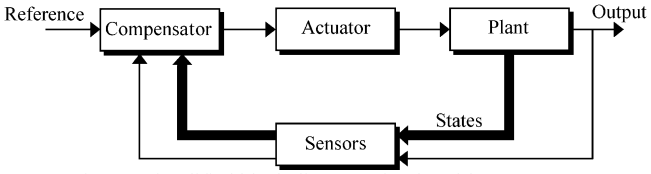

Fig. 1 – Simplified block diagram of a closed-loop system.

Aiming to fill this gap, this paper presents a qualitative analysis of hybrid multilevel inverters operating as actuators in closed-loop systems. This investigation will show that the frequency limitations of some cells, caused by the use of high-voltage and slow semiconductor switching devices, are not respected under certain disturbances. Therefore, this paper proposes an alternative to overcome this actuator limitation and investigates the effects of this alternative on the synthesis of the desired control signal.

This paper is organized as follows: Section II includes a basic description of hybrid multilevel inverters and Section III illustrates their physical limitations under nonsinusoidal command signals. Section IV proposes an alternative to overcome frequency limitations of higher power cells and Section V shows some experimental results to demonstrate the practical viability of the proposed approach.

II. BASIC DESCRIPTION OF HYBRID MULTILEVEL INVERTERS

Fig. 2 presents the generalized structure of one phase of a voltage-source multilevel inverter with n series-connected DC-AC cells. Several topologies of single-phase DC-AC cells can be connected in series to synthesize multilevel voltage waveforms [7]. However, this paper considers only multilevel inverters with H-bridge cells, as shown in Fig. 3.

As mentioned before, if at least one of the DC voltage sources differs from the others, the multilevel inverter shown in Fig. 3 can be called asymmetrical multilevel inverter. Considering that the lowest DC voltage source ($V_{dc,1}$) is chosen as base value for the p.u. notation, the normalized values of all DC sources (V_j) must be natural numbers and respect the following relation to obtain uniform step multilevel waveforms [6]:

$$V_{j-1} \le V_j \le 1+2\sigma_{n-1}, \quad j = 2, 3, ..., n. \tag{1}$$

where:

$$\sigma_{n-1} = \sum_{j=1}^{n-1} V_j \,. \tag{2}$$

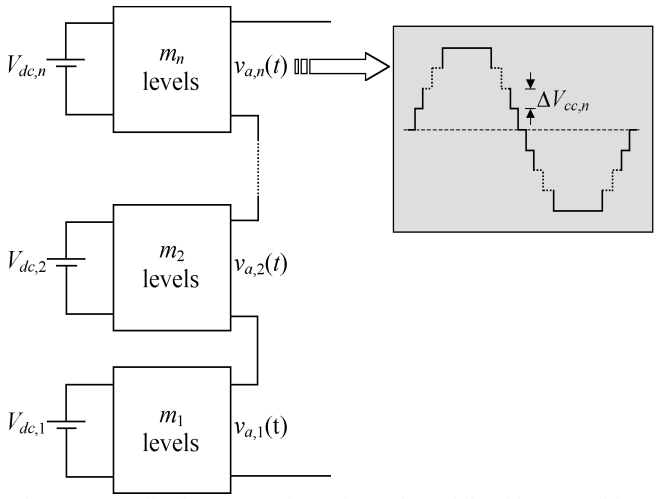

Fig. 2 – Generalized structure of one phase of a multilevel inverter with n series-connected cells.

With this, the maximum number of levels of an output phase-to-neutral voltage waveform can be given as:

$$m = 1+2\sigma_n \,. \tag{3}$$

It can be seen that, for the same number of cells, asymmetrical inverters can generate a larger number of levels than those obtained by using equal DC voltage sources. However, the power devices of different cells are subjected to distinct voltage levels, so that the high-voltage switching devices cannot operate at high frequency.

To overcome this problem without affecting the output harmonic performance, a hybrid modulation strategy was proposed in [5] for H-bridge series-connected cells, using low frequency modulation strategies in higher voltage cells in conjunction with high-frequency PWM in the lowest voltage cell. Consequently, these hybrid multilevel inverters can use different semiconductor technologies in synergism, under distinct voltage and frequency ratings.

With this hybrid modulation strategy, the output voltage harmonics are clustered around multiples of the switching frequency of the lowest power cell when the normalized value of the j^{th} DC voltage source satisfies this restriction:

$$V_j \le 2\sigma_{j-1} \,. \tag{4}$$

Fig. 4 presents a block diagram representing this hybrid multilevel modulation strategy. This figure shows that the command signal of the hybrid inverter is the reference of the H-bridge cell with the highest DC source (V_n). This signal is compared with constant levels Ψ_n and $-\Psi_n$ to generate a three-level waveform. The command signal of the j^{th} cell is the difference between the reference and the output voltage of the cell j+1. Therefore, this command signal, which is compared with Ψ_j and $-\Psi_j$, contains information about the harmonic content of the output voltages synthesized by higher power cells. Finally, the command signal of the lowest power cell is compared with high frequency triangle carrier signals, resulting in a high frequency output voltage.

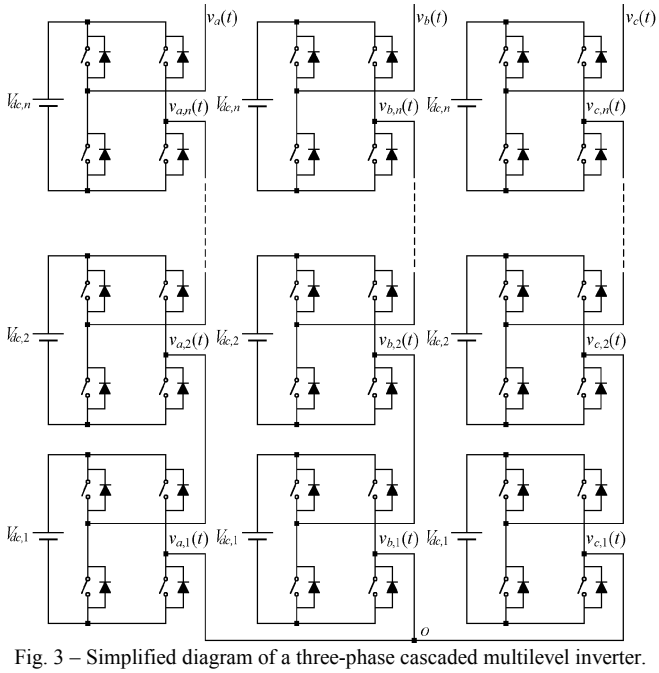

Fig. 3 – Simplified diagram of a three-phase cascaded multilevel inverter.

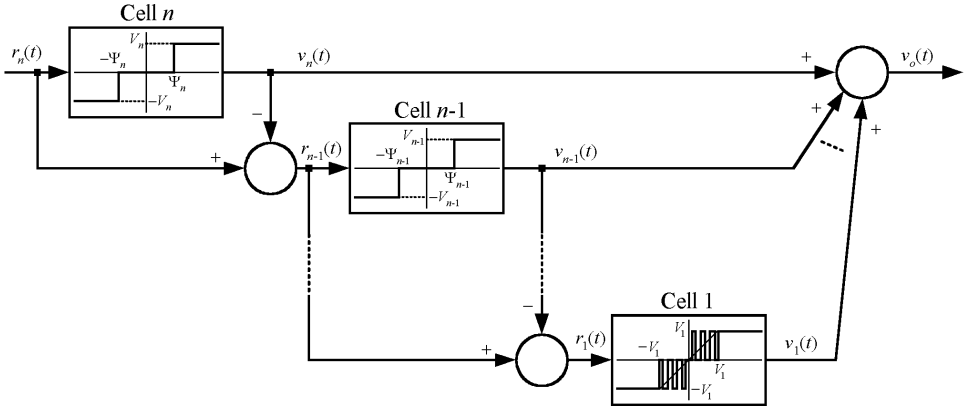

Fig. 4 – Hybrid multilevel modulation strategy.

The output voltage of the j^{th} cell should be equal to V_j when the command signal of this cell is greater than the sum of the DC voltage sources of the first j–1 cells. Then, it is possible to obtain the following restriction:

$$\Psi_j \leq \sigma_{j-1}. \tag{5}$$

The first j–1 cells are also not able to synthesize an instantaneous voltage less than $-\sigma_{j-1}$. It is also possible to demonstrate that the command signal of the cell j–1 will not be smaller than $-\sigma_{j-1}$ when:

$$\Psi_j \geq V_j - \sigma_{j-1}. \tag{6}$$

Therefore, any comparison level Ψ_j that satisfies the following restriction will result in identical output voltages [8]:

$$V_j - \sigma_{j-1} \leq \Psi_j \leq \sigma_{j-1}. \tag{7}$$

As an example, Fig. 5 shows a phase-to-neutral voltage waveform synthesized by a 9-level hybrid inverter with three H-bridge cells in series (V_1 = V_2 = 1 p.u. and V_3 = 2 p.u.), using the maximum comparison levels that satisfy (7) (Ψ_2 = 1 p.u. and Ψ_3 = 2 p.u.). This figure illustrates that the command signal is adequately synthesized among all adjacent levels.

III. PHYSICAL LIMITATIONS OF THE HYBRID ACTUATOR

Disturbance rejection with fast transient response is closely related to the bandwidth of the closed-loop system. The feedback system is able to synthesize higher frequency harmonic components and, consequently, to quickly reject disturbances, for large bandwidth values. On the other hand, the closed-loop system cannot synthesize high-frequency signals when it has a small bandwidth, resulting in slow transient responses. Therefore, the output signal of the compensator, which should be synthesized by the actuator, can be a nonsinusoidal waveform, whose harmonic spectrum depends on the measured signals, the structure of the controller and the bandwidth of the closed-loop system.

Nevertheless, until now, previous analyses were conducted under the assumption that a sinusoidal signal is used to control the hybrid multilevel inverter. Fig. 6 presents the voltage waveforms of the same 9-level hybrid

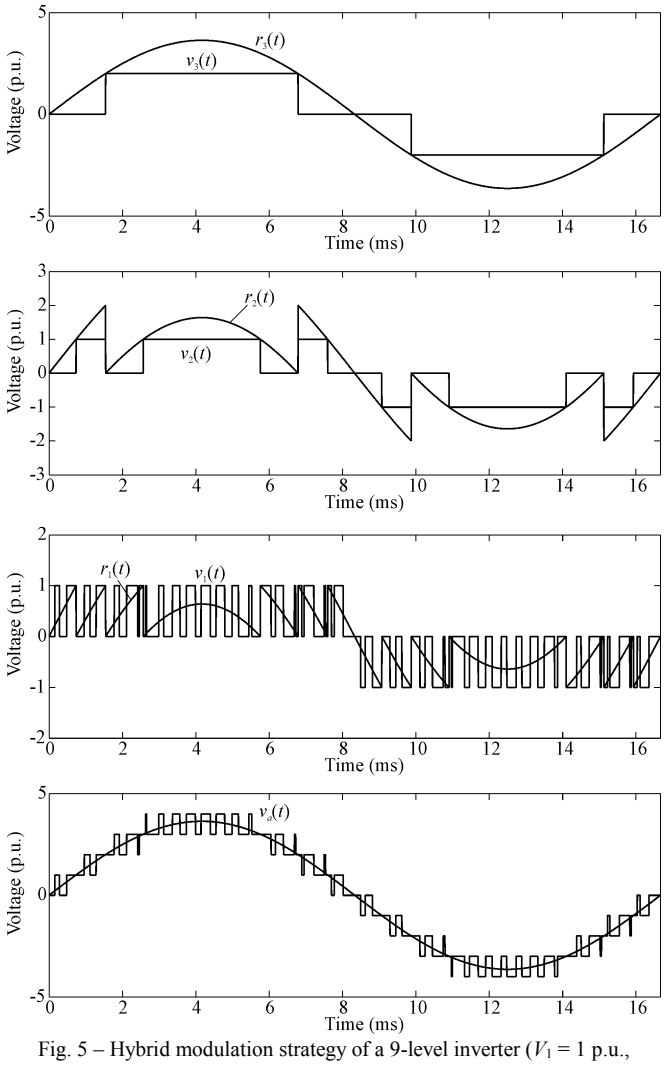

Fig. 5 – Hybrid modulation strategy of a 9-level inverter (V_1 = 1 p.u., V_2 = 1 p.u., V_3 = 2 p.u., f_s = 2460 Hz, Ψ_2 = 1 p.u. and Ψ_3 = 2 p.u.).

inverter, with V_1 = V_2 = 1 p.u. and V_3 = 2 p.u., by employing a nonsinusoidal command signal. This signal corresponds, for instance, to the control action produced by a closed-loop control system to minimize the voltage drop caused by a sudden increasing load change. Fig. 6(a) illustrates that, depending on the amplitude of a disturbance and the position that it occurred, the highest power cell have to operate at a higher frequency to synthesize the desired control signal. When the control action exceeds the

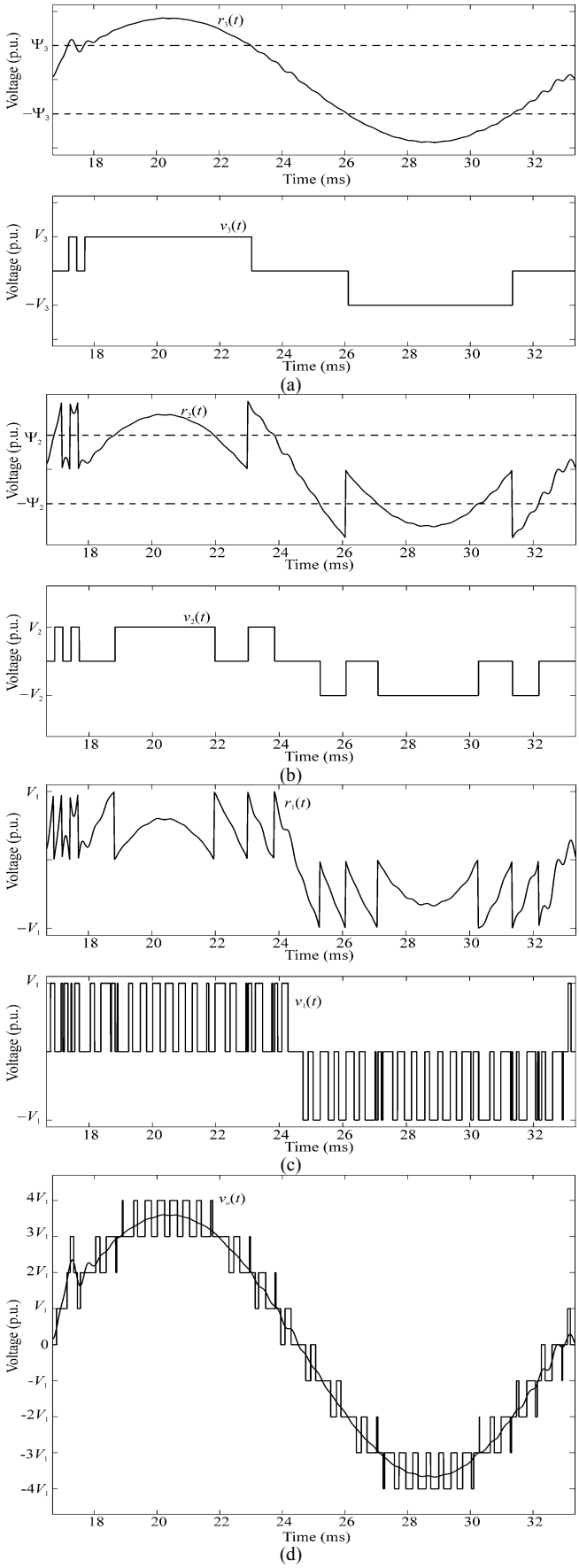

Fig. 6 – Command signals (top) and output voltages (bottom) with a nonsinusoidal reference. (a) Cell 3. (b) Cell 2. (c) Cell 1. (d) Phase voltage.

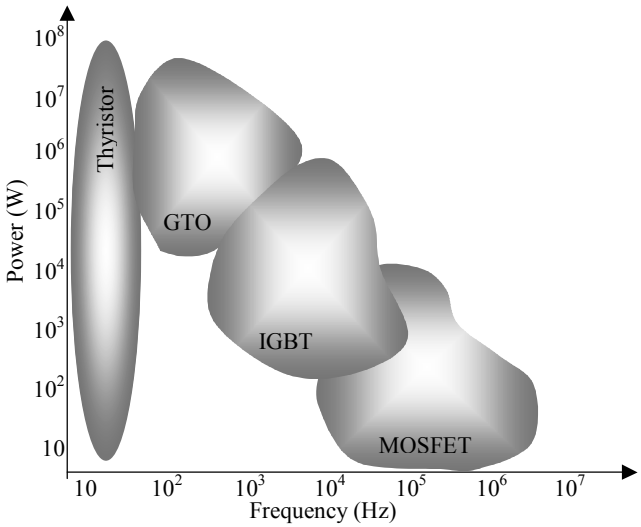

Fig. 7 – Semiconductor switching devices: Power *versus* frequency.

the comparison level Ψ_3, the output voltage of the highest power cell changes from zero to V_3. However, after the occurrence of this disturbance, the control action becomes smaller than this comparison level, and the output voltage level changes from V_3 to zero. Soon after, the control action becomes greater than Ψ_3 again, causing the third commutation in a small time interval. Fig. 6(d) shows the output phase-to-neutral voltage waveform, which synthesizes the desired control action to reduce the effects of this disturbance.

Although the switching devices of the highest power cell commutate only two more times in this situation, this switching period can be too small. Depending on the application, the voltage and power levels processed by each cell require the utilization of high-voltage and slow semiconductor devices. It is well known that the maximum switching frequency of a semiconductor switching device decreases as higher is its power processing capability [13]. The relationship between the power level processed by a switching device and its switching frequency can be approximated by an inversely proportional law, as shown in Fig. 7. Therefore, this high-frequency operation can damage slow semiconductor switching devices used in the highest power cell.

IV. PROPOSED ALTERNATIVES TO OVERCOME THE LIMITATIONS OF THE HYBRID ACTUATOR

A simple alternative to overcome power and frequency limitations of the actuator is to design compensators that result in closed-loop systems with a bandwidth smaller than the frequency limitations of the slowest semiconductor used in the hybrid multilevel inverter. However, this alternative can lead to a very slow dynamic performance for some applications.

Another alternative proposed in this paper to avoid undesired commutations is to include an algorithm in the modulation strategy to lock additional commutations, resulting from a nonsinusoidal control action. Nevertheless, depending on the hybrid multilevel configuration, this

method can affect the synthesis of the desired command signal. Then, it should be verified in which cases it is necessary to include this locking algorithm. Initially, the bandwidth of the closed-loop system must be determined. This bandwidth should be computed from the dynamic performance specifications for a given application. Once defined the bandwidth, it must be necessary to analyze which switching devices are used in each series-connected cell. By considering that there are high-voltage cells using slow semiconductors, which are not able to operate at a switching frequency around the bandwidth, these cells should be subjected to the locking algorithm. This locking algorithm can be applied to the higher voltage cells to avoid extra-commutations during a given period time, which depends on the semiconductor devices, even when the command signal crosses with the comparison levels.

Fig. 8 presents the voltage waveforms of the same 9-level hybrid inverter and using the same nonsinusoidal command signal used in the previous section. Nevertheless, in this case, a locking algorithm is included to the hybrid modulation strategy, which verifies when the control action exceeds the comparison level Ψ_3 and locks any commutation of the switching devices of the highest power cell during a time period that depends on the semiconductor technology.

The shadowed area illustrated in Fig. 8(a) represents the permissible range that Ψ_3 can vary (7) to correctly synthesize the command signal. Thus, when the control action is inside of this area, the output voltage level of the highest power cell can be zero or V_3 (2 p.u.), because the other two lower power cells are able to synthesize this control action. Due to this fact, the hybrid multilevel inverter synthesizes the desired control action to reject this disturbance, even with the locking algorithm, as shown in Fig. 8(d), whose output voltage waveform is identical to that presented in Fig. 6(d) (without the locking algorithm).

On the other hand, the flexibility to vary the comparison levels Ψ_j without affecting the synthesis of the command signal decreases as the asymmetry among the DC voltage sources increases. For instance, when the DC voltage sources present the maximum asymmetry (V_1 = 1 p.u., V_2 = 2 p.u., V_3 = 6 p.u., ..., $V_n = 2\sigma_{j-1}$) to synthesize the maximum number of levels [5], there is not flexibility to choose the comparison levels, that is, $\Psi_j = \sigma_{j-1}$ [8]. To illustrate this fact, Fig. 9 shows the voltage waveforms of a 7-level hybrid inverter, with V_1 = 1 p.u. and V_2 = 2 p.u. [4], under a nonsinusoidal command signal (which corresponds, for instance, to the control action produced by a closed-loop control system to minimize the overvoltage caused by a sudden decreasing load change). Therefore, with this configuration of DC voltage sources, the comparison level Ψ_2 must be equal to 1 p.u. It can be seen from Fig. 9(c) that the desired control action could not be correctly synthesized by the hybrid multilevel inverter by including the proposed locking algorithm, because the lowest voltage cell cannot synthesize its reference signal during the external disturbance, as illustrated in Fig. 9(b). This problem occurs because the command signal of the highest voltage cell becomes smaller than the comparison level, but the locking algorithm did not allow the change of the output voltage from V_2 to zero.

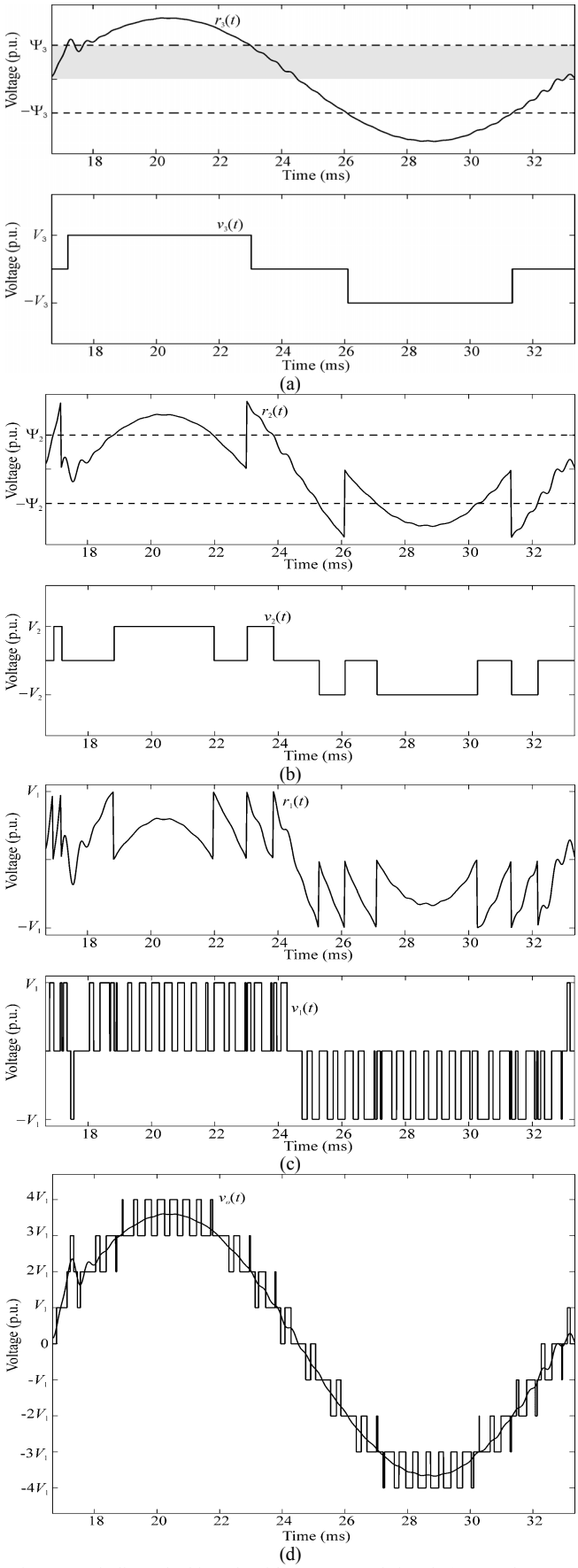

Fig. 8 – Including a locking algorithm: command signals (top) and output voltages (bottom) with a nonsinusoidal reference. (a) Cell 3. (b) Cell 2. (c) Cell 1. (d) Phase voltage.

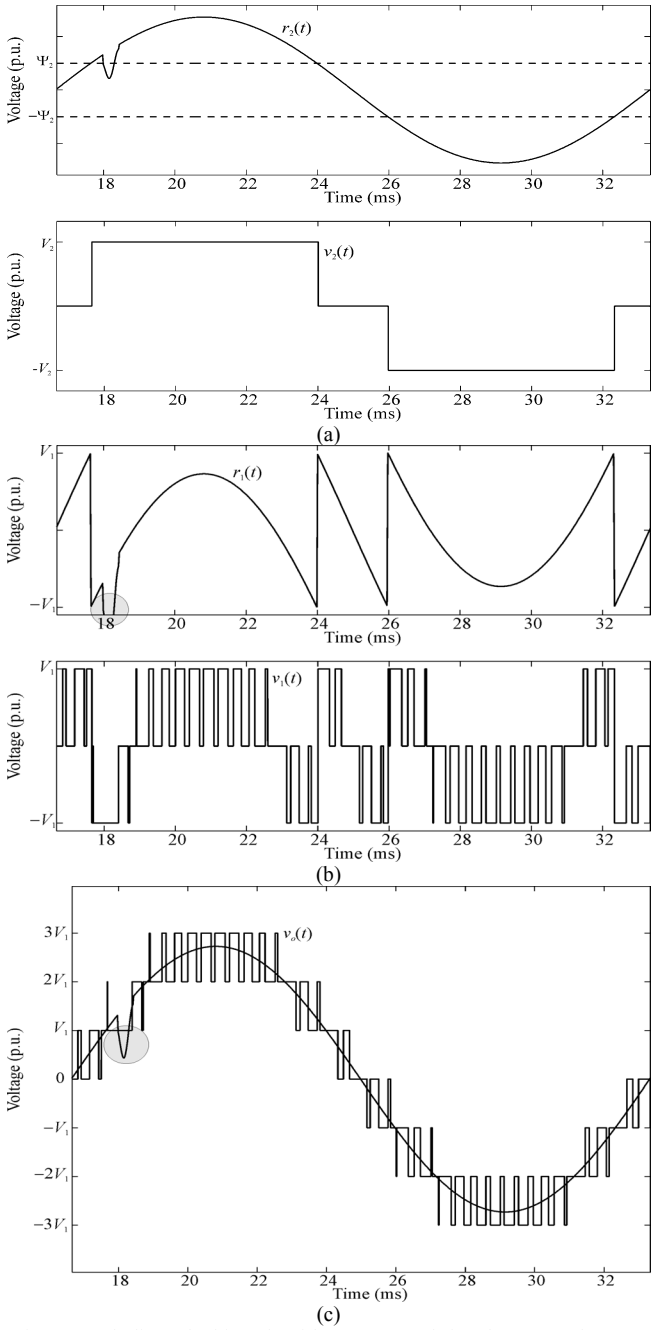

Fig. 9 – Including a locking algorithm: command signals (top) and output voltages (bottom) with a nonsinusoidal reference. (a) Cell 2. (b) Cell 1. (c) Phase voltage.

V. EXPERIMENTAL RESULTS

A low-power prototype of one phase of a 9-level hybrid inverter has been built in laboratory, using three H-bridge cells in series with the following DC voltage levels: $V_{dc,1}$ = 85 V, $V_{dc,2}$ = 85 V, $V_{dc,3}$ = 170 V (V_1 = V_2 = 1 p.u., V_3 = 2 p.u.). Initially, Fig. 10(a) presents the output voltages synthesized by the H-bridge cells and Fig. 10(b) shows the output phase voltage waveform with a sinusoidal command signal.

Fig. 11 illustrates the voltage waveforms with the same nonsinusoidal command signal used in simulation results. It can be verified that third and second cells operate at a higher frequency to obtain the desired command signal. Due to this

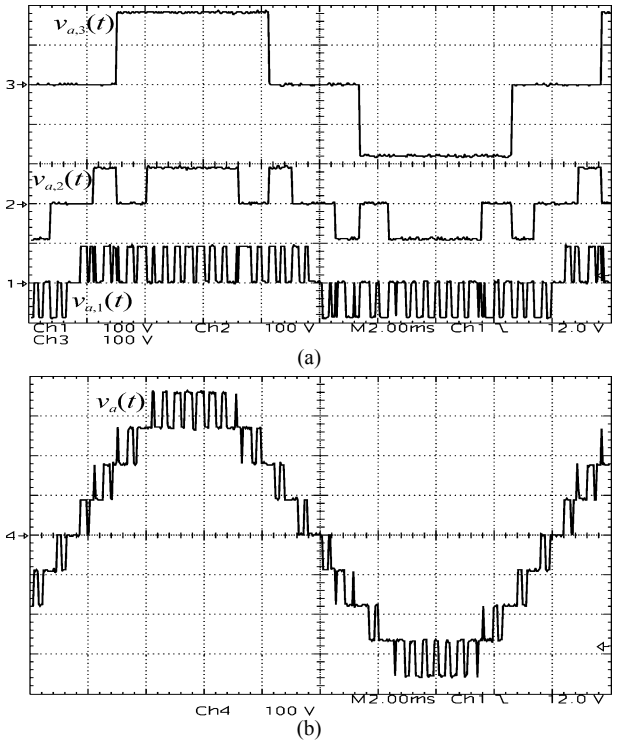

Fig. 10 – Experimental results of 9-level hybrid inverter with a sinusoidal command signal ($V_{dc,1}$ = $V_{dc,2}$ = 85V and $V_{dc,3}$ = 170, f_s = 2460 Hz, m_a = 0.9): (a) Output voltages of H-bridge cells. (b) Phase-to-neutral voltage.

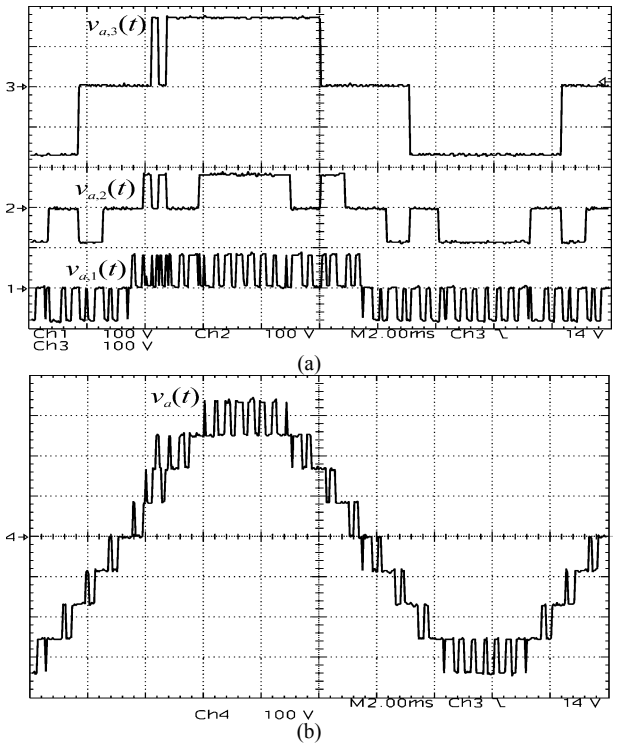

Fig. 11 – Experimental results of 9-level hybrid inverter with a nonsinusoidal command signal ($V_{dc,1}$ = $V_{dc,2}$ = 85 V, $V_{dc,3}$ = 170 V and f_s = 2460 Hz): (a) Output voltages of H-bridge cells. (b) Phase-to-neutral voltage.

fact, a locking algorithm was included to the modulation strategy to maintain the same number of commutations obtained with a sinusoidal signal, as presented in Fig. 12(a). Fig. 12(b) illustrates that the same command signal can be synthesized, even with the inclusion of the locking algorithm.

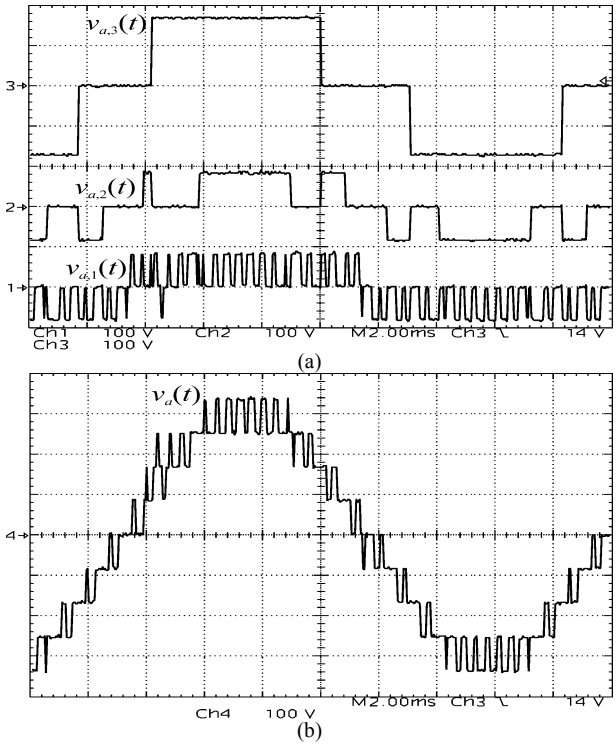

Fig. 12 – Including a locking algorithm: experimental results of 9-level hybrid inverter with a nonsinusoidal command signal ($V_{dc,1} = V_{dc,2} = 85$ V, $V_{dc,3} = 170$ V and $f_s = 2460$ Hz): (a) Output voltages of H-bridge cells. (b) Phase-to-neutral voltage.

VI. CONCLUSIONS

Hybrid multilevel inverters employ distinct semiconductor technologies under different voltage, power and frequency ratings. In this concept, slow switching devices are used in higher voltage cells whereas fast semiconductor devices are used only in the lowest voltage cell, taking advantage of the different semiconductor technologies.

Nevertheless, this paper demonstrated that frequency limitations of some series-connected cells, caused by the use of high-voltage and slow semiconductor switching devices, are not respected under certain disturbances, mainly in feedback control systems in which their bandwidths are higher than the frequency restrictions of some devices. Therefore, this paper analyzed the inclusion of an algorithm in the original hybrid modulation strategy to lock undesired commutations. It has been shown that this locking algorithm avoids extra-commutations in higher voltage cells and generates the desired control signal if lower voltage cells are able to synthesize their reference signals. Otherwise, this locking algorithm can have a negative impact on the synthesis of the desired control signal.

REFERENCES

[1] K. J. Aström and B. Wittenmark, *Computer-controlled systems: Theory and design*. Upper Saddle River, NJ: Prentice Hall, 1997: pp. 334–369.

[2] P. Youbin, D. Vrancic and R. Hanus, "Anti-windup, bumpless, and conditioned transfer techniques for PID controllers", *IEEE Trans. Control Systems*, vol. 16, pp. 48–57, Aug. 1996

[3] J. Sum and R. M. Bass, "Modeling and practical design issues for average current control," in *IEEE Applied Power Electr. Conf. Proc.*, 1999, pp. 980–986.

[4] M. D. Manjrekar, P. K. Steimer and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 36, pp. 834–841, May/June 2000.

[5] T. A. Lipo and M. D. Manjrekar, "Hybrid topology for multilevel power conversion," U. S. Patent 6 005 788, 1999.

[6] J. S. Manguelle, S. Mariethoz, M. Veenstra and A. Rufer, "A generalized design principle of a uniform step asymmetrical multilevel converter for high power conversion," in *EPE Rec.*, 2001, CD-ROM.

[7] C. Rech and J. R. Pinheiro, "Uma abordagem unificada para conversores multiníveis híbridos: inversores e choppers", in *CBA Rec.*, 2004, CD-ROM.

[8] C. Rech and J. R. Pinheiro, "Impact of hybrid multilevel modulation strategy on input and output harmonic performances", in *IEEE APEC Conf. Proc.*, 2005, CD-ROM.

[9] R. Lund, M. D. Manjrekar, P. Steimer and T. A. Lipo, "Control strategies for a hybrid seven-level inverter," in *EPE Rec.*, 1999, CD-ROM.

[10] Y. Wang, H. Li, X. Shi and B. Xu, "A novel carrier-based PWM strategy for hybrid multilevel inverters", in *IEEE PESC Conf. Proc.*, 2004, pp. 4233–4237.

[11] M. G. Lopez, L. T. Morán, J. C. Espinoza and J. Dixon, "Performance analysis of a hybrid asymmetric multilevel inverter for high voltage active power filter applications," in *IEEE IECON Conf. Proc.*, 2003, pp. 1050–1055.

[12] J. Zhang, Y. Zou, X. Zhang and K. Ding, "Study on a modified multilevel cascade inverter with hybrid modulation", in *IEEE PEDS Conf. Proc.*, 2001, pp. 379–384.

[13] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Trans. Power Electr.*, vol. 15, pp. 1102–1117, Nov. 2000.