SYNCHRONOUS FRAME HALF-PERIOD REPETITIVE CONTROLLER FOR THREE-PHASE UPS

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***Abstract* – This paper demonstrates that by modifying the basic period of the conventional repetitive controller in synchronous reference frame a number of benefits can be achieved. Among these benefits are: (i) a simple solution for the saturation of the output transformer due to the pole-zero cancellation issue; (ii) an additional degree of freedom for the selection of the harmonics to be rejected in *abc* stationary frame; (iii) a reduction of the memory space requirement for the implementation; (iv) an increase of the stability margin. As a result it is possible to obtain output voltages with reduced total harmonic distortion (THD) for both linear and non-linear loads. In order to confirm the claimed advantages of the proposed repetitive controller in synchronous reference frame and to demonstrate the steady-state performance, experimental results from a 10kVA space vector modulated three-phase inverter, fully controlled by a DSP TMS320F241, are presented.**

***Keywords* –** Three-phase UPS, Digital Control, Repetitive Control, Internal Model Principle, Insulating Transformer, DC component.

I. INTRODUCTION

The use of uncontrolled rectifiers within critical loads, e.g., in computers and medical equipments, requires uninterruptible power supplies (UPS) which maintain low total harmonic distortion (THD) at the output voltages even with these highly non-linear currents [1].

The UPS output voltages are distorted mainly by balanced and unbalanced non-linear currents drawn by the loads, since they cause voltage drops across the output LC filter which is used to attenuate PWM inverter high frequency harmonics. This becomes a concern in medium and high power UPS where the switching frequency is bounded by the switching losses. Other factors contribute as well to the UPS output voltages distortion. Among them are the inherent nonlinearities of the PWM inverter, fluctuations of the DC-bus voltage and power semiconductors voltage drops. Moreover, transformerless UPS are susceptible to interference from spikes and transients caused by a varied of device connected to the utility grid. These interferences can be transferred through the UPS to the load. Thus, UPS's with output transformer provides a safer and more robust solution than transformerless UPS, since the transformer offer a galvanic isolation that isolates the load from undesirable disturbances of the main supply [2].

In digital controlled systems, quantization of the AD converters, digital pulse width modulators and truncation of the fixed-point arithmetic can generate errors that results in DC component at the output voltage. These errors added up the inevitable real live circuit implementation non-idealities and amplified by an inappropriate selection of the controller, can lead the output transformer to saturate, degrading the overall performance of the system [12]-[13]. It is important to point out that standard such as the IEC62040-3 recommends that the output voltage DC component shall be less than 0.1 % of its rms rated value and specify that the distortion factor "D" of sinusoidal UPS output voltages must to be less than 8%. In order to deal with the above mentioned issues, many control structures for UPS have been reported in the literature.

With the well known Repetitive Controller [4]-[6], established on the Internal Model Principle [3], several high performance approaches have been proposed, in order to achieve high quality output voltages in three-phase PWM inverters [7]-[11]. In [7], a two-layer voltage controller scheme in synchronous frame is proposed: A PI regulator is used to ensure zero steady-state error at the fundamental frequency and a repetitive-based controller with a high-pass filter to compensate the harmonics at the inverter output voltages. However, inadequate choices of the high-pass filter cut-off frequency may result in DC components that can saturate the transformer at the inverter output. Moreover, the repetitive controller with a high-pass filter produce pole-zero cancellation which the plant, violating the internal model principle conditions [3]. More recently, the modified plug-in repetitive controller combined with the conventional OSAP compensator (*One-sampling-ahead preview*) in stationary $\alpha\beta$ frame has been reported in [8] to improve the output voltage distortion when three-phase rectifier loads are connected at the UPS output. However, in this case the output transformer is not considered. Then, if the isolator transformer is connected at the inverter output, a pole zero cancellation occurs with the plug-in repetitive controller in the closed-loop. In [9], a discrete-time control strategy using a repetitive controller extended to a PI compensator structure in stationary $\alpha\beta$ frame is proposed to compensate voltage distortions due to nonlinear and unbalanced loads. The steady-state performance is improved using a 30^{th} order low-pass FIR filter after the measures to attenuate the high frequency components, making the voltage error to contain only lower frequencies. Nevertheless, this implementation presents cancellation of the repetitive controller pole with the zero of the plant introduced by transformer and eventually leaves the transformer to the saturation. Other solutions that can also be described on the internal model principle have been presented in [10] and [11]. In [10] a three-layer control scheme is proposed. It consist of a proportional compensator in stationary $\alpha\beta$ frame, an integral controller in synchronous frame to compensate the fundamental component and a selective harmonic compensator in stationary frame based in a pass-band FIR filter with unity gain and zero phase at the selected harmonics. In reference [11] is proposed a robust controller based on the passivity theory for three-phase UPS. This controller guarantees asymptotic stability with good steady-state performance for nonlinear and unbalanced loads. Although, the controllers proposed in [10] and [11] can be adequate solutions to reduce the output voltages distortion and to operate with an insulating transformer, the computational requirements for the

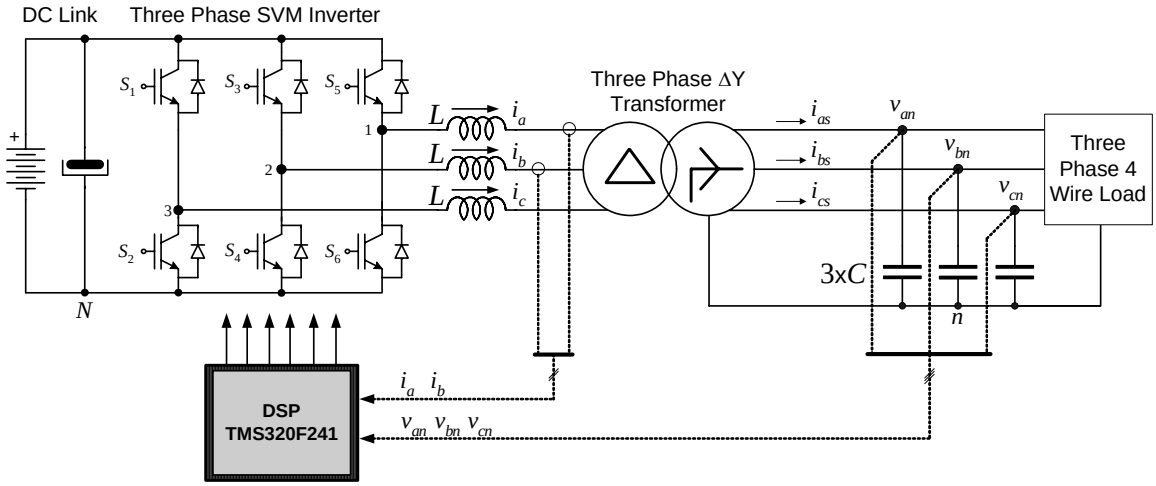

Fig. 1– Digitally controlled system. Three-phase PWM inverter, ΔY transformer, filter and load

implementation of these controllers increases significantly as the number of the harmonics to compensate increases.

In reference [14] and [15] an odd-harmonic digital repetitive plug-in controller is proposed in order to reject this class of disturbance that is usually found in uncontrolled rectifier non-linear loads. This odd-harmonic repetitive controller does not have a pole at $z = 1$; making it suitable to operate with output transformer. However, in real life, even harmonics are often present which result in an increase in the output voltage THD.

In order to obtain output voltages with reduced THD this paper proposes a half-period repetitive controller in synchronous *dq* reference frame. The main feature of the proposed controller is that it is a simple solution for the output transformer saturation. In addition, it provides a degree of freedom to select the load harmonics to be rejected. In order to demonstrate the claimed advantages experimental results from a 10kVA prototype are given.

II. System Description

A typical double-conversion UPS power circuit is shown in the Fig. 1. Among the three-phase inverter configurations, the one shown is a strong candidate since (i) it provides galvanic isolation to the load; (ii) it allows selecting the output voltage according to the customer needs, (iii) it provides a neutral by the delta-star (ΔY) connection. This figure does not show the input rectifier, which commonly is a six or twelve pulses three-phase uncontrolled diode rectifier. The DC bus voltage is almost constant and supplied by a battery, which provide energy to the inverter in the backup mode in absence of the main supply. The DC to AC conversion is accomplished by a space vector modulated three-phase three-leg inverter with insulated-gate-bipolar-transistor (IGBT). The high frequency harmonics introduced by the modulation are attenuated by the LC filter. It is important to point out, that the filter inductors are located at the primary side of the transformer in order to not introduce distortions in the output voltages that result from zero sequence voltages produced by unbalanced load currents, which will be shorted on the delta connection at the transformer primary side. Since this inverter it is not capable to control zero sequence voltages, it is important to minimize the zero sequence impedance to reduce the distortions in the output voltages.

III. Three-Phase PWM Inverter, ΔY Transformer, Filters and Load Model

Stationary Frame Model

From the circuit of Fig. 1 it is possible to obtain the dynamic equations of the inverter, transformer, filter and load, applying the Kirchhoff laws. To simplify the system modeling, it is considered that the leakage inductances of the primary and secondary side of the transformer are lumped at the secondary side. In addition, the coil resistances are neglected. Then, by applying the voltage and current Kirchhoff laws the equations (1), (2) and (3), can be obtained. In these equations, M is the mutual inductance, L is the filter inductance, L'_d the equivalent leakage inductance, and C' is the filter capacitance. u_{12}, u_{23} and, u_{31}, are the line-to-line PWM voltages produced by the inverter. v'_{an}, v'_{bn} and v'_{cn}, are the phase-to-neutral voltages and i'_{oa}, i'_{ob} and i'_{oc} are the load currents, referred to the primary side, respectively, and i_{ab}, i_{bc} and i_{ca} are the phase current at the primary side of the transformer.

Synchronous Frame Model

Transforming the equations (1), (2) and (3) to αβ, and then to synchronous *dq* frame as in [18] it is possible to obtain the state-space model, useful to design the state feedback controller, given by, $\dot{\mathbf{x}}_{dq}(t) = \mathbf{A}_{dq}\mathbf{x}_{dq}(t) + \mathbf{B}_{dq}\mathbf{u}_{dq} + \mathbf{F}_{dq}\mathbf{w}_{dq}$, where the matrices $\mathbf{A}_{dq}$, $\mathbf{B}_{dq}$, and $\mathbf{F}_{dq}$, are given in (4). The state vector has been selected as $\mathbf{x}_{dq}(t) = \begin{bmatrix} i_{dp} & i_{qp} & i_{ds} & i_{qs} & v_d & v_q \end{bmatrix}^{\mathrm{T}}$, and the input and disturbance vectors as $\mathbf{u}_{dq}(t) = \begin{bmatrix} u_d & u_q \end{bmatrix}^{\mathrm{T}}$ and $\mathbf{w}_{dq}(t) = \begin{bmatrix} i_{od} & i_{oq} \end{bmatrix}^{\mathrm{T}}$ respectively. In this matrices D is defined as: $D = 3LM + 3LL'_d + ML'_d$. In order to obtain a discrete-time model for the state feedback controller design, the synchronous frame state equation, obtained above, must be solved along of the sampling period T. For the purpose, it is considered that the control action $\mathbf{u}_{dq}(t)$

$$\begin{bmatrix} u_{12} \\ u_{23} \\ u_{31} \end{bmatrix} = \begin{bmatrix} 2L + \dfrac{ML'_d}{M+L'_d} & -L & -L \\ -L & 2L + \dfrac{ML'_d}{M+L'_d} & -L \\ -L & -L & 2L + \dfrac{ML'_d}{M+L'_d} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} + \frac{M}{M+L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v'_{an} \\ v'_{bn} \\ v'_{cn} \end{bmatrix} \tag{1}$$

$$\frac{d}{dt} \begin{bmatrix} i'_{as} \\ i'_{bs} \\ i'_{cs} \end{bmatrix} = \frac{M}{M+L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} - \frac{1}{M+L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v'_{as} \\ v'_{bs} \\ v'_{cs} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} \dot{v}'_{an} \\ \dot{v}'_{bn} \\ \dot{v}'_{cn} \end{bmatrix} = \frac{1}{C'} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i'_{as} \\ i'_{bs} \\ i'_{cs} \end{bmatrix} + \frac{1}{C'} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} i'_{oa} \\ i'_{ob} \\ i'_{oc} \end{bmatrix} \tag{3}$$

$$\mathbf{A}_{dq} = \begin{bmatrix} 0 & -\omega & 0 & 0 & -M/D & 0 \\ \omega & 0 & 0 & 0 & 0 & -M/D \\ 0 & 0 & 0 & -\omega & -(3L+M)/D & 0 \\ 0 & 0 & \omega & 0 & 0 & -(3L+M)/D \\ 0 & 0 & 1/C & 0 & 0 & -\omega \\ 0 & 0 & 0 & 1/C & \omega & 0 \end{bmatrix}$$

$$\mathbf{B}_{dq} = \begin{bmatrix} (M+L_d)/D & 0 \\ 0 & (M+L_d)/D \\ M/D & 0 \\ 0 & M/D \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad \mathbf{F}_{dq} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1/C & 0 \\ 0 & -1/C \end{bmatrix} \tag{4}$$

keep constant in a sampling period T. Thus, the discrete-time state-space equation of the plant is given by,

$$\begin{bmatrix} \mathbf{x}_{dq}(k+1)T \\ \mathbf{u}_{dq\_d}(k+1)T \end{bmatrix} = \begin{bmatrix} \mathbf{G} & \mathbf{H_0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{x}_{dq}(kT) \\ \mathbf{u}_{dq\_d}(kT) \end{bmatrix} + \begin{bmatrix} \mathbf{H_1} \\ \mathbf{I} \end{bmatrix} \mathbf{u}_{dq}(kT) \tag{5}$$

Where, the additional state variable $\mathbf{u}_{dq\_d}$ represent the delay control action that model the real time digital implementation delay, and the matrices $\mathbf{G}$, $\mathbf{H_0}$ and $\mathbf{H_1}$ are obtained as shown in (6). In equation (6), T is the sampling period and T_d is the above mentioned time delay. The sampling of the interest variables and the control law updating is performed as shown in Fig. 2.

$$\mathbf{G} = e^{\mathbf{A}_{dq}T}, \quad \mathbf{H_0} = e^{\mathbf{A}_{dq}(T-T_d)} \mathbf{A}_{dq}^{-1} (e^{\mathbf{A}_{dq}T_d} - \mathbf{I}) \mathbf{B}_{dq}$$
$$\mathbf{H_1} = \mathbf{A}_{dq}^{-1} \left[e^{\mathbf{A}_{dq}(T-T_d)} - \mathbf{I} \right] \mathbf{B}_{dq} \tag{6}$$

With the sampling scheme of Fig. 2 it is possible to use a low switching frequency for higher power levels preserving an acceptable sampling frequency. In addition, due to the sampling is carry out at the zero vectors, the resulting low frequency harmonics are reduced if compared with one sample in a sampling period [17]. It is important to note that the currents at the transformer secondary side, i_{as}, i_{bs} and i_{cs}, are states of the modeled system.

However, the measures of these variables are not available. These currents can be obtained with a predictive observer, since that the system is observable. That is, it is possible to obtain the above mentioned currents from the measures of the output voltages and the input current and delayed control actions.

IV. Proposed Digital Voltage Controller in Synchronous *dq* Frame

The control law applied to the plant, given by equation (7) is a sum of the state feedback control action plus the repetitive control action, as shows in Fig. 3, that is

$$\mathbf{u}_{dq}(k) = \mathbf{u}_{\mathbf{c}dq}(k) + \mathbf{u}_{\mathbf{r}dq}(k) \tag{7}$$

Where,

$$\mathbf{u}_{\mathbf{c}dq}(k) = -\mathbf{K}_{re}\mathbf{x}_{dq} \tag{8}$$

$$\mathbf{u}_{\mathbf{r}dq}(k) = k_r \sum_{i=1}^{\infty} \mathbf{e}_{dq}(k - iN_r + d) \tag{9}$$

The repetitive controller with an integral action given in equation (9), has been presented in [16]. In this equation, $\mathbf{e}_{dq}(k) = \mathbf{r}_{dq}(k) - \mathbf{y}_{dq}(k)$ is the voltage error vector, "d" represent the time advance step size that compensate the phase at high frequencies introduced by the plant delay, N_r is the number (an integer) of samples in a fundamental voltage period, and k_r is the repetitive controller gain. The gain k_r must be designed in order to guarantee a fast convergence of the error to zero maintaining the closed-loop system stability. Higher values of k_r results in a fast convergence of the output error, however the closed-loop system may become unstable [16]. For the design of the state feedback gain matrix $\mathbf{K}_{re}$ given in (8), has been selected the steady-state discrete linear quadratic regulator technique. This approach is simple and provides a steady-state solution asymptotically stable. With this technique, the feedback gains are designed in order to minimize a cost function (10):

$$J = \sum_{k=1}^{\infty} [\mathbf{x}_{dq}(k)^{\mathrm{T}} \mathbf{Q}\, \mathbf{x}_{dq}(k) + u_{dq}(k)^{\mathrm{T}} \mathbf{R}\, u_{dq}(k)] \,. \tag{10}$$

By an adequate choices of the performance matrices $\mathbf{Q}$ and $\mathbf{R}$, the closed-loop system result asymptotically stable. However, the system performance depends on the choices of the specific entries of the $\mathbf{Q}$ and $\mathbf{R}$, related to the states and control action energy, respectively [18]. The weighting

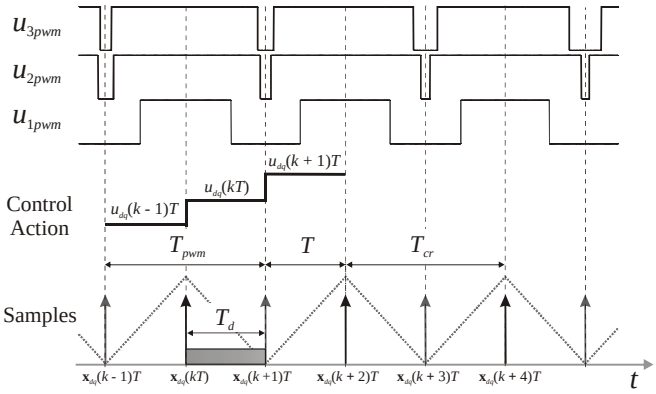

Fig. 2 – SV pattern, *dq* control action and sampling instants. T_{pwm}: Switching period, T: Sampling period, T_d: Time delay. T_{cr}: Repetitive controller sampling period.

matrices **Q** and **R** have been assumed diagonal and its entries has been chosen to stabilize the closed-loop system and to obtain a damped response without transient oscillations. This procedure must be accomplished without the repetitive control action. In this case **Q** and **R** have been chosen in the following form:

$$\mathbf{Q} = diag\begin{bmatrix}1 & 1 & 1 & 1 & 1 & 1 & 100 & 100\end{bmatrix},$$
$$\mathbf{R} = diag\begin{bmatrix}100 & 100\end{bmatrix} \quad (11)$$

It is important to note that the sampling frequency of the variables of interest to compute the states feedback is $f_s = 1/T$, as depicted in Fig. 2. However, the sampling frequency of the repetitive controller can be different and this selection has an impact on the system performance. Next section investigates this issue and proposes an adequate repetitive controller for the system of Fig. 1.

V. Selection of the Repetitive Controller Period

Note that the repetitive controller of Fig. 3 is implemented in synchronous frame. Since usually the harmonics are expressed in stationary frame, Table I shows the relationship between the harmonic components in these frames. It is possible to see that each harmonic component in *dq* synchronous frame, result in a shifting, equal to the fundamental frequency, above and/or below of the harmonic component in *abc* stationary frame. Usually the sampling period of the repetitive controller T_{cr} (see Fig. 2), is selected to be equal to the sampling period T, of state variables, as a result, the repetitive basic period N_r is equal to the reference fundamental period N in *abc* stationary frame. In this case the repetitive controller can compensate harmonics of the output voltages from DC up to the Nyquist frequency [5]. For example, let us consider the sampling as defined in accordance with the scheme depicted in Fig. 2. The states variable sampling frequency is f_s = 10.08 kHz, and a switching frequency $f_{sw} = f_s/2$, that is, 5.04 kHz.

As mentioned at beginning of this section $N_r = N = 168$ (for a fundamental frequency f_1 = 60 Hz). Then, the compensated harmonics by this repetitive controller in *dq* synchronous frame, are DC, 1th, 2th, 3th, ...,up to $N/2 = 84^{th}$. Note that, in stationary coordinates the compensated harmonics are DC, 1th, 2th, 3th, 4th, ..., up to 83th. Therefore, the highest frequency compensated by the repetitive controller is 5.04 kHz, which is within the sideband of the

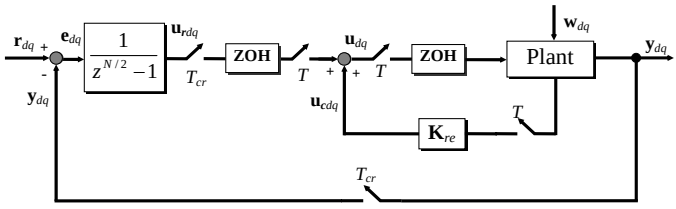

Fig. 3 – Control structure of the closed-loop multirate MIMO system in synchronous *dq* frame. $T_{cr} \geq T$.

TABLE I. Harmonics Relationship Between *abc* Stationary Frame and *dq* Synchronous Frame

Harmonics in *abc* stationary frame	Harmonics in *dq* synchronous frame
1°(+)	DC
DC	1°
1°(-) (unbalance)	2°
2º(+)	1º
2º(-)	3°
3º(+)	2º
3º(-)	4º
4º(+)	3º
4º(-)	5º
5º(+)	4º
5º(-)	6º
6º(+)	5°
6º(-)	7°
7º(+)	6°
7º(-)	8°
8º(+)	7°
8º(-)	9°
9º(+)	8°
9º(-)	10°

(+): Positive Sequence, (-): Negative Sequence.

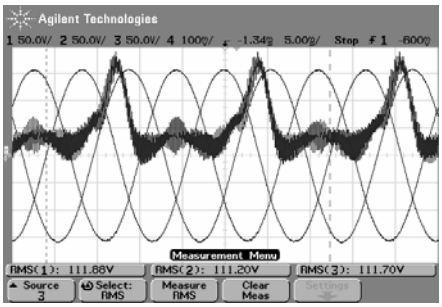

Fig. 4 – Experimental result. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, and line current i_a at the transformer primary side. Voltage scale: 50 V/div. Current scale: 10 A/div. $N_r = N = 168$.

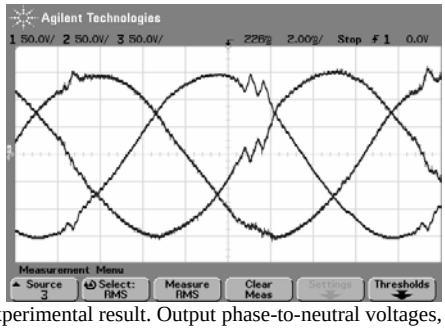

Fig. 5 – Experimental result. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, Voltage scale: 50 V/div. $N_r = N = 168$.

harmonics centered at the switching frequency of the PWM inverter. This selection of N is adequate to control the output voltages of a three-phase inverter without the isolator transformer. That is, the presence of the isolator transformer at the output of the inverter produce a pole-zero cancellation when this repetitive controller is introduced in the closed-loop making any residual DC component to be amplified by this controller. This can lead to the transformer saturation, degrading the overall system performance [13]. Fig. 4 presents experimental results obtained from the system of Fig. 1 with the controller described above. It is possible to see that the phase-to-neutral voltages v_{an}, v_{bn} and v_{cn} remain at the desired levels with a reduced THD, however, the currents at the transformer primary side have a DC component that increases up to the transformer saturation. In addition, due to the fact that the open-loop poles of the repetitive controller are on the stability boundary, (with infinite gain at repetitive frequencies), the system becomes very sensitive to unmodeled dynamics in the system. These model uncertainties are normally present at high frequencies, that is, near the switching frequency, which is also the maximum frequency compensated by repetitive controller. This issue is shown in Fig. 5, where high frequency oscillations appear at the output phase-to-neutral voltages, and this will eventually lead the system to the instability. In order to gain robustness a non-causal moving average filter with zero phase shift characteristics can be used [6] to reduce the repetitive frequency gains, with the drawback of compromise the tracking and disturbance rejection.

To overcome the above mentioned problems, here it is proposed two modifications in the conventional repetitive controller: the first one is on its sampling frequency which defines the highest harmonic compensated by the repetitive controller. This frequency should be selected to ensure that the Nyquist frequency of the repetitive controller be smaller than the first set of the harmonics generated by the switching operation of the PWM inverter. This first modification makes it possible to implement the repetitive controller without the moving average filter. The second one is regarding the basic period N_r of the repetitive controller which gives a degree of freedom for the selection of the harmonics that are compensated below the Nyquist frequency. Let us consider again the scheme depicted in Fig. 2. The state variable sampling frequency f_s is kept at 10.08 kHz and the repetitive controller sampling frequency is reduced to half of f_s, that is, 5.04 kHz. As result, the basic reference fundamental period is N = 84 and the highest frequency compensated by the repetitive controller, 2.52 kHz, is smaller than the PWM inverter harmonic centered around de switching frequency, 5.04 kHz. It is important to point out that in this case, there are no repetitive poles in the model uncertainty region close to switching frequency. On the other hand, there is an additional degree of freedom in the design of the repetitive controller that is selection of its basic period N_r. By choosing $N_r = N$ the harmonics compensated are DC, 1^{th}, 2^{th}, 3^{th}, 4^{th},...,up to 42^{th}. Note that, in stationary coordinates the compensated harmonics are DC, 1^{th}(+),1^{th}(-), 2^{th}(+), 2^{th}(-), 3^{th}(+), 3^{th}(-), 4^{th}(+), ...,up to 41^{th}(-). However, the selected value of N_r is undesired since this repetitive controller will attempt to compensate any residual DC component which eventually will saturate the output transformer, as shown in Fig. 4.

Let us now modify the basic period of the repetitive controller, by choosing $N_r = N/2$. In this case the harmonics compensated in dq frame are: DC, 2^{th}, 4^{th}, 6^{th}, 8^{th}, ...,up to 42^{th}. In stationary coordinates the compensated harmonics are 1^{th}(+), 1^{th}(-), 3^{th}(+), 3^{th}(-), 5^{th}(+), 5^{th}(-), 7^{th}(+), 7^{th}(-), 9^{th}(+),..., up to 41^{th}(-). Consequently, the repetitive controller does not amplify frequency component of 60 Hz in *dq* synchronous frame, that is, DC component in *abc* stationary frame, avoiding, in this way the transformer saturation. In this case, the periodic signal generator turns into:

$$G_{rdq}(z) = \frac{1}{z^{N/2} - 1}, \tag{12}$$

which poles map is indicated in Fig. 6. Fig. 8 shows the experimental result for the system of Fig. 1, using the periodic signal generator (12) with a basic period of N_r = 42. It is possible to see again that, the output-to-neutral voltages v_{an}, v_{bn} and v_{cn} remain controlled with reduced THD. In addition to, the currents at the transformer primary side appear without DC components, demonstrating that the transformer does not saturate.

Furthermore, using this approach other repetitive controller can be obtained. For instance, by selecting the basic period as $N_r = N/4$ for a repetitive controller in synchronous frame, the harmonics compensated are DC, 4^{th}, 8^{th}, 12^{th}, ...,up to 40^{th} and the following rejected harmonic in *abc* frame are: 1^{th}(+), 3^{th}(-), 5^{th}(+), 7^{th}(-), 9^{th}(+), 11(-), 13(+)..., up to 39^{th}(-). In this case the periodic signal generator assumes the following form:

$$G_{rdq}(z) = \frac{1}{z^{N/4} - 1}, \tag{13}$$

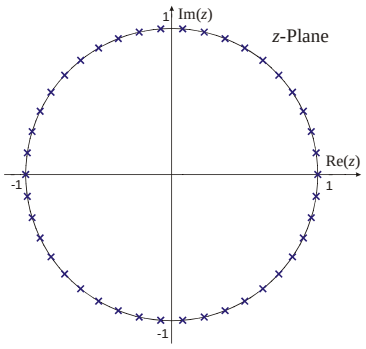

Fig. 6. Poles map of the repetitive controller (12) in *dq*. N_r = 42.

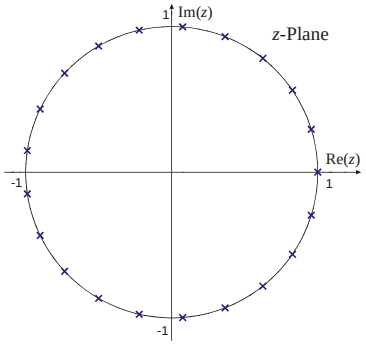

Fig. 7. Poles map of the repetitive controller (13) in *dq*. N_r = 21.

The periodic signal generator (13) has a poles map as indicated in Fig. 7.

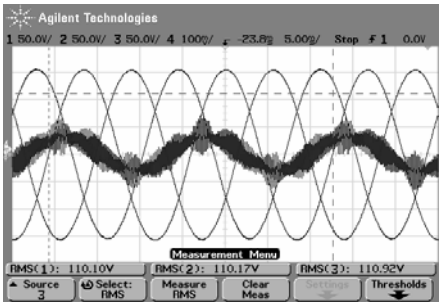

Fig. 8 – Experimental result. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, and line current i_a at the transformer primary side. Voltage scale: 50 V/div. Current scale: 10 A/div. $N_r = 42$.

VI. Experimental Results

The circuit of Fig. 1 has been tested experimentally to verify the proposed digital voltage controller, using a DSP TMS320F241 to control a 10 kVA UPS. The steady-state load tests have been performed using non-linear single-phase and three-phase uncontrolled diode rectifiers. The three-phase PWM inverter with the output transformer and filter parameters, as well as, the repetitive controller gain are given in Table II. Fig. 9, shows the three-phase line-to-neutral voltages and the load current in the phase *a*, when operating without the proposed controller. It is possible to see that the THD of the output voltage is very high around 10 %. Fig. 10 and 11 shows the operation with the proposed controller with both three-phase and single-phase uncontrolled rectifier loads, respectively. Fig. 11 shows the output phase voltages and current for single-phase uncontrolled rectifier connected between one phase and neutral. This represents the worst case with the phase rated unbalanced non-linear load. It is possible to see from these experimental results that the total harmonic distortion of the output voltages is very low, around 1%, even with this severe operation condition. In addition, with the proposed controller, the unbalanced factor has been reduced to a value below 1%.

VII. Conclusions

This paper proposes a digital voltage controller that uses the repetitive controller plus feedback states compensation in *dq* synchronous frame, adequate for three-phase three-leg PWM inverters that operate with an insulating output transformer. This paper demonstrates that by modifying the basic period N_r of the conventional repetitive controller in synchronous *dq* frame it is possible to avoid that residual DC component (in stationary *abc* coordinates), that is, 60 Hz in *dq* frame, that can be amplified and eventually saturate the output transformer. This simple modifications besides to solve the saturation of the transformer allows to improve the performance for both linear and non-linear loads, as well as the closed-loop stability. It is demonstrate that it is possible to achieve an accurate regulation of reference and reject the periodic harmonics at the output voltages. Related to the digital implementation, this solution is attractive for DSP and microcontrollers with reduced RAM memory, since its saves memory space that is required to store the voltage error in the circular buffer. The experimental results presented here demonstrate the good steady-state performance for both non-linear unbalanced and balanced loads with reduced THD and unbalanced factor in the UPS output voltages.

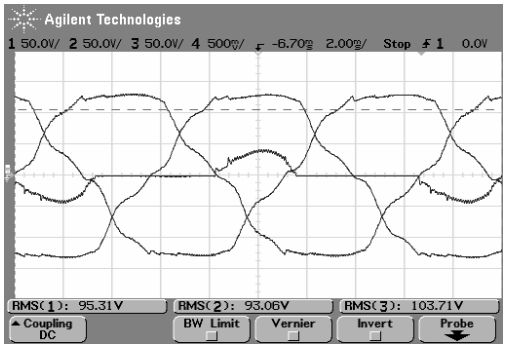

Fig. 9 – **Experimental result.** Single-Phase uncontrolled rectifier 10 kVA. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, load current i_a. Voltage scale: 50 V/div. Current scale: 50 A/div. **THD = 9 %.**

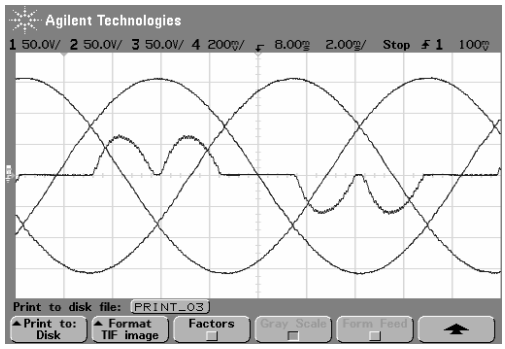

Fig. 10 – **Experimental result.** Three-Phase uncontrolled rectifier 10kVA. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, and load current i_a. Voltage scale: 50 V/div. Current scale: 20 A/div. **THD = 0.8 %.**

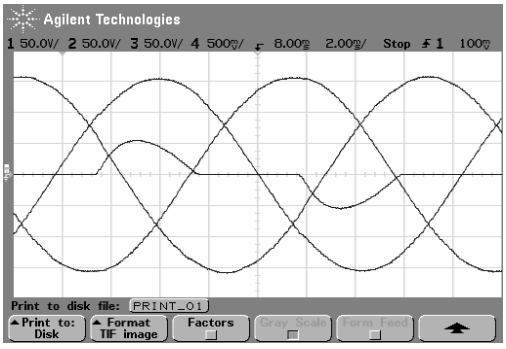

Fig. 11 – **Experimental result**. Unbalanced load. Single-Phase uncontrolled rectifier 3.3 kVA. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, load current i_a. Voltage scale: 50 V/div. Current scale: 50 A/div. **THD = 1.2 %. Unbalanced factor = 0.92%.**

Table II. Parameters of the Three-Phase PWM Inverter and Repetitive Controller

Switching Frequency (f_s)	5.04 kHz
Plant Sampling Frequency (f_a)	10.08 kHz
Repetitive Controller Sampling Frequency (f_{cr})	5.04 kHz
Fundamental Frequency (f_1)	60 Hz
DC Bus Voltage	450 V
Mutual Inductance (M)	200 mH
Output Filter Inductor (L)	500 µH
Output Filter Capacitor (C)	120 µF
Transformer Turns Ratio	1.732
Nominal Output Voltage	3x220/127V
Repetitive Controller Basic Period in *dq* (N_r)	42
Repetitive Gain (k_r)	1.2
Time Advance Step Size (d)	2

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