DESIGN METHODOLOGY FOR LOW THD SINGLE-PHASE VOLTAGE-SOURCE UPS INVERTER SUPPLYING NON-LINEAR LOADS

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***Abstract* – This paper describes a design methodology for low THD single-phase voltage-source UPS inverter supplying non-linear loads. In order to describe the methodology the inverter transfer functions are evaluated. The L-C filter design procedure is then presented, including an analysis of the optimum transformer conversion ratio. Simulation and experimental results are provided in order to validate the methodology.**

***Keywords* – UPS, inverter, design methodology.**

I. INTRODUCTION

Uninterruptible Power Supplies (UPS) are used to conditioning and back-up critical loads such as computers and communications systems. A sinusoidal waveform with a restrictive minimum total harmonic distortion is required at the UPS inverter output voltage. In order to achieve such waveform is normally employed a combination of unipolar sinusoidal pulse width modulation [1][10], second order filter at the inverter output and voltage loop control. When the UPS system uses a transformer, it is also necessary to take care of the core saturation problem and another control loop is required. Several studies have been accomplished on the optimal L-C filter design [2][3][4][5].

This paper investigates the inverter transfer functions and the L-C filter design, and analyses the transformer conversion ratio and its relationship with the system in order to present a suitable design methodology considering the load to be a full bridge rectifier with a capacitive filter. Another aim is to significantly improve the methodology proposed in [6]. The results are verified through computer simulation and a 1kVA prototype.

II. SINGLE-PHASE VOLTAGE-SOURCE UPS INVERTER

Fig. 1 shows the power circuit and the control block diagram of the single-phase voltage-source inverter. V_i is the system DC input voltage. S_1 to S_4 represent the switches, which could be power MOSFETs or IGBTs as shown in Fig. 1. C_1 to C_4 are the switches command signals, which are generated at the sinusoidal pulse width modulator (SPWM). D_1 to D_4 are power diodes. The primary winding current is represented by I_{pri}. L_f and C_f are the filter inductor and capacitor, respectively. V_{ref} is the voltage reference input signal. The output filter voltage is represented by V_o. $C_v(s)$ is a conventional PID controller and is responsible for maintaining the output voltage as much sinusoidal as possible. The $C_i(s)$ controller eliminates the DC current component at the transformer primary windings, avoiding the transformer core saturation. T_i and T_v are the current and the voltage transducers, respectively. Finally, *n* represents the transformer conversion ratio.

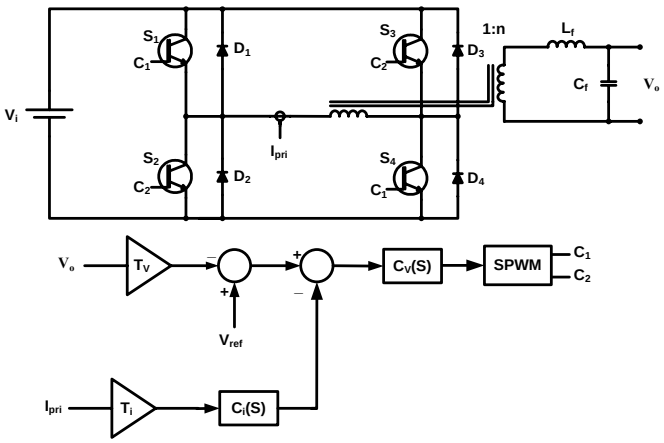

Fig. 1 - Power circuit and control block diagram of the inverter.

The inverter mathematical model can be divided up into a transfer function involving the output voltage and other involving the average current at the transformer primary winding, both related to the input modulator voltage. The load di/dt is considered as a disturbance to the system, as can be noticed in Fig. 2. The transfer function between the inverter output voltage and the output voltage control signal (V_c), obtained as described in [13], considering the inverter operating with no load is given by (1). V_p is the peak value of the triangular waveform used in the modulator.

$$\frac{V_o(s)}{V_c(s)} = \frac{1}{V_p} \cdot \frac{n \cdot V_i}{s^2 \cdot L_f \cdot C_f + 1} \tag{1}$$

The primary winding current can be divided up into two components: the current reflected from the secondary and the transformer magnetizing current. As the current reflected from the secondary carries no DC component, if the average value of the magnetizing current is kept to zero, one ensures that there's no DC component applied over the primary terminals and thus no core saturation. The transfer function between the magnetizing current and the primary transformer winding voltage (V_{pri}) is given by (2), where L_m is the magnetizing inductance of the transformer and r_s is the primary winding resistance.

$$\frac{i_{Lm}(s)}{V_{pri}(s)} = \frac{1}{s \cdot L_m + r_S} \quad (2)$$

Fig. 2 shows the simplified control scheme of the system. The $1/V_p$ gain block represents the modulator [13]. The inverter is represented by the gain block V_i [13]. The output of this block is the primary winding voltage (V_{pri}). From this voltage the magnetizing current and the secondary winding voltage (V_{sec}) are obtained. There are two blocks between the secondary and primary winding voltage: the gain block *n* and a DC component blockage, which emphasizes that there is no DC component in the secondary. The output filter transfer function interacts with the load, particularly if high di/dts are present. The load block represents a non-linear load, which the relation between the load current (I_{Lo}) and the output voltage (V_o) could not be simply obtained.

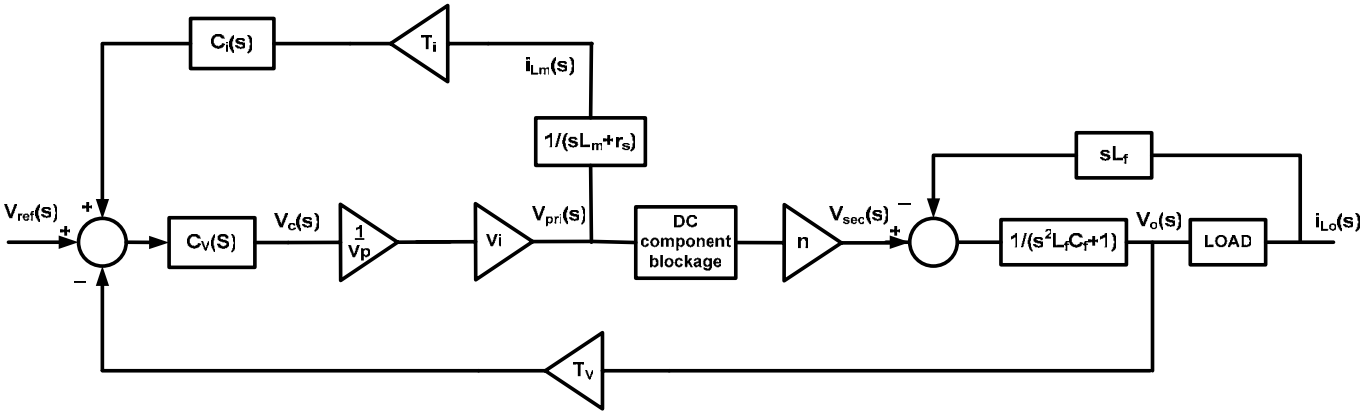

Fig. 2 - Simplified inverter control scheme.

III. NON-LINEAR LOAD

The non-linear load considered in this work is the full bridge rectifier with a capacitive filter presented in Fig. 3. Its crest-factor (Fc) [8] is limited by the inductance L_o.

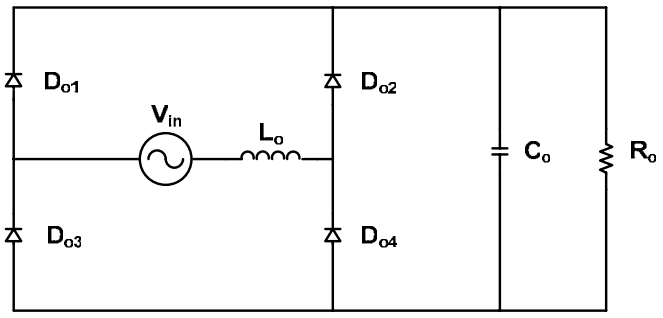

Fig. 3 – Load circuit.

The di/dt maximum values of the load are calculated from expressions developed previously based on the crest-factor (F_c), apparent power (S_o), operation frequency (f_r) and input voltage (V_{in}), where [9] was used as a start point. The expressions will not be displayed due to their large size.

IV. L-C FILTER DESIGN

The filter inductance value is given by (3), being chosen such that a desired maximum current ripple is attained. V_{op} is the peak value of the output voltage V_o. The switching period is represented by T_s. $\Delta I_{L_f \max}$ is the maximum peak to peak L_f current ripple and V_{imax} is the maximum system input DC voltage. The respective filter capacitance value is given by (7), where $\Delta V_{C_f \max}$ is the maximum peak to peak V_o ripple.

Equation (3) is obtained from the voltage loop comprising V_{sec}, V_{Lf} and V_o, which can be seen in Fig. 1. Equation (7) is determined as in [13]. In both cases, it is supposed that during a switching period the modulating signal is constant, i.e. the switching frequency is very high.

$$L_f = \frac{T_s}{\Delta I_{L_f \max}} \cdot \frac{\left(n \cdot V_{i\max} - V_{op} \cdot sin\left(\frac{\pi}{4}\right)\right) \cdot \left(V_{op} \cdot sin\left(\frac{\pi}{4}\right)\right)}{2 \cdot n \cdot V_{i\max}} \quad (3)$$

The most important contribution to the output waveform distortion comes from non-linear loads, such as full bridge rectifiers with capacitive filters. In this case the load current rises and falls with very high di/dt each half period. The effect of the high di/dt in the rise was presented in [7]. However, during the current fall time there is a very high di/dt, which can also affect the output waveform particularly when the inverter is operating at low modulation index.

The current flowing through L_f is composed by the load current and the filter current. When the load current rises with a high di/dt there is also a high di/dt through L_f. Therefore, there will be a high voltage drop across L_f and the voltage compensator will raise its output signal in order to maintain a sinusoidal voltage at V_o. If the control signal exceeds V_p there will be a distortion in V_o as there won't be enough voltage in the secondary winding.

On the other hand, if there is a high di/dt during the L_f current fall, the controller will have to decrease its duty cycle, which can invert and even exceed $-V_p$, generating an overvoltage at V_o.

Assuming a maximum modulation index of 0,9 and based on the study of the rectifier [9] and the situation described above, it is possible to find two restrictions for the L_f value, which are given by (4) and (5). $di_{Lo}(t)/dt_{maxsub}$ is the maximum value of di/dt during the rise of i_{Lo}. $di_{Lo}(t)/dt_{maxdes}$

is the maximum value of di/dt during the fall of i_{Lo}. These values can be estimated if the crest-factor (F_C), apparent power, operation frequency and input voltage of the rectifier are known.

$$L_f < \frac{0,9 \cdot n \cdot V_{i\min} - V_{op}}{\left.\frac{di_{Lo}(t)}{dt}\right|_{\max sub}} \quad (4)$$

$$L_f < \frac{\left(0,9 \cdot n \cdot V_{i\min} + V_{op}\right) \cdot 0,9}{\left|\left.\frac{di_{Lo}(t)}{dt}\right|_{\max des}\right|} \quad (5)$$

Equation (4) is used when the maximum rise di/dt is more relevant to the system and (5) when the fall di/dt is more important. There is a threshold that defines which equation has to be used. If the transformer conversion ratio *n* obeys the relation in (6), equation (4) is valid.

$$n < \frac{V_{op} \cdot \left(\left|\left.\frac{di_{Lo}(t)}{dt}\right|_{\max des}\right| + \left.\frac{di_{Lo}(t)}{dt}\right|_{\max sub} \cdot 0,9\right)}{V_{i\min} \cdot \left(\left|\left.\frac{di_{Lo}(t)}{dt}\right|_{\max des}\right| - \left.\frac{di_{Lo}(t)}{dt}\right|_{\max sub} \cdot 0,9\right) \cdot 0,9} \quad (6)$$

$$C_f = \frac{\left(n \cdot V_{i\max} - V_{op} \cdot sin\left(\frac{\pi}{4}\right)\right) \cdot \left(V_{op} \cdot sin\left(\frac{\pi}{4}\right)\right) \cdot T_s^2}{32 \cdot L_f \cdot \Delta V_{C_f \max} \cdot n \cdot V_{i\max}} \quad (7)$$

V. TRANSFORMER

Considering the high frequency output voltage ripple waveform as a sinusoidal wave operating at twice the switching frequency, as shown in (8), the RMS capacitor current as well as the RMS primary winding current can be evaluated in function of the transformer conversion ratio *n*. With this information one can have a good estimation of the most suitable conversion ratio, which must have the commitment to diminish the semiconductors current efforts in the inverter stage and the filter inductor ripple, at an acceptable capacitor current.

From (8) the capacitor current expression is evaluated and represented by (12). Fig. 4 shows equation (12) behavior when Table I parameters are used.

$$V_{C_f}(t) = V_{op} \cdot sin(\omega_r \cdot t) + \frac{\Delta V_{C_f}(\omega_r \cdot t)}{2} \cdot sin(2 \cdot \omega_s \cdot t + \pi) \quad (8)$$

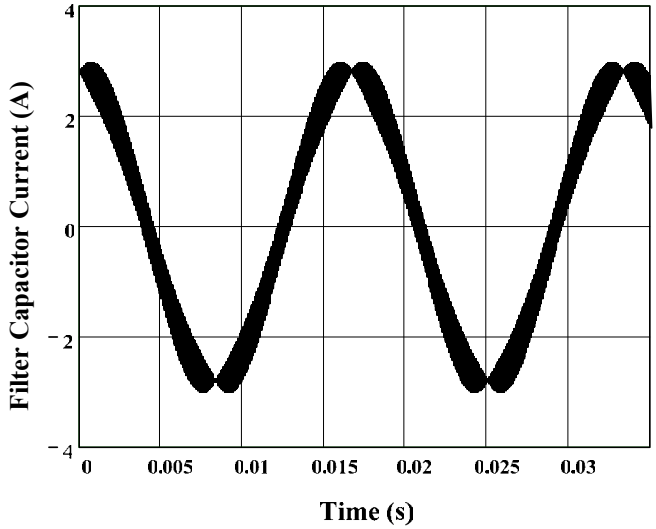

Fig. 4 – i_{Cf} as a function of time.

It is known that the minimum primary winding current is found when the maximum filter inductance value is used. Besides, with a greater inductance value one needs a smaller capacitance value to maintain the same ripple specification and thus the RMS current in the filter is the lowest. Another advantage is related to the cost function defined in [2], where it says that if the L-C filter components are a set of a small capacitance and a large inductance, it minimizes the cost function. However, the restrictions at (4) and (5) must be respected.

The filter inductor ripple equations in function of *n* are given by equations (9) and (10). It can be noticed that equation (10) substitutes (9) just when the relation in (6) is not valid. These equations are obtained by substituting (4) and (5) in (3), respectively. Equation (11) is obtained by substituting (3) in (7).

$$\Delta i_{Lf\max}(n) = \frac{\left.\frac{di_{Lo}(t)}{dt}\right|_{\max sub} \cdot \pi \cdot V_{op} \cdot \left(\sqrt{2} \cdot n \cdot V_{i\max} - V_{op}\right)}{2 \cdot n \cdot V_{i\max} \cdot \omega_s \cdot \left(0,9 \cdot n \cdot V_{i\min} - V_{op}\right)} \quad (9)$$

$$\Delta i_{Lf\max}(n) = \frac{\left.\frac{di_{Lo}(t)}{dt}\right|_{\max des} \cdot \pi \cdot V_{op} \cdot \left(\sqrt{2} \cdot n \cdot V_{i\max} - V_{op}\right)}{1,8 \cdot n \cdot V_{i\max} \cdot \omega_s \cdot \left(0,9 \cdot n \cdot V_{i\min} + V_{op}\right)} \quad (10)$$

$$C_f(n) = \frac{\pi \cdot \Delta i_{Lf\max}(n)}{8 \cdot \omega_s \cdot \Delta V_{Cf\max}} \quad (11)$$

$$i_{C_f}(t) = \frac{V_{op}}{16 \cdot L_f \cdot n \cdot V_{i\max} \cdot \omega_s^2} \cdot \left(\begin{array}{l} 16 \cdot L_f \cdot C_f \cdot n \cdot V_{i\max} \cdot \omega_r \cdot \omega_s^2 \cdot \cos(\omega_r t) \\ +\pi^2 \cdot \left(\begin{array}{l} 2 \cdot \omega_s \cdot \cos(2 \cdot \omega_s t) \cdot \left(\begin{array}{l} V_{op} \cdot Sin^2(\omega_r t) \\ -n \cdot V_{i\max} \cdot \left|Sin(\omega_r t)\right| \end{array} \right) \\ +\omega_r \cdot \left(\begin{array}{l} V_{op} \cdot Sin(2 \cdot \omega_r t) - \\ n \cdot V_{i\max} \cdot \left|Sin(\omega_r t)\right| \cdot Cot(\omega_r t) \end{array} \right) \cdot Sin(2 \cdot \omega_s t) \end{array} \right) \end{array} \right) \quad (12)$$

In the same manner, the RMS capacitor current in function of *n* is given by (13), the RMS load current is represented by (14) and the RMS primary winding current is given by (15). Equation (13) can't be displayed here due to its large size.

It should be noticed that the RMS capacitor current does not depend on L_f and C_f values due to the substitution of (4), (5), (9), (10) and (11) in (12).

Therefore, it is interesting to note that from the system input and output parameters, load parameters and a desired output voltage ripple, one can find the RMS capacitor current as well as the RMS primary winding current and the inductor current ripple, considering the maximum allowable filter inductance based on the load characteristics.

Moreover, it is also ensured that the primary winding current will be the lowest at each *n* chose due to the adoption of the referred inductor value.

The filter inductor current ripple as a function of *n* can be seen in Fig. 5. The behavior of equations (13), (14) and (15) in function of *n* are shown in Fig. 6.

$$i_{Cf_{RMS}} = f\left(n, \omega_r, \omega_s, V_{op}, V_{i\max}, \Delta V_{Cf\max}\right) \quad (13)$$

$$i_{Lo_{RMS}} = \frac{\sqrt{2}\cdot S_o}{V_{op}} \quad (14)$$

$$i_{pri_{RMS}} = n\cdot\sqrt{i_{Cf_{RMS}}^2 + \left(i_{Lo_{RMS}}\right)^2} \quad (15)$$

TABLE I
Parameters

S_o	V_{imax}	V_{imin}	V_o	f_r	f_s
1 kVA	160 V	160 V	127 V	60 Hz	20 kHz
F_c	di/dt_{sub}	di/dt_{des}	n	L_f	C_f
3.54	42000 A/s	-125000 A/s	1.6	1.2 mH	40 uF

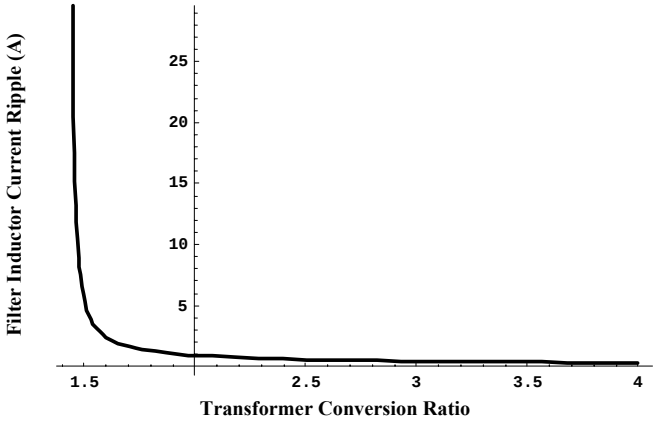

Fig. 5 – Filter inductor current ripple as a function of *n*.

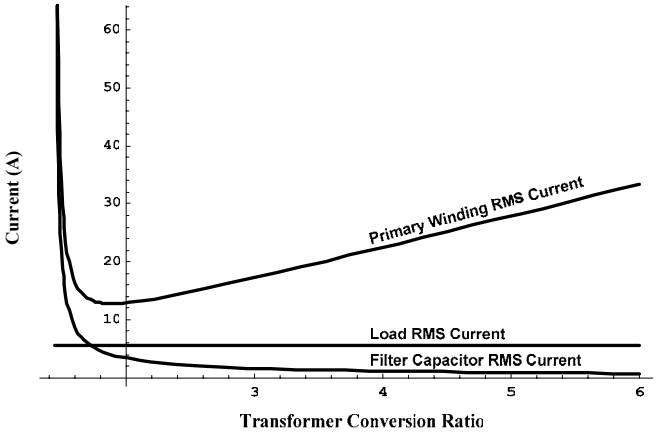

Fig. 6 – Inverter RMS currents as a function of *n*.

It can be seen that the RMS capacitor current is very high at the minimum value of the primary RMS current. The inductor current ripple is very high at this point as well. Therefore, one should not choose a conversion ratio based only in diminishing the semiconductors current efforts in the inverter stage. The conversion ratio must respect all the components current efforts.

VI. DESIGN METHODOLOGY

The proposed design methodology starts with the determination of the transformer conversion ratio from the following specifications: V_{imax}, V_{imin}, V_o, f_r, f_s, S_o, F_c and the output voltage ripple. The latter parameter is directly related to the output voltage THD. Its value should be less than 1% of V_o. The di/dt maximum values of the load are calculated from expressions developed previously, where [9] was used as a start point. A graph similar to Fig. 6 can thus be plotted and a coherent conversion ratio be chosen based on the semiconductors and the filter capacitor current efforts.

The expression (9) or (10) is then employed to find the filter inductance current ripple value. This value ought to be suitable for a high frequency inductor project. The filter inductance value is then calculated from (3). Equation (7) is utilized to find the filter capacitance value.

Once all parameters have been determined, the voltage and current controllers' project can be carried out. The voltage loop control project can be entirely performed using the traditional Bode Diagram Method and a conventional PID controller. The only restriction to determine the current loop compensator is that an integrator must be present in order to guarantee no core saturation under voltage disturbance steps in the voltage reference and in the primary winding voltage.

VII. SIMULATION RESULTS

The simulation is performed on a 1kVA inverter designed with the proposed methodology. In order to effectively test the methodology the inverter is simulated using five distinct transformer conversion ratios and thus five sets of filter components. The specifications as well as the results obtained with the methodology are presented in Table II and III, respectively. The results are approximated and recalculated with the purpose of finding commercial filter capacitance values.

TABLE II
Project Specifications

V_{imax}	V_{imin}	V_o	S_o
160 V	160 V	127 V	1025 VA
F_c	f_r	f_s	ΔV_{Cfmax}
3.54	60 Hz	20 kHz	100 mV

TABLE III
Methodology Results

n	1.6	1.8	2	2.2	2.4
i_{priRMS}	13.28 A	14.76 A	16.32 A	17.87 A	19.45 A
i_{CfRMS}	1.93 A	1.45 A	1.21 A	0.97 A	0.73 A
Δi_{Lfmax}	1.33 A	0.98 A	0.8 A	0.68 A	0.58 A
C_f	40 uF	30 uF	25 uF	20 uF	15 uF
L_f	1.2 mH	1.8 mH	2.4 mH	3 mH	3.65 mH
ΔV_{Cfmax}	104 mV	77 mV	62 mV	53 mV	45 mV

The inverter output voltage and the filter inductor current waveforms are shown in Fig. 7. Fig. 8 shows the control signal and Fig. 9 shows the filter capacitor current waveform. The output voltage THD is 1.041%. The conversion ratio used in these graphs is 1.6.

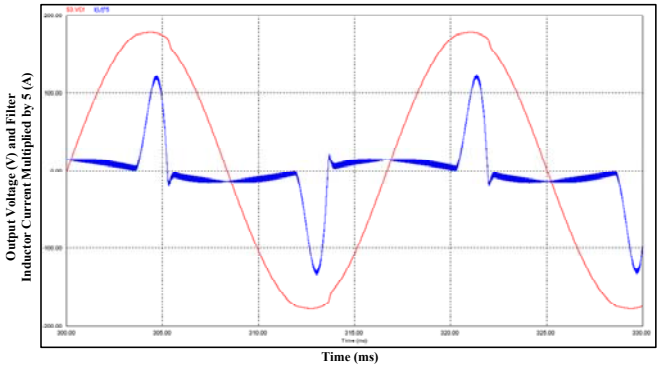

Fig. 7 – V_o and i_{Lf} as a function of time.

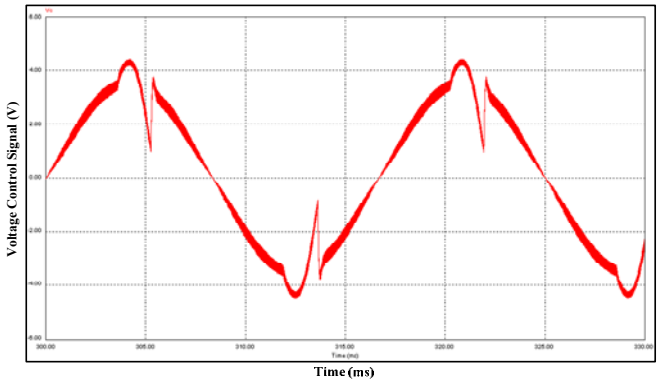

Fig. 8 – Voltage control signal as a function of time.

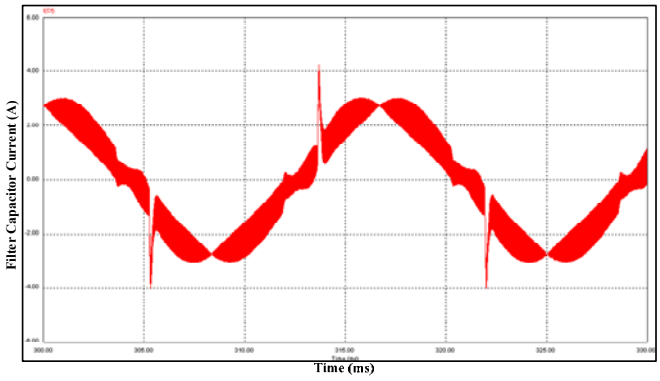

Fig. 9 – Filter capacitor current as a function of time.

The distortion which can be seen at the output voltage waveform can be explained. It can be noticed that a short period of time before the inductor current reaches zero there is a very high di/dt, which causes a high voltage drop over the filter inductor. In order to maintain the output voltage shape, the duty cycle is decreased by the compensator to very low values and can even invert, as can be seen in Fig. 8. So when the current extinguishes the voltage drop over the inductor is zero, as there is no di/dt, and thus the compensator must recover its nominal duty cycle in a short period of time. As more time the controller takes to recover more the capacitor voltage will discharge. It is obvious that with a larger capacitance or a higher switching frequency this effect will probably disappear. If it is not possible to do such a change in the system, another control loop can be implemented [11][12].

VIII. EXPERIMENTAL RESULTS

As it was done in the simulation, five distinct conversion ratios were implemented in lab. The waveforms for n = 1.6 are presented in Fig. 10, Fig. 11 and Fig. 12.

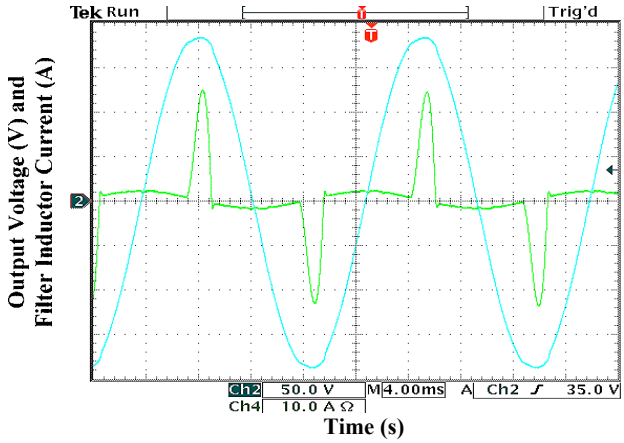

Fig. 10 – V_o and i_{Lf} as a function of time.

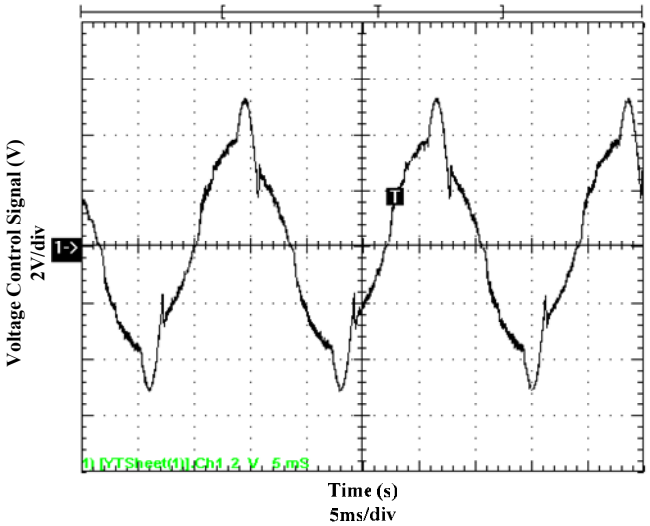

Fig. 11 – Voltage control signal as a function of time.

A harmonic analysis of the output voltage takes place in Fig. 13. The output voltage THD is 1.081%.

Table IV shows RMS filter capacitor currents values obtained in the methodology, in the simulation and in the experiment (in Amperes).

It can be seen that all experimental waveforms as well as the output voltage THD are very close to those obtained from simulation. Moreover, the current values displayed in Table IV show that the simplification when considering the high frequency output voltage ripple waveform as a sinusoidal wave operating at twice the switching frequency was successfully adopted.

TABLE IV
RMS Filter Capacitor Currents Values

n	1.6	1.8	2	2.2	2.4
Methodology	1,93	1,45	1,21	0,97	0,73
Simulation	1,93	1,48	1,21	0,99	0,76
Experiment	1,99	1,4	1,24	0,99	0,77

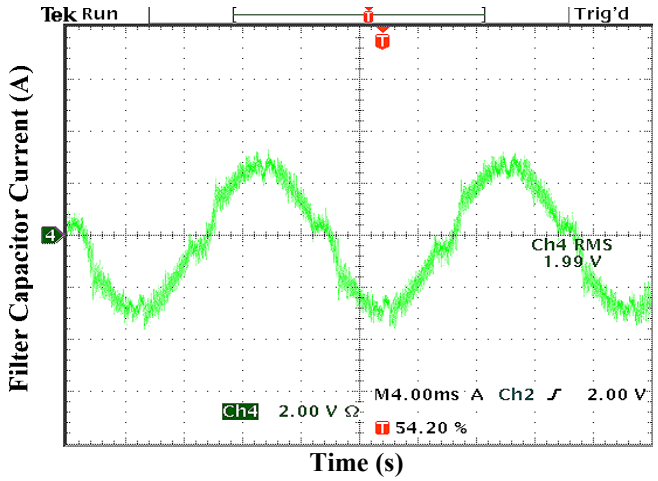

Fig. 12 – Filter capacitor current as a function of time.

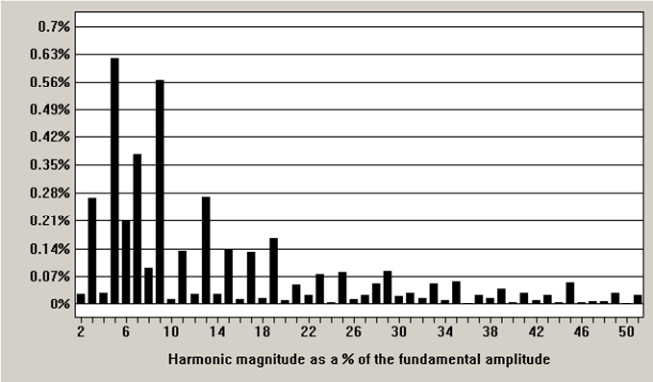

Fig. 13 – Harmonic analysis of the output voltage.

IX. CONCLUSION

The main positive point of this methodology is that it takes advantage of the interaction between the filter and the transformer to find the parameters such that current efforts are always the lowest for each conversion ratio. Moreover, these current efforts can be seen before the choice of the conversion ratio is taken.

In addition, one can use the transformer dispersion to substitute entirely L_f, if the relation *n x dispersion* is known. This could be the best project, but it depends on transformer manufacturer's technical information.

Another important point is that the methodology can only be used if the load characteristics are known. It depends strongly on the rise and fall maximum di/dt values. Those values are proportional to the crest-factor. If the crest-factor of a load is not known, one should determine a maximum allowable crest-factor and then carry out the methodology. A distortion in the output voltage will be found if the crest-factor is sub estimated.

The inverter output voltage presents a high quality waveform where the THD was approximately 1%, although the voltage compensator is just a conventional and well known PID controller designed by Bode Diagram Method. The current loop controller is also determined directly by Bode Diagram and avoids successfully the core saturation.

By comparing the methodology results with all simulation and experimental results the methodology is successfully verified.

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