DESIGN ORIENTED ANALYSIS OF THE DIGITALLY CONTROLLED DC TO DC INTERLEAVED ZCS – FM BOOST CONVERTER USING A FPGA DEVICE

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***Abstract* – A two-cells interleaved DC to DC boost converter employing a soft-switching technique and controlled by Field Programmable Gate Array (FPGA) is presented in this paper. Zero-current-switching (ZCS) cells are used to provide conditions for non-dissipative commutations during the switches' and boost diodes' turn-on and turn-off. The ZCS cells operate at the boundary of continuous and discontinuous modes, designated as critical conduction mode, eliminating the disadvantages related to reverse recovery effects of boost diodes operated in continuous conduction mode, namely: additional losses, and electromagnetic interference (EMI) problems. Furthermore, the interleaving technique is applied in a cellular conversion approach leading to reduced ripple in the input and output waveforms. The digital controller has been developed using a hardware description language (VHDL) and implemented using a XC2S200E-SpartanII-E/Xilinx FPGA. The converter and its topological stages are discussed and analyzed, with the complete description of the control technique. The feasibility of the converter is confirmed by experimental results obtained from a prototype with two interleaved cells, rated at 1kW, 400V output voltage and 220V input voltage.**

***Keywords* - Boost ZCS-FM, critical conduction mode, FPGA control and interleaved techniques.**

I. INTRODUCTION

Basically, the operation modes of DC to DC boost converters can be divided in two types, called continuous mode and discontinuous mode, according to the condition of the boost inductor current. However, if the condition of the current through inductor is at the boundary of continuous and discontinuous mode, a particular operation mode is derived and designated as critical conduction mode [1].

In the critical conduction mode, the main switch is immediately turned on when the inductor current reaches the zero value. Consequently, the boost diode is blocked under the same conditions, leading to minimization in the related reverse recovery losses, due to reduced charge stored in its intrinsic junction capacitance. This control scheme also results in variable switching frequency, increasing the difficulty in the design of electromagnetic interference input filters. Thereby, the critical conduction mode is generally recommended for low-power applications, because of the peak currents through the inductor and the switch [2, 3].

One approach to increase the capability of power processing is to construct a large power converter system using cellular architecture. In this approach, power cells are paralleled to create a single large converter. One of the most fundamental system aspects is the current distribution among each power cell. In practice, the switching cell may not have identical characteristics and their current rating may not be exactly the same. Thus, it is necessary to ensure that the individual interleaved switching cells equally share the load current. Particularly, the balance in the current sharing among the switching cells can be naturally achieved in the critical conduction mode, because mismatch errors between inductor currents are not accumulated [4, 5].

Additionally, in a system of parallel connected switching cells, such as interleaved converters, the output power is distributed among the cells, so that "low-stress" devices (low breakdown voltage and/or low forward current) can be used to achieve a cost effective design with a reduction in the system's size and weight.

Moreover, the employment of interleaved techniques becomes especially appropriate in DC to DC boost converters operating in critical conduction mode, because they minimize the need for voluminous input filters due to the elimination of the pulsating nature of the input current, present in single structures. In this way, the levels of EMI can be drastically reduced [6-8].

Several low cost commercial integrated circuits are available for implementation of the boundary control mode in a single boost converter. However, there is no available IC capable to provide the ideal operating phase shift among the cells, required by interleaved technique, together with critical conduction mode in the cells. Usually, due to inherent variable switching period, the solution for the determination of the ideal phase-shift lead to a relatively complex analog control circuit [8]. In this context, a digital control can easily incorporate this task by monitoring the switching periods to perform the interleaved technique.

A digital control based on programmable logic devices, such as FPGAs, can use the recent advances in digital design methodologies, where hardware description language (VHDL) allows the descriptions of digital systems using their behavior models [9,10].

Therefore, this paper presents a complete analysis and description of a digital control technique using a FPGA device and VHDL language, applied to a DC to DC interleaved ZCS-FM boost converter.

II. THE DC TO DC INTERLEAVED ZCS-FM BOOST CONVERTER

The proposed DC to DC interleaved ZCS-FM boost converter is shown in Fig. 1.

The analysis of this structure is developed assuming some simplifying conditions, such as: all components are ideal; the output voltage (V_o) is constant and the converter's cells have the same parameters.

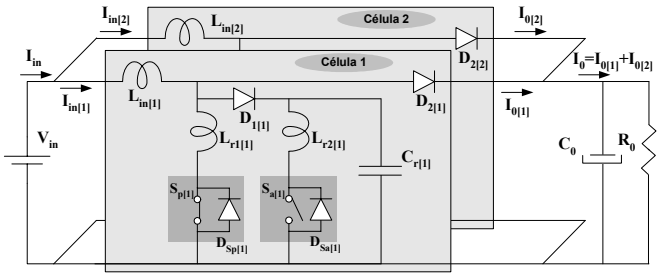
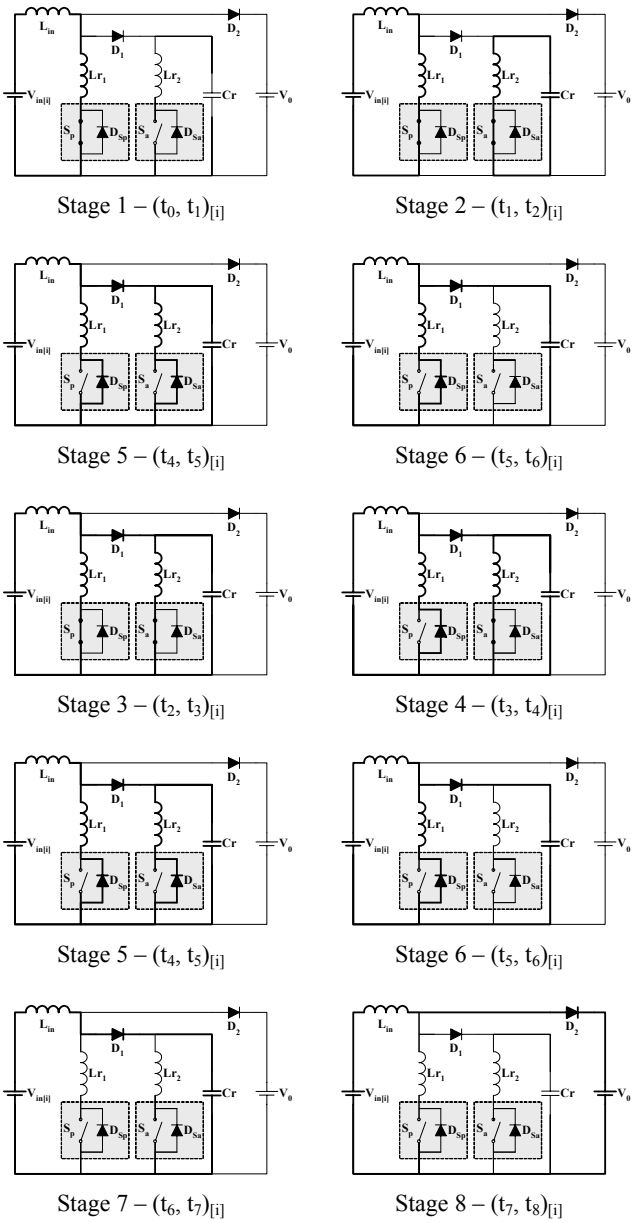


Fig.1 - DC to DC Interleaved ZCS-FM Boost converter with two cells.



Stage 1 – $(t_0, t_1)_{[i]}$ Stage 2 – $(t_1, t_2)_{[i]}$

Stage 3 – $(t_2, t_3)_{[i]}$ Stage 4 – $(t_3, t_4)_{[i]}$

Stage 5 – $(t_4, t_5)_{[i]}$ Stage 6 – $(t_5, t_6)_{[i]}$

Stage 5 – $(t_4, t_5)_{[i]}$ Stage 6 – $(t_5, t_6)_{[i]}$

Stage 7 – $(t_6, t_7)_{[i]}$ Stage 8 – $(t_7, t_8)_{[i]}$

Fig.2 - Topological stages for a generic cell of DC to DC ZCS-FM boost in the critical conduction mode, during a generic switching period $_{[i]}$.

Therefore, in steady state, during a generic switching period, the circuit of one generic cell goes through the eight topological stages showed in Fig. 2, while the main ideal waveforms are shown in Figs. 3 and 4.

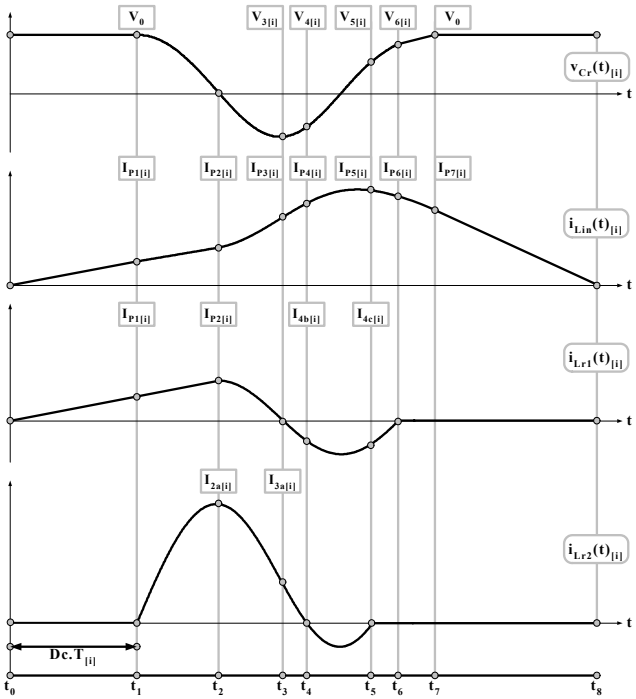


Fig.3- Main ideal waveforms for a generic cell of DC to DC ZCS-FM boost in the critical conduction mode, during a generic switching period$_{[i]}$.

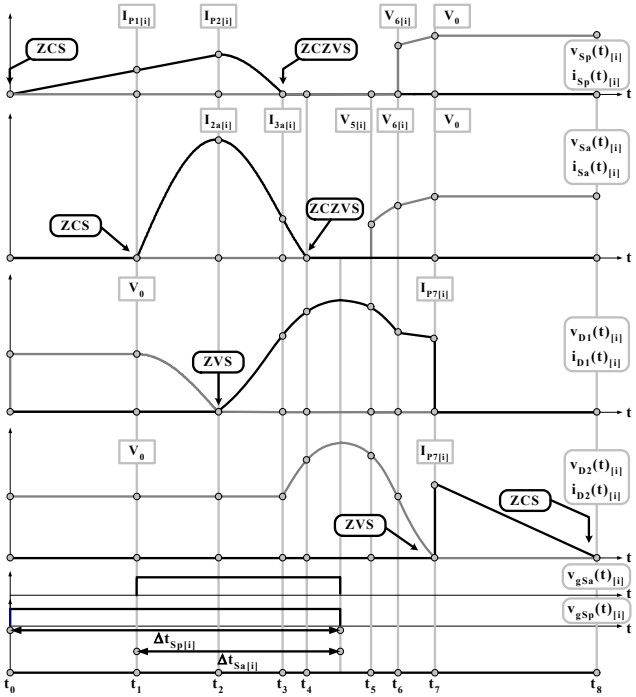


Fig.4- Stresses waveforms in semiconductors for a generic cell of DC to DC ZCS-FM boost in the critical conduction mode, during a generic switching period$_{[i]}$.

The topological stages are briefly described as follows:

First Stage $(t_0, t_1)_{[i]}$ – The main switch S_p turns on under zero current (ZCS). The current through boost inductor (L_{in}) rises linearly, starting from zero, as a function of input voltage and L_{r1} resonant inductance, while the resonant capacitor voltage $v_{Cr}(t)_{[i]}$ is kept constant and equal to V_0 (output voltage).

The time interval of this topological stage is correspondent to the main switch on time. It should be noticed that the non-dissipative commutation provided to the main switch turn-on is also sustained regarding the critical conduction mode.

Second Stage (t_1, t_2)$_{[i]}$ – This stage begins when the auxiliary switch S_a is turned on under zero current (ZCS). The current through L_{in} and L_{r1} remains rising in a linear rate until the instant when the voltage $v_{Cr}(t)_{[i]}$ reaches zero, providing zero-voltage turn-on (ZVS) for the diode D_1.

Third Stage (t_2, t_3)$_{[i]}$ - When the diode D_1 is turned on, a resonance stage starts due to the link between two circuits that were working apart in the previous stage. The currents through the resonant inductors L_{r1} and L_{r2} decrease in a resonant way until the current $i_{Lr1}(t)_{[i]}$ reaches zero. Moreover, the voltage across the resonant capacitor increases in a resonant way, but with negative polarity course.

Fourth Stage (t_3, t_4)$_{[i]}$ – This stage begins when D_{Sp}, co-packed antiparallel diode of S_p, turns on and it finishes when the current flowing trough L_{r2} reaches to zero, providing the turn-on of diode D_{Sa}, co-packed antiparallel diode of S_a.

Fifth Stage (t_4, t_5)$_{[i]}$ – In this time interval, S_p and S_a can be turned off, simultaneously, in an especial non-dissipative condition with zero-current and zero-voltage (ZCZV). The end of this stage occurs when the current through L_{r2} reaches zero again, providing the turn-off of D_{Sa}.

Sixth Stage (t_5, t_6)$_{[i]}$ - The turn-off of D_{Sa} is responsible for removing the auxiliary branch of the commutation cell (switch S_a and resonant inductance L_{r2}). The current $i_{Lin}(t)_{[i]}$ and the voltage $v_{Cr}(t)_{[i]}$ evolve in a resonant way until the current through L_{r1} reaches zero, providing the turn off of the D_{Sp}.

Seventh Stage (t_6, t_7)$_{[i]}$ – In this stage, the voltage $v_{Cr}(t)_{[i]}$ evolves, reaching the output voltage value, in $t=t_7$. At this moment, the boost diode D_2 is turned on under ZVS and D_1 is consequently turned-off.

Eighth Stage (t_7, t_8)$_{[i]}$ – During this stage, D_2 is responsible for transferring energy to the load. The current $i_{Lin}(t)_{[i]}$ decreases in a linear way with a soft slope, while the voltage $v_{Cr}(t)_{[i]}$ is kept with the constant value of V_0. The end of this stage occurs when $i_{Lin}(t)_{[i]}$ arrives to zero, providing the turn-off of D_2 with reduced charge stored in its intrinsic junction capacitance, minimizing the reverse recovery effects.

In order to achieve soft-commutation at zero current for both active switches (S_p and S_a) as described before, some constraints must be satisfied. Basically, it is necessary to guarantee that the current through L_{r1} will reaches zero before the current through L_{r2}.

III. DIGITAL CONTROL STRATEGY

The control method used in the proposed converter is based on keeping a constant on time for the gate signal of the main switch of each cell, providing them a variable off time, which means that the converter operates with variable switching frequency. One of the ZCS boost cells is adopted as reference for the phase shifting required in the interleaved technique.

It is reasonable to consider that the cells' switching period is almost constant for previous and forward switching periods. So, in order to determine the ideal phase-shift instant regarding the reference cell, information from its previous switching period is used. Particularly, the digital control monitors the rise edge of the gate signal from the main switch of the reference cell.

Additionally, in order to derive the small-signal average model of a converter using a state-space technique, the time averaged values of inductor currents and capacitor voltages are chosen as state variables, while the input voltage and output current are assigned as input variables, and input current and output voltage as output variables.

It should be emphasized that the control variable in this case due to the variable-frequency operation is the switch on-time t_{on} in voltage mode control instead of duty cycle.

The digital controller has been implemented using a Field Programmable Gate Array (FPGA) and the control algorithm has been developed using a hardware description language VHDL. The FPGA device employed was XC2S200E-pq208-6C by XILINX and mounted in a prototype board D2E by DIGILENT INC. Figure 5 shows the control algorithm developed using VHDL.

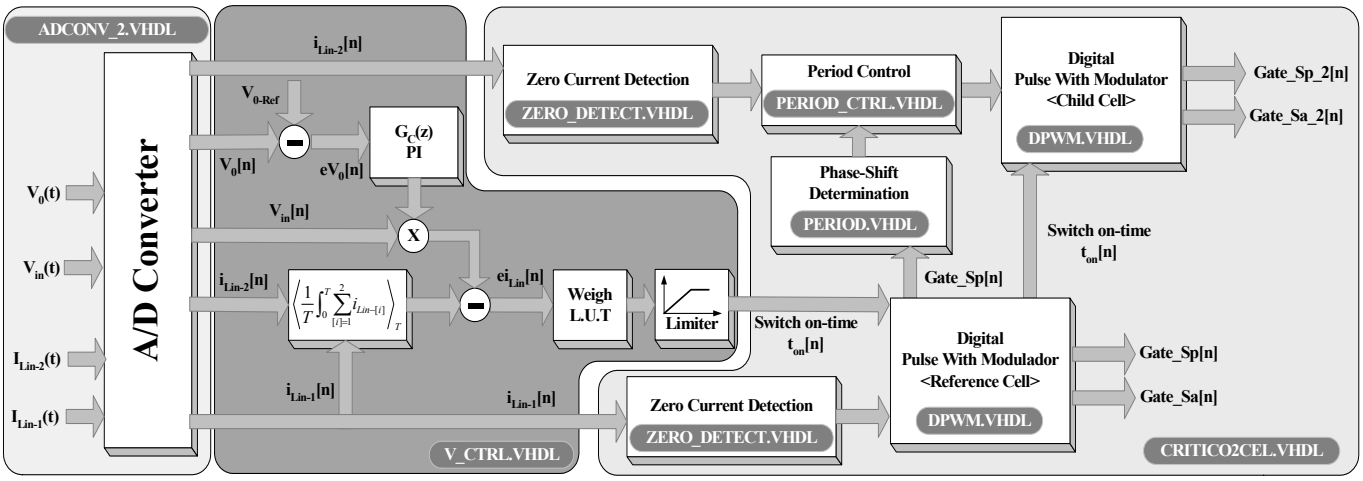


Figure 5 – Block diagram of the control algorithm.

The voltage control compensator is a PI type, and can be expressed as (1) in discrete time domain.

$$g_{PI}(z) = \frac{U(z)}{X(z)} = \frac{A_0 z + A_1}{Z - 1} \quad (1)$$

Where:

$$u_N = A_0 x_N + A_1 x_{N-1} + u_{N-1} \quad (2)$$

The transfer function of the equivalent analog controller is

$$g_{PI}(s) = \frac{U(s)}{X(s)} = K_{PI}\left(1 - \frac{1}{s\tau_{PI}}\right) \quad (3)$$

Using the Tustin rule (4), the parameters of the digital controller A_0 and A_1 can be linked to the parameters of the analog equivalent K_{PI} and τ_{PI}., as equations listed in 5.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \quad (4)$$

$$A_0 = K_{PI}\left(\frac{1}{2}\frac{T_S}{\tau_{PI}} + 1\right) \qquad A_1 = K_{PI}\left(\frac{1}{2}\frac{T_S}{\tau_{PI}} - 1\right) \quad (5)$$

The output voltage controller acts on the input conductance to keep the input and output power balanced, resulting in a constant output voltage.

IV. EXPERIMENTAL RESULTS

The proposed converter presented in Fig. 1 has been tested using an experimental prototype. The circuit parameters utilized are described in table I. These values are based on design methodology previously presented in [11].

The experimental results are depicted in the Figs. 6 to 9. The commutation details for the main and auxiliary switches in each cell are shown in the Figs. 6 and 7. The turn on commutations of the main switches occur naturally with zero current conditions in each cell, due to the critical conduction mode.

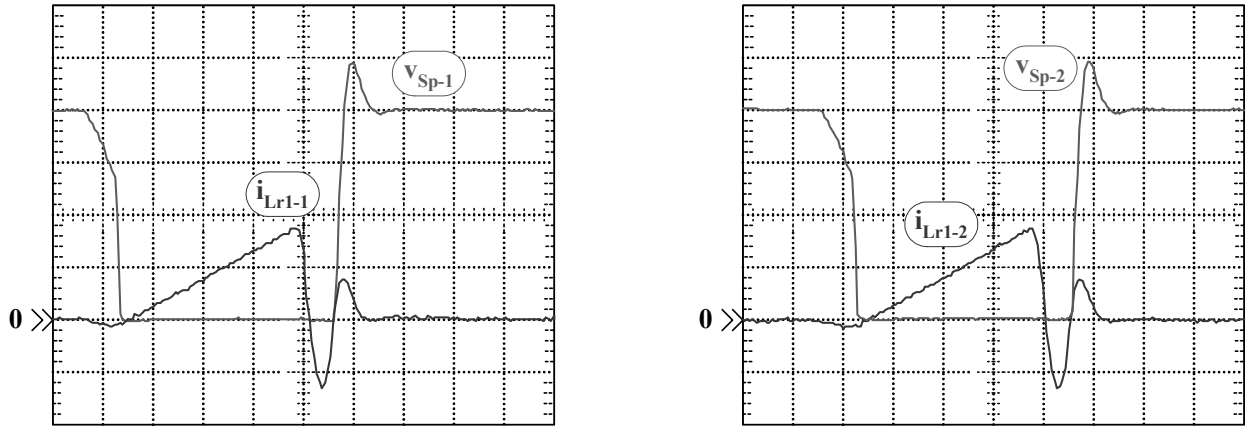
Furthermore, the main switches also have their turn off commutations under non-dissipative conditions (ZCZVS), provided by the proposed ZCS switching cell.

TABLE I -
CONVERTER PARAMETERS

Input and Output Requirements	
Parameter	**Value**
V_{in}	220 V
V_O	400 V
P_O	1 kW
$f_{s[Quiescent\ Point]}$	50 kHz
Number of Cells (N)	2
Phase-Shift [rad]	π/2

Where: [i] is the number of ZCS boost cell;

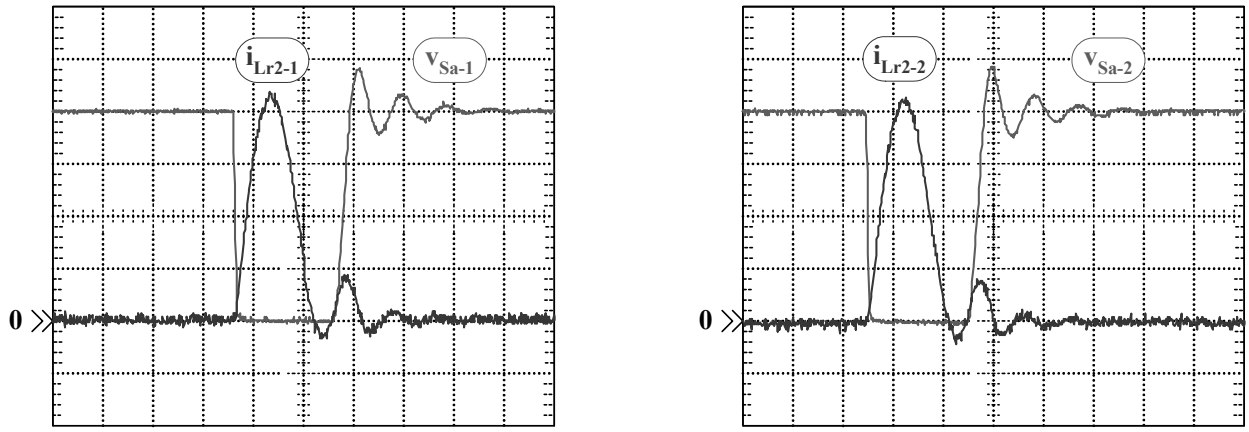
Circuit Parameters	
Parameter	**Value**
S_{P1-i}	HGTP12N60A4D
S_{A1-i}	HGTP7N60A4D
D_{1-i}	RHRP860
D_{2-i}	RHRP8100
L_{in-i}	428.5µH (Litz: 7 x 26 AWG)
L_{r1-i}	28.6µH (Litz: 5 x 26 AWG)
L_{r2-i}	20.0µH (Litz: 5 x 26 AWG)
C_{r-i}	10.0nF
Co	390.0µF



(a) Cell 1 (b) Cell 2

i_{Lr1-i}: 2 A/div; v_{Sp-i}: 100 V/div; 2 µs/div

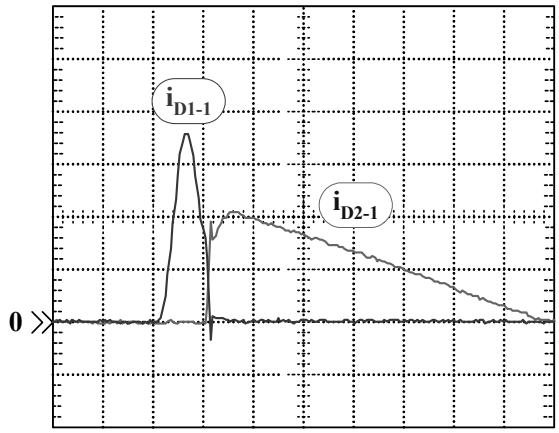
Fig. 6 - Commutation details, voltage and current through the main switches Sp in the ZCS boost cells 1 and 2, at full load.



(a) Cell 1 (b) Cell 2

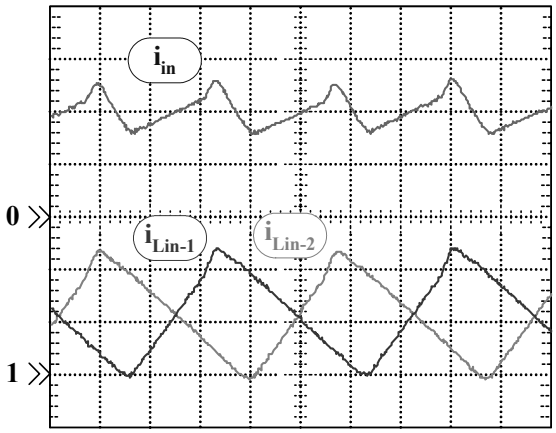
i_{Lr2-i}: 2 A/div; v_{Sa-i}: 100 V/div; 1 μs/div

Fig. 7 - Commutation details, voltage and current through auxiliary switches Sa in the ZCS boost cells 1 and 2, at full load.



i_{D1-1} e i_{D2-1}: 2 A/div; 2 μs/div

Fig. 8 - Details of currents through the diodes D_{1-1} e D_{2-1} in the ZCS boost cell 1 (reference).



i_{Lin-1}, i_{Lin-2} e i_{in}: 2A/div e 5μs/div

Fig. 9 - Input current i_{in}, and the currents through the boost inductors in each cell, for some switching periods.

The currents through diodes D_1 and D_2 are shown in the Fig.8, for cell 1, and full load. It can be observed that D_1 and D_2 do not conduct together, and only D_2 performs the transference of energy from the input to the load. The current through D_2 decrease with a soft slope until reaches zero, minimizing its reverse recovery effects.

Figure 9 shows the input current and the currents through the boost inductors in each cell. One can observe that the interleaved technique eliminates the discontinuity in the input current.

V. CONCLUSION

In this paper, a DC to DC interleaved boost topology operating in critical conduction mode was investigated, using a non dissipative commutation cell. The control logic has been implemented using a programmable logic device FPGA and hardware description language VHDL.

Considering the fact that all commutations are soft-switched and the reverse recovery effects related to boost diodes were minimized, this converter may allow the reduction of the electromagnetic interference. Due to interleaved technique, the converter's features include the minimization of input and output current ripple, the reduction of the output voltage ripple and consequently the related filters, due to increase in the ripple frequency.

The cellular architecture also permits the employment of "low-stress" devices, once the required current ratings are only a fraction of the current through the switch of a conventional boost converter.

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