REDUCED SWITCH COUNT UNIVERSAL POWER FILTER

C. B. Jacobina, R. R. Matias, I. S. Freitas, A. C. Oliveira, A. M. N. Lima and E. R. C. da Silva
LEIAM - Dep. de Eng. Elétrica - CCT - UFCG - Caixa Postal 10.105
58109-970 Campina Grande, PB - Brasil
E-mails: [jacobina,rafael,isaacfreitas,aco,amnlima,edison]@dee.ufcg.edu.br

Abstract: **This paper proposes a three-phase universal power filter with a reduced number of switches. Such a topology uses only ten switches. The topology and its operating principles are presented. A suitable control strategy is proposed to improve the use of the topology. Simulation and experimental results are presented.**

Keywords **– Universal power filter, reduced switch count**

I. INTRODUCTION

The strict regulations about the flow of electrical energy has stimulated the use active power compensation schemes [1, 11]. The active power compensation is normally achieved with the help of switching converters connected as an active filter to the load and the grid. A universal power filter provides simultaneously voltage and power factor control. One series-active filter may eliminate voltage disturbances, such as sag, notch, flicker and imbalance. That is, the series-active filter is responsible by voltage regulation and voltage harmonic compensation. The purpose of a shunt-active filter is to absorb current harmonics, compensate for reactive power and negative sequence current, and regulate the *dc*-bus voltage between both active filters. That is, a shunt-active filter is responsible for controlling the power factor, harmonic compensation and dc-bus voltage regulation.

The study of topologies with a reduced number of switches is an important topic in power electronics since it may provide alternative solutions to reduce the cost of the energy conversion process still preserving power quality. In the recent years, several research groups have been investigating such topic [2, 4, 5, 7, 9].

This paper proposes a three-phase universal power filter with a reduced number of switch. Such a topology uses only ten switches, while the standard topology (six-leg converter) uses twelve-switches [8]. The topology proposed and its operating principles are presented. Particularly, a suitable control strategy is proposed to improve the use of the topology. Experimental results are presented.

II. CONVERTER VOLTAGES

Fig. 1 shows the system configuration. The converter topology is composed by the converter G and converter L. Converter G is composed by switches q_{g1}, $\overline{q}_{g1}$, q_{g2}, $\overline{q}_{g2}$, q_3 and $\overline{q}_3$. Converter L is composed by switches q_{l1}, $\overline{q}_{l1}$, q_{l2}, $\overline{q}_{l2}$, q_3 and $\overline{q}_3$. The leg constituted by q_3 and $\overline{q}_3$ is shared by both series and shunt converters. The switch pairs $q_{g1}-\overline{q}_{g1}$, $q_{g2}-\overline{q}_{g2}$, $q_{l1}-\overline{q}_{l1}$, $q_{l2}-\overline{q}_{l2}$ and $q_3-\overline{q}_3$ are complementary. The conduction state of all switches can be represented by an homonymous binary variable q_{g1}, $\overline{q}_{g1}$, q_{g2}, $\overline{q}_{g2}$, q_{l1}, $\overline{q}_{l1}$, q_{l2}, $\overline{q}_{l2}$, q_3 and $\overline{q}_3$, where $q=1$ indicates a closed switch, while $q=0$ indicates an open one.

The voltages delivered by the converter are the grid voltages (v_{g1}, v_{g2} and v_{g3}, among points $g1$, $g2$, 3 and n, respectively) and the load voltages (v_{l1}, v_{l2} and v_{l3}, among $l1$, $l2$, 3 and m, respectively). These voltages depend on the conduction states of the power switches and may be expressed in terms of the previously defined binary variables q_{g1}, q_{g2}, q_3, q_{l1} and q_{l2} as

$$v_{g1} = v_{g10}-v_{n0} = (2q_{g1}-1)\frac{E}{2}-v_{n0} \quad (1)$$

$$v_{g2} = v_{g20}-v_{n0} = (2q_{g2}-1)\frac{E}{2}-v_{n0} \quad (2)$$

$$v_{g3} = v_{g30}-v_{n0} = (2q_{3}-1)\frac{E}{2}-v_{n0} \quad (3)$$

$$v_{l1} = v_{l10}-v_{m0} = (2q_{l1}-1)\frac{E}{2}-v_{m0} \quad (4)$$

$$v_{l2} = v_{l20}-v_{m0} = (2q_{l2}-1)\frac{E}{2}-v_{m0} \quad (5)$$

$$v_{l3} = v_{l30}-v_{m0} = (2q_{3}-1)\frac{E}{2}-v_{m0} \quad (6)$$

where E ($E=v_c$) is the *dc*-bus voltage, v_{g10}, v_{g20}, v_{g30} and v_{l10}, v_{l20}, v_{l30} are the grid and load voltages, respectively, referred to the *dc*-bus mid-point ($'0'$), and v_{n0} and v_{m0} are the voltages of points n and m referred to the *dc*-bus mid-point. Note that

$$v_{g30} = v_{l30} = v_{30}.$$

III. *PWM* CONTROL

Pulse-width modulation can be determined directly from the grid and load voltages referred to the *dc*-bus mid-point, which in turn are defined from the desired reference phase voltages for the grid and load. If the desired reference voltages are given by v^*_{g1}, v^*_{g2}, v^*_{g3}, v^*_{l1}, v^*_{l2} and v^*_{l3}, then the voltages referred to the mid-point $'0'$ can be expressed by

$$v^*_{g10} = v^*_{g1}+v^*_{n0} \quad (7)$$

$$v^*_{g20} = v^*_{g2}+v^*_{n0} \quad (8)$$

$$v^*_{g30} = v^*_{g3}+v^*_{n0} \quad (9)$$

$$v^*_{l10} = v^*_{l1}+v^*_{m0} \quad (10)$$

$$v^*_{l20} = v^*_{l2}+v^*_{m0} \quad (11)$$

$$v^*_{l30} = v^*_{l3}+v^*_{m0} \quad (12)$$

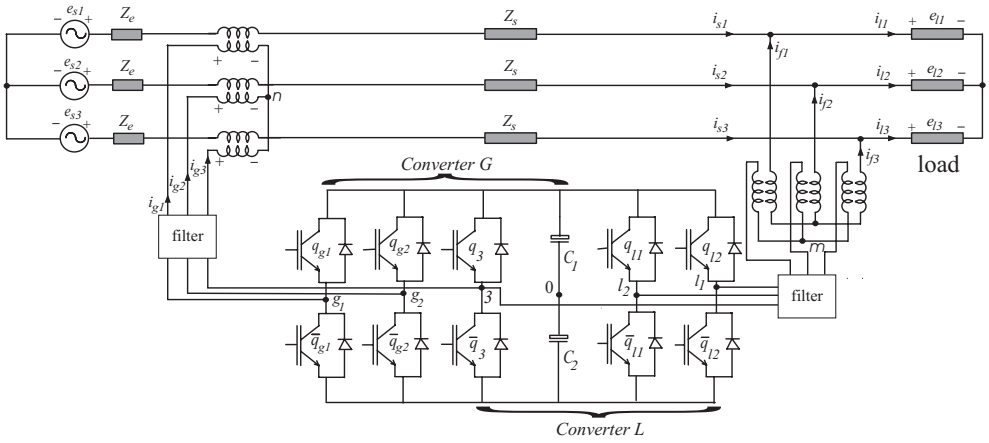


Figura 1 Three-phase universal power filter system.

By using equation (9) and (12) and considering that for the shared leg $v^*_{g30} = v^*_{l30} = v^*_{30}$ we obtain

$$v^*_{m0} = v^*_{gl} + v^*_{n0} \tag{13}$$

where $v^*_{gl} = v^*_{g3} - v^*_{l3}$. This equation shows that v^*_{n0} and v^*_{m0} cannot be defined independently. For example, if v^*_{n0} is chosen, then v^*_{m0} is automatically defined since v^*_{gl} is given.

By placing (13) into (10) and (11), the reference mid-point voltages become

$$v^*_{g10} = v^*_{g1} + v^*_{n0} \tag{14}$$
$$v^*_{g20} = v^*_{g2} + v^*_{n0} \tag{15}$$
$$v^*_{30} = v^*_{g3} + v^*_{n0} \tag{16}$$
$$v^*_{l10} = v^*_{l1} + v^*_{gl} + v^*_{n0} \tag{17}$$
$$v^*_{l20} = v^*_{l2} + v^*_{gl} + v^*_{n0} \tag{18}$$

Now the set of reference voltages is composed by v^*_{g1}, v^*_{g2}, v^*_{g3}, $v^*_{l1} + v^*_{gl}$ and $v^*_{l2} + v^*_{gl}$. The difference between these voltages is restricted to the interval $[-E, E]$.

In the following, two techniques will be presented for generating the PWM gating signals for the converters.

Method A (global apportioning factor)

The voltage v^*_{n0} can be calculated based on the global apportioning factor μ, that is

$$v^*_{n0} = E(\mu - \frac{1}{2}) - \mu v^*_{\max} + (\mu - 1)v^*_{\min}. \tag{19}$$

where $v^*_{\max} = \max V$ and $v^*_{\min} = \min V$ where $V = \{v^*_{g1}, v^*_{g2}, v^*_{g3}, v^*_{l1} + v^*_{gl}, v^*_{l2} + v^*_{gl}\}$. This expression was derived by using the same approach as used to obtain the equivalent one for the three-phase PWM modulator [6], [3].

The apportioning factor μ $(0 \le \mu \le 1)$ is given by

$$\mu = t_{oi}/t_o \tag{20}$$

to split the free-wheeling period t_o at the beginning ($t_{oi} = \mu t_o$) and at the end ($t_{oe} = (1 - \mu)t_o$) of the switching period [6], [3]. The apportioning factor can be changed as a function of the modulation index (mi) to reduce the THD (total harmonic distortion) of one of the output voltage [6], [3].

In this case, the proposed algorithm is:

Step 1. Choose the global apportioning factor μ and calculate v^*_{n0} from (19).

Step 2. Determine v^*_{g10}, v^*_{g20}, v^*_{30}, v^*_{l10}, and v^*_{l20} from (14)-(18).

Step 3. Finally, once the mid-point voltage have been determined, calculate the pulse-widths τ_{g1}, τ_{g2}, τ_3, τ_{l1} and τ_{l2} by using

$$\tau_j = \frac{T}{2} + \frac{T}{E}v^*_{j0} \quad \text{for} \quad j = g1, g2, 3, l1, \text{or } l2 \tag{21}$$

and programmable timers.

Method B (local apportioning factor)

The voltage v^*_{n0} can be calculated based on the local apportioning factor μ_s for the grid $(s = g)$ or load side $(s = l)$, that is

$$v^*_{n0} = E(\mu_s - \frac{1}{2}) - \mu_s v^*_{s\max} + (\mu_s - 1)v^*_{s\min}. \tag{22}$$

where $v^*_{s\max} = \max V_g$ and $v^*_{s\min} = \min V_g$ if $s = g$ or $v^*_{s\max} = \max V_l$ and $v^*_{s\min} = \min V_l$ if $s = l$., where $V_g = \{v^*_{g1}, v^*_{g2}, v^*_{g3}\}$ and $V_l = \{v^*_{g3}, v^*_{l1} + v^*_{gl}, v^*_{l2} + v^*_{gl}\}$. Besides (22), the voltage v^*_{n0} must also obey the other converter side (reference load voltages $U_l = \{v^*_{l1} + v^*_{gl}, v^*_{l2} + v^*_{gl}\}$ (if $s = g$) or reference grid voltages $U_g = \{v^*_{g1}, v^*_{g2}\}$ (if $s = l$)). Then, from (17)-(18) and (14)-(15) the limits for v^*_{n0}, for $s = g$ and $s = l$, can be calculated as

$$v^*_{n0\,\max} = E/2 - \max U_l \quad (\text{if } s = g) \tag{23}$$
$$v^*_{n0\,\min} = -E/2 - \min U_l \tag{24}$$

$$v^*_{n0\,\max} = E/2 - \max U_g \quad (\text{if } s = l) \tag{25}$$
$$v^*_{n0\,\min} = -E/2 - \max U_g. \tag{26}$$

In this case, it is possible to control how the harmonic distortion is split between the converters A and B. The proposed algorithm is:

Step 1. Choose the local apportioning factor μ_s so that grid or load converter is optimized and calculate v^*_{n0} from (22).

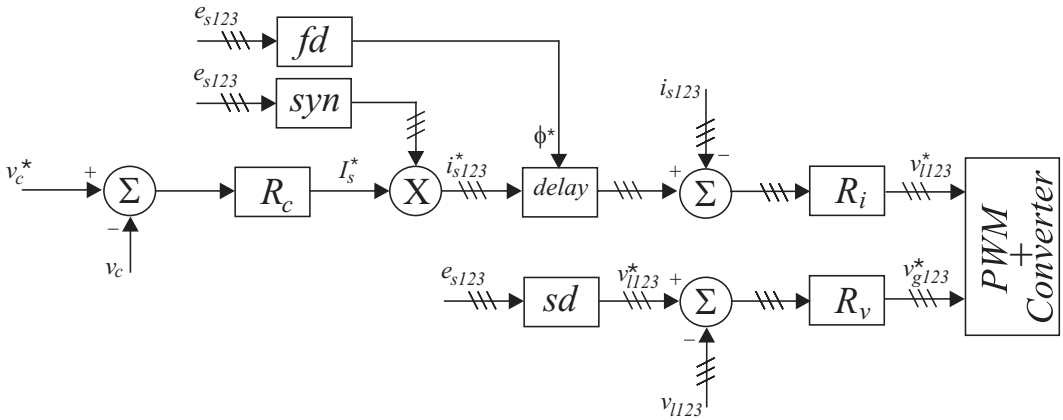


Figura 2 Control block diagram of the system.

Step 2. Determine the v_{n0}^* limits $v_{n0\,\max}^*$ and $v_{n0\,\min}^*$ from (23) and (24) or (25) and (26). Limit v_{n0}^* to $v_{n0\,\max}^*$ if $v_{n0}^* > v_{n0\,\max}^*$ and v_{n0}^* to $v_{n0\,\min}^*$ if $v_{n0}^* < v_{n0\,\min}^*$.
Step 3. Determine v_{g10}^*, v_{g20}^*, v_{30}^*, v_{l10}^*, and v_{l20}^* from (14)-(18).
Step 4. The same as the Step 3 of the *Method A*.

IV. VOLTAGE ANALYSIS

The maximum three-phase voltage capability for sinusoidal steady-state operation of the G and L converters is obtained when the desired voltage for the shared leg is given by $v_{30}^* = 0$ (i.e., $v_{n0}^* = -v_{g3}^*$). In this case the maximum amplitude of the sinusoidal voltage for each phase voltage is $(E/\sqrt{3})/2$. This corresponds to same voltage capability of the four-leg converter [7,10], while the maximum amplitude for the six-leg converter is $E/\sqrt{3}$.

With the use of the proposed schemes the maximum three-phase voltage capability for sinusoidal steady-state operation of the G and L converters is $V_g + V_l = E/\sqrt{3}$, where V_g is the amplitude of the grid voltage and V_l is the amplitude of the load voltage. That is, we can define the amplitude of grid and load voltage as: $V_g = (1-\delta)E/\sqrt{3}$ and $V_l = \delta E/\sqrt{3}$ where the constant δ is given by $0 < \delta < 1$. We conceive three control modes:

i) mode 0: $(\delta = 1/2)$: $V_g = V_l = (E/\sqrt{3})/2$ that corresponds to $v_{30}^* = 0$.

ii) mode G $(0 < \delta < 1/2)$: i.e., $V_g > V_l$, what increases the voltage capability of Converter G toward to that of the six-leg converter.

iii) mode L $(1/2 < \delta < 0)$: i.e., $V_l > V_g$, what increases the voltage capability of Converter L toward to that of the six-leg converter.

V. OVERALL CONTROL

As discussed in the Section IV, to obtain with the proposed converter the same maximum voltages of the six-leg converter, the *dc*-bus must be doubled. However, the proposed converter allows to split voltage capability and to relax some control objectives which may avoid the need for doubling the dc-bus voltage.

For that, system is designed such that in steady-state the voltages $v_{g1} - v_{g3}$ are small than the voltages $v_{l1} - v_{l3}$. That is, the system operates as in mode L of Section IV, where more voltage is available to the converter L. In this mode the system can compensate the steady-state load voltage imbalance and control the grid current. In the other hand, the compensation for a short time interval of fast variation of $e_{g1} - e_{g3}$, where it is need large values of $v_{g1} - v_{g3}$, can be accomplished with the system operating as in mode G, relaxing the power-factor control provide by converter L (because the available voltages $v_{l1} - v_{l3}$ is reduced).

Fig. 2 presents the control block diagram of the system. The capacitor voltage v_c (*dc*-bus voltage) is adjusted at a reference value by using controller R_c. This controller defines the amplitude I_s^* of all three-phase grid currents. To obtain a unity power factor, the instantaneous reference currents i_{s1}^*, i_{s2}^* and i_{s3}^* (i_{s123}^*) must be synchronized with the voltages e_{s1}, e_{s2} and e_{s3} (e_{s123}). This is obtained by using block *syn*.

The regulation of the voltages is implemented by using the block R_v. The block *sd* detect the positive sequence of the grid voltage. Block R_i implements the current control strategy. The change of the converters mode of operation is done by detecting the fast voltages variation and defining the power factor. That is implemented in block fd.

VI. SIMULATION RESULTS

The system presented in Fig. 1 have been studied by simulation supplying a RL load. In the tests the switching frequency was $10kHz$ and $C = 1000\mu F$.

The simulation results were obtained to study an unbalance transient of grid voltage (e_{s1}, e_{s2}, and e_{s3}). In the test third-order harmonic voltages are added to the grid voltages at $t = 2.6s$. Fig. 3 presents simulations results. The six parts of this figure are: (a) the grid voltages, (b) the grid currents, (c) the load voltages (d) the load currents, (e) the converter grid voltages (after the transformer) and (f) converter currents. The power filter compensates the harmonic voltages and warrant sinusoidal grid currents with power factor close to one.

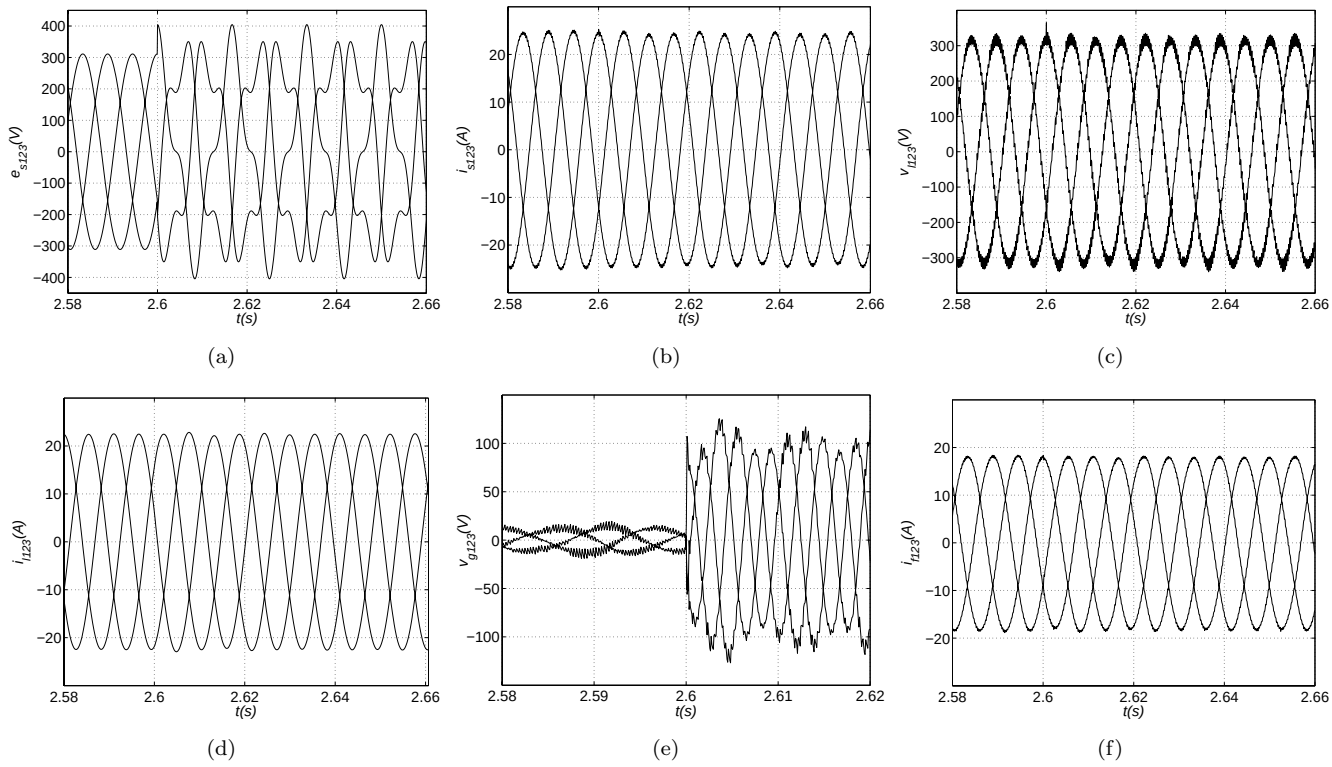


Figura 3 Simulation result: (a) grid voltages, (b) grid currents, (c) load voltages (d) load currents, (e) converter grid voltages and (f) converter currents.

VII. EXPERIMENTAL RESULTS

The set-up used in the experimental tests is based on a microcomputer (PC-Pentium) equipped with appropriate plug-in boards and sensors.

Fig. 4(a)-(c) presents a experimental results (i.e.: $v_s - 3\text{x}i_s$, v_c, i_{l1}) obtained with system operating ac/ac converter in steady-state. The converter L supplys an induction motor with $\omega_s = \omega_l = 120\pi\ rad/s$. The overall control of system is adequate.

VIII. CONCLUSIONS

This paper proposed a three-phase universal power filter with a reduced number of switches. Such a topology uses only ten switches, while the standard topology (six-leg converter) uses twelve-switches [8]. The operating principles are presented. A suitable control strategy are presented to improve the use of the topology. Experimental and simulated results are presented.

ACKNOWLEDGMENT

The authors would like to thank the financial support provided by the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq) of Brazil.

REFERENCES

[1] H. Akagi. Trends in active power line conditioners. *IEEE Trans. Power Electron.*, 9(3):263–268, May 1994.

[2] F. Blaabjerg, S. Freysson, H. H. Hansen, and S. Hansen. Comparison of a space-vector modulation strategy for a three phase standard and a component minimized voltage source inverter. In *Proc. EPE*, pages 1806–1813, Sevilha - Spain, 1995.

[3] V. Blasko. Analysis of a hybrid pwm based on modified space-vector and triangle-comparison methods. *IEEE Trans. Ind. Applicat.*, 33(3):756–764, May/June 1996.

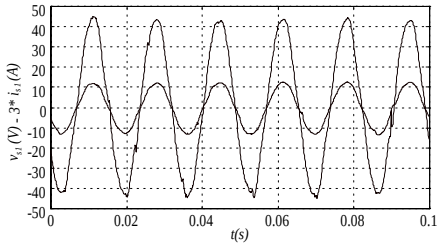
[4] P. Enjeti and A. Rahman. A new single phase to three phase converter with active input current shaping for low cost ac motor drives. In *Conf. Rec. IEEE-IAS Annu. Meeting*, pages 935–939, 1990.

[5] C. B. Jacobina, M. B. R. Correa, E. R. C. da Silva, and A. M. N. Lima. Induction motor drive system for low-power applications. *IEEE Trans. Ind. Applicat.*, 35(5):52–61, Jan./Feb. 1999.

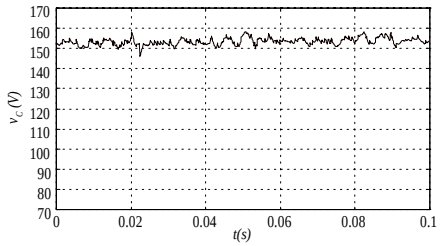
[6] C. B. Jacobina, A. M. N. Lima, E. R. C. da Silva, R. N. C. Alves, and P. F. Seixas. Digital scalar pulse width modulation: a simple approach to introduce non-sinusoidal modulating waveforms. *IEEE Trans. Power Electron.*, 16(3):351–359, May 2001.

[7] G.-T. Kim and T.A. Lipo. Vsi-pwm rectifier/inverter system with a reduced switch count. In *Conf. Rec. IEEE-IAS Annu. Meeting*, pages 2327 – 2332, 1995.

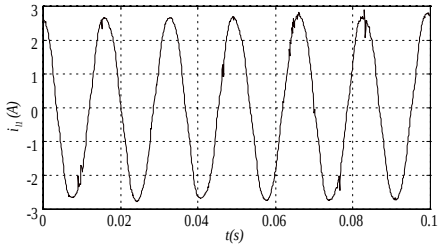
[8] H. Kohlmeier, O. Niermeyer, and D. F. Schroder. Highly dynamic four-quadrant ac motor drive with improved power factor and on-line optimized pulse pattern with promc. *IEEE Trans. Ind. Appl.*,



(a)



(b)



(c)

Figura 4 Experimental result. Voltage and current of the grid (a), capacitor voltage (b) and load current (c).

23(6):1001–1009, Nov./Dec. 1987.

[9] C.-T. Pan and M.-C. Jiang. Control and implementation of three phase voltage-double reversible ac to dc converter. In *Proc. IEEE PESC*, pages 437–443, 1995.

[10] R. L. A. Ribeiro, C. B. Jacobina, E. R. C. da Silva, and A. M. N. Lima. Ac/ac converter with four switch three phase structures. In *Proc. IEEE PESC*, pages 134–139, 1996.

[11] B. Singh, K. Al-Haddad, and A. Chandra. A review of active filters for power quality improvement. *IEEE Trans. Ind. Electron.*, 46(5):960–971, Oct. 1999.