NOVEL SINGLE-STAGE BOOST PFC USING THE THREE-STATE SWITCHING CELL

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***Abstract* —The intention of this work is to introduce and to analyze a new single-phase AC-to-DC PWM converter, with only one stage including rectification and power factor correction, using the three-state switching cell. The advantages of this considered converter using two of the three-state cells to replace the diodes of the bridge, such reduction of conduction losses and the volume and size of the reactive components are demonstrated, instead of the existing configurations. Furthermore it can be used inexpensive semiconductors due to the feature of parallelism of the switching cell. The operation stages for duty-cycle lower and greater than 0.5 is described. To verify theoretical agreement, this paper presents some simulation results and experimental design procedure for a single-stage AC-to-DC converter with 220V of AC input voltage source, 400V of DC output and 1kW of load. The preliminary experimental results are presented too.**

***Keywords* – Boost, PWM, PFC, single stage, power factor three-state.**

I. INTRODUCTION

Nowadays, it is still very common to find switching power supplies that have in the topology a diode rectifier followed by a capacitive filter. This process generates high harmonic content in the input current, resulting in a low power factor (around 0.6).

The increasing diversity of possible applications and the continuous demand for smaller, lighter and more efficient power converters have spurred the interest in fundamental topological properties of PWM networks and the constructions of new converter topologies. In a search for other configurations, elementary converters were modified by various circuit manipulation techniques [1].

To satisfy international standards, like IEC-61.000-3-2, they are required AC-to-DC conversions that present power factor very close to unit. The technique normally used to correct the power factor consists of an input full-bridge diode rectifier, followed by a boost converter, as shown in Fig. l(a). The conduction losses are significant because the current always flows simultaneously through three power semiconductors, two diodes, and other semiconductor that depends on the operation stage (it can be a switch or a diode).

The circuit shown in Fig. 1(b) operates with lower conduction losses [2, 3], because the current always flows simultaneously through two semiconductors, instead of three. It is also noticed that this circuit replaces the pair D1, D3 and D2, D4 for two simple switching cells (two-state), composed by a passive switch (diode) and an active switch (MOSFET). It can be observed, between the a-b terminals have a voltage source (capacitive link - Co) wile in terminal c, is connected a current source (inductive link – L1).

Fig. 2 shows the proposed single stage AC-to-DC converter using the three-state switching cell, named as "cell B", [4-6]. When this proposed converter is compared with the converter of the Fig. 1(b), the following advantages are listed:

- The double of the commutation frequency is applied in the reactive components, resulting lower weight and volume.
- The current through the semiconductors becomes a half for a project rating the same voltage and output power.
- The heat distribution coming from the semiconductors is more uniform and efficient in the heat sink, consequently, the losses are distributed among them.
- Part of the input power is transferred directly to the load (output) through the autotransformers, without being processed by the active switches, thus, both the conduction and switching losses become lower.

Due to the characteristics of parallelism of the three-state switching cell inexpensive devices can be used. Furthermore, this topology is suitable when the process with high power is needed.

II. PRINCIPLE OF OPERATION

The power circuit shown in Fig. 2 is obtained replacing the simple switching cells (two-state), shown in Fig. 1(b), for two three-state switching cells, operating as two boost converters. Each boost converter operates during one semi-cycle of the mains.

Applying the three-state switching cells in the Ac - to- DC converter becomes possible, because in each leg (each cell) has two diodes and two active switches and the switches have a

body diode connected in antiparallel. Thus, the characteristics of the bridge rectification are preserved.

The proposed boost converter operates in continuous conduction mode (CCM) and it is controlled using average current mode technique to achieve PFC. It has two mode of operation with regarding to the duty cycle D. The first mode is to duty cycle lower than 50% (D<0.5) and there are four stages by one switching period. The second mode is to duty cycle greater than 50% (D>0.5) and also occurs four operation stages in a period of switching.

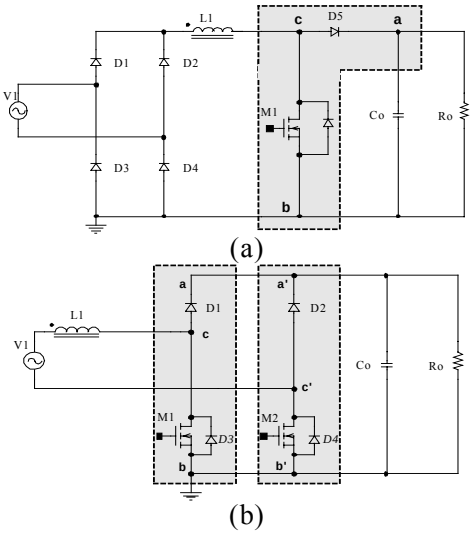

Fig. 1 - (a) Conventional two-stage boost PFC. (b) Single-stage converter with rectification and boost converter using two simple switching cells (two-state).

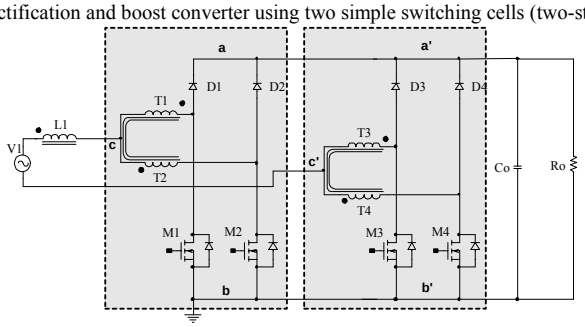

Fig. 2 - Proposed single-stage AC-to-DC boost converter using two three-state switching cells.

When the converter operates in the first semi-cycle of the mains voltage, one cell operates with commanded switches, according to the PWM logic, while the other cell conducts only through the body diodes of the switches. During the next semi-cycle occurs an inversion of the conduction for the cells.

The operation stages are defined by the comparison of the rectified voltage (V1) and the output voltage (Vo) in function of the duty cycle (D). Thus, when the voltage V1 is lower than a half of the voltage Vo, the converter operates with duty cycle greater than 0.5 (overlapping mode) and when the voltage V1 is greater than a half of the voltage Vo, the converter operates with duty cycle lower than 0.5 (non-overlapping mode). These two operations method are presented in Fig. 3.

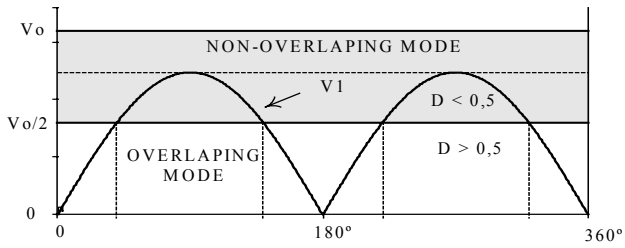

Fig. 3 - Operation methods for one cycle of the line.

A – OPERATION STAGES FOR D > 0.5

First stage (t0 < t < t 1)

Initially, during the positive semi-cycle, the switch M1 is turned on and M2 keep conducting. The diodes D1 and D2 are reverse. For the current through inductor L1 ($I1=I_{L1}$) one part flows through T1 and M1 ($I_{T1} = I_{M1}$) and another part flows through T2 and M2 ($I_{T2} = I_{M2}$). Since T1 and T2 have the same turn-ratio, the current through them are equals ($I_{T1} = I_{T2}$), the opposite polarity between the windings shown in Fig. 4.a, generates a null voltage across the windings (short-circuit), after that, the current returns to the source through body diodes of M3 and M4. One part flows through M3 and T3 ($I_{M3} = I_{T3}$) and another part flow through M4 and T4 ($I_{M4} = I_{T4}$). Similarly T1 and T2, the voltage across T3 and T4 are also zero. Moreover, the inductor L1 stores energy and its current grows linearly, without transferring energy to the load.

This stage is illustrated in Fig. 4.a, and the current circulation in the circuit is marked in boldface. This stage finishes when M2 is turned off.

Second stage (t1 < t < t2)

The switch M2 is turned off and M1 keep conducting. The voltage across the inductor is inverted. The diode D2 is forward biased while D1 is inversely biased. The current $I1 = I_{L1}$, which circulates through inductor L1, one part flows from T1 and M1 ($I_{T1} = I_{M1}$) and another part flows from T2 and D2 ($I_{T2} = I_{D2}$), toward the load. Moreover, this current decreases linearly, transferring the energy stored in the previous stage and the energy of the source V1 to the load. Since T1 and T2 have the same turn ratio, the current through them are equals ($I_{T1} = I_{T2}$). Likewise the first stage, the current returns to the source. This stage is shown in Fig. 4.b and the current circulation is marked in boldface. This stage finishes when M2 is turned on.

Third stage (t2 < t < t3)

This stage is similar to the first one with the difference that the switch M2 begins to conduct while M1 keep conducting. The diodes D1 and D2 are reverse without transferring energy to the load. Fig. 4.c illustrates this stage and the current circulation in the circuit is marked in boldface.

Fourth stage (t3 < t < t4)

This stage is similar to the second one with the difference that the switch M1 is turned off and M2 keep conducting. The diode D1 is forward biased and D2 is reverse. In this way, there is energy transference from source V1 and from inductor, stored in the previous stage, to the load. The current through the circuit is shown in Fig. 4.d.

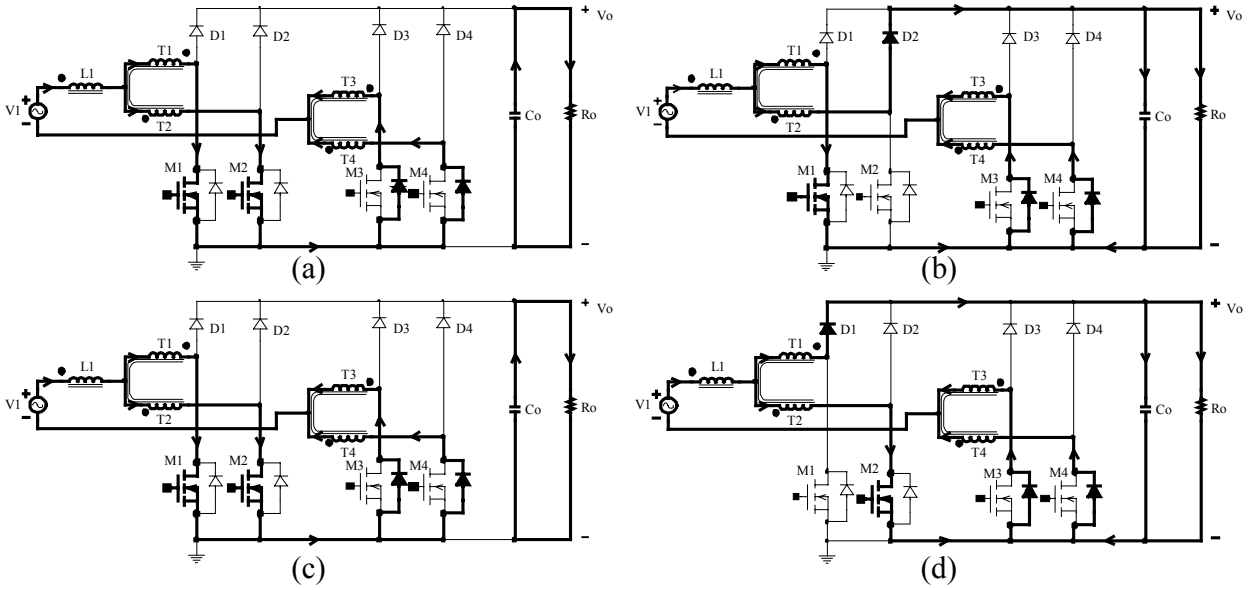

Fig. 4 - Operation stages for, D>0.5 and positive semi-cycle.

B – OPERATION STAGES FOR D < 0.5

First stage ($t_0 < t < t_1$)

In the instant $t = t_0$ (positive semi-cycle), switch M1 begins conducting and M2 is turned-off. The diode D1 is reverse and D2 begins conducting. The current through inductor L1 ($I1=I_{L1}$), one part flows from T2 and D2 ($I_{T2} = I_{D2}$) to the load and another part flows through T1 and M1 ($I_{T2} = I_{M1}$). Since T1 and T2 have the same turn-ratio, the current through the windings are equals ($I_{T1} = I_{T2}$). The current through the inductor L1 grows linearly and stores energy. The windings T1 and T2 have the same impedance, therefore, the voltages across them become equals and the magnitudes are equal to a half of the output voltage Vo. The return of the current for the source is through body diodes of M3 and M4. One part flows through M3 and T3 ($I_{M3} = I_{T3}$) and another part flows through M4 and T4 ($I_{M4} = I_{T4}$). The voltage across the windings T3 and T4 are zero. This operation stage is illustrated in Fig. 5.a and the current circulation in the circuit is marked in boldface. This stage finishes when M1 is tuned off.

Second stage ($t1 < t < t2$)

In the instant $t = t_1$ the switch M1 is turned off and M2 keep turned off. The voltage across the inductor is inverted. The diode D1 is forward biased and D2 keep conducting. The energy stored in L1, during the previous stage, is transferred to the load. The current circulation through T1 and T2 ($I_{T1} = I_{T2}$), in agreement with the polarity, generates a null magnetic flow through core. The current returns to the source like in the previous stage. This stage is illustrated in Fig. 5.b and the current circulation is in boldface. This stage finishes when M2 is turned on.

Third stage ($t2 < t < t 3$)

Due to symmetry of the circuit, this stage is similar to the first one with the difference that M2 is turned on while M1 keep turned off. The diode D1 keep conducting and D2 is reverse. The return of the current to the source is also the same. The current loop through the circuit is shown in Fig. 5.c.

Fourth stage ($t3 < t < t4$)

This stage is similar to the second one and the circuit is shown in Fig. 5.d. The current circulation is in boldface.

During the negative semi-cycle occurs the symmetry of all described stages for D>0.5 and D<0.5. M1 and M2 begin to have conduction by their body diodes while M3 and M4 operate as active switches and PWM modulation.

C - STATIC GAIN AND OUTPUT CHARACTERISTIC

The ideal gain is illustrated trough expression (1) and plotted in Fig. 6. The ideal output characteristic of the converter is shown in Fig. 7, where the voltage gain is shown as a function of the load having the duty cycle as parameter. In Fig. 9 DCM refers the discontinuous conduction mode whereas CCM refers to the continuous conduction mode.

$$G = \frac{Vo}{V1} = \frac{1}{1-D} \qquad (1)$$

The static gain in Fig. 6 is equal to the one of the classic boost converter.

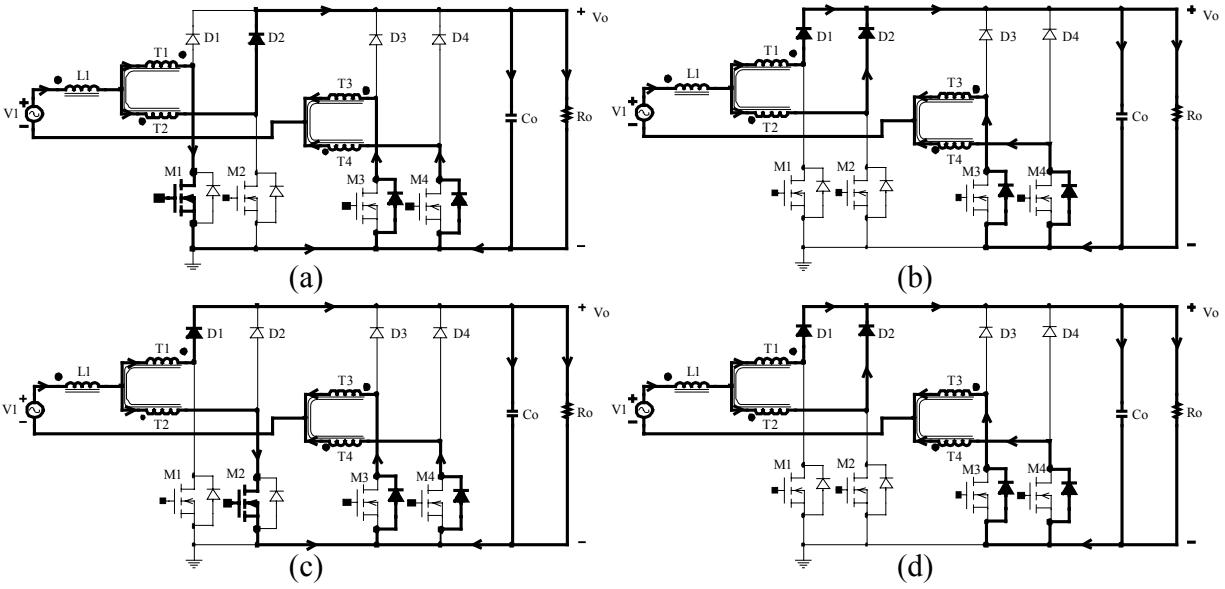

Fig. 5 - Operation stages for D < 0.5 and positive semi-cycle.

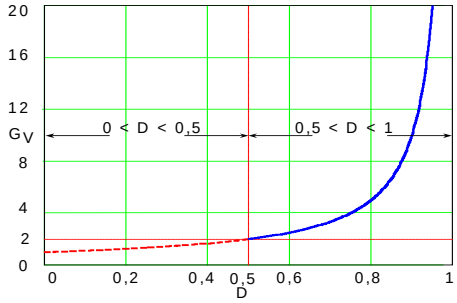

Fig. 6 – Static gain of the converter.

The plot of Fig. 7 shown that the area of DCM is smaller than the same area for the classic converter boost (formed with the two states switching cell). The highest load limit (γ) in DCM for the classic converter boost it finds in 0.25 while boost converter formed with three states switching cell the limit happen in 0.125.

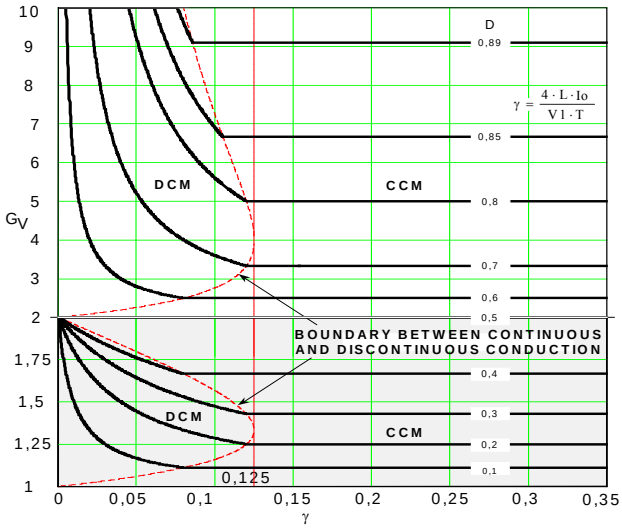

Fig. 7 – Output characteristic of the converter.

III. Design Procedure

The design procedure of the pre-regulator with high power factor and lower THD is presented in this section. Furthermore, average current mode control is applied to the single-stage three-states boost converter. The design is accomplished in base the proposed converter shown in Fig. 2.

A. Specifications

Input considerations:

Po = 1kW output power;
V1 = 220V rms input voltage;
Vo = 400V DC output voltage.

For the design are adopted the following parameters:

Fs = 30kHz switching frequency;
ΔIL = 1.5A ripple current (20% of I1p);
ΔVo = 10V ripple of the output voltage;
$\eta = 97\%$ efficiency;
$\alpha = \frac{Vo}{Vp} = 1.286$ parameter;
$\theta 1 = sin^{-1}(\frac{\alpha}{2}) = 0.6982 rad$ transition angle between the two operation modes.

B. Computation of the reactive components

Inductor L:

$$L = \frac{Vo}{16 \cdot \Delta I_{L\max} \cdot Fs} = 555.6 \mu F$$

Capacitor C:

$$C \geq \frac{Po}{4 \cdot \pi \cdot Fr \cdot Vo \cdot \Delta Vo} = 331.6 \mu F$$

C. Voltage and current

a) Inductor (rms and peak currents)

$$Irms_L = \frac{\sqrt{2}\cdot\alpha\cdot Io}{\eta} = 4.785A \qquad I_{pL} = \frac{2\cdot\alpha\cdot Io}{\eta} = 6.767A$$

b) Transformer (rms and peak currents and DC voltage)

$$V_{T1} = \frac{Vo}{2} = 200V \qquad Irms_{T1} = \frac{\sqrt{2}\cdot\alpha\cdot Io}{2\cdot\eta} = 2.392A$$

$$Ip_{T1} = \frac{\alpha\cdot Io}{\eta} = 3.383A$$

c) Switches (rms and peak currents and voltage)

$$Irms_{M1} = \frac{\alpha\cdot Io}{2\cdot\eta}\cdot\sqrt{\frac{(2\cdot\alpha - \sin(\alpha))}{\alpha}} = 1.894A$$

$$V_{M1} = 400V$$

$$I_{pM1} = \frac{\alpha\cdot Io}{\eta} = 3.383A$$

d) Diodes (average and peak currents and voltage)

$$V_{D1} = Vo = 400V \qquad Iavg_{D1} = \frac{\alpha\cdot Io}{4\cdot\eta} = 0.846A$$

$$I_{pD1} = \frac{\alpha\cdot Io}{\eta} = 3.383A$$

With these calculated values of voltage and current the main components of the converter are specified and the input current is controlled by average current mode technique to get PFC using UC3854 integrate circuit [7], the full schematic diagram is shown in Fig. 13.

IV. Evaluation of Semiconductor Losses

In this section a comparative evaluation of the switch losses between the converters shown in Fig. 1(b) and Fig. 2 will be presented. The equations (2) to (4) show the switch losses.

$$P_C := R_{DSon}\cdot I_{rms}^2 \qquad (2)$$

$$P_{SW} := \frac{Fs\cdot(tr+tf)\,I_{rms}\cdot V_{S1}}{2} \qquad (3)$$

$$P_T := P_{SW} + P_C \qquad (4)$$

P_C	conduction losses
R_{DSon}	Drain-Source conduction resistance
I_{rms}	rms current
P_{SW}	switching losses
Fs	switching frequency
tr	rise time of the current
tf	fall time of the current
V_{S1}	voltage on the switch
P_T	total losses in the switch

For correct loss estimation between the converters, we must be taken the same switches for both converters. It is important to remember that the ripple frequency in the reactive elements of the proposed converter (Fig. 2) is the double of the switching frequency and only the half of the power proceeding from input source is delivered to the load without being processed by the switches. Taking V_{S1} = 100V, R_{DSon} = 100mΩ, tr = tf = 10ηs, Fs = 30kHz and input rms current (I1) as equal 10A, the table I is present to show a comparative conduction losses on the switches for both converters.

TABLE I
MOSFET losses for two described converters

Converter	I_{rms} (A)	Numbers of switch	Losses for switch	Total loss
Fig. 1(b)	0.77*I1 7.7	2	6.3W	12.6W
Fig. 2	0.39*I1 3.9	4	1.7W	6.8W

In these calculations, the double switching frequency of the converter shown in Fig 1(b) was not considered. Besides, the conduction losses on the diodes and transformer were not considered too. Thus, a first analysis becomes the proposed converter as an attractive option for high power density applications. In addition, it has possible to work with cheaper MOSFETs because the reduced switching frequency and distributed power semiconductors on the heat sink.

VI. Experimental Results

In this section, some preliminary experimental results, obtained with only the command circuit, are presented. The power circuit is not able yet to operate as a PFC because we are waiting for an acquired transducer (current sensing).

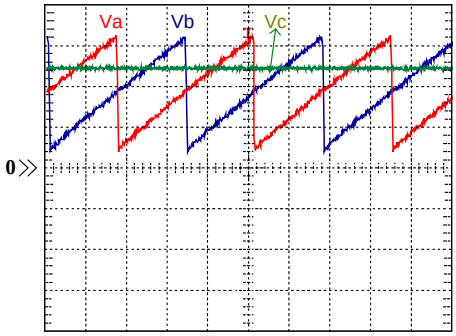

Fig. 8 - Details of the saw-tooth carriers (Va and Vb) and control voltage (Vc). Scales: 1V/div and 10us/div.

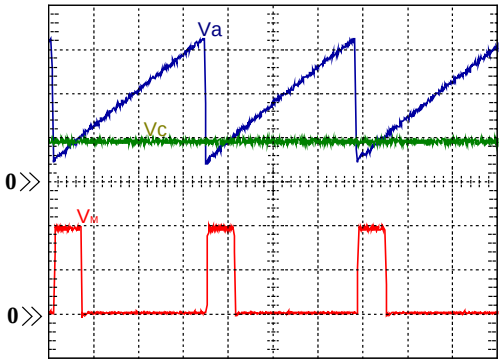

Fig. 9 - Relationship between saw-tooth carriers (Va), control voltage (Vc) and gate voltage V_M (D < 0.5). Scales: 1V/div (Va, Vc), 5V/div (V_M) and 10us/div.

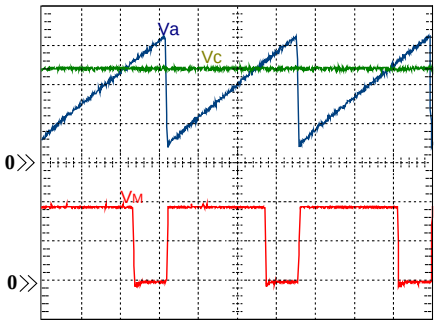

Fig. 10 - Relationship between saw-tooth carriers (Va) and the control voltage (Vc) and gate voltage V_M (D > 0.5). Scales: 1V/div (Va, Vc), 5V/div (V_M) and 10us/div.

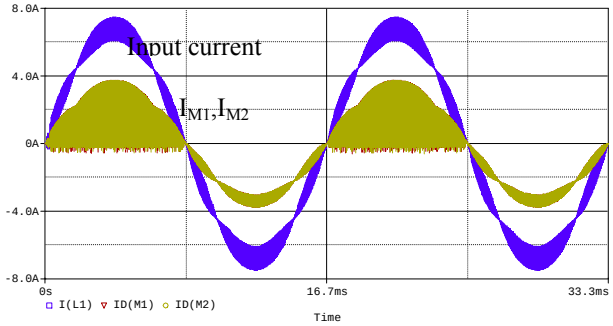

Fig. 11 - Current through the pair M1-M2 and input current.

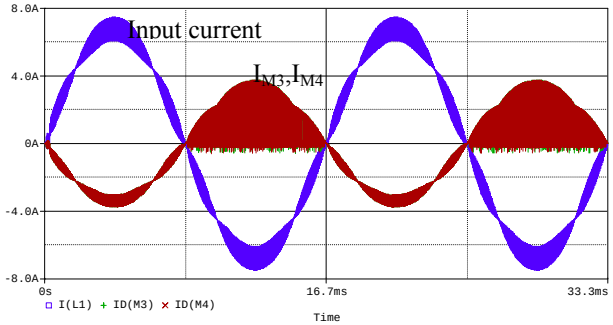

Fig. 12 - Current through the pair M3-M4 and input current.

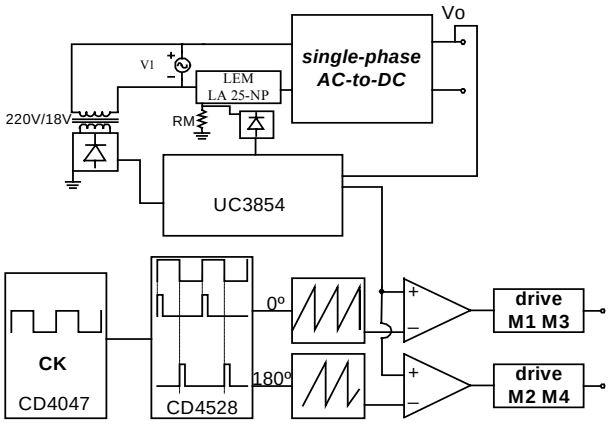

Fig. 13 – Full schematic diagram.

V. Simulation Results

It can be observed the peak currents through the semiconductors are half of the peak current through the inductor, as shown in Fig. 11 and Fig. 12. From input current, it can be observed that the ripple (harmonic distortion too) of the line current I1 is very low. In addition, Fig. 11 and Fig. 12 show that the pair M1-M2 keeps operating according to the PWM modulation in the positive semi-cycle, while the body diodes of the pair M3-M4 have forward biased. During the negative semi-cycle, occurs an inversion of the pairs to operate with PWM modulation.

VI. Conclusion

This work proposed a new technique to improve the power factor and the efficiency of the single-phase and single-stage AC-to-DC converter. The semiconductor conduction losses are minimized because the current circulation is distributed among the semiconductors and the energy processing for each semiconductor is reduced because part of the energy is directly transferred to the load without being processed by the active switches. In addition, the losses are better distributed on the heat sink and inexpensive devices can be used. The simulation results are important to verify the principle of operation and to observe that this technique allows to increase the power factor to approximately 0.99 and to reduce the THD below 2%. The design procedure and some preliminary results for command circuit were also presented.

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