IMPLEMENTATION OF A HIGH PERFORMANCE ELECTRONICS CIRCUIT TO CONTROL THE LIGHTING INTENSITY OF HIGH POWER HALOGEN INCANDESCENT LAMPS

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***Abstract* – This paper presents the study and the implementation of a high performance electronics system, with PWM modulation and low harmonic distortion. This system is used to control the level of the lighting system of high power halogen incandescent lamps. The power circuit structure is particularly simple and robust. It is very attractive for single-phase high power applications. Switching losses are reduced due to implementation of the Williams snubber circuit that provides ZCS commutation in the turn-on, and ZVS commutation in the turn-off of the main switch. The main features of the system are: simple control strategy, robustness, lower weight and volume, low harmonic distortion of the input current, and high efficiency. The principle of operation for steady-state conditions, mathematical analysis and experimental results from a 5 kW laboratory prototype are presented.**

***Keywords*: Static Converter, Williams Snubber, High Power Factor, PWM Modulation, Lighting Control, High Power Halogen Lamps.**

I. INTRODUCTION

We never have talked so much about electrical energy before, like we do right now, due to the supply crisis in many countries. This sudden valorization of the electrical energy product shows how the electricity is an indispensable part in our lives, even in the domestic, commercial or industrial activities. In reason of this, it is imperative that this source of energy be utilized and administrated in an adequate and efficient manner. The scientific community, in special the power electronics area, has been contributing in the searching of new technologies for the adequate utilization of the electrical energy. The frequent use of the electronic systems in the industrial, commercial and even residential processes, affects the quality of the energy.

In general in the power plants predominate the linear loads, that is, those where the current is proportional to the applied voltage. However, in the last 20 years, with the dissemination of the non linear loads, some problems in the electrical energy quality of the power plants set up to appear. This kind of load generates many harmonic current affecting the equipments connected in the electrical grid.

In most situations the lighting systems present a significant contribution in the harmonic distortion of the electrical plants [1]. Among the main responsible for the high harmonic distortion in the electrical light systems we have the high power light intensity controls, known in the literature as dimmer, due to the nature of the electronics circuits used in this systems. The power control of these devices is made through power thyristors by the abrupt commutation of the input current provoking high levels of harmonic distortion, audible noises and electromagnetic interferences. Some manufacturers, seeking to become competitive internationally, try to minimize these problems investing in palliative solutions, putting a high inductance for minimizing the rapid increase of the thyristor current, or using radio-frequency conventional filters. However, good quality filters become not proper in the high power applications, because their volume and cost are proportional to the equipment power.

The present work aims to solve the problem from its origin searching a simple and robust topology, that when it is employed in lighting intensity control of high power incandescent lamps keeps the efficiency in a high level and minimize the problems of harmonic distortion and electromagnetic interference, maintaining them in an acceptable levels suggested by international rules (CISPR22 and IEC61000-3-2).

II. PROPOSED TOPOLOGY

With the power electronics progress, after the emergence of the thyristors between 1960 and 1970, the conception of the small, cheaper and high efficient dimmer device became easier. Nowadays, the thyristor are still used largely due to the occurrence of natural commutation, besides the robustness, reduced size, high efficiency, and mainly low cost. In low power applications we can use TRIACs, while for high power applications we used 2 SCRs in anti-parallel.

This electronic system also permits the lighting intensity remote control, and can be used in many places such as: houses, restaurants, conference rooms, theaters, stages, etc. However, these components operate cutting the grid sinusoidal voltage and commuting abruptly the input current, causing serious problems of electromagnetic interference, harmonic distortion, and audible noises, which need be solved.

In order to minimize the mentioned problems it is proposed in this paper a structure that operates with high frequency commutation. Fig. 1 presents the power circuit diagram. The snubber circuit is incorporated with the objective to decrease the commutation losses of the switch S (IGBT) [2, 3].

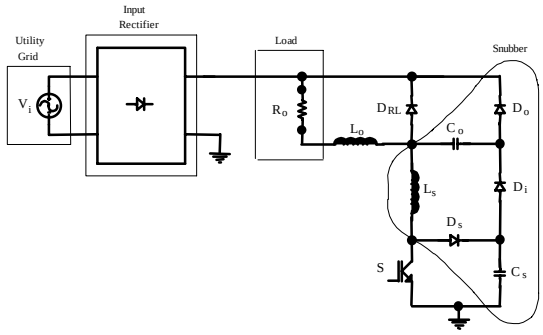

Fig. 1: Power circuit diagram.

III. OPERATION STAGES AND MATHEMATICAL ANALYSIS

It will be considered the operation in the DC-DC configuration with the aim to simplify the converter analysis. Such simplification is valid taking into account the fact that during one commutation period the input voltage has a very little variation. The following assumptions are also made: a) the operation of the circuit is steady state; b) the components are considered ideal, excluding the IGBT tail current; c) Ls is a non linear inductance, having a high value during the turn off of the switch S, and a very little value when the switch S turns on. So, the current through the switch S does not changed with the presence of the inductance Ls.

1st Stage (t0 – t1): This stage starts when the switch S turns on. The switch current is given by Is=Io-IDRL. The current in the diode DRL decrease linearly from Io to zero. The inductor Ls controls diS/dt (diS/dt = E/Ls). The output current is given by:

$$Io = D \cdot E/Ro \tag{1}$$

The current in the switch, which starts from zero, will be:

$$i_{s(t)} = \frac{E}{Ls} t \tag{2}$$

This stage finishes when ILs = Io. Therefore, substracting (1) and (2), we obtain the interval time of the 1st stage.

$$\Delta t_{1-0} = D \cdot Ls/Ro \tag{3}$$

2nd Stage (t1 – t2): This is the diode DRL reverse recovery energy stage. The switch current continues increasing with the same di/dt. The end of this stage occurs when DRL is blocked. Thus, the switch current is given by:

$$i_{s(t_2)} = \frac{E}{Ls}\left(\Delta t_{1-0} + t_{rr}\right) \tag{4}$$

Equation (5) gives the time interval of this stage.

$$\Delta t_{2-1} = t_{rr} \tag{5}$$

Where: trr = reverse recovery time of the diode DRL.

3rd Stage (t2 – t3): At the moment that DRL blocks, a resonant current flows through the mesh formed by Cs, Di, Co, Ls, and S. It is responsible for the pick current in the switch S. The energy stored in Cs is transferred to Co. This stage ends when the voltage in Cs goes to zero.

The initial conditions of this stage are:

$$Is_{(t_2)} = Is_2 \quad ; \quad Ir_{(t_2)} = 0\text{A} \tag{6}$$

$$Vc_{o(t_2)} = 0\text{V} \quad ; \quad Vc_{s(t_2)} = E \tag{7}$$

To guarantee that the capacitor Cs will be completely discharged for the beginning of the next stage it is necessary that Co ≥ Cs. Thus, we can establish that:

$$Cs = n \cdot Co \tag{8}$$

where: $0 < n \leq 1$

The voltages across de capacitors Cs and Co can be written as:

$$v_{Cs(t)} = E\left[1 - \frac{1}{1+n}\left(1 - \cos \omega t\right)\right] \tag{9}$$

$$v_{Co(t)} = E\frac{n}{1+n}\left(1 - \cos \omega t\right) \tag{10}$$

The Eq. (11) gives us the current in the resonant circuit.

$$i_{r(t)} = \frac{E}{Z}\operatorname{sen} \omega t \quad ; \quad 0 \leq \omega t \leq \pi \tag{11}$$

where:

$$\omega = \omega_o \sqrt{\frac{1+n}{n}} = \sqrt{\frac{1}{Ls \cdot Co} \cdot \frac{1+n}{n}} \tag{12}$$

$$Z = Zo\sqrt{\frac{1+n}{n}} = \sqrt{\frac{Ls}{Co} \cdot \frac{1+n}{n}} \tag{13}$$

The current in the switch S and consequently in Ls is obtained by:

$$i_{S(t)} = Is_2 + i_{r(t)} \tag{14}$$

The equation (15) presents the pick current in the switch.

$$Is_{\max} = Is_2 + \frac{E}{Z} \tag{15}$$

The duration of this stage is obtained from (16).

$$\Delta t_{3-2} = \frac{\cos^{-1}\left(-n\right)}{\omega} \tag{16}$$

4th Stage (t3 – t4): When the voltage across Cs reaches zero, Ds conducts and the energy stored in Ls is transferred to Co, ending the charge process of this capacitor. While the switch S is maintained in conduction, the capacitor Co is kept charged.

The initial conditions of this stage are:

$$Is_{(t_3)} = Is_3 \tag{17}$$

$$Ir_{(t_3)} = Ir_3 \tag{18}$$

$$Vc_{o(t_3)} = Vc_{o_3} \tag{19}$$

The expressions of the voltage in Co and the resonant current are presented below.

$$v_{Co(t)} = \sqrt{n}\, E \cos\left(\omega t + \phi\right) \tag{20}$$

$$i_{r(t)} = \frac{E}{Z}\operatorname{sen}\left(\omega_o t + \phi\right) \tag{21}$$

where:

$$\phi = \pi - \text{sen}^{-1}\left(\sqrt{\frac{1-n^2}{1+n}}\right) - \frac{\cos^{-1}(-n)}{\sqrt{1+n}} \quad (22)$$

In the end of this stage the maximum voltage across the capacitor Co is given by:

$$V_{Co_4} = \sqrt{n}\,E \quad (23)$$

The duration of this stage is obtained from (24).

$$\Delta t_{4-3} = \frac{1}{\omega_o}\left(\pi - \phi - \frac{\cos^{-1}(-n)}{\sqrt{1+n}}\right) \quad (24)$$

5th Stage (t4 – t5): It begins when the voltage across Co reaches VCo4 and its current goes to zero. At this moment the diodes Ds and Di block, and the switch S conducts the output current.

The duration of this stage is given by:

$$\Delta t_{5-4} = DT - \Delta t_{4-3} - \Delta t_{3-2} - \Delta t_{2-1} \quad (25)$$

6th Stage (t5 – t6): This stage starts when S is blocked. The output current flows through Cs via diode Ds. The voltage across the switch S is clamped by the capacitor Cs voltage. The initial conditions of this stage are:

$$Is_{(t_5)} = Io \quad (26)$$

$$V_{Cs(t_5)} = zero \quad (27)$$

$$V_{Co(t_5)} = V_{Co_4} \quad (28)$$

The voltage across Cs varies according to (29).

$$v_{Cs(t)} = \frac{Io \cdot t^2}{2Cs \cdot t_{tail}} \quad (29)$$

where: ttail represents the IGBT tail current time.

The stages after the sixth one are dependent on the output current. So, when the current in Ls reaches zero before the complete charge of the capacitor Cs the output current is considered low, and it is considered high when Cs is completely charged before the current in Ls reaches zero. Each one of these conditions is analyzed in the next paragraph.

A. Low Output Current

7th Stage (t6 – t7): When VCs = E – VCo the diode Do turns on and the stored energy in the capacitor Co is transferred to the load through the mesh formed by Co, Do, Ro, and Lo. In this stage the tail current still exists.

Considering n ≅ 1, that is, Cs ≅ Co, the current in Ls and the voltage across Cs can be approximated by:

$$i_{Ls(t)} = Io\left(1 - \frac{t}{2 \cdot t_{tail}}\right) \quad (30)$$

$$v_{Cs(t)} = \frac{Io \cdot t^2}{4Cs \cdot t_{tail}} \quad (31)$$

This stage ends when the current in Ls reaches zero.

8th Stage (t7 – t8): When the current in Ls comes to zero the diode Ds turns off and Co continues its discharge through the load via Do. This stage finishes when the voltage across Do reaches E-VCs and Ds conducts again. The voltage in Co decreases according (32).

$$v_{Co(t)} = \frac{Io}{Co}t + V_{Co} \quad (32)$$

9th Stage (t8 – t9): This stage is similar to the 7th stage; however, we consider here that the tail current has finished. At the moment that VCo=E-VCs the diode Ds turns on and keep conducting until that the voltage across Cs reaches the source voltage E.

10th Stage (t9 – t10): When the voltage in Cs reaches E, the diode Di turns on and the stored energy in Ls is transferred to the load through the mesh formed by Ls, Ds, Di, and Do. This stage finishes when the voltage across the Co comes to zero.

11th Stage (t10 – t11): At the moment that the voltage across Co comes to zero the diode DRL turns on and the current through Ls decreases until zero.

12th Stage (t11 – t12): This stage starts when the current in Ls reaches zero, and it maintains itself in this condition until the moment that the switch S turns on, restarting a new operation cycle.

B. High Output Current

For high output current the stages 8 and 9 do not exist. So, we consider that the stages 10, 11, and 12 are the operation sequences from the 7th stage.

Fig. 2 presents the equivalent circuits of the described operation stages, and the principal waveforms are shown in Fig. 3.

IV. COMMUTATION, MODULATION AND CONTROL STRATEGY

A. Commutation Strategy

The commutation strategy is based on the use of the Williams snubber [3], which permits soft commutation in the IGBT turns on and turns off. Thus, the commutation losses are very low if compared with the conduction losses. Fig. 1 shows the implemented snubber circuit. The inductor Ls controls the di/dt in the IGBT. The expression of Ls is obtained from (33).

$$L_S \geq \frac{Vi_{pk}}{(di/dt)_{D_{RL}}} \quad (33)$$

The inductor Ls is designed to have a low magnetizing current and to saturate after the IGBT voltage fall to zero in the turns on condition.

The capacitor Cs must be designed to minimize: 1st) the IGBT turn off losses, due to the tail current; and 2nd) the turn on pick current.

Concerning to the first item the capacitor should be bigger enough to delay the pick voltage during the tail current. This is achieved applying the following expression:

$$Cs \geq \frac{t_{tail}}{Ro} \quad (34)$$

The second item is characterized by the attribution of a maximum value to the pick current through the switch S. The

equation (35) presents the pick current variation during the IGBT turn on.

$$I_{Tpk} = di/dt\left(\frac{Ls}{Ro} + t_{rr}\right) + \frac{Vi_{pk}}{Z} \qquad (35)$$

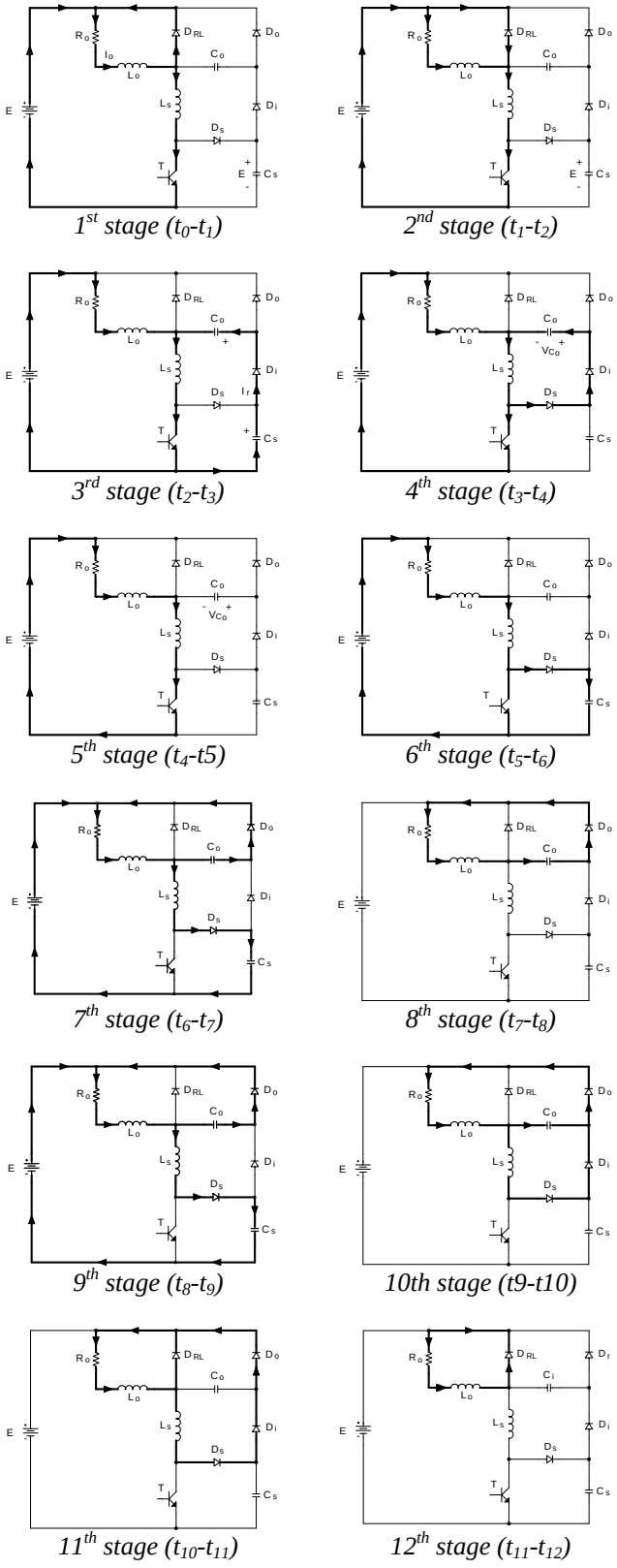

Fig. 2: Operation stages.

B. Modulation Strategy

The modulation strategy used is the well-known pulse width modulation (PWM). This technique was chosen due the following reasons: ease implementation; low cost; and constant frequency, facilitating the magnetic design. The switch drive signal is obtained by comparison of a control signal with a sawtooth waveform.

C. Control Strategy

The switch S control strategy uses a circuit composed by a PWM generator and a drive circuit. The LM-3524 integral circuit was used for generating the PWM signal. The drive circuit is a interface between the PWM generator and the IGBT, its function is to adapt the voltage and current levels of the control signal with the necessary levels to the IGBT control, and promoting the galvanic isolation between the converter control circuit and the IGBT drive circuit.

The IGBT is blocked with negative voltage, increasing the drive circuit reliability.

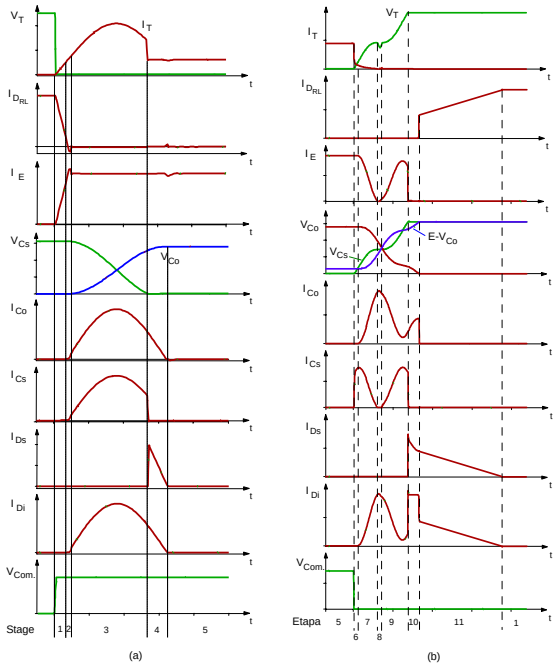

Fig. 3: Main waveforms ; (a) switch S turns on; (b) switch S turns off.

V. DESIGN EXAMPLE

A. Utility Grid Specifications

Input voltage: Vin = 220V ± 20%
Input frequency: f = 60Hz

B. Converter Specifications

Switching frequency: fs = 25kHz
Input current ripple: ΔIin = 10%
Output current ripple: ΔIo = 10%
Efficiency: η = 95%

C. Load Specifications

Output power: Po = 5kW
RMS output voltage: Vo = 220V
Output resistance: Ro = 9,68Ω

D. Input Rectifier

Average and RMS diode current:

$$I_{Dr_{av}} = \frac{\sqrt{2}}{\pi} Iin_{\max_{RMS}} = 13.462\text{A} \quad (36)$$

$$I_{Dr_{RMS}} = \frac{\sqrt{2}}{2} Iin_{\max_{RMS}} = 21.146\text{A} \quad (37)$$

where $Iin_{\max_{RMS}}$ is the RMS maximum input current.

Maximum reverse voltage:

$$V_{Dr_{\max}} = \sqrt{2}\, Vin_{\max} = 373.352\text{V} \quad (38)$$

where Vin_{max} is the maximum input voltage.

E. Commutation Cell

Power IGBT:
Maximum average and RMS current for a grid period:

$$I_{Tav_{\max}} = \frac{2}{\pi} \cdot \frac{Vin_{\max_{pk}}}{Ro} = 24.554\text{A} \quad (39)$$

$$I_{T_{RMS_{\max}}} = \frac{\sqrt{2}}{2} \cdot \frac{Vin_{\max_{pk}}}{Ro} = 27.273\text{A} \quad (40)$$

where

$$Vin_{\max_{pk}} = \sqrt{2} \cdot Vin_{\max} \quad (41)$$

Maximum voltage:

$$V_{IGBT_{\max}} = Vin_{\max_{pk}} = 373.352\text{V} \quad (42)$$

Free-Wheeling diode:
Maximum average and RMS current for a grid period:

$$I_{D_{RLav_{\max}}} = \frac{Vin_{\max_{pk}}}{2\pi \cdot Ro} = 6.139\text{A} \quad (43)$$

$$I_{D_{RL_{RMS\max}}} = \frac{\sqrt{2} \cdot Vin_{\max_{pk}}}{8Ro} = 6.818\text{A} \quad (44)$$

Maximum voltage:

$$V_{D_{RL\max}} = Vin_{\max_{pk}} = 373.352\text{V} \quad (45)$$

Output inductor
The output inductance is given by:

$$Lo = \frac{Ro}{2\,fs} \cdot \frac{-1}{\ln\left(\frac{Vin_{\max} - \Delta Io_{\max} \cdot Ro}{Vin_{\max} + \Delta Io_{\max} \cdot Ro}\right)} = 1.159\text{mH} \quad (46)$$

The RMS and pick current in the output inductor are respectively:

$$I_{Lo_{RMS}} = Io_{RMS} = 22.7\text{A} \quad ; \quad Io_{pk} = Io_{RMS} + \Delta Io = 24.97\text{A} \quad (47)$$

F. SNUBBER CIRCUIT

Snubber inductor (Ls):
Adopting a maximum di/dt of 200A/μs for the free-wheeling diode, we obtain:

$$Ls \geq \frac{\sqrt{2} \cdot Vin}{(di/dt)_{D_{RL}}} \geq \frac{\sqrt{2} \cdot 220}{200} \geq 1.55\mu\text{H} \quad (48)$$

The RMS and pick current in Ls are respectively:

$$I_{Ls_{RMS}} = Iin_{RMS} = 23.92\text{A} \quad ; \quad I_{Ls_{pk}} \cong 3I_{Ls_{RMS}} = 72\text{A} \quad (49)$$

The construction of the snubber inductor (Ls) is made in such way that after a finite time its inductance goes down to a very low value, and it has no influence in the IGBT current. The inductance (Ls) values before and after of the saturation are given below.

$$Ls = A_L \cdot N^2 = 7\mu\text{H} \quad ; \quad Ls_{sat} = \frac{\mu_0 \cdot Ae}{le} N^2 = 4.5\text{nH} \quad (50)$$

where:
AL → Core inductance factor (AL = 1750nH for type E ferrite cores);
μo = 4π·10-7H/m;
Ae → Core transverse cross-section area;
le → Core effective length;

$$N = \frac{Vs \cdot t_{fv}}{2Ae \cdot B\max} = 1.23\,\text{turns} \Rightarrow N = 2\,\text{turns} \quad ;$$

Vs = 400V → Maximum voltage across Ls;
Tfv = 129ns → IGBT voltage time fall;
Bmax = 0.35T → Maximum flux density;
Snubber capacitor (Cs)
According to the item 4.1 the capacitor Cs is obtained with the aim to achieve two objectives. From equation (34) Cs is determined in fuction of the IGBT tail current time. The tail current time is obtained via simulation using the IGBT model from PSPICE [13] (ttail = 420ns).

$$Cs = \frac{t_{tail}}{Ro} = 43\text{nF} \quad (51)$$

It was choose Cs = 39nF
The second objective is characterized by the attribution of a maximum IGBT pick current. Fig. 4 shows that, how much Cs is shorter and n is bigger, the maximum IGBT pick current, and consequently the input source current, will be shorter.

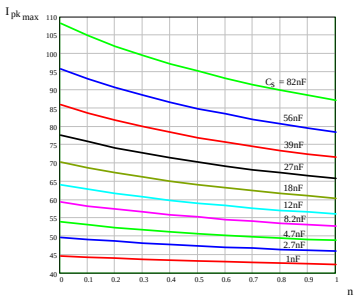

Fig. 4: Variation of the IGBT picks current in function of n, having the capacitor Cs as parameter.

The maximum IGBT pick current is given by:

$$I_{Tpk_{\max}} = 3 \cdot I_{Tav} = 73.66\text{A} \quad (52)$$

From Fig. 4 and the values of Cs and $I_{Tpk_{\max}}$ we obtain the parameter n and consequently the capacitance Co.

$$n = 0.9 \Rightarrow Co = \frac{Cs}{n} = 43.33\text{nF} \qquad (53)$$

We adopted Co = 47nF.

G. Diodes Ds, Di, and Do

The diodes Ds, Di, and Do were obtained by simulation considering the worst operation conditions (D ≅ 1). Thus:

$$I_{Ds_{\max\ pk}} = 26\text{A} \qquad I_{Ds_{\max\ av}} = 0.8\text{A} \qquad I_{Ds_{\max RMS}} = 3\text{A}$$

$$I_{Di_{\max\ pk}} = 44\text{A} \qquad I_{Di_{\max\ av}} = 0.8\text{A} \qquad I_{Di_{\max RMS}} = 3.5\text{A}$$

$$I_{Do_{\max\ pk}} = 32\text{A} \qquad I_{Do_{\max\ av}} = 0.8\text{A} \qquad I_{Do_{\max RMS}} = 3\text{A}$$

VI. EXPERIMENTAL RESULTS

The experimental results obtained from a laboratory prototype of 5kVA, where the specifications and design were detailed in the item 5, are presented below.

Fig. 5 shows the input voltage and the current for the full load condition and D ≅ 1. We can observe that both curves are in phase, operating with high power factor.

Fig. 6 presents the voltage and the current in the load. Due to the diodes bridge rectifier and IGBT drops voltage the RMS load voltage is about 215V, and the load current is 23A, corresponding to a power about 5kW.

The IGBT turn on high frequency commutation detail is presented in Fig. 7. The efficiency curve is represented in Fig. 8. It was obtained at full load condition, submitting the system to duty cycle variation from 0.1 to near 1.0. The harmonic analysis of the input current is shown in Fig. 9. It is important to mention that during the experiment the THD of the input voltage was 2.49%.

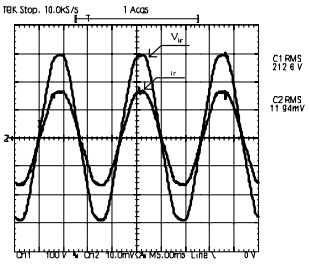

Fig. 5: Input voltage and current for full load condition.

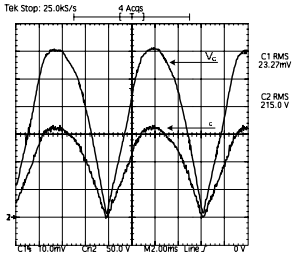

Fig. 6: Load voltage and current at full load condition.

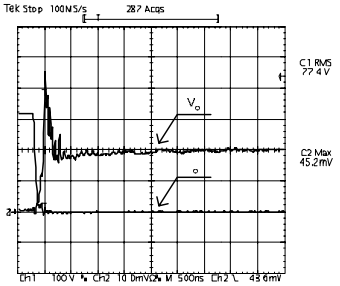

Fig. 7: IGBT turn on detail.

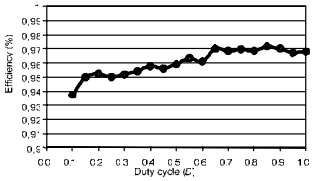

Fig. 8: Efficiency curve.

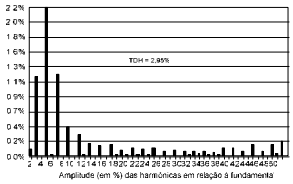

Fig. 9: Total harmonic distortion of the input current.

VII. CONCLUSION

A high performance converter to control the lighting intensity of the high power halogen incandescent lamps has been presented. The proposed circuit presented soft commutation and high power factor in all load range. It operates with PWM modulation and low harmonic distortion of the input current. The reduced number of components besides the robustness and simplicity of the structure become this system very attractive for single-phase high power industrial applications.

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