A SINGLE-PHASE THREE-LEVEL RECTIFIER EMPLOYING A PASSIVE NONDISSIPATIVE SNUBBER

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Abstract—This paper presents the study of a single-phase Boost-type three-level rectifier. The converter is supposed to present high input power factor, low current harmonics, low total harmonic distortion and simple control scheme. In order to minimize switching losses, a new passive nondissipative snubber is associated with the aforementioned converter. The theoretical analysis, design procedure, as well as analytical results regarding a 1.2kW prototype are presented to validate the proposal.

***Keywords* — power factor correction, soft switching, three-level rectifiers.**

I. INTRODUCTION

The single-phase Full Bridge diode rectifier associated with the conventional Boost converter is the former choice for power factor correction, employing the average current control technique for input current waveshaping [1]. Numerous soft switching schemes have been proposed so far, allowing the operation at high switching frequency [2] [3] and also implying reduced volume and high efficiency, although complexity is increased.

Conduction losses are significant because the current flows through three elements simultaneously during the converter operation. An interesting alternative to reduce them was proposed in [4], where the current flows simultaneously through two elements instead, in any operating stage. Additionally, soft switching techniques can be applied to the converter, minimizing switching losses and increasing overall efficiency [5].

For three-phase applications, several PWM Boost rectifiers are available in literature [6]. Such topologies are supposed to overcome common limitations imposed by high current stresses through the switches, appreciable losses and reverse recovery of diodes. Desirable features are the reduced number of components and input current with low harmonic content, resulting in low cost and increased robustness. The Full Bridge rectifier shown in Fig. 1 allows bidirectional power flow, although current stresses are quite high and very high switching frequencies are necessary to reduce the filters size. This converter presents high cost and low efficiency if compared to similar topologies.

The proposal developed in [7] presents low cost and inherent simplicity, but it operates in discontinuous conduction mode, causing high EMI levels. Another alternative lies in the converter represented in Fig. 2, where a three-phase Full Bridge rectifier is associated with a wye-connected six-switch bridge. It presents low cost, reduced losses and high reliability, but the unidirectional power flow is a limitation. By connecting the switching elements of each phase with the capacitive center point of the output voltage, one can obtain the three-phase three-level rectifier shown in Fig. 3 [8]. According to [9], it can operate with half of the losses verified in the topology depicted in Fig. 2. For low power applications, the concept of three-level rectifiers can be extended to a single-phase structure, shown in Fig. 4.

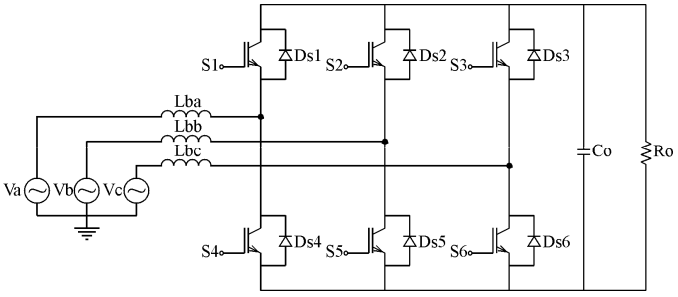


Fig. 1. Three-phase Full Bridge rectifier.

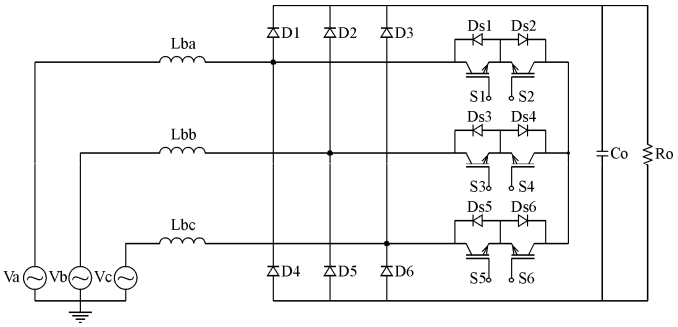


Fig. 2. PWM Boost rectifier associated with a wye-connected six-switch bridge.

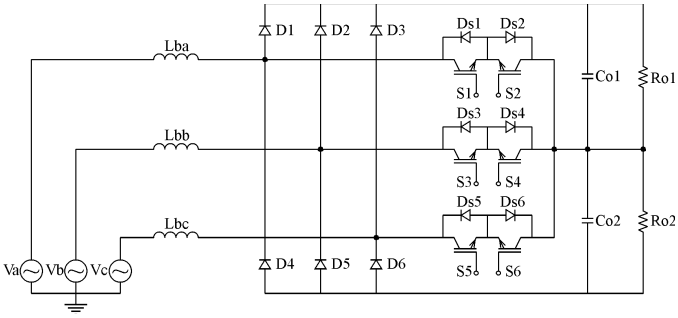


Fig. 3. Three-phase three-level rectifier.

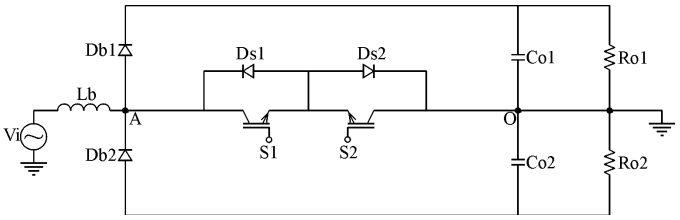


Fig. 4. Single-phase three-level rectifier.

The following advantages can be addressed to three-level rectifiers [10]:
- Reduced number of components, due to the association of the Boost converter and the diode rectifier;
- Reduced conduction losses;
- Reduced blocking voltage across the semiconductors, equal to half of the output voltage;
- Minimization of the harmonic content of the input current.

As a possible drawback of the three-level rectifier, there is the need of a specific control loop to minimize eventual disequilibrium when loads are unbalanced.

In three-level rectifiers, the reverse recovery of Boost diodes is an undesirable effect [11]. It occurs via a low impedance loop, formed by the turned on switches and the output stages, causing high current peaks in the switches at the same time when they are submitted to the output voltage. Therefore conduction losses are quite high during turning on. The introduction of inductors between diodes and switches establishes some impedance path regarding the diodes recovery. Therefore it limits the current increasing rate during the turning on and reduces the peak current, which also flows through the switches, providing zero-current switching at turning on [12]. Another problem related to commutation lies in the *dv*/*dt* rates and high frequency voltage ripple during turning off, which can be mitigated by the introduction of capacitors in parallel with the switches, providing zero-voltage switching during turning off.

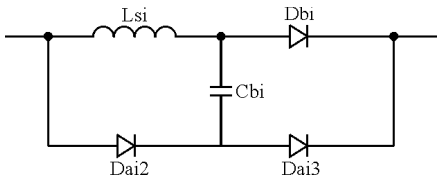
The energy resulting from the reverse recovery of the diodes is stored in the inductors, as well as the energy stored in the capacitors is transferred to the output capacitors, and then to the load. The association of passive elements such as inductors, capacitors and diodes constitute a nondissipative snubber. The use of the aforementioned elements results in simplicity and low cost [13]. As there are no active switches, control complexity is reduced, and the lack of resistive elements implies robustness and highly efficient operation.

Within this context, this paper studies a single-phase three-level rectifier with soft switching. Theoretical background on the proposed snubber is presented, which is associated with the topology. The theoretical study, design procedure, as well as simulation and experimental results regarding the converter are presented to validate the proposal.

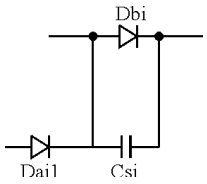
II. THE NONDISSIPATIVE SNUBBER

The proposed snubber cell can be seen as the combination of a turn-on snubber cell and a turn-off snubber cell. The turn-on snubber, shown in Fig. 5 (a), limits *di*/*dt* of the reverse recovery current by a snubber inductor in series with the Boost diode. Two diodes and one capacitor are added to recover the absorbed energy to output. Most of the turn-off snubbers proposed in literature use a snubber capacitor parallel to the switch to limit *dv*/*dt* of drain-source voltage. However, in a switching circuit, the voltage across the freewheeling diode always varies with the drain-source voltage across the switch. In other words, *dv*/*dt* can also be limited in the turn-off snubber, shown in Fig. 5 (b), by paralleling a snubber capacitor to the diode. An additional diode is added to isolate the switch from the snubber capacitor. The isolation can prevent the snubber capacitor from being discharged in the switch at light load and high line.

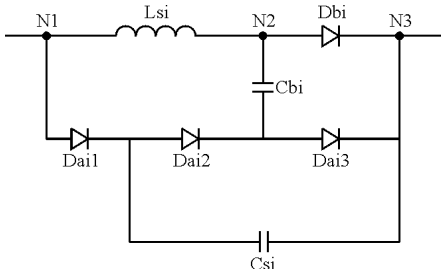
By combining the turn-on and turn-off snubber cells described above, the proposed passive lossless snubber cell can be defined (Fig. 5 (c)). Nodes *N2* and *N3* are connected to the anode and the cathode of the Boost diode, respectively. Node *N1* is connected to the component which was connected to the anode of the Boost diode in the original circuit.



(a) Turn-on cell



(b) Turn-off cell



(c) Passive lossless snubber cell

Fig. 5. Passive lossless turn-on and turn-off snubber cells.

The proposed general snubber cell consists of one inductor L_{si}, two capacitors C_{si} and C_{bi}, and three diodes D_{ai1}, D_{ai2} and D_{ai3}, where i=1, 2 and corresponds to the converter legs. The snubber inductor L_{si} is placed in series with the Boost diode D_{bi}. It is designed to restrict *di*/*dt* of the reverse recovery current to achieve ZCS turning-on. The snubber capacitor C_{si} is placed in parallel with D_{ai2} and D_{ai3}, and isolated by diode D_{ai1}. Diodes D_{ai2} and D_{ai3} are freewheeling during turn-off. It is designed to restrict *dv*/*dt* of drain-source voltage to achieve ZVS turn-off. ZVS turning-on and turning-off of the Boost diode are also obtained. Switching losses and EMI noises during turning-on and turning-off are

eliminated by the snubber cell. All energy absorbed in the snubber inductor and snubber capacitor are transferred to the buffer capacitor C_{bi}. Energy recovery is achieved by discharging C_{bi} to the output. The snubber operating principles are discussed for the single-phase three-level rectifier as follows.

III. OPERATING PRINCIPLE AND MATHEMATICAL ANALYSIS

The operating stages regarding the three-level rectifier and the nondissipative snubber are described according to Fig. 6, and the main theoretical waveforms are depicted in Fig. 7. Only the operation in the positive half cycle of the supply voltage is considered, yielding eight stages. In the analysis, the following issues are assumed:

- Output capacitances C_{o1} and C_{o2} are considered as constant voltage sources V_o;
- The input current I_i is constant;
- The Boost inductance is much greater than L_{s1} and L_{s2}.

√ **First Stage [t_0, t_1]:** Switch S is turned on at t_0. During turn-on process, diode D_{b1} is not immediately turned off because of the reverse recovery phenomenon. The increase rate of the drain current is restricted by the snubber inductor to softly turn on the MOSFET. The current through L_{s1} is:

$$i_{Ls1}(t) = I_i(t_0) - \frac{V_o}{L_{s1}} \cdot (t - t_0) \tag{1}$$

where $i_i(t)$ is the input current.

√ **Second Stage [t_1, t_2]:** The reverse recovery phenomenon finishes at t_1. As soon as D_{b1} is turned off, diode D_{a12} is naturally turned on because V_{Cs1} and V_{Cb1} are equal to zero. Snubber inductor L_{s1}, snubber capacitor C_{s1} and buffer capacitor C_{b1} are charged by the output through the first resonant path V_o-C_{s1}-D_{a12}-C_{b1}-L_{s1}-S. The increase rate of the voltage across D_{b1}, which is equal to V_{Cs1}+V_{Cb1}, is restricted to achieve ZVS turn-off of diode D_{b1}. Snubber inductor current, snubber capacitor voltage and buffer capacitor voltage are:

$$\begin{aligned} i_{Ls1}(t) = &-\frac{V_o}{Z_1} \cdot \sin\left[\omega_1 \cdot (t - t_1)\right] \\ &-I_{rr} \cdot \cos\left[\omega_1 \cdot (t - t_1)\right] \end{aligned} \tag{2}$$

$$v_{Cs1}(t) = \frac{C_{b1}}{C_{s1} + C_{b1}} \cdot v(t) \tag{3}$$

$$v_{Cb1}(t) = \frac{C_{s1}}{C_{s1} + C_{b1}} \cdot v(t) \tag{4}$$

where:

$$\begin{aligned} v(t) = &I_{rr} \cdot Z_1 \cdot \sin\left[\omega_1 \cdot (t - t_1)\right] \\ &-V_o \cdot \cos\left[\omega_1 \cdot (t - t_1)\right] + V_o \end{aligned} \tag{5}$$

$$I_{rr} = \frac{V_o}{L_{s1}} \cdot (t_1 - t_0) - I_i(t_0) \tag{6}$$

$$Z_1 = \sqrt{\frac{L_{s1} \cdot (C_{s1} + C_{b1})}{C_{s1} \cdot C_{b1}}} \tag{7}$$

$$\omega_1 = \sqrt{\frac{C_{s1} + C_{b1}}{L_{s1} \cdot C_{s1} \cdot C_{b1}}} \tag{8}$$

Peak value of the drain current of switch S is obtained by the summation of the input current and peak snubber inductor current $I_{Ls1(pk)}$. The peak value appears when V_{Cb1}+V_{Cs1} is equal to V_o, and it is given by:

$$I_{Ls1(pk)}(t_2) = \frac{\sqrt{V_o^2 + (I_{rr} \cdot Z_1)^2}}{Z_1} \tag{9}$$

The first resonance stops at t_2 when $V_{Cs1}(t_2)$ equals V_o because diode D_{a11} is turned on. By using reciprocity theorem, snubber inductor current at t_2 is given by:

$$I_{Ls1}(t_2) = \frac{\sqrt{(I_{rr} \cdot Z_1)^2 + V_o^2 - \left(V_o \cdot \frac{C_{s1}}{C_{b1}}\right)}}{Z_1} \tag{10}$$

From (11), the energy stored in L_{s1} and C_{s1} can be given by:

$$\begin{aligned} &E_{Ls1}(t_2) + E_{Cb1}(t_2) = \frac{1}{2} \cdot L_{s1} \cdot I_{Ls1}^2(t_2) \\ &+\frac{1}{2} \cdot C_{b1} \cdot V_{Cb1}^2(t_2) = \frac{1}{2} \cdot L_{s1} \cdot I_{rr}^2 + \frac{1}{2} \cdot C_{s1} \cdot V_o^2 \end{aligned} \tag{11}$$

√ **Third Stage [t_2, t_3]:** After V_{Cs1} is charged to output voltage V_o at t_2, D_{a11} is turned on and V_{Cs1} keeps constant. The current through L_{s1} starts charging C_{b1} through the second resonant path D_{a11}-D_{a12}-C_{b1}. L_{s1} and C_{b1} are performing one-way resonance because of diodes D_{a11} and D_{a12}. The current through L_{s1} and the voltage across C_{b1} are given by (12) and (13), respectively.

$$i_{Ls1}(t) = \frac{C_{s1}}{C_{b1}} \cdot \frac{V_o}{Z_2} \cdot \sin\left[\omega_2 \cdot (t - t_2)\right] - I_{S2} \cdot \cos\left[\omega_2 \cdot (t - t_2)\right] \tag{12}$$

$$\begin{aligned} v_{Cb1}(t) = &I_{S2} \cdot Z_2 \cdot \sin\left[\omega_2 \cdot (t - t_2)\right] \\ &+\frac{C_{s1}}{C_{b1}} \cdot V_o \cdot \cos\left[\omega_2 \cdot (t - t_2)\right] \end{aligned} \tag{13}$$

where:

$$I_{S2} = \frac{V_o}{Z_1} \cdot \sin\left[\omega_1 \cdot (t_2 - t_1)\right] + I_{rr} \cdot \cos\left[\omega_1 \cdot (t_2 - t_1)\right] \tag{14}$$

$$Z_2 = \sqrt{\frac{L_{s1}}{C_{b1}}} \tag{15}$$

$$\omega_2 = \frac{1}{\sqrt{L_{s1} \cdot C_{b1}}} \tag{16}$$

The second resonance stops at t_3 when $I_{Ls1}(t_3)$ equals zero. Since the energy in L_{s1} is completely transferred to C_{b1} in this stage, the energy stored in C_{b1} at t_3 can be found following to be:

$$E_{Cb1}(t_3)=\frac{1}{2}\cdot C_{b1}\cdot V_{Cb1}{}^2(t_3)$$
$$=E_{Ls1(t2)}+E_{Cb1(t2)}=\frac{1}{2}\cdot L_{s1}\cdot I_{rr}{}^2+\frac{1}{2}\cdot C_{s1}\cdot V_o{}^2 \quad (17)$$

Also, the peak voltage across the buffer capacitor $V_{Cb1(pk)}$ is:

$$V_{Cb1(pk)}=V_{Cb1}(t_3)=\sqrt{\frac{L_{s1}\cdot I_{rr}{}^2+C_{s1}\cdot V_o{}^2}{C_{b1}}} \quad (18)$$

It also determines the voltage stress across Boost diode, which is equal to V_o plus $V_{Cb1(pk)}$.

- ✓ **Fourth Stage [t_3, t_4]:** At t_3, I_{Ls1} is decreased to zero while D_{a11} and D_{a12} are turned off. The current through L_{s1} keeps zero and the voltage across C_{b1} remains constant after t_3. From (17), the total energy transferred to C_{b1} can be viewed as the summation of the energy which were absorbed in L_{s1} and C_{s1}.
- ✓ **Fifth Stage [t_4, t_5]:** After switch S turns off at t_4, current $I_i(t_4)$ flows through D_{a11} to discharge C_{s1} to the output. Diodes D_{a12} and D_{a13} are not turned on because they are reverse biased by V_{Cs1}. Drain-source voltage across S is equal to V_o-V_{Cs1}. Slow dv/dt of drain-source voltage is obtained while V_{Cs1} is discharged from V_o to zero. Assuming that $i_i(t)$ is constant during this stage, V_{Cs1} is given by:

$$v_{Cs1}(t)=V_o-\frac{I_i(t_4)}{C_{s1}}(t-t_4) \quad (19)$$

- ✓ **Sixth Stage [t_5, t_6]:** Diodes D_{a12} and D_{a13} are turned on by $I_i(t_5)$ when V_{Cs1} is discharged to zero at t_5. The voltage across L_{s1} equals V_{Cb1} and makes I_{Ls1} increase to discharge C_{b1} to the output. Circuit operation is similar to the second resonance in the second stage. I_{Ls1} and V_{Cb1} are given by (20) and (21), respectively.

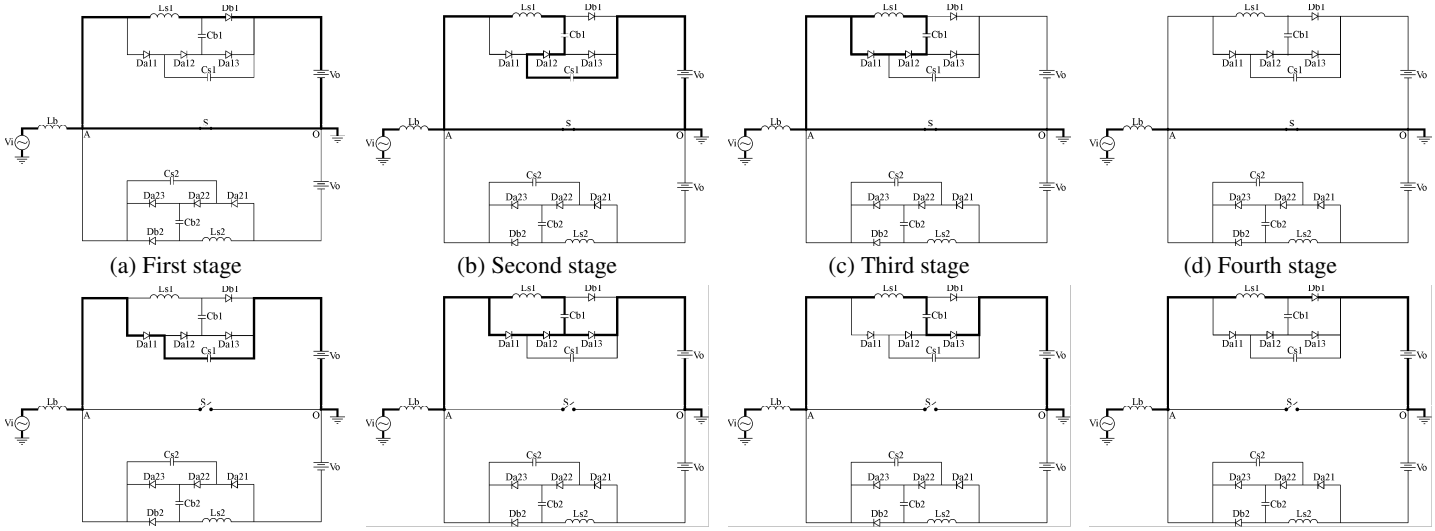
$$i_{Ls1}(t)=\frac{V_{Cb1}(t_2)}{Z_2}\cdot\sin\left[\omega_2\cdot(t-t_5)\right] \quad (20)$$

$$v_{Cb1}(t)=V_{Cb1}(t_2)\cdot\cos\left[\omega_2\cdot(t-t_5)\right] \quad (21)$$

- ✓ **Seventh Stage [t_6, t_7]:** Inductor current I_{Ls1} is increased to $I_i(t_6)$ at t_6, D_{a11} and D_{a12} are turned off. After t_6, $i_i(t)$ discharges C_{b1} to output through D_{a13}. ZVS turn-on of diode D_{b1} is achieved by slow dv/dt of V_{Cb1}. Assuming that $i_i(t)$ is constant in this stage, $v_{Cb1}(t)$ is given by:

$$v_{Cb1}(t)=V_{Cb1}(t_6)-\frac{I_i(t_6)}{C_{b1}}\cdot(t-t_6) \quad (22)$$

- ✓ **Eighth Stage [t_7, t_8]:** Capacitor voltage V_{Cb1} is discharged to zero at t_7. D_{a13} is turned off and D_{b1} is turned on simultaneously. Snubber energy recovery process is accomplished when all energy in the buffer capacitor C_{b1} is transferred to the output. After that, input current $i_i(t)$ flows through D_{b1} instead of D_{a13} to prevent C_{s1} from being charged reversely. Circuit operation will be analogous to the first stage, as the operation in the negative half cycle begins.



(a) First stage (b) Second stage (c) Third stage (d) Fourth stage

(e) Fifth stage (f) Sixth stage (g) Seventh stage (h) Eighth stage

Fig. 6. Equivalent circuits of the operating stages.

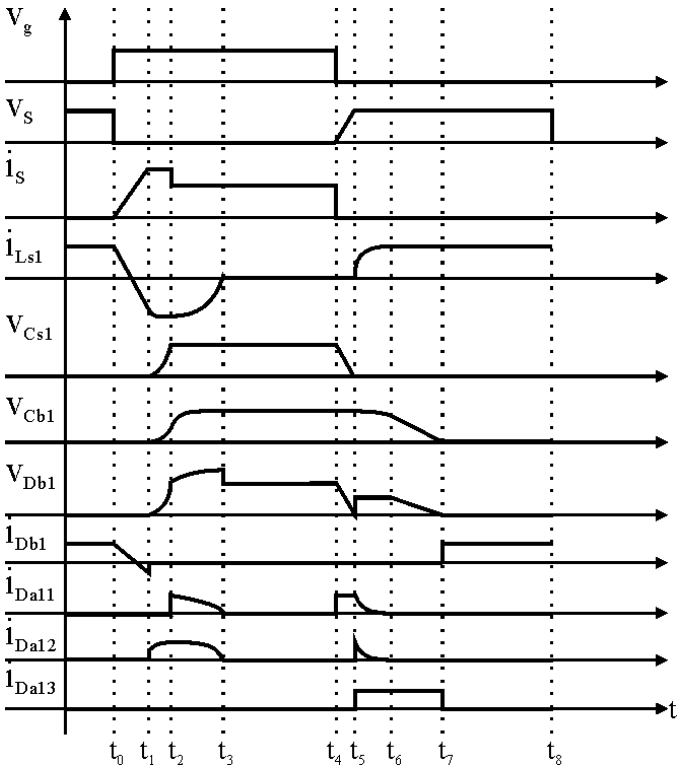


Fig. 7. Main theoretical waveforms.

IV. DESIGN PROCEDURE

A. Preliminary Calculation

The ratio between the output voltage and the peak input voltage is:

$$\beta = \frac{V_o}{\sqrt{2}\cdot V_i} \tag{23}$$

where V_o is the output voltage and V_i is the rms input voltage.

If $\beta \leq 2$, the maximum normalized input current ripple is given by (24). Otherwise, if $\beta > 2$, it is given by (25).

$$\overline{\Delta I_{Lb(\max)}} = \frac{\beta}{4} \tag{24}$$

$$\overline{\Delta I_{Lb(\max)}} = 1 - \frac{1}{\beta} \tag{25}$$

The peak input current is given by (26).

$$I_{i(pk)} = \frac{\sqrt{2}\cdot P_o}{\eta \cdot V_i} \tag{26}$$

where P_o is the output power and η is the converter efficiency.

B. Boost Inductor

The Boost inductance is calculated as follows:

$$L_b = \frac{\sqrt{2}\cdot V_i \cdot \overline{\Delta I_{Lb(\max)}}}{f_s \cdot \Delta I_{Lb(\max)}} \tag{27}$$

where f_s is the switching frequency and $\Delta I_{Lb(max)}$ is the maximum input current ripple.

C. Output Capacitors

The output capacitances are obtained from (28).

$$C_{o1} = C_{o2} = \frac{P_o}{\eta \cdot 2 \cdot (2\cdot\pi\cdot f)\cdot V_o \cdot \Delta V_o} \tag{28}$$

where f is the grid frequency and ΔV_o is the output voltage ripple.

D. Passive Snubber Elements

Snubber inductor L_{s1}, snubber capacitor C_{s1} and buffer capacitor C_{b1} are the three main elements to be designed. The following rules should be noticed when designing the respective values.

1. In stage 6, diodes D_{a11} and D_{a12} should be naturally turned off before the voltage across C_{b1} is discharged to zero, or the remaining current will turn on D_{a11}, D_{a12} and D_{a13} for the entire switching period. In other words, following inequality has to be obeyed:

$$\frac{1}{2}\cdot L_{s1}\cdot I_i^{\,2} < \frac{1}{2}\cdot L_{s1}\cdot I_{rr}^{\,2} + \frac{1}{2}\cdot C_{s1}\cdot V_o^{\,2} \tag{29}$$

2. Current stress through MOSFET and voltage stress across Boost diode are given in (9) and (18), respectively. Larger C_{s1} results in higher MOSFET current stress and higher diode voltage stress.

3. According to (18), C_{b1} has to be at least 16 times as C_{s1} to limit V_{Cb1} to 100V with a 400V output, for instance. Practically, C_{b1} should be about 30 times as C_{s1} considering reverse recovery energy.

4. Snubber inductor L_{s1} should be selected as large as possible to decrease reverse recovery loss. According to the following equation in [14], larger L_{s1} results in lower I_{rr}.

$$I_{rr} \propto \sqrt{i_i \cdot \frac{di_i}{dt}} \propto \sqrt{\frac{I_i}{L_s}} \tag{30}$$

5. Resonant frequency in (16) should be much larger than switching frequency to ensure correct operation of the snubber cell.

Trade-offs have to be made when designing L_{s1}, C_{s1} and C_{b1}. Voltage and current stresses of diode D_{a11}, D_{a12} and D_{a13} are equal to the output voltage and the input current. However, lower component ratings are also acceptable due to short snubber operating time. Voltage stress across D_{b1} and current stress through MOSFET are increased by $V_{Cb1(pk)}$ and $I_{Ls1(pk)}$, respectively. Voltage stress across MOSFET and current stress through D_{b1} are the same as those without the snubber embedded.

V. SIMULATION AND EXPERIMENTAL RESULTS

Design specifications for digital simulation and prototype are shown in Table I. In order to evaluate the performance of the soft-switched single-phase three-level rectifier, the parameters set described in Table II was determined to be employed in the tests.

Simulation tests using software Orcad Capture 9.2.3 were performed on the converter. Fig. 8 (a) shows power factor correction, as the input current is nearly sinusoidal and the displacement power factor is 0.998. As it can be noticed in Fig. 9 (a), the total harmonic distortion is low i.e. THD_I=2.33%, as the supply voltage is purely sinusoidal. Fig.

10 (a) represents the dc voltages on both output stages with satisfactory regulation for balanced loads. Fig. 9 (a) shows the voltage and current waveforms concerning switch S1, where it can be seen that it is turned on and off in ZCS and ZVS modes, respectively.

A prototype of the circuit was built with the same parameters set shown in Table II, and experimental results were obtained.

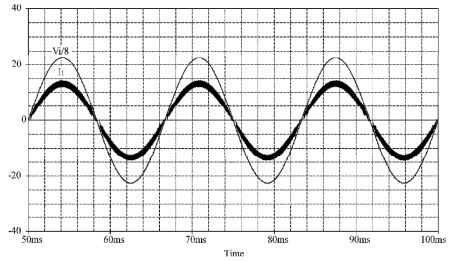
Table I
Design Specifications

Parameter	Value
Input voltage	V_i=127V$_{rms}$
Grid frequency	f=60Hz
Switching frequency	f_s=100kHz
Output voltage	V_{o1}=V_{o2}=V_o=250V
Output power	P_o=1200W
Efficiency	η=98%
Output voltage ripple	ΔV_o=2.5%·V_o
Maximum input current ripple	$\Delta I_{Lb(max)}$=2.5A

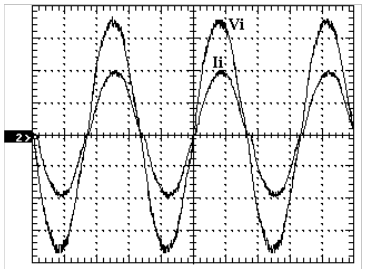
In Fig. 8 (b) and Fig. 9 (b), power factor correction and low harmonic content of the input current are evidenced, respectively, as the displacement power factor is 0.9998 and THD_I=4.94%, since THD_V=2.93%. Fig. 10 (b) shows the output voltage waveforms when loads are balanced, and Fig. 11 (b) demonstrates soft commutation of switch S_1.

Table II
Parameters Set Employed in The Evaluation Tests

Parameter	Value
Boost inductor	L_b=250µH
Output capacitors	C_{o1}=C_{o2}=1.41mF
Switches S_1, S_2	IRFP264
Boost diodes D_{b1}, D_{b2}	HFA15TB60
Snubber inductor	L_{s1}=L_{s2}=5µH
Buffer capacitors	C_{b1}=C_{b2}=100nF
Snubber capacitors	C_{s1}=C_{s2}=10nF
Snubber diodes D_{a11}, D_{a12}, D_{a13}, D_{a21}, D_{a22}, D_{a23}	HFA08TB60



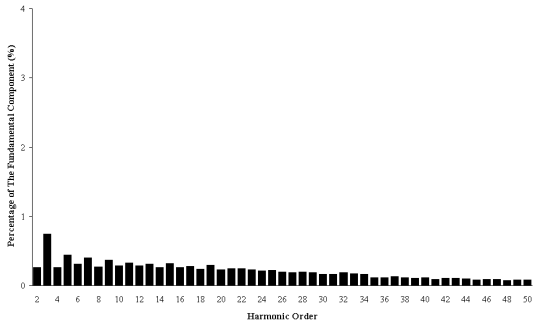
(a) Simulation result



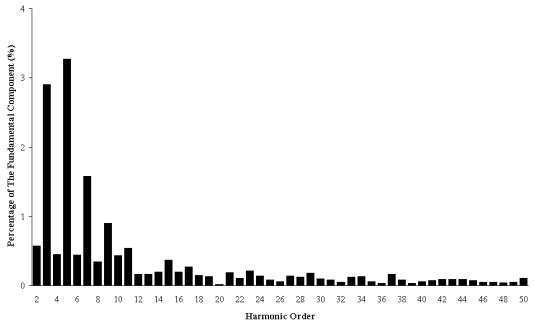
(b) Experimental result

Scales: V_i – 50V/div.; I_i – 1A/div.; time – 5ms/div.

Fig. 8. Input current (I_i) and input voltage (V_i).

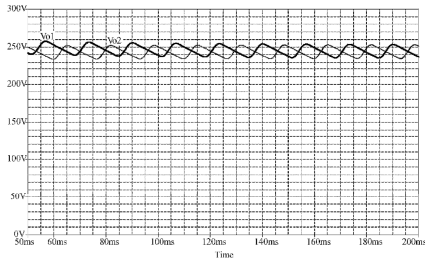


(a) Simulation result

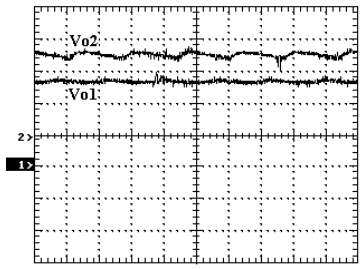


(b) Experimental result

Fig. 9. Harmonic content of the input current.



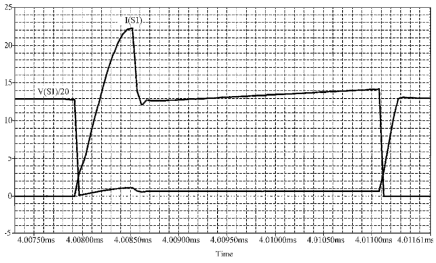
(a) Simulation result



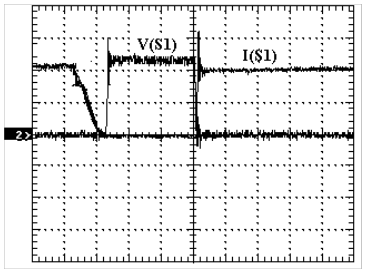
(b) Experimental result

Scales: V_{o1}, V_{o2} – 100V/div.; time – 10ms/div.

Fig. 10. Output voltages (V_{o1} and V_{o2}).



(a) Simulation result



(b) Experimental result

Scales: V_{S1} – 100V/div.; I_{S1} – 1A/div.; time – 2µs/div.

Fig. 11. Drain-source voltage and drain current waveforms in switch S_1.

VI. CONCLUSION

This paper has reported significant analytical results on a single-phase three-level rectifier. The topology is supposed to present high efficiency once that it operates with reduced conduction losses. The device voltage rating is only half of the output voltage, which is desirable for high power applications, and minimizes both conduction and switching losses. By using average current mode control, the converter achieves nearly unity power factor operation and low harmonic content of the input current.

The use of a passive nondissipative snubber provides soft commutation of the main switches, without the aid of auxiliary switches, reducing control complexity. If *di*/*dt* and *dv*/*dt* rates are limited, ZCS turning on and ZVS turning off can be achieved, as switching losses become negligible.

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