CONTROL OF SINGLE-PHASE THREE-LEG CONVERTER OPERATING AS UNIVERSAL POWER FILTER

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Abstrac*:* This paper presents a single-phase universal power filter based on the single-phase three-leg converter. Such a topology uses only six switches. The topology and its operating principles are presented. A suitable control strategy is proposed to improve the use of the topology. Simulated and experimental results are presented.

Keywords **– Universal power filter, reduced switch count**

I. INTRODUCTION

The strict regulations about the flow of electrical energy has stimulated the use active power compensation schemes [1, 13]. The active power compensation is normally achieved with the help of switching converters connected as an active filter to the load and the grid. A universal power filter provides simultaneously voltage and power factor control. One series-active filter may eliminate voltage disturbances, such as sag, notch, flicker and imbalance. The purpose of a shunt-active filter is to absorb current harmonics, compensate for reactive power and negative sequence current, and regulate the *dc*-bus voltage between both active filters.

The study of topologies with a reduced number of switches is an important topic in power electronics. For single-phase to single-phase conversion a very interesting approach is the three-leg converter (six switches) [12], [10], [4], [9] [5], [2], [14], [6], [11].

This paper presents a single-phase universal power filter based on the single-phase three-leg converter, as shown in Fig. 1. Such a topology uses only six switches, while the standard topology (full-bridge four-leg converter) uses eight-switches. The topology and its operating principles are presented. Particularly, a suitable control strategy is presented to improve the use of the topology. Experimental results are presented.

II. CONVERTER VOLTAGES

The basic scheme of the *ac*/*ac* converter presented in this paper is shown in Fig. 1. It comprises three legs (six semiconductor switches) and a capacitor bank at the *dc*-bus. Sub-converter A is composed by switches q_g, $\overline{q}_g$, q_a and $\overline{q}_a$. Sub-converter B is composed by switches q_l, $\overline{q}_l$, q_a and $\overline{q}_a$. The leg $q_a - \overline{q}_a$ is shared by both sub-converters. The conduction state of all switches can be represented by an homonymous binary variable q_g, $\overline{q}_g$, q_l, $\overline{q}_l$, q_a and $\overline{q}_a \in \{0, 1\}$, where $q = 1$ indicates a closed switch while $q = 0$ an open one. Pairs $q_g - \overline{q}_g$, $q_l - \overline{q}_l$ and $q_a - \overline{q}_a$ are complementary and, therefore $\overline{q}_g = 1 - q_g$, $\overline{q}_l = 1 - q_l$ and $\overline{q}_a = 1 - q_a$.

The converter pole voltages v_{g0}, v_{l0} and v_{a0} depend on the states of the power switches and may be expressed in terms of the previously defined binary variables q_g, q_l and q_a as

$$v_{g0} = (2q_g - 1)\frac{E}{2} \quad (1)$$

$$v_{l0} = (2q_l - 1)\frac{E}{2} \quad (2)$$

$$v_{a0} = (2q_a - 1)\frac{E}{2} \quad (3)$$

where E ($E = v_c$) is the *dc*-bus voltage.

III. *PWM* CONTROL

The pulse-widths of the gating signals can be directly calculated from the voltage referred to the *dc*-bus midpoint, which is given by the desired voltages for the grid and loads. If the desired phase voltages are specified as v_g^* and v_l^* then the reference midpoint voltages can be expressed as

$$v_{g0}^* = v_g^* + v_{a0}^* \quad (4)$$

$$v_{l0}^* = v_l^* + v_{a0}^* \quad (5)$$

Note that these equations cannot be solved unless v_{a0}^* is specified. Relations (4) and (5) can be formulated as

$$v_{g0}^* = v_g^* + v_\mu^* \quad (6)$$

$$v_{l0}^* = v_l^* + v_\mu^* \quad (7)$$

$$v_{a0}^* = v_\mu^* \quad (8)$$

The problem to be solved is to determine v_{g0}^*, v_{l0}^* and v_{a0}^* from (6)-(8) once the desired voltages v_g^* and v_l^* have been specified.

In the following, two techniques will be presented for generating the PWM gating signals for the converters.

Method A (general apportioning factor)

The voltage v_μ^* can be calculated taking into account the general apportioning factor μ, that is

$$v_\mu^* = E(\mu - \frac{1}{2}) - \mu v_{\max}^* + (\mu - 1)v_{\min}^*. \quad (9)$$

where $v_{\max}^* = \max V$ and $v_{\min}^* = \min V$ where $V = \{v_g^*, v_l^*, 0\}$. This expression was derived by using the same approach as used to obtain the equivalent one for the three-phase PWM modulator [7], [3].

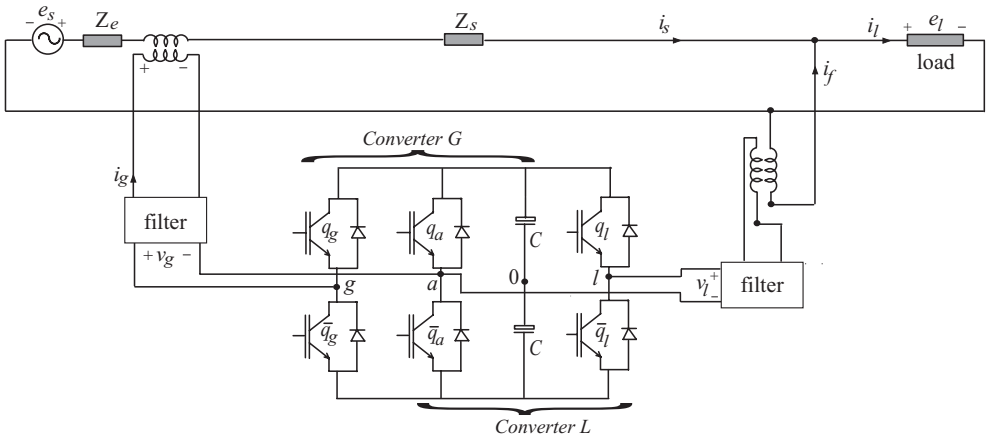

Figura 1 Single-phase universal power filter system.

The apportioning factor μ ($0 \leq \mu \leq 1$) is given by

$$\mu = t_{oi}/t_o \tag{10}$$

and indicates the distribution of the general free-wheeling period t_o (period in which voltages v_{g0}, v_{l0} and v_{a0} are equals) between the beginning ($t_{oi} = \mu t_o$) and the end ($t_{of} = (1-\mu)t_o$) of the switching period [7], [3]. The apportioning factor can be changed as a function of the modulation index (mi) to reduce the THD (total harmonic distortion) of both converter voltages [7], [3].

In this case, the proposed algorithm is:
Step 1. Choose the general apportioning factor μ and calculate v^*_μ from (9).
Step 2. Determine v^*_{g0}, v^*_{l0} and v^*_{a0} from (6)-(8).
Step 3. Finally, once the mid-point voltage have been determined, calculate pulse-widths τ_g, τ_l, and τ_a by using

$$\tau_j = \frac{T}{2} + \frac{T}{E} v^*_{j0} \quad \text{for} \quad j = g, l \text{ or } a. \tag{11}$$

Method B (local apportioning factor)
The voltage v^*_μ can be calculated taking into account the local apportioning factor μ_s:

i) for the grid $\mu_s = \mu_g$, splitting the period t_{og} (in which voltages v_{g0} and v_{a0} are equals) at the beginning ($t_{oig} = \mu_g t_{og}$) and at the end ($t_{ofg} = (1-\mu_g)t_{og}$) of the switching period.

ii) for the load $\mu_s = \mu_l$, splitting the period t_{ol} (in which voltages v_{l0} and v_{a0} are equals) at the beginning ($t_{oil} = \mu_g t_{ol}$) and at the end ($t_{ofl} = (1-\mu_g)t_{ol}$) of the switching period.

That is

$$v^*_{\mu s} = E(\mu_s - \frac{1}{2}) - \mu_s v^*_{s\max} + (\mu_s - 1)v^*_{s\min}. \tag{12}$$

where $v^*_{s\max} = \max V_g$ and $v^*_{s\min} = \min V_g$ if $s = g$ or $v^*_{s\max} = \max V_l$ and $v^*_{s\min} = \min V_l$ if $s = l$, where $V_g = \{v^*_g, 0\}$ and $V_l = \{v^*_l, 0\}$. Besides (12), the voltage $v^*_{\mu s}$ must also obey the other converter side**.** Then, from (6) and (7) the limits for $v^*_{\mu s}$ can be calculated as

$$v^*_{\mu s\max} = E/2 - v^*_l \quad (\text{if } s = g) \tag{13}$$
$$v^*_{\mu s\min} = -E/2 - v^*_l \tag{14}$$
$$v^*_{\mu s\max} = E/2 - v^*_g \quad (\text{if } s = l) \tag{15}$$
$$v^*_{\mu s\min} = -E/2 - v^*_g. \tag{16}$$

In this case, it is possible to control how the harmonic distortion is split between the converters A and B. The proposed algorithm is:
Step 1. Choose the local apportioning factor μ_s so that grid or load converter is optimized and calculate $v^*_{\mu s}$ from (12).
Step 2. Determine the $v^*_{\mu s}$ limits $v^*_{\mu s\max}$ and $v^*_{\mu s\min}$ from (13) and (14) or (15) and (16). Limit $v^*_{\mu s}$ to $v^*_{\mu s\max}$ if $v^*_{\mu s} > v^*_{\mu s\max}$ and $v^*_{\mu s}$ to $v^*_{\mu s\min}$ if $v^*_{\mu s} < v^*_{\mu s\min}$.
Step 3. Determine v^*_{g0}, v^*_{l0}, and v^*_{a0} from (6)-(8) using $v^*_\mu = v^*_{\mu s}$.
Step 4. Use Step 3 of *Method A*.

IV. VOLTAGE ANALYSIS

The maximum single-phase voltage capability for sinusoidal steady-state operation of the G and L converters is obtained when the shared leg voltage is given by $v^*_{a0} = 0$. In this case the maximum amplitude of the sinusoidal voltage for each phase voltage is $E/2$. This corresponds to same voltage capability of the half-bridge two-leg converter, while the maximum amplitude for the full-bridge four-leg converter is E.

With the use of the proposed schemes the maximum single-phase voltage capability for sinusoidal steady-state operation of the G and L converters is $V_g + V_l = E$, where V_g is the amplitude of the grid voltage and V_l is the amplitude of the load voltage. That is, we can define the amplitude of grid and load voltage as: $V_g = (1-k)E$ and $V_l = kE$ where the constant k is given by $0 < k < 1$. We conceive three control modes:

i) mode 0: ($k = 1/2$): $V_g = V_l = E/2$ that corresponds to $v^*_{a0} = 0$.

ii) mode G ($0 < k < 1/2$): i.e., $V_g > V_l$, what increases the voltage capability of Converter G toward to that of the six-leg converter.

iii) mode L ($1/2 < k < 0$): i.e., $V_l > V_g$, what increases the voltage capability of Converter L toward to that of the six-leg converter.

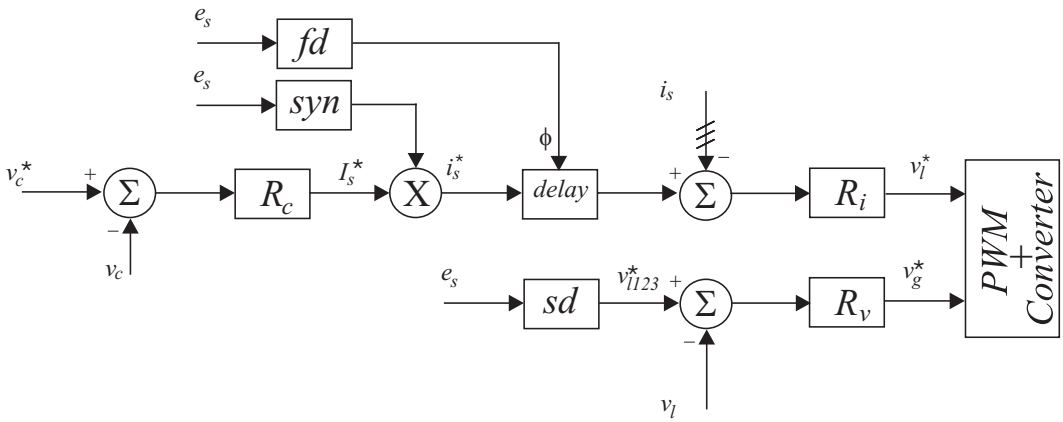

Figura 2 Control block diagram of the system.

V. OVERALL CONTROL

As discussed in the Section IV, to obtain with the proposed converter the same maximum voltages of the six-leg converter, the *dc*-bus must be doubled. However, that can be avoid.

For that, system is designed such that in steady-state voltage v_g are small than voltage v_l. That is, the system operates as in mode L of Section IV, where more voltage is available to the converter L. In this mode the system can compensate the steady-state load voltage imbalance and control the grid current. In the other hand, the compensation for a short time interval of fast variation of e_g, where it is need large values of v_g, can be accomplished with the system operating as in mode G, relaxing the power-factor control provide by converter L (because the available voltages v_l is reduced).

Fig. 2 presents the control block diagram of the system. The capacitor voltage v_c (*dc*-bus voltage) is adjusted at a reference value by using controller R_c. This controller defines the amplitude I_s^* of the grid current. To obtain a unity power factor, the instantaneous reference currents i_s^* must be synchronized with the voltage e_s. This is obtained by using block *syn*.

The regulation of the voltages is implemented by using the block R_v. The block *sd* detect the positive sequence of the grid voltage. Block R_i implements the current control strategy. The change of the converters mode of operation is done by detecting the fast voltages variation and defining the power factor. That is implemented in block fd.

VI. SIMULATION RESULTS

The system presented in Fig. 1 have been studied by simulation. It is considered that the voltage grid is sinusoidal and the load is a current source. The switching frequency was $10kHz$ and $C = 1000\mu F$.

The simulation results correspond to a load transient. In the test the amplitude of load current is reduced of 20% at $t = 0.4s$.

Simulations results are shown in Fig. 3. The four parts of this figure are: (a) grid voltage and current, (b) load current, (c) converter load current (reference and real), and (e) capacitor voltage. The compensator warrant sinusoidal grid current with power factor close to one.

VII. EXPERIMENTAL RESULTS

Fig. 4 presents the experimental results (i.e., v_g, i_g, v_c and i_c) for the three-leg converter operating as ac/ac converter in steady-state supplying a RL load with $\omega_g = 120\pi\ rad/s$ and $\omega_l = 60\pi\ rad/s$. Both capacitor voltage and power factor control are very effective.

VIII. CONCLUSIONS

This paper presents a single-phase universal power filter with a reduced number of switches. Such a topology uses only six switches, while the standard topology (four-leg converter) uses eight-switches [8]. The operating principles are presented. A suitable control strategy are presented to improve the use of the topology. Experimental and simulated results were presented.

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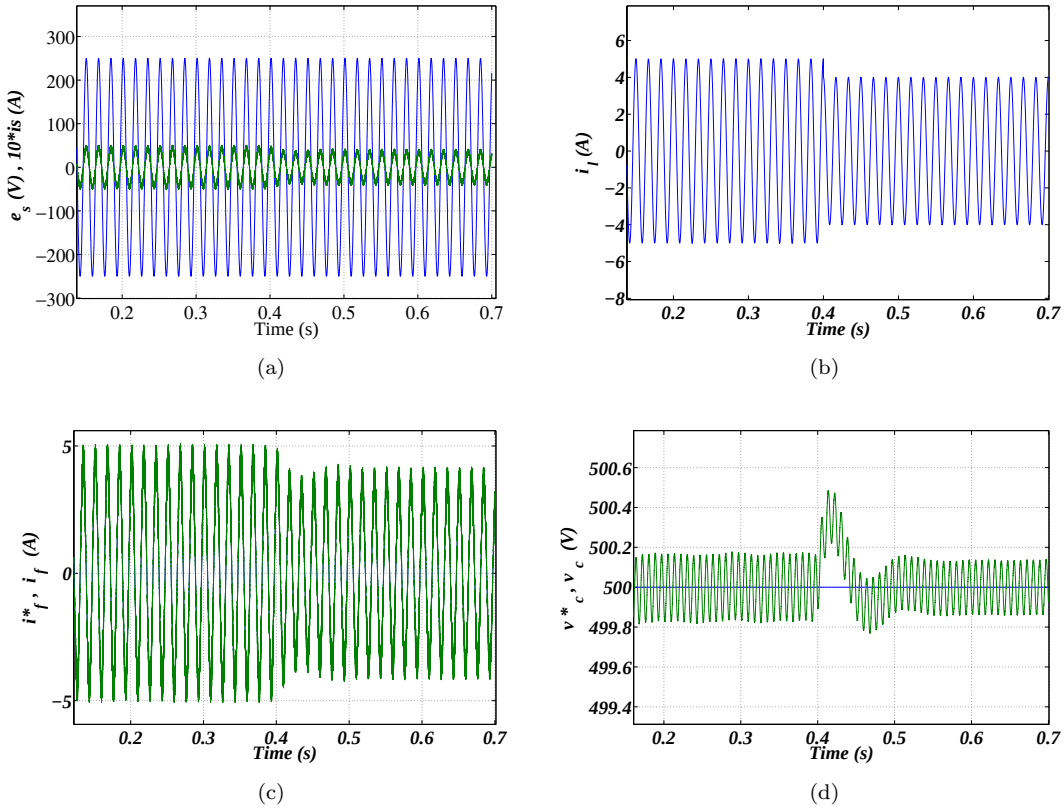

Figura 3 Simulation result: (a) grid voltage and current, (b) load current, (c) converter load current (reference and real), and (e) capacitor voltage.

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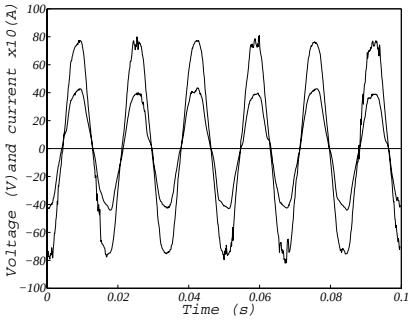
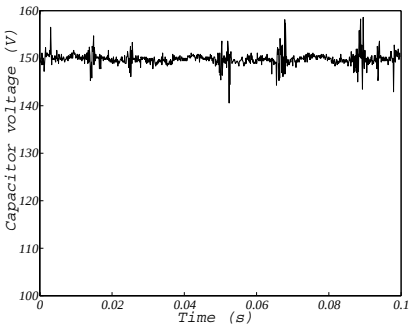
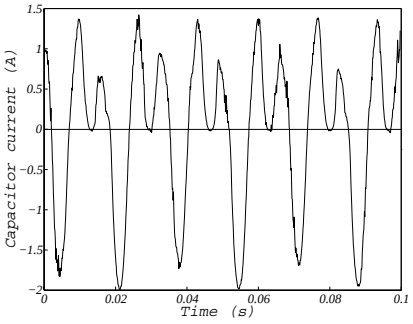


(a)



(b)



(c)

Figura 4 Experimental waveforms for the three-leg converter. (a) Voltage and current grid. (b) Capacitor voltage. (c) Capacitor current.