# GENERALIZED SWITCHING LOGIC SCHEME FOR CCM-PFC INTERLEAVED BOOST CONVERTERS

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***Abstract* — This paper presents an improvement in the operation of the interleaved boost PFC achieved by a new switching logic scheme. In this technique, the choice of the operation mode is defined by the value of the duty cycle of the converter, which does not depend on the relationship between input and output voltages. The new switching logic scheme keeps the input current ripple minimum through the appropriate phase shifting of the command signals. The concept of the switching logic scheme is extended to n cells. Both the switching logic algorithm and the impact of number of cells under input current ripple are discussed. Experimental results of a conventional boost and an interleaved boost converter with two cells are compared.**

***Keywords* – Digital Control, DSP, Interleaved boost converter, PFC, Switching logic scheme.**

## I. INTRODUCTION

With more stringent and demanding standards limiting the input current harmonics [1] and the power factor [2] of the equipments connected to the AC utility grid, the passive methods of power factor correction, using LC filters, become impracticable for medium power applications [3]-[4]. Active circuits for power factor correction using buck, boost, buck-boost, Sepic and Cuk converters has been proposed in the last years. The power factor correction based on the boost cell is the most popular technique [3], due to its reduced number of components, easy control and high efficiency. Moreover, this topology has a step-up feature, which becomes it a strong candidate for universal input voltage applications (85 – 265 $V_{RMS}$).

Boost cells operating with interleaving techniques are useful for applications in which high values of current are required [5]-[7]. The interleaving technique permits to increase the power density of the system, because the volume of the boost inductors and volume of the EMI (Electromagnetic Interference) input filter are reduced [8]. Moreover, input current ripple frequency can be increased, without affect significantly the switching losses [9]. On the other way, the cost of the system is greater than the conventional boost, due to the extras components. Furthermore, the control and the circuits used to generate the command signals of the switches are more complex, because they should ensure the equalization of the currents through the boost cells.

A switching logic scheme of the interleaved boost switches, which minimizes the input current ripple and eliminates discontinuity in the input current, was proposed in [7]. This technique presents two operation regions that depends on the relationship between the input and output voltages of the converter. This dependence results in a limitation of the duty cycle applied to the switches, penalizing the dynamic response of the converter and, at low power range, leading the system to the instability.

In this paper an improvement in the operation of the interleaved boost PFC (Power Factor Corrector) is achieved by a new switching logic scheme. Now, the choice of the operation region is defined by value of its duty cycle, which does not depend on the relative amplitude of the input and output voltages. The problems previously mentioned were eliminated, keeping still the minimization of input current ripple by appropriate phase shifting of the command signals, even in low power range.

The addition in the number of cells leads to reduction of input current ripple. In this way, the concept of the switching logic scheme is extended to *n* cells in parallel (Fig. 1). The decision of logic scheme, to control the *n* switches, is also based on the duty cycle. Algorithms to implement the switching logic scheme for *n* cells converter and the effect of this under the input current ripple are explained. In the final sections of this paper, simulation and experimental results are presented to verify the performance, pros and cons of the new switching technique.

## II. SWITCHING LOGIC SCHEME

Fig. 2 shows the single phase two cells interleaved boost converter, composed of a diode bridge, two switches ($S_1$ and $S_2$), two diodes ($D_1$ and $D_2$), two boost inductors ($L_1$ and $L_2$) and one output capacitor ($C$). In this section the technique of generation of the command signals proposed

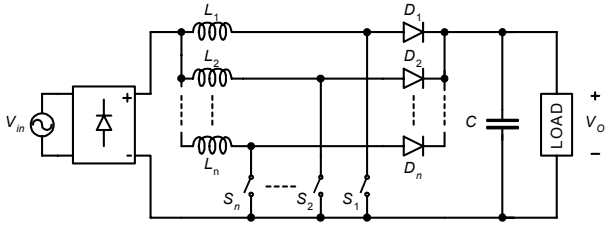


Fig. 1. Interleaved boost converter with two cells.

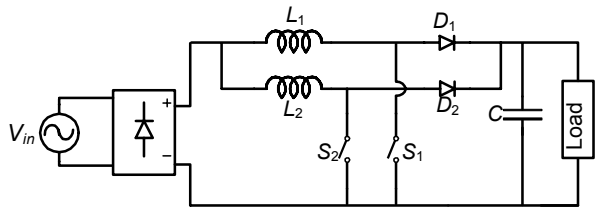


Fig. 2. Interleaved boost converter with two cells.

TABLE I
SWITCHING LOGIC SCHEME PRESENTED IN [7].

| Region 0: $V_{pk}sin(\theta)<V_0/2$ | |
|---|---|
| Control Signal ($D_C$) | Gate signal ($D_{S1}$ e $D_{S2}$) |
| *High* | $S_1$ and $S_2$ *on* |
| *Low* | $S_1$ or $S_2$ *on* |
| Region 1: $V_{pk}sin(\theta)>V_0/2$ | |
| Control Signal ($D_C$) | Gate signal ($D_{S1}$ e $D_{S2}$) |
| *High* | $S_1$ or $S_2$ *on* |
| *Low* | $S_1$ and $S_2$ *off* |

in [7] and the new technique wil be presented.

### *A. Original switching logic scheme, proposed in* [7]

The objective of this switching logic scheme is to minimize the input current ripple. To analyze this technique is assumed that the duty cycle in both switches are the same, and that the variations of the input voltage during one switching period are negligible.

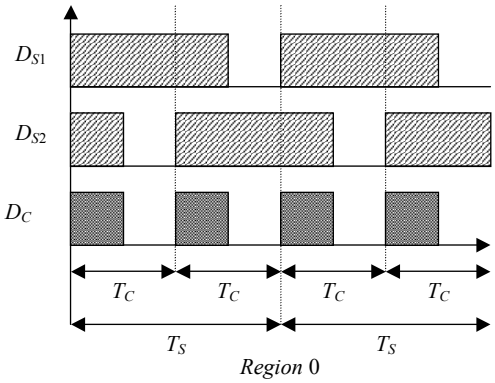


Fig. 3.Gate signals $D_{S1}$ and $D_{S2,}$ and control signal $D_C$ at *Region* 0.

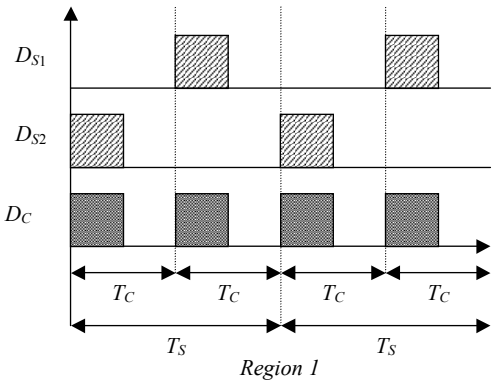


Fig. 4. Gate signals $D_{S1}$ and $D_{S2}$, and control signal $D_C$ at *Region* 1.

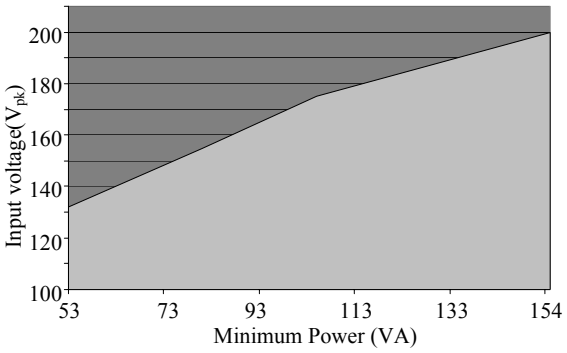


Fig. 5. Minimum power of the interleaved boost converter operating at *Region* 0.

The operation regions of this technique depend on the relative amplitude of the input and output voltages, as presented in TABLE I and their command signals are shown in Fig. 3 and Fig. 4. The problem of this technique is that the definition of operation region is associated to input-output voltage relationship. As there is a limit value for the duty cycle for each region, it will cause penalties on converter performance, instability, and input current distortion as well. The minimum duty cycle applied to the switches ($D_{S1}$ and $D_{S2}$) at *Region* 0 is 0.5, when the width of $D_C$ is zero. On the other side, at *Region* 1 the maximum duty cycle applied to the switches is 0.5, when the width of $D_C$ is 1.

So, a converter operating into the Region 0 ($V_{in}<V_0/2$), being this one designed to operate with a wide input voltage range (85-265$V_{RMS}$), there is a minimum power boundary in which the converter can follow the reference current, shown in Fig. 5. For instance, when the input voltage is 141$V_{RMS}$ (200$V_{pk}$), and the inductance cell is 1mH, the converter can not operate with a load smaller than 15.4% of the nominal load.

### *B. Proposed switching logic scheme*

The aiming of this switching logic scheme is to solve the problems previously mentioned. By using this technique the choice of the operation region is not dependent of the relationship between input and output voltages. The new switching logic scheme should keep the minimization of the input current ripple and eliminate the limitation of the duty cycle at the switches.

The choice of the operation region is defined by the value of the duty cycle of the converter ($D_{S1}$ *and* $D_{S2}$), as presented in TABLE II. By using the proposed switching

TABLE II
SWITCHING LOGIC SCHEME PROPOSED.

| Region 0: ***Ds* > 0,5** | |
|---|---|
| Control Signal ($D_C$) | Gate Signal ($D_{S1}$ and $D_{S2}$) |
| *High* | $S_1$ and $S_2$ *on* |
| *Low* | $S_1$ or $S_2$ *on* |
| Region 1: ***Ds* < 0,5** | |
| Control Signal ($D_C$) | Gate Signal ($D_{S1}$ and $D_{S2}$) |
| *High* | $S_1$ or $S_2$ *on* |
| *Low* | $S_1$ and $S_2$ *off* |

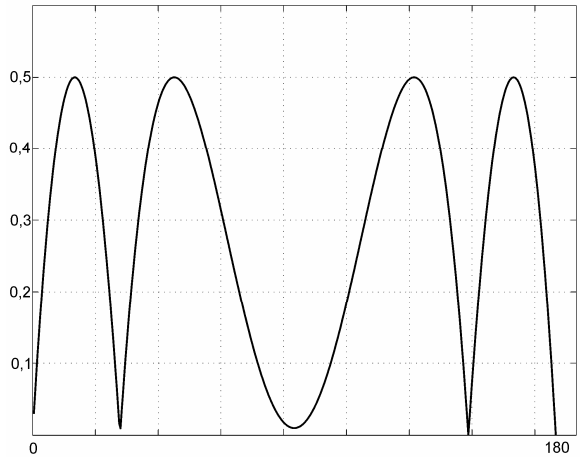


Fig. 6. Amplitude of the input current ripple in a utility grid half-cycle for two cells.

logic scheme, both minimum value of duty cycle in Region 0 and maximum value in Region 1 are equal to $0.5T_S$. But now, when $D_S$ reaches to the limit value ($0.5T_S$), the logic scheme changes automatically its operation region, eliminating the limitation of $D_S$. Therefore, the choice of the region of operation is not dependent of the input voltage value, being only this choice linked to the dynamic of the converter.

Using the logic presented in TABLE II, the input current ripple equation will be:

$$\Delta I_{in} = \frac{V_{pk}\sin(\theta)T_S}{L}\left(2D_S(\theta)-1\right) \tag{1}$$

for *Region* 0, and

$$\Delta I_{in} = \frac{V_{pk}\sin(\theta)T_S}{L}D_S(\theta)+\frac{\left(V_{pk}\sin(\theta)-V_O\right)T_S}{L}D_S(\theta) \tag{2}$$

for *Region* 1.

Fig. 6. shows the amplitude of the input current ripple for a half-cycle of the utility grid. There are three points where the input current ripple is equal to zero, whenever:

- Input voltage is equal to zero ($V_{in} = 0$), i.e., $D_S = 1$;
- Input and output voltages are equals ($V_{in} = V_O$), i.e., $D_S = 0$ and
- Input voltage is equal to half of the output voltage, i.e., $D_S = 0.5$.

This last point occurs due to the fact that:

$$\Delta I_{in} = \Delta I_1 + \Delta I_2 = 0 \tag{3}$$

In this way, for that the input current ripple becomes equal to zero, it is necessary that:

$$\Delta I_1 = -\Delta I_2 \tag{4}$$

$$V_{pk}\sin(\theta)\frac{D_S T_S}{L} = -\left(V_{pk}\sin(\theta)-V_O\right)\frac{D_S T_S}{L} \tag{5}$$

$$V_{pk}\sin(\theta) = -\left(V_{pk}\sin(\theta)-V_O\right) \tag{6}$$

$$V_{pk}\sin(\theta) = \frac{V_O}{2} \tag{7}$$

TABLE III
REGIONS OF THE SWITCHING LOGIC SCHEME FOR AN INTERLEAVED BOOST CONVERTER WITH *n* CELLS.

| Region | Duty Cycle ($D_S$) |
|---|---|
| 0 | $(n-1)/n < D_S < 1$ |
| 1 | $(n-2)/n < D_S < (n-1)/n$ |
| 2 | $(n-3)/n < D_S < (n-2)/n$ |
| ... | ... |
| n-2 | $1/n < D_S < 2/n$ |
| n-1 | $0 < D_S < 1/n$ |

$$D_S = 0.5 \tag{8}$$

## III. GENERALIZATION OF THE SWITCHING LOGIC SCHEME FOR AN N CELLS CONVERTER

As presented into section II, the switching logic scheme for the interleaved boost converter with two cells is divided in two regions. Furthermore, at transition of regions, the input current ripple is null. Extending the analysis for an interleaved boost converter with *n* cells, the input current ripple will be null when:

$$D_S = \left(0, \frac{1}{n}, \frac{2}{n}, \frac{3}{n}, \cdots, \frac{n-2}{n}, \frac{n-1}{n}, 1\right) \tag{9}$$

Thereby, the switching logic scheme for an interleaved boost converter with *n* cells will be divided into *n* regions. TABLE III and Fig. 7 show how the regions of commutation are divided in function of the duty cycle $D_S$.

In Region 0, the minimum duty cycle at switches is (*n*-1)/*n*. To synthesize smaller values of duty cycle, the switching logic scheme must change to the next region of modulation. In the same way, when *n*=2, if the transition of the region does not occur at right time, the input current

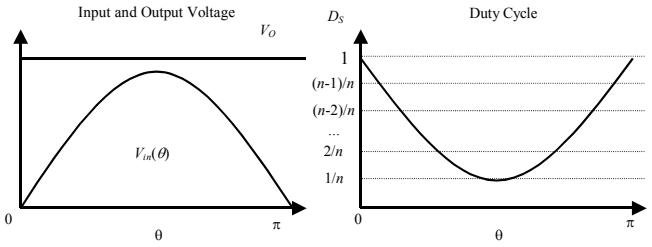


Fig. 7. Division of operation regions in an *n* cells interleaved boost converter, in function of the duty cycle.

TABLE IV
NUMBER OF TURN-ON SWITCHES IN EACH SWITCHING REGION.

| | Number of switches *on* | |
|---|---|---|
| *Region* | $D_C$ *High* $\rightarrow$ *Low* | $D_C$ *Low* $\rightarrow$ *High* |
| 0 | $N \rightarrow n$-1 | $n$-1 $\rightarrow n$ |
| 1 | $n$-1 $\rightarrow$ $n$-2 | $n$-2 $\rightarrow$ $n$-1 |
| 2 | $n$-2 $\rightarrow$ $n$-3 | $n$-3 $\rightarrow$ $n$-2 |
| ... | ... | ... |
| $n$-2 | 2 $\rightarrow$ 1 | 1 $\rightarrow$ 2 |
| $n$-1 | 1 $\rightarrow$ 0 | 0 $\rightarrow$ 1 |

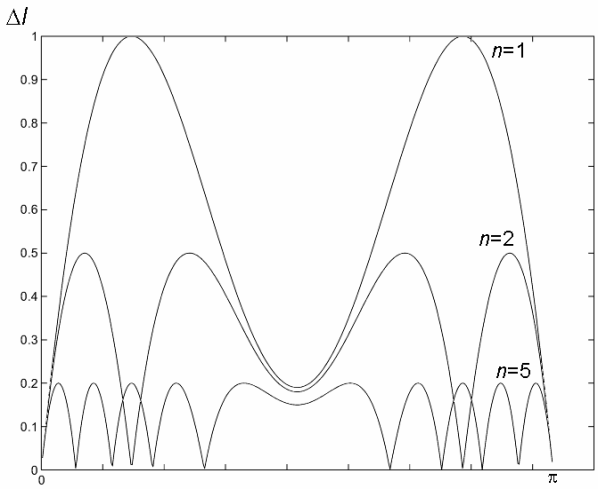


Fig. 8. Behavior of the input ripple for $V_{in}/V_o$ = 0.975, for different number of cells.

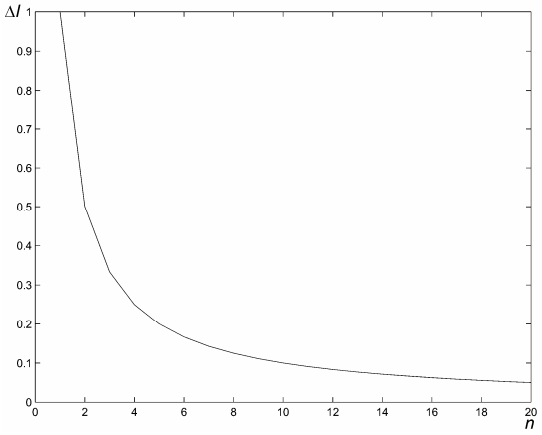


Fig. 9. Maximum amplitude of the input current ripple in function of the number of cells.

will not track the reference. During the transition of regions, the input current ripple will be null.

TABLE IV shows how many switches are *on* in each region. It is introduced a control logic to guarantee the current equalization through the cells: When the PWM signal is *high*, the switch with smaller current must be turned on; And when the PWM signal is *low*, the switch with higher current must be turned off.

The input current ripple in each region, for $n$ cells, is given by:

$$\Delta Iin(n,R) = (n-R)\left(D_S(\theta) - \frac{n-(R+1)}{n}\right)\frac{V_{pk}\sin(\theta)}{L}T_S + R\left(D_S(\theta) - \frac{n-(R+1)}{n}\right)\frac{V_{pk}\sin(\theta) - V_O}{L}T_S \quad (10)$$

where:

- $n$ – number of cells in parallel,
- $R$ – region of modulation (0 to $n$-1),
- $D_S(\theta)$ – switch duty cycle,
- $L$ – cell inductance,
- $T_s$ – switching period.

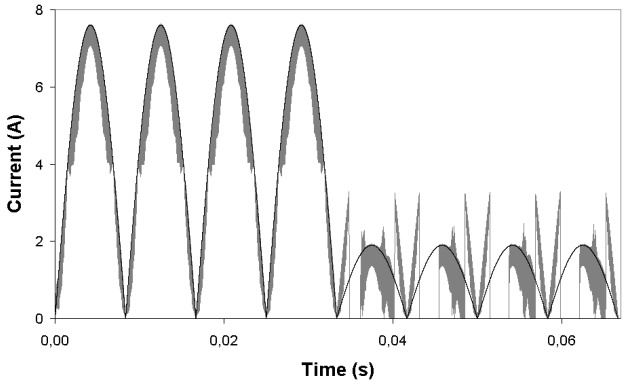


Fig. 10. Input current using the technique presented in [7].

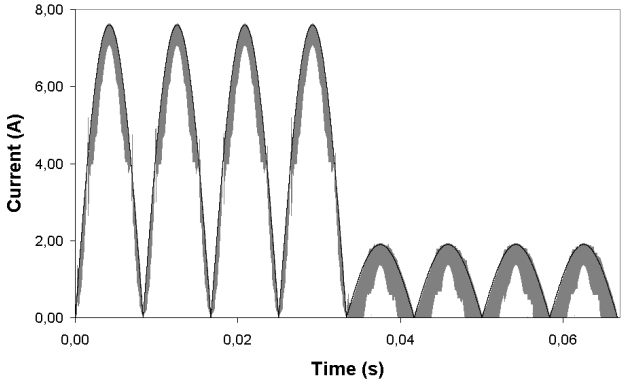


Fig. 11. Input current using the technique proposed.

Fig. 8 shows the behavior of the input current ripple for one input voltage half-cycle using the proposed switching logic scheme. As $n$ increases the amplitude of maximum input current ripple decreases, as shown in Fig. 9.

## IV. SIMULATION RESULTS

In this section simulation results are presented to demonstrate the behavior of the technique proposed. Moreover, the simulation results will be used for a comparison between the new technique and the original technique presented in [7]. The parameters adopted for the simulations are: $L_1$ and $L_2$ = 3mH, $f_s$=25kHz, $V_{in}$=311V and $V_0$ = 400V.

Fig. 10 and Fig. 11 show the input current when the converter is subjected to a large variation into the input current reference. Fig. 11 shows the input current when the proposed technique is used. In this case, there is no limitations of values of duty cycle, which allows a good performance of the converter, even in low power range. Fig. 10 shows the distortion of the input current due to limitations of the technique presented in [7]. When the converter is operating at Region 0, the minimum duty cycle applied to the switches is 0.5, which causes distortions.

## V. EXPERIMENTAL RESULTS

An experimental prototype was implemented to demonstrate the reduction in the input current ripple, when another cell is added to the system. Figs. 12 and 13 show the circuitry of the prototypes implemented in the laboratory. In the first case a conventional PFC boost converter was tested. The parameters adopted were $P_O$ = 500W, $L$ = 3mH, $f_s$ = 25kHz, $V_{in}$ = 110/220V and $V_O$ = 400V. The semicondutors $S$ and $D$ are IRFP460 and 8ETH06 respectively. DSP TMS320F243, from Texas instruments, implemented the digital controllers of the system (input current controller and output voltage regulator).

Figs. 14 and 15 shows the input current and the input voltage of the conventional PFC boost converter operating at 110 $V_{RMS}$ and 220$V_{RMS}$ input voltage, respectively.

After this, the PFC interleaved boost converter with two cells in parallel was implemented. The parameters adopted into the scheme presented in 13 were the same of those adopted into the conventional PFC boost converter.

DSP controller also implemented the switching logic scheme and the controllers of the system. Fig. 16 and Fig. 17 show the input current and the input voltage of the interleaved PFC boost converter operating at 110 $V_{RMS}$ and 220$V_{RMS}$ input voltage, respectively.

A detail of the input current in both converters operating at 110$V_{RMS}$ is presented in Fig. 18 and Fig. 19. It can be observed the reduction in the input current ripple of the interleaved converter. Moreover, the high frequency component for this topology is two times greater than that appear in the conventional boost.

In the same way, in Fig. 20 and Fig. 21 can be observed a reduction of the maximum amplitude of the interleaved converter input current ripple, when the converter are operating at 220$V_{RMS}$ utility grid.

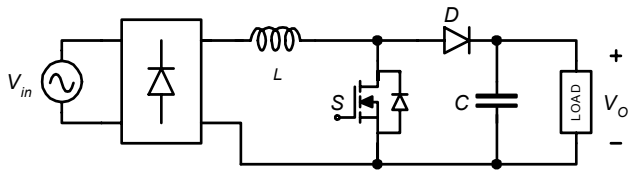


Fig. 12. Conventional boost converter implemented.

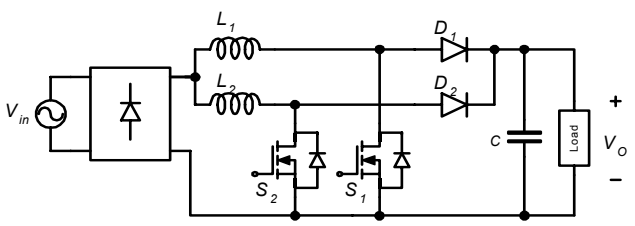


Fig. 13. Two cells Interleaved boost converter implemented.

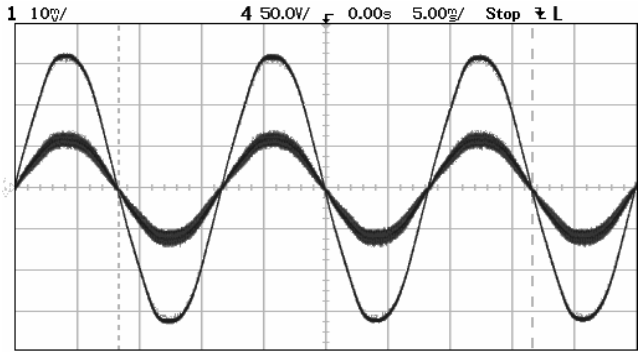


Fig. 14. Input current and input voltage of the conventional boost converter at 110$V_{RMS}$. ($V_{in}$ 50V/div and $I_{in}$ 5A/div).

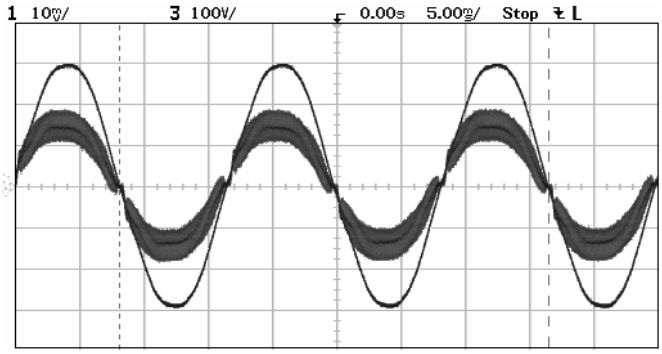


Fig. 15. Input current and input voltage of the conventional boost converter at 220$V_{RMS}$ ($V_{in}$ 100V/div, and $I_{in}$ 2A/div).

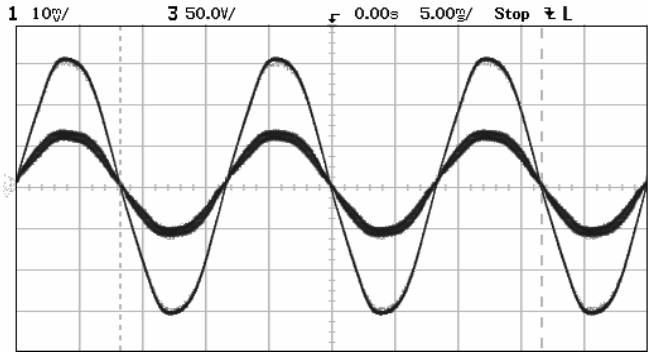


Fig. 16. Input current and input voltage of the interleaved boost converter at 110$V_{RMS}$ ($V_{in}$ 50V/div, and $I_{in}$ 5A/div).

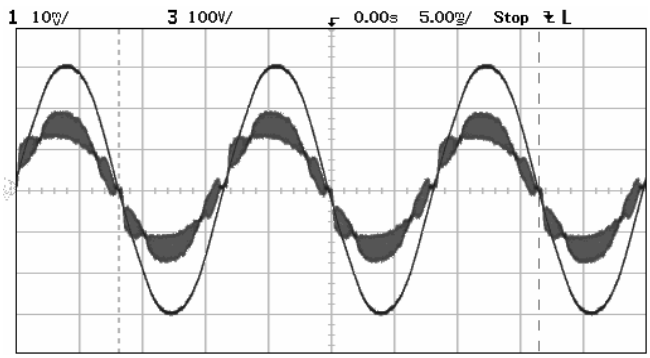


Fig. 17. Input current and input voltage of the interleaved boost converter at 220$V_{RMS}$ ($V_{in}$ 100V/div, and $I_{in}$ 2A/div).

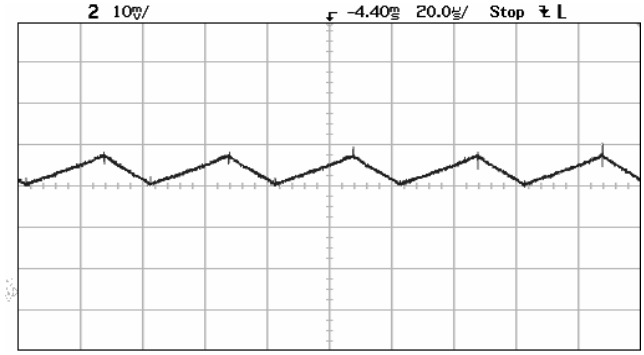


Fig. 18. Detail of conventional boost converter maximum input ripple, at $110V_{RMS}$($I_{in}$ 2A/div).

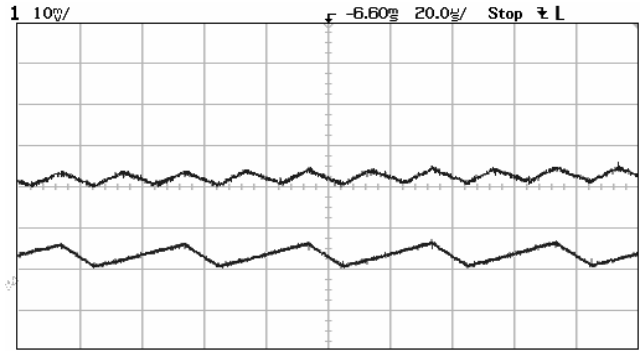


Fig. 19. Detail of interleaved boost converter maximum input ripple and inductor ripple at $110V_{RMS}$($I_{in}$(top) and $I_{L1}$(bottom) 2A/div).

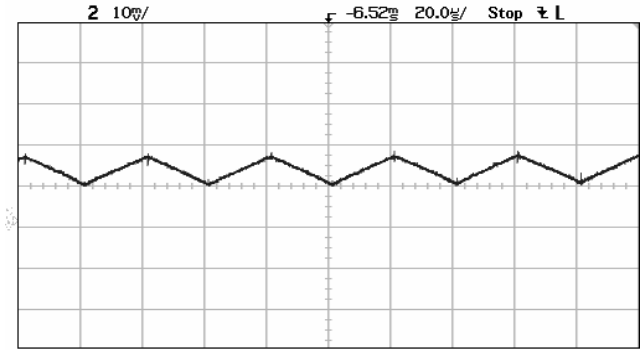


Fig. 20. Detail of conventional boost converter maximum input ripple at $220V_{RMS}$ ($I_{in}$ and $I_{L1}$ 2A/div).

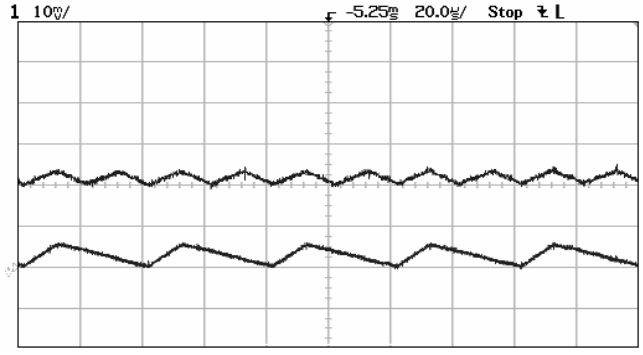


Fig. 21. Detail of interleaved boost converter maximum input ripple and inductor ripple at $220V_{RMS}$ ($I_{in}$(top) and $I_{L1}$(bottom) 2A/div).

## VI. CONCLUSIONS

This paper presents an improvement in the switching logic scheme of the interleaved boost converter. In this new technique the choice of the operation region is based on the duty cycle of the converter. Therefore, the choice of the operation region is related straight with the dynamic of the converter. The minimization of the input current ripple was obtained through the appropriate shifting of command signals applied to the switches. The concept of the switching logic technique was extended to *n* cells, and algorithms to implement the switching logic scheme were presented.

The simulation results of the interleaved boost converter, used for PFC, proved the advantages of the proposed logic scheme. This technique and the control system can be easily implemented by a low cost DSP.

The experimental results show the reduction of the interleaved boost converter input ripple, when another cell is added to the system. Since the amplitude of harmonic components, which now are related to high frequencies, are smaller than those obtained with the conventional boost converter, consequently the EMI input filter can be reduced.

In this way, the interleaved boost converter is a strong candidate for applications where a low input current ripple and low EMI emission are required, as telecommunications power supplies.

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