IMPLEMENTATION OF DIGITAL CONTROL FOR A DC-DC SOFT-SWITCHING PHASE-SHIFT FULL BRIDGE CONVERTER

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***Abstract* – The present work has as aim the development and implementation of a digital control system to the output stage of telecommunications power supply, FB-ZVS-PS converter, using the digital signal processor TMS320LF2407 from Texas Instruments. This project was motivated, not only by the digital control advantages such as flexibility and volume reduction, but also by the necessity of digital control technique development in single fase rectifiers. To accomplish this work it was necessary to propose an original digital solution of phase-shift control applied to FB-ZVS-PS converter. A prototype using a 600 W commercial supply's power lay-out was developed to validate this technique. Obtained results were extremely satisfactories standing out the dynamic behavior verified by reduced variations on the output voltage under load changes.**

***Keywords* – Power supply, digital control, DSP, telecommunications, FB-ZVS-PS.**

I. INTRODUCTION

Among the main applications of Power Electronics are the rectifying units that with the necessity of telephony system enlargement, as much of fixed telephony as mobile, and supplying of several equipments from batteries have become focus of many researches in the most varied technology centers. However, for applications in single-phase equipments, the structure of Boost PFC converter cascaded to FB-ZVS-PWM converter can be considered as a standard solution for its robustness and high income. With intention to perfect details in this structure, researches also had already been accomplished, but the current tonic is turned to questions of control and monitoring of the source.

Nowadays the necessity of conforming power supplies to a series of rigid security norms, electromagnetic compatibility and, in the case of telephony systems, psofometric noise, has demanded from the designers innovative solutions to keep their products in a competitive market. The use of digital control techniques is a world-wide trend and its studies have advanced for application in static converters, mainly when some analogic control techniques and some converters are already considered standard solutions for determined purpose. It can be pointed as the main advantages of the employment of a digital control:

- Flexibility on the controlling of converters.
- Volume reduction due to the number of functions that a processor can accomplish.
- Costs reduction on the product development.

This work consists on the development of a technique for the application of digital control using DSP TMS320LF2407 from Texas Instruments for the Soft-switching Phase-shift Full Bridge converter (FB-ZVS-PS) and its implementation in a prototype of 600 W. It was used a power circuit lay-out with commercial characteristics with intention of reproducing the difficulties found in the development of high power density equipments.

A. Converter characteristics

The main characteristics of the FB-ZVS-PS converter are:

- Maximum power = 600 W.
- Load current = 10 A.
- Switching frequency = 140 kHz.
- Input voltage = 400 V.
- Expected income = %.

The following figure presents the power structure of the FB-ZVS-PS converter employed.

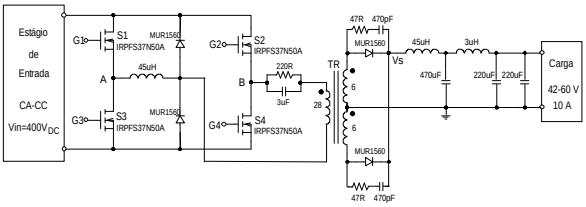

Fig. 1.1 – FB-ZVS-PS converter employed.

B. Digital signal processor characteristics

In this work was employed the Spectrum Digital's kit containing the DSP TMSLF2407 from Texas Instruments. Its basics characteristics are:

- Clock frequency = 30 MHz.
- 16 multiplexed analogic input ports.
- Conversion time ≅ 500 ns.
- Serial communication.
- 2 independent "event manager".
- 32-bit sum and product register.
- Appropriate instructions to applicate in control loops.
- Pipeline processing structure.

II. COMMAND STRATEGY

The technique of modulation used to control the output variable of the FB-ZVS-PS converter is the phase-shift modulation. Using the analogic control, the pulses are generated by the integrated circuit from the Phase-Shift Resonant Controllers family (Unitrode/Texas Instruments). Among them, the UC3875, UC3895 and UC3879 can be cited.

From the basic working of the FB-ZVS-PS converter, it is known that just the command of one of the arms must be controlled. Its command pulse is displaced in the time through the comparison of the control signal to a double switching frequency saw-tooth. The meeting points define the alternation between the states of the signal. The command of the other arm is fixed. It is important to mention that the displacement between the pulses is gradual, which guarantees the soft-start function.

The Fig 2.1 examples how these integrated define the command pulses of the S1 and S2 switches. The dead-band time is not considered.

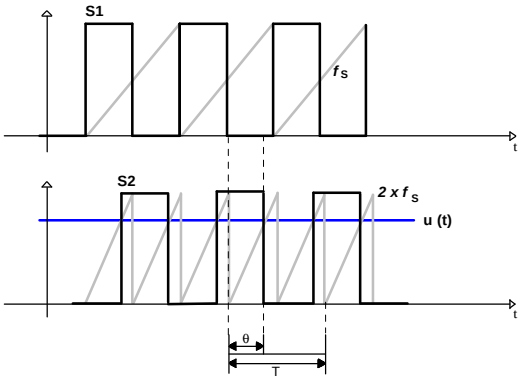

Fig. 2.1 – Command technique implemented by the integrated of the Phase-Shift Resonant Controllers family.

To implement this modulation using DSP TMS320LF2407 was opted for defining a new strategy to make possible the best use of the processor's peripherals. This way the update of the states of the command pulses would become less dependent of the programming and the definition of the dead-band time much more simplified.

In both strategies the command signal of S1 switch does not suffer any action of control and presents 50 % duty-cycle. The command signal of S2 switch, which was defined through the comparison of the control signal to a double switching frequency saw-tooth using a non-conventional technique in relation to the traditional PWM modulation, now comes back to use the traditional method comparing a control value to a numerical counter which acts as a digital saw-tooth. This method is extremely interesting for the DSP's PWM output employment, however it creates a difficulty for the displacement between the pulses. The developed solution was to vary the counting that defines the digital saw-tooth in one unit of its register, keeping fixed the pulse width. The digital compensator output control is compared to a reference value that determines the displacement between the pulses in the moment. From the result of this comparison will be defined if the period-counter referent to the command of S2 will be increased or decreased of one unit. This difference between the period-counters makes, naturally, the pulses displace themselves one in relation to the other in the time and still guarantees the soft-start function since the initial value of comparison is zero. When the displacement between the pulses reaches the desirable point, the period-counter referent to S2 reestablishes its nominal value and the displacement maintains itself fixed.

Following it is presented a simplified block diagram from the program working, where T_C and D_C are, respectively, the values used in the period and duty-cycle registers which define the waveforms of the DSP's PWM outputs.

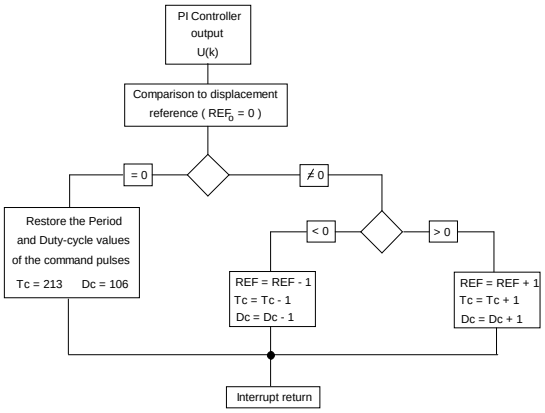

Fig. 2.2 – Algoritm block diagram which defines the command pulse displacement between the converter's switches.

To illustrate the implementation of this technique, the following figures present the command pulses applied to S1 and S2 switches applying the method of phase-shift control proposed. The values presented are illustrative.

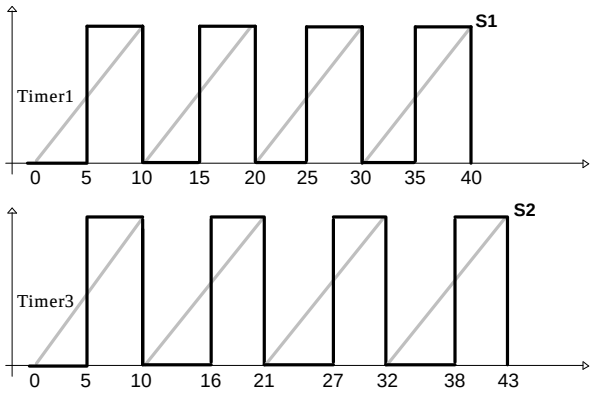

Fig. 2.3 – Example of the digital implementation of the phase-shift modulation proposed – 0° to 180°.

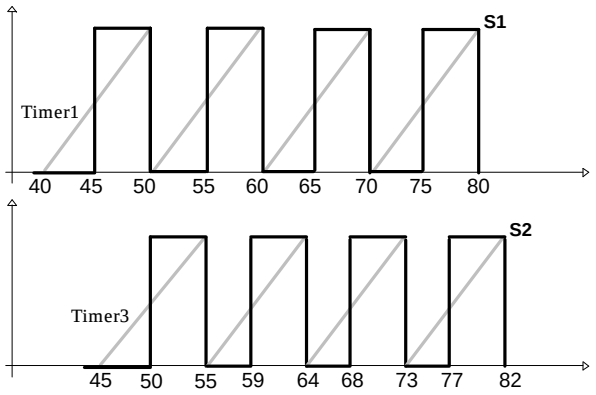

Fig. 2.4 – Example of the digital implementation of the phase-shift modulation proposed – 180° to 0°.

It is important to mention that this variation on the period counting makes the switching frequency of one arm vary in relation to the other. However, due to the operation speed of the processor, this difference is approximately ± 700 Hz what is well acceptable considering that the dedicate integrated circuit, already mentioned, present bigger differences.

III. CONTROLLER DESIGN

Using the model of PWM switch [1] in order to get the output characteristic of the converter presented in Fig. 1.1, meets a transference function of 7a. order due to the output filter used. Equation (1) presents the obtained converter model in symbolic form, being the coefficients following presented.

$$G(z)=\frac{N_6z^6-N_5z^5+N_4z^4-N_3z^3-N_2z^2+N_1z-N_0}{z^7-D_6z^6+D_5z^5-D_4z^4+D_3z^3-D_2z^2+D_1z-D_0} \quad (1)$$

N_6 = 0,00195	D_6 = 5,428
N_5 = 0,0073	D_5 = 12,27
N_4 = 0,0095	D_4 = 14,86
N_3 = 0,00393	D_3 = 10,29
N_2 = 0,00165	D_2 = 3,99
N_1 = 0,0018	D_1 = 0,777
N_0 = 0,00038	D_0 = 0,0551

The used filter, even so makes it difficult the mathematical treatment, presented good results about the psofometric noise reduction [2]. An approach for a model of 2a. order is unnecessary since using Matlab's RLTOOLS, the PI digital compensator could be projected using the direct method, or either, without the necessity of translating the calculated compensator between plans s and z.

For the design of the controller the modulator PWM, the voltage sampler and A/D converter gains and a 70 kHz cut-off frequency anti-aliasing filter have been still considered. It was adopted 140 kHz as sampling and switching frequency. Observing simultaneously the root locus, the step response, the phase margin and the crossover frequency through Matlab's RLTOOLS, it was defined the compensator to be used presented in (2), under the Telebrás norm. Among others points this norm defines that the static regulation of the output voltage must guarantee a maximum variation of ± 1% from the nominal value that corresponds approximately to ± 500 mV and that the maximum duration of the dinamic state must be 25 ms and the maximum output voltage error must be ± 8% from the adjusted voltage value for a 50% load variation.

$$C(z)=3{,}48\cdot\frac{z-0{,}977}{z-1} \quad (2)$$

From the definition of the plant and digital compensator models, it is interesting to observe the behavior of the complete system through the root locus diagram.

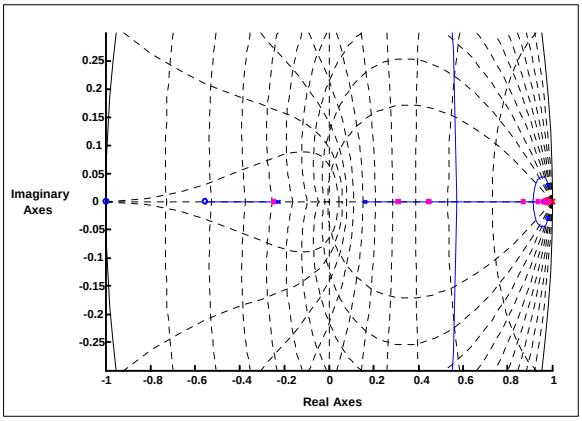

Fig. 3.1 – Root locus diagram of the compensated system.

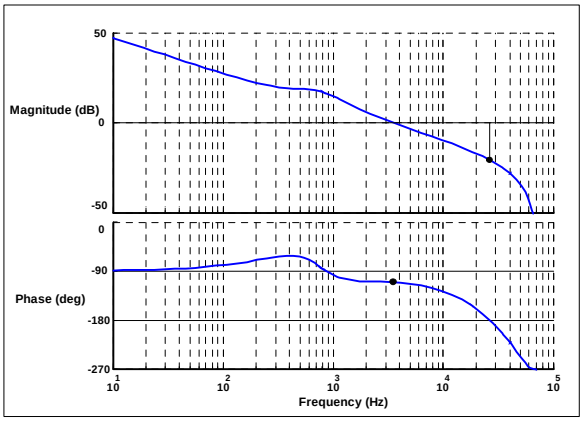

Fig. 3.2 – Root locus diagram of the compensated system.

The phase margin obtained was 64º and the crossing frequency, 4470 Hz. These values are adequate not only to guarantee good dinamic responses as also to control the output voltage in a range of frequency in which the psophometer is more sensible.

Another important analysis is to verify the step response of the system. In this case is verified an overshoot much bigger than what was observed in the experimental results. It happens because for software analysis was not possible to implement the soft-start characteristc employed by the command strategy.

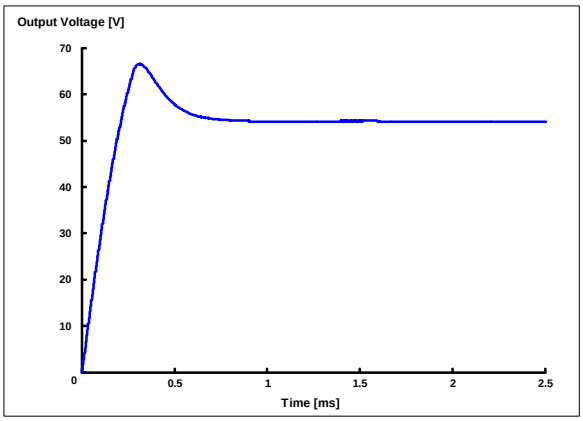

Fig. 3.3 – Step response.

IV. EXPERIMENTAL RESULTS

At first, before presenting the results about the output characteristics of the converter, it is important to present the voltage waveforms acquired on the S1 and S2 switches with the intention of demonstrating that the phase-shift modulation is being properly executed by the DSP, as well the voltage waveform on the node immediately previous to the output filter (node Vs – Fig. 1.1).

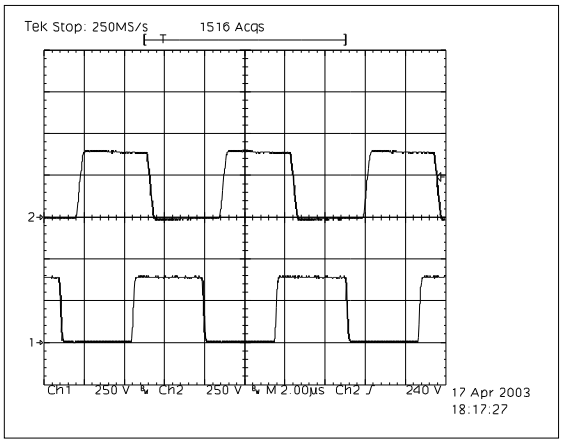

Fig. 4.1 – Voltage waveforms on S1 and S2 switches..

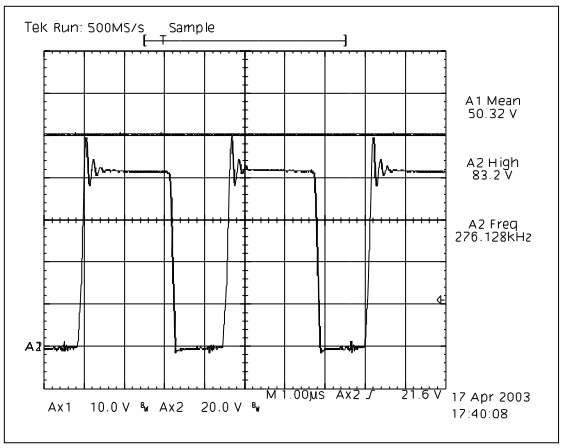

Fig. 4.2 – Rectifier and converter output voltage waveforms.

Calculating the static gain of the converter when applying the values of the duty-cycle measured, the calculated loss of duty-cycle and the transformation reason it is obtained approximately 50.3 V for which the output voltage was adjusted. This also can be calculated of direct form analyzing Fig. 4.2, since the output voltage of the rectifier already considers the loss of duty-cycle, the losses of the primary side and the transformer one. This way it is just to apply the static gain of the Buck converter.

Another important verification to be done about the command is the realization of the null voltage transition. This is what guarantees the ZVS characteristics. The following figure presents voltage and current waveforms on a critical leg switch. It can be noticed the soft-switching, since at any point of the ramps that define the transition state is verified alteration in their inclinations, what would characterize the forced switching.

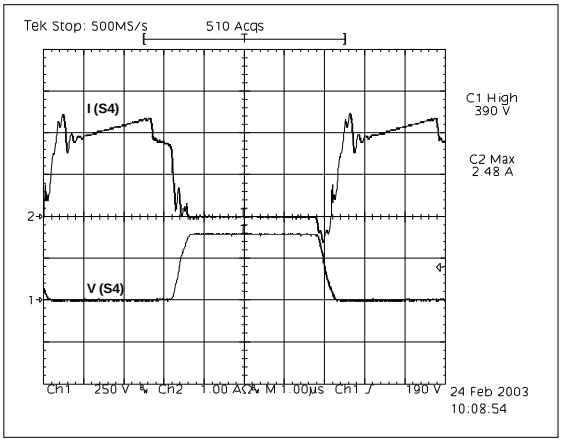

Fig. 4.3 – Critical leg switching with load current.

Fig. 4.4 presents load current and voltage waveforms. It can be observed, mainly in the current signal, the 120 Hz ondulation effect provoked for the input rectifier (capacitive filter rectifier). It influences the ondulation in the output voltage waveform presented in Fig. 4.5, even so it is among the limits of the Telebrás norms. Anyway it is necessary to reduce this ondulation, since psophometric analysis is strongly influenced by noises between 100 Hz and 2 kHz. .The ondulation measured in the input voltage of the FB-ZVS-PS converter was equal to 20 V and with the employment of the Boost converter with power factor correction, standard solution for single-phase rectifier units, it is expected that this ondulation does not exceed 12 V.

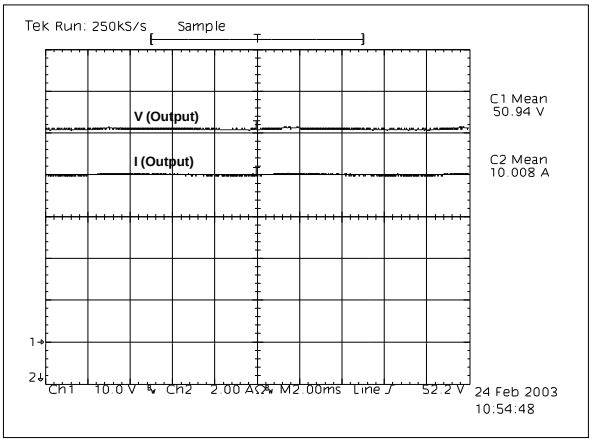

Fig. 4.4 – Output voltage and current.

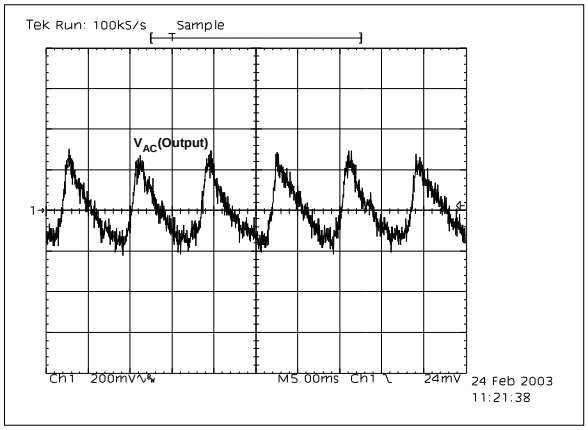

Fig. 4.5 – Output voltage ondulation.

The analysis of the dynamic characteristics of this converter mainly corresponds to the verification of the behavior of the output voltage in relation to load variations.

The dynamic regulation of the output voltage regulated by Telebrás norm [3] determines that the maximum duration of the transient-state must be 25 ms and its maximum overshoot must be ± 8% of the voltage value adjusted for a step of 50% of load. Due to the availability of load variation it was opted to work with steps of 70% of the nominal load. The following figures present the obtained results where is verified the norm attendance.

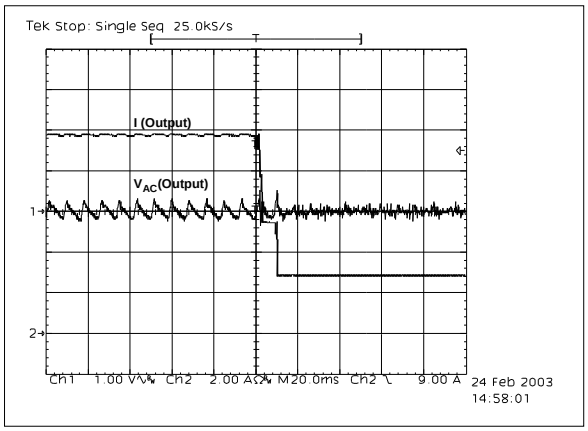

Fig. 4.6 – Voltage analysis for load withdrawal.

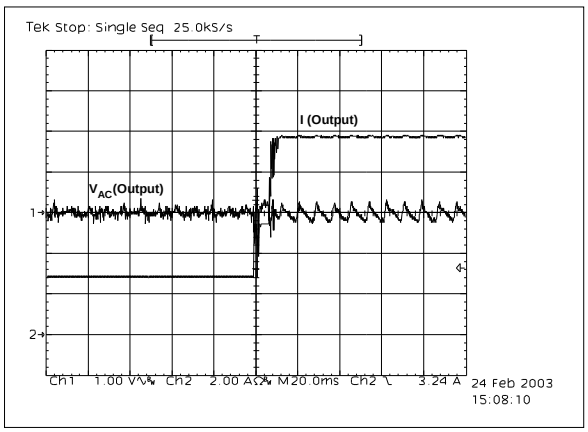

Fig. 4.7 – Voltage analysis for load insertion.

Although Telebras norm do not impose limits to a total load variation, it determines that the output variables stability should be kept. The Fig. 4.8 demonstrate that the proposed control attend the norm for a total load withdrawal that is the most severe condition to take the converter to instability.

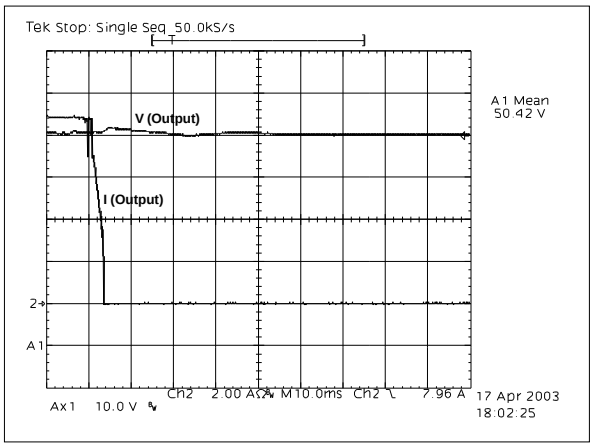

Fig. 4.8 – Total load withdrawal analysis.

V. CONCLUSION

The employment of digital techniques of control in static converters begins to show an important instrument of technological development in the Power Eletronics area. This way is possible to reach distinct performances from already well known structures. This is the case of the medium power Single-phase Rectifying Units with application in telephony systems and net security (UPS).

The FB-ZVS-PS converter cascaded to Boost PFC converter can be considered a standard solution for Single-phase Rectifying Units, due to its high performance, robustness and domain of the technology. Compared to Boost PFC converter, still exists a need for researches referring to digital control employed to the FB-ZVS-PS converter. It was the main motivation of this work, that reached the goal of implementing the output voltage control of FB-ZVS-PS converter using the digital processor DSP TMS320LF2407. An original solution was developed via software for the accomplishment of the phase-shift modulation.

All the obtained results have been considered satisfactory, standing out the performance in transitory regimen, since even submitting the converter to load variations bigger than that defined in norm, the variation voltage values stabilished by this was reached.

It can be quoted, as the main contributions of this work, to obtain practical results of the implementation of output voltage digital control of the FB-ZVS-PS converter, in view of, not only the established norms, as well as constructive aspects of the prototype and the development of a technique for the accomplishment of the phase-shift modulation integrally for software. This last one, how it was developed, besides of taking care of the necessities of control of the converter in study, also can be used in any other converter that makes use of this modulation, as the Three Levels converter.

ACKNOWLEDGEMENT

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