THREE PHASE FULL-BRIDGE C-DUMP CONVERTER COMMUTATION AND CONTROL STRATEGY APPLIED TO SWITCHED RELUCTANCE MOTOR DRIVES

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Abstract **- This paper presents new "C-Dump" topologies for switched reluctance motor drives: the "Full-bridge C-Dump converter" with and without the equalization leg. The increase in the number of switches is acceptable since a standard full bridge transistor module is used. The paper will also show the commutation and control strategy applied to these topologies. These topologies can be used to produce low-power, low-cost switched reluctance drives.**

Keywords **- Switched reluctance drives, Reluctance machines**

1. INTRODUCTION

The conventional C-Dump converter used for switched reluctance motor drives, first presented in 1985 [1], is shown in Fig. 1 where inductances L1, L2 and L3 represent the switched reluctance motor windings.

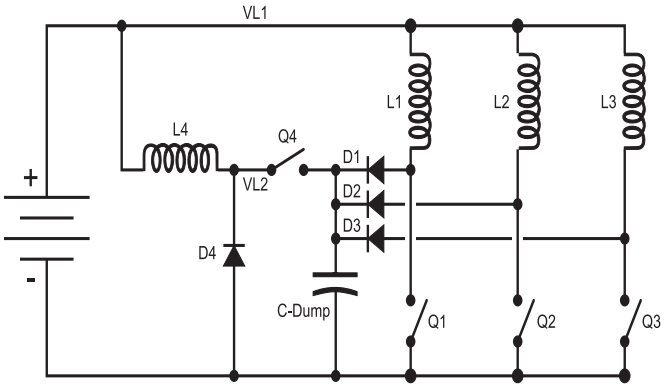

Fig. 1. Conventional C-Dump converter [1].

Further developments were made to eliminate the chopper inductor [2] and to increase converter efficiency [3].

The "2+1 C-Dump with equalization leg" topology presented in [4, 5, 6] is shown in Fig. 2.

The "2+1" name comes from the fact that currents in phases L2 and L3 are positive (according to the conventional C-Dump) and current in phase L1 flows in the opposite direction. This has no effect in the torque since the machine is based on the reluctance principle [8,9].

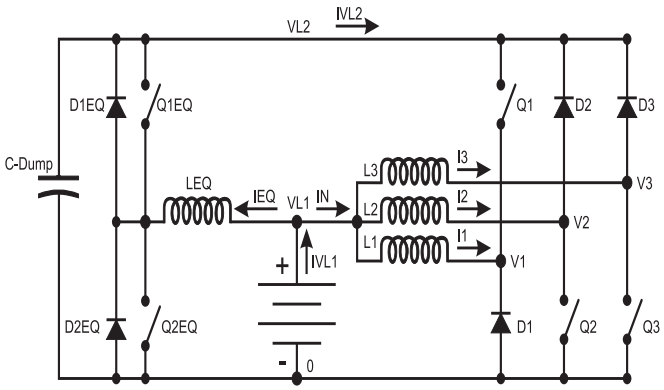

Fig. 2. "2+1 C-Dump converter with equalization leg converter" [4], including voltage and current symbols and conventions.

The "Full-bridge C-Dump converter with equalization leg", is shown in Fig. 3. The converter in the right-side of Fig. 3 uses a six transistor bridge module, with a rather low silicon utilization factor. Although the number of semiconductors has increased when compared with Fig. 1 one should consider that the full bridge is a low cost, large scale production component. This argument was also used in [7] but in that case the motor has non-standard connections and extra diodes connected inside the machine.

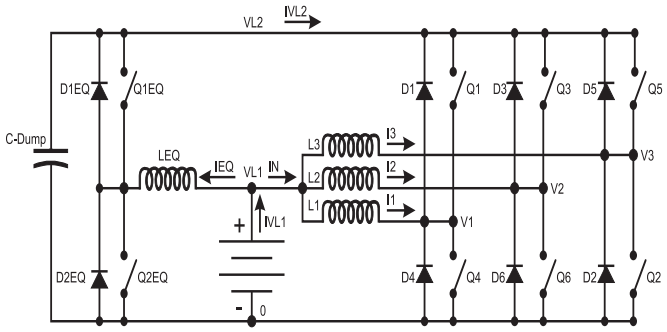

Fig. 3. "Full-Bridge C-Dump converter, with equalization leg", including voltage and current symbols and conventions.

Under special circumstances, **with appropriate control**, the equalization leg can be completely eliminated. The resultant topology is shown in Fig. 4 and is called the "Full-bridge C-Dump without equalization leg" or simply "Full-bridge C-Dump converter" [6]. The switched reluctance machine in Figs. 3 and 4 has a standard star connection.

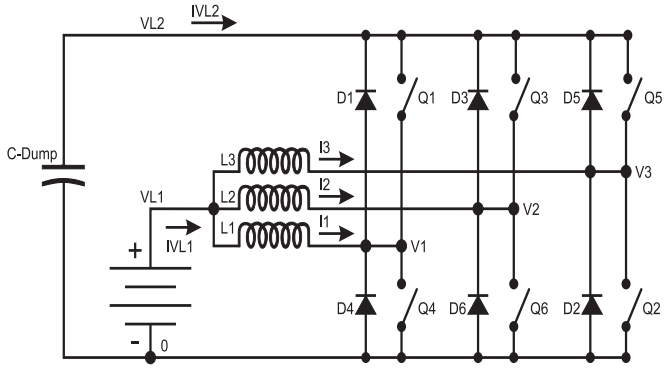

Fig. 4. "Full-Bridge C-Dump converter without equalization leg".

II. FULL-BRIDGE CONVERTER ANALYSIS, COMMUTATION AND CONTROL STRATEGY

The analysis of the "Full-Bridge C-Dump converter" shown in Fig. 3 is performed by dividing this arrangement in two sub-circuits. Figure 5 shows the "equalization leg" which is a conventional buck-boost chopper and keeps the VL2 voltage constant at the level VL2=2×VL1.

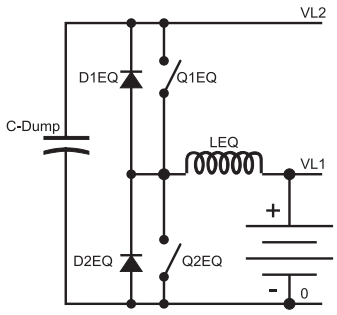

Fig.5.Equalization leg, with the C-Dump capacitor.

The "Full-bridge converter", which actually drives the switched reluctance machine, is shown in Fig. 6. The equalization leg is replaced by an ideal voltage source.

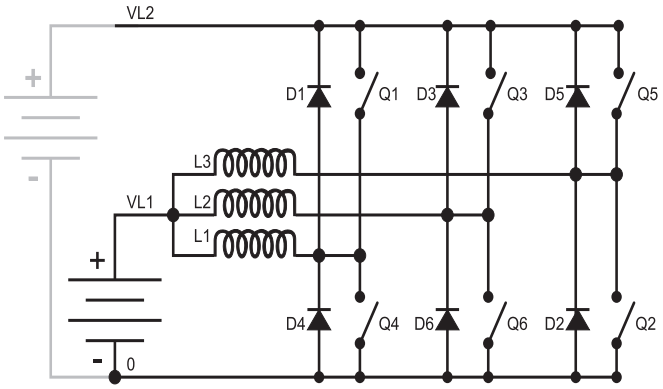

Fig. 6. Sub-circuit which shows the "Full-Bridge C-Dump converter" which actually drives the switched reluctance motor.

The sub-circuit shown in Fig. 6 can be decomposed in 8 different configurations which can be activated by the control circuit. These configurations are related to the conduction state of transistors Q1...Q6, and the most relevant configurations are shown in Figs. 7 to 10. In these figures the C-Dump capacitor, if sufficiently large, plays the role of the VL2 voltage supply.

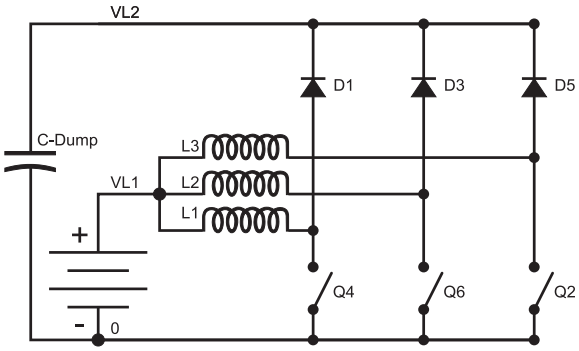

Fig. 7. "3+0" configuration where 3 transistors force current in the positive direction.

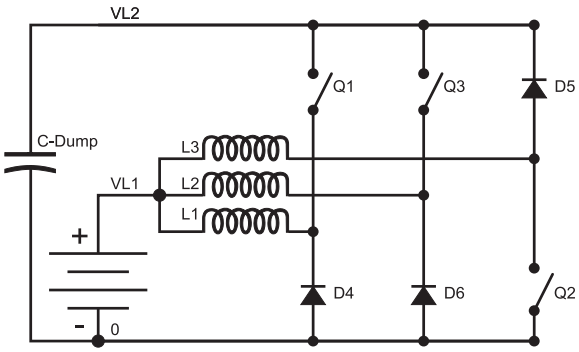

Fig. 8. "1+2" configuration where 1 transistor forces current in the positive direction and 2 other transistors in the negative direction.

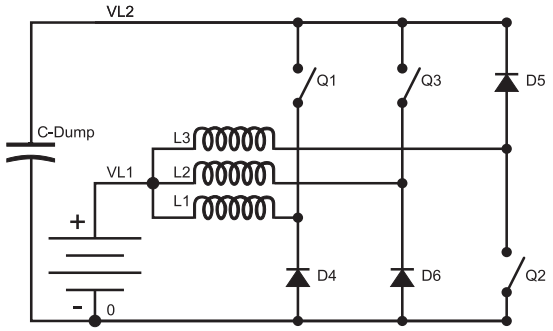

Fig. 9. "2+1" configuration where 2 transistors force current in the positive direction and 1 transistor in the negative direction.

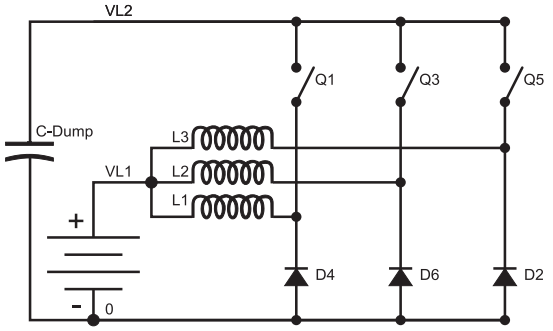

Fig. 10. "0+3" configuration where 3 transistors force current in the negative direction.

Table I presents all eight possible configurations using a "Full-bridge C-Dump converter".

Table I
Configurations in a "Full-bridge C-Dump converter"

Configuration			Current polarity			Active transistors		
Name	Number	Figure	L1	L2	L3			
"3+0"	111	7	+	+	+	Q4	Q6	Q2
"2+1"	110	N.A.	+	+	-	Q4	Q6	Q5
"2+1"	101	N.A.	+	-	+	Q4	Q3	Q2
"2+1"	11	9	-	+	+	Q1	Q6	Q2
"1+2"	100	N.A.	+	-	-	Q4	Q3	Q5
"1+2"	10	N.A.	-	+	-	Q1	Q6	Q5
"1+2"	1	8	-	-	+	Q1	Q3	Q2
"3+0"	0	10	-	-	-	Q1	Q3	Q5

Obs:
a) N.A. = figure is not presented due to space limitation;
b) Current polarity follows conventions of Fig. 3.

The question to be answered is: *"which one of these 8 configurations should be selected to drive the switched reluctance motor properly?"*

The best answer is that this choice should be made dynamically by the control circuit. Instead of adopting one single configuration (which was done in the "2+1 C-Dump arrangement" shown in Fig. 2, the choice is made just before the beginning of the conduction period of the a new phase.

Consider, for instance, that the winding L1 should begin conduction. One can choose between transistors Q4 or Q1. In the first case, the winding current will be positive (flowing from potential VL1 to potential 0). In the second case, the winding current will be negative (flowing from potential VL2 to VL1). The choice between Q4 and Q1 is an energy flux choice: *"which of these power supplies should be charged or discharged at a given instant?"*. If this decision is made dynamically it is possible to find a transistor command strategy which minimizes the power handled by the "equalization leg". In a limit condition, it is possible to eliminate completely this "equalization leg", which produces the "Full bridge C-Dump, without equalization leg", shown in Fig. 4.

The "2+1 C-Dump converter" shown in Fig. 2 can be understood as a particular case of the "Full-bridge C-Dump converter" shown in Figs. 3 and 4. By using the "Full-bridge C-Dump converter" the control can impose both positive or negative current at either phase, which corresponds to a bipolar current excitation. This choice is made at the beginning of the phase conduction and is closely related to the management of the C-Dump energy (voltage). The best policy is to use the stored energy directly in the consecutive motor phase, without using the equalization leg.

III. SIMULATION OF FULL-BRIDGE C-DUMP CONVERTER

The simulation program of the Full-Bridge C-Dump converter made with *Matlab/Simulin*k program [10] includes:

- inductances vary as a function of rotor angle;
- inductances vary as a function of current level (saturation);
- mutual inductances are neglected (they were measured and their values are low when compared to self inductances);
- semiconductor voltage drop is taken into account;
- all three phases are simulated since the current direction is different among phases;
- the same program can cover all converter topologies (the standard C-Dump, the 2+1 or 1+2 or 3+0 or 0+3 C-Dump and the Full-bridge C-Dump (with and without the equalization leg).

The control includes some standard features such as:

- phases can be controlled in "single-pulse mode" or with a current control loop (hysteresis band control);
- the commutation angles (θ_{ON} and θ_{OFF}) can be changed;
- the machine can be operated as a motor or generator

The main switched reluctance motor parameters (used for simulations and experimental measurements) are given in Table II.

Table II
Switched reluctance machine parameters

Number of phases	3
Stator poles	6
Rotor poles	4
Nominal speed (at nominal load conditions)	300 [rpm] = 31.42 [rd/s]
Mean torque	1.5 [N.m] (below 300 [rpm]
Power	47 [W]
Nominal voltage	12 [V]
Phase current	9.2 [A-peak] / 4.1 [ARMS]
Phase resistance	0.683 Ω at 20°C
Self inductance (max/min)	50.69 [mH] / 3.34 [mH]

To illustrate the "Full-Bridge C-Dump converter" operation, simulation results are presented in Figs. 11, 12 and 13, where the SR is operating as a motor.

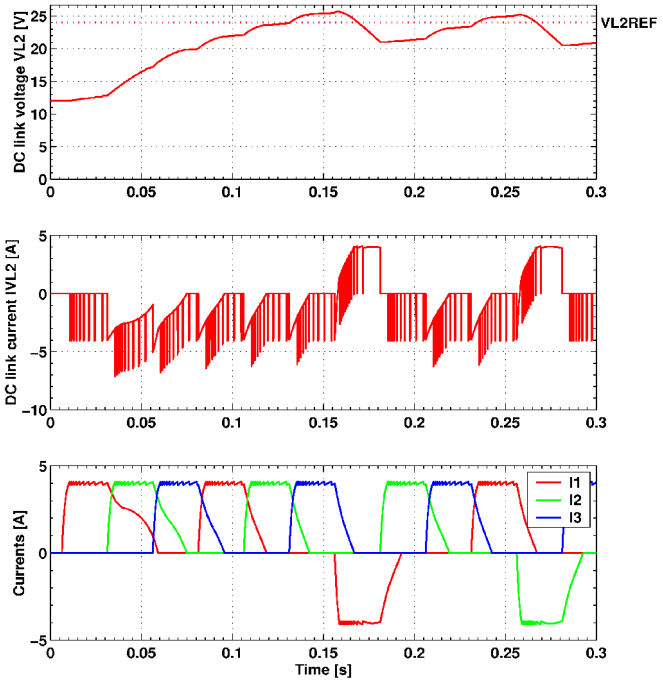

Fig. 11. (Upper figure) Voltage VL2; (central figure) DC link current IL2; (lower figure) Phase currents I1, I2 and I3, Current reference = 4 [A] and initial VL2=24 [V]. Obtained at 200 [rpm] and commutation angles θ_{ON} = -75° and θ_{OFF} = -15°.

The control chooses different polarities for the machine phase currents. According to these choices the C-Dump capacitor will charge/discharge along the time, as it can be seen in the upper part of Fig. 11. Despite this voltage fluctuation, currents in motor phases are balanced due to the hysteresis current control. Figure 11 depicts a *simulated* condition where the DC link #1 voltage VL1 was settled at 12V.

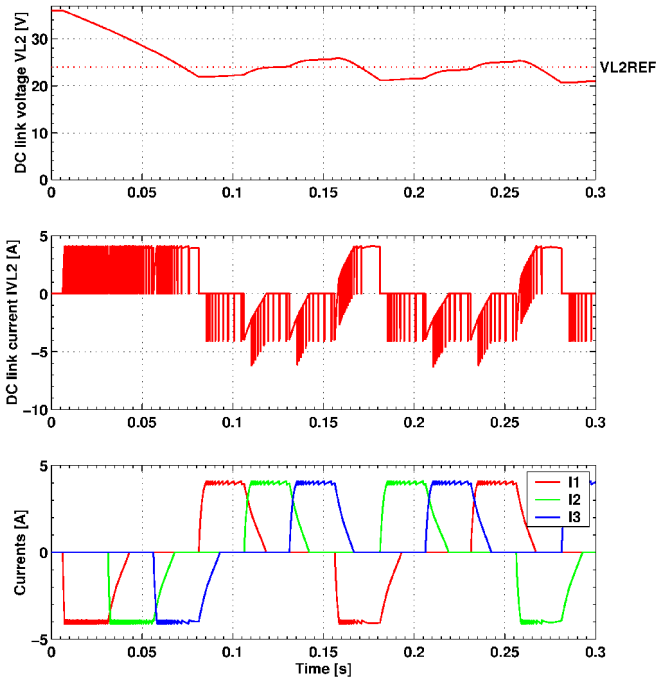

Fig. 12. (Upper figure) Voltage VL2; (central figure) DC link current IL2; (lower figure) Phase currents I1, I2 and I3, Current reference = 4 [A] and initial VL2=36 [V]. Results obtained at the same conditions of Fig. 11.

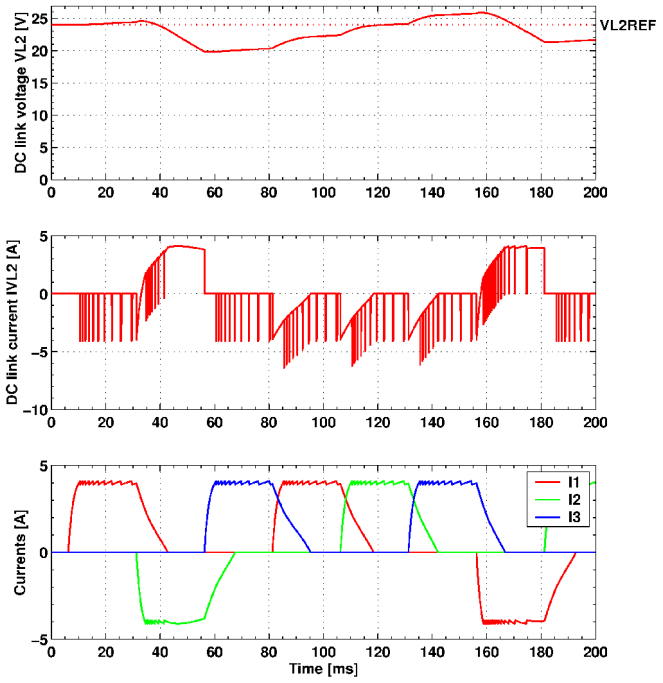

Fig. 13. (Upper figure) Voltage VL2; (central figure) DC link current IL2; (lower figure) Phase currents I1, I2 and I3, Current reference = 4 [A] and initial VL2=12 [V]. Results obtained at the same conditions of Fig. 11.

Figures 12 and 13 show the discharging and charging process of the C-Dump capacitor, when the *simulation* starts at different initial voltage conditions, 36V and 12V respectively.

It can be seen that the machine phase currents assume positive and negative directions and control is always able to bring this voltage VL2 near to the reference level.

IV. EXPERIMENTAL RESULTS OF FULL-BRIDGE C-DUMP CONVERTER

Some characteristics of the experimental arrangement are:

- switched reluctance parameters are given in Table II;
- the control operates in the single pulse mode;
- commutation angles (θ_{ON} and θ_{OFF}) are fixed;
- the hysteresis current controller is switched off;
- there is no current (torque) control loop;
- there is no speed control loop;
- the transistor choice is made dynamically, according to the configuration C-Dump capacitor voltage VL2. When this voltage is “low”, only the lower side transistors (Q4, Q6, Q2) are activated. When this voltage is “high”, only the higher side transistors (Q1, Q3, Q5) are activated;
- the criterium established for “low/high” voltage VL2 is a fixed level of 2xVL1 with an hysteresis band;
- the current signals are relatively noisy, due to the layout problems.

The main objective of the control was to demonstrate that the “Full-bridge C-Dump converter”.

The switched reluctance drive was kept at no-load conditions in Figs. 13, 14 and 15. The only change was the value of the C-Dump capacitor: 470, 940 and 2200µF respectively.

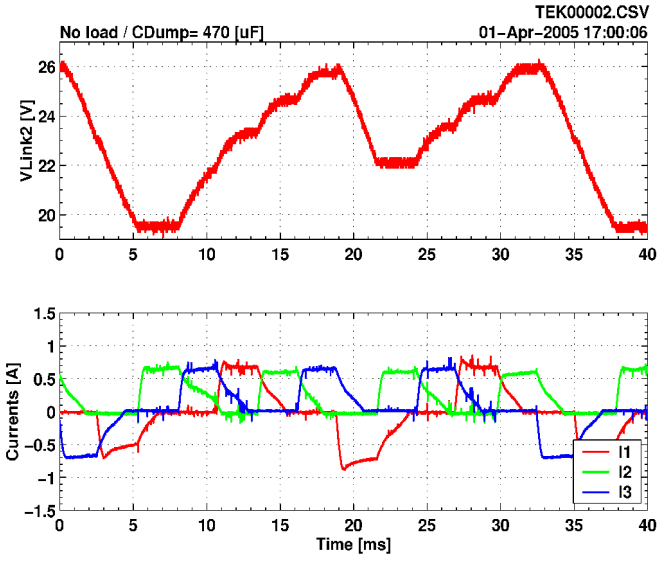

Fig. 14. Experimental results with C-Dump capacitor=470 µF and motor running at no-load conditions. (Upper figure) Voltage VL2. (Lower figure) Phase currents I1, I2 and I3.

Comparing these 3 figures one can see that the voltage fluctuation (shown in the upper part of Figs. 13, 14 and 15) decreases when the capacitor increases, as expected.

Analysis of phase currents I1, I2 and I3 (shown in the lower part of Figs. 13, 14 and 15) enables the following conclusions:

- although the voltage fluctuation affects the shape of individual current pulses the control is able to establish a “long term mean pulse” which could be acceptable in terms of torque ripple.
- when a smaller capacitor is being used the discharge period requires typically one single pulse at t~20 ms. Larger capacitors will require more pulses to discharge the C-Dump capacitor, which can be seen in Fig. 15 (2 discharge pulses at t~20 ms) and Fig. 16 (3 pulses at t~20 ms);

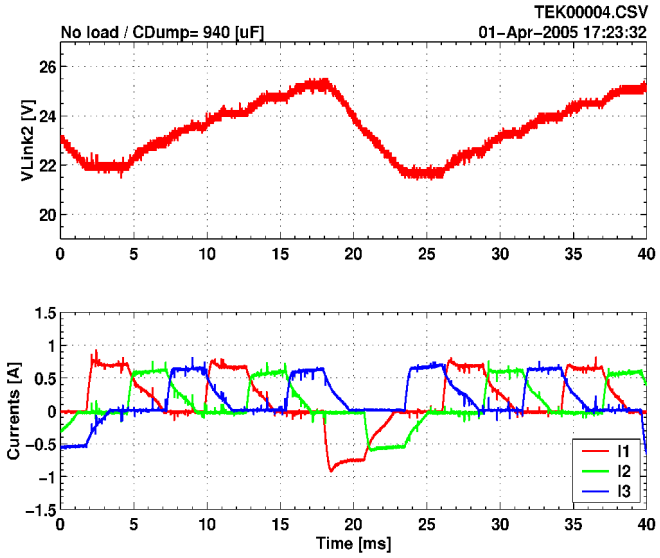

Fig. 15. Experimental results with C-Dump capacitor=940 µF and motor running at no-load conditions. (Upper figure) Voltage VL2. (Lower figure) Phase currents I1, I2 and I3.

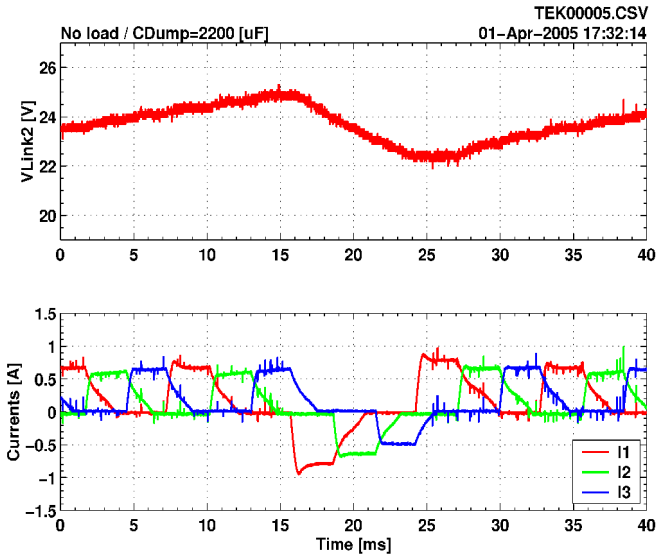

Fig. 16. Experimental results with C-Dump capacitor=2200 µF and motor running at no-load conditions. (Upper figure) Voltage VL2. (Lower figure) Phase currents I1, I2 and I3.

The mechanical load of the switched reluctance motor was changed in Figs. 16, 17 and 18 while keeping the C-Dump capacitor fixed at 2200µF. The mechanical load is referred qualitatively as “no-load” , “medium load” or “high load”.

Comparing these 3 figures one can see that the current pulse magnitude (shown in the lower part of Figs. 13, 14 and 15) increases when the mechanical load increases, as expected. As a consequence of these larger currents the number of discharging pulses decrease.

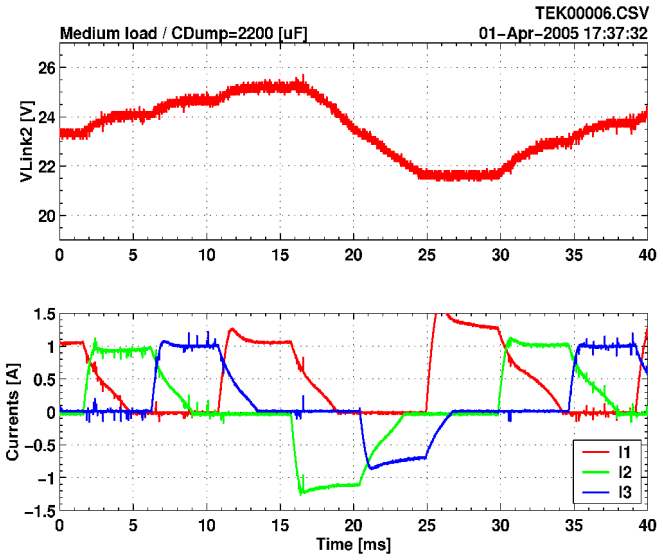

Fig. 17. Experimental results with C-Dump capacitor=2200 µF and motor running at “medium” load conditions. (Upper figure) Voltage VL2. (Lower figure) Phase currents I1, I2 and I3.

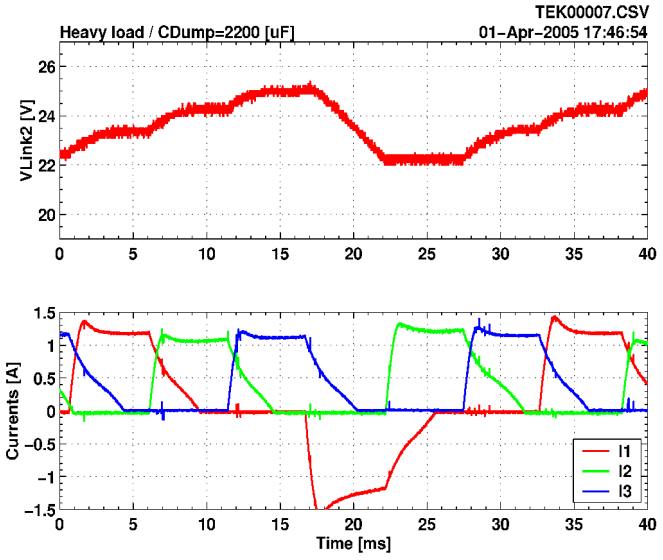

Fig. 18. Experimental results with C-Dump capacitor=2200 µF and motor running at “high” load conditions. (Upper figure) Voltage VL2. (Lower figure) Phase currents I1, I2 and I3.

It can be noticed from Figs. 16, 17 and 18 that although the voltage fluctuation affects the shape of individual current pulses the control is able to establish a “long term mean pulse” which could be acceptable in terms of torque ripple.

Figures 19, 20 and 21 show the C-Dump capacitor voltage and current at three different mechanical loads of the switched reluctance motor, referred qualitatively as “no-load” , “medium load” or “high load”. The C-Dump capacitor is kept fixed at 2200µF.

Comparing these 3 figures one can see that the current pulse magnitude (shown in the lower part of Figs. 19, 20 and 21) increases when the mechanical load increases, as expected. As a consequence of these larger currents the number of discharging pulses decrease.

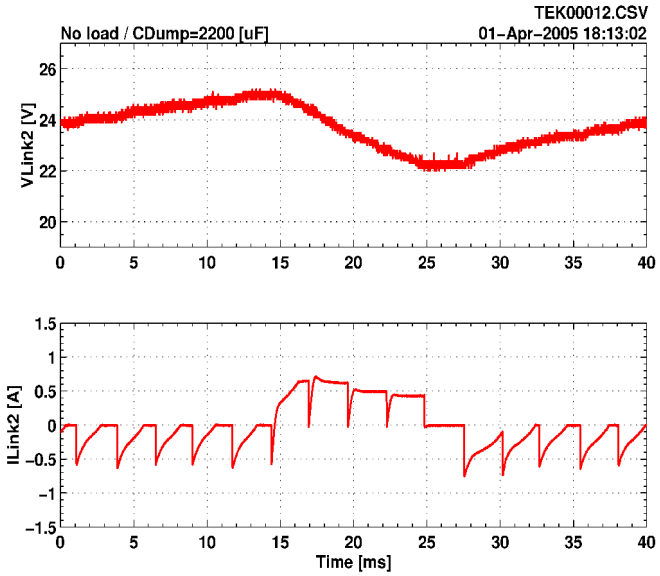

Fig. 19. Experimental results with C-Dump capacitor=2200 µF and motor running at no-load conditions. (Upper figure) Voltage VL2. (Lower figure) Current on C-Dump capacitor.

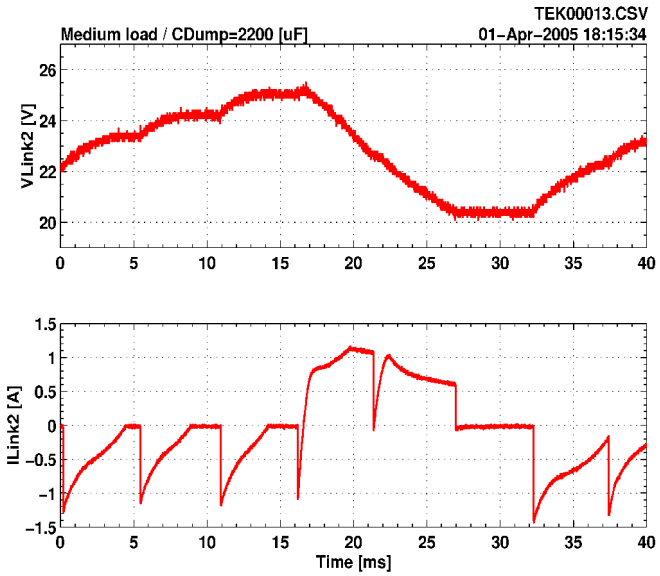

Fig. 20. Experimental results with C-Dump capacitor=2200 µF and motor running at “medium” load conditions. (Upper figure) Voltage VL2. (Lower figure) Current on C-Dump capacitor.

A closer look at the ILINK2 current shown in Figs. 18, 19 and 20 enables the following conclusions:

- the "long term mean value" of this current is zero, since the "long term mean VLINK2 voltage" is kept constant;
- the C-Dump capacitor charging current (negative, according to Fig. 4 convention) corresponds to the demagnetizing current of the switched reluctance machine phases;
- this negative current charges the C-Dump capacitor through one of the diodes D1, D3 or D5;
- when the C-Dump capacitor voltage is relatively low, the demagnetizing interval is longer;
- the C-Dump discharging current (positive) corresponds to the activation of one of the Q1, Q3, Q5 transistors.

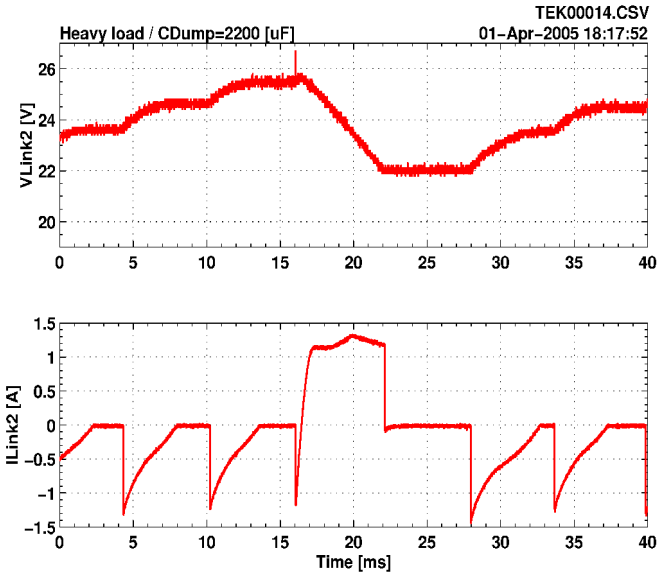

Fig. 21. Experimental results with C-Dump capacitor=2200 µF and motor running at "high" load conditions. (Upper figure) Voltage VL2. (Lower figure) Current on C-Dump capacitor.

V. SPECIAL CONTROL CONSIDERATIONS

This topic discusses two control aspects of the Full-bridge C-Dump converter without equalization leg:

- the "voltage buildup interval" of the C-Dump capacitor;
- the current control when the switched reluctance drive operates in the single-pulse mode.

A. The "voltage buildup interval"

When the switched reluctance drive begins to operate, the C-Dump capacitor voltage VL2 is equal to VL1 (see Fig. 4). At the end of this "voltage buildup interval" the C-Dump capacitor voltage should reach a nominal VL2=2×VL1 condition. There are two control strategies that can be adopted:

A1. The control switches one single phase of the machine (consider Q4 as an example). This action will direct all the demagnetizing energy of phase L1 to the C-Dump capacitor through diode D1. As soon the voltage VL2 reaches the nominal level (2×VL1) the motor phases start switching consecutively. During this charging period eventually the rotor will align one of its poles with stator phase L1, increasing this inductance to its maximum value. In this first strategy the "voltage buildup interval" is independent of the running period of the switched reluctance drive.

A2. In second control strategy the switched reluctance drive starts running during the "voltage buildup interval". In this strategy the transistors Q2, Q4 and Q6, which are connected to the ground potential, are switched consecutively. Since the C-Dump capacitor is initially discharged, these first demagnetization will take a longer period.

B. Operation in the "single pulse mode"

The C-Dump capacitor voltage will fluctuate around the nominal value VL2=2×VL1 (see Figs. 11 to 21) and will depend on several characteristics such as:

- C-Dump capacitor value;
- switched reluctance machine inductances;
- θ_{ON} and θ_{OFF} commutation angles;
- switched reluctance machine demagnetizing energy.

The main point is *"how to make the current control (torque control) independent of this unavoidable voltage fluctuation?"*. The answer will depend of the transistor operating mode. When the switched reluctance drive operates at lower speed the transistors normally operate at the "chopped" mode. At higher speed the phases are normally driven by a single pulse.

B1. When the transistors are "chopped" normally exists some sort of hysteresis current control. Simulations presented in Figs. 11 to 13 show how this current loop is able to keep the current within the hysteresis band despite the fluctuation of the C-Dump capacitor voltage.

B2. When the transistors operate in the single pulse mode this voltage fluctuation will affect directly the current magnitude of each pulse. This can be seen in the experimental results shown in Figs. 14 to 18. One solution is to accept this torque ripple, considering a given C-Dump capacitor value. A more sophisticated solution would be to change dynamically the commutation angles (θ_{ON} and θ_{OFF}) in order to increase/decrease the magnitude of the individual current pulses. Normally this commutation angle adjustment is made in order to optimize the torque/current ratio of the switched reluctance drive and it takes the mechanical speed and torque (which change relatively slowly) as the input variables of a commutation angle look-up table. The proposal is to adjust slightly these commutation angles in order to decrease/increase the individual magnitude of the current pulses. Consider, as an example, that there is a

pair of optimum commutation angles (θ_{ON} and θ_{OFF}) for a given operating speed/torque condition. If the C-Dump voltage level is high (compared to the nominal value) and that one of the upper side transistors will be the next to be switched, it is possible to estimate a small delay that will be applied on θ_{ON} in order to decrease the magnitude of that particular pulse.

VI. CONCLUSION

This paper presented the "Full bridge C-Dump converter", with and without the equalization leg. Elimination of this equalization leg is very attractive since it will reduce semiconductor number and also eliminate the L4 inductor (see Fig. 1) which existed in all previous C-Dump topologies.

The "Full bridge C-Dump converter" was simulated and experimental results were presented. Several control details were presented, which solve the main issues caused by the fluctuation of the C-Dump capacitor voltage.

The main contribution of this work is the use of standard full bridge transistor modules, which have low-cost and a large volume production, to drive switched reluctance machines. These machines can be easily assembled since they require no special winding connections.

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REFERENCES

[1] Bass, J.T.; Ehsani, M.; Miller, T.J.E.; Steigerwald, R.L. *Development of a unipolar converter for variable reluctance motor drives.* IEEE Industry Application Society Conference IAS 85, pp. 1062-1068, 1985.

[2] Hava, A.M.; Blasko, V.; Lipo, T. A. *A modified C-Dump converter for variable- reluctance machines.* IEEE Transactions on Industry Applications, Vol. 28, No. 5, pp. 1017-1022, September/October 1992.

[3] Mir, S.; Husain, I.; Elbuluk, M.E. *Energy-efficient C-dump converters for switched reluctance motors.* IEEE Transactions on Power Electronics, Vol. 12, No. 5, pp. 912-921, September, 1997.

[4] Silva, W.M.; Paula, P.P.; Goldemberg, C.; Tersarioli, V.; Souza, D.R.; Bossche, A.V.D. *Analysis of low cost switched reluctance motor drives topologies: 2+1 C-dump and the 2+1 with double supply*. 10th European Conference on Power Electronics and Applications, EPE2003, Toulouse, France, 2003.

[5] Silva, W.M.; *Proposal of new "C-Dump" topologies for switched reluctance motors and generator drives.* PhD thesis, University of Sao Paulo, 2004.

[6] Silva, W.M.; Goldemberg, C.; Bossche, A.V.D. *New C-Dump topologies for switched reluctance motor drives.* 16th International Conference on Electrical Machines, ICEM2004, Cracow, Poland, 2004.

[7] Clothier, A.C.; Mecrow, B.C. *The use of three phase bridge inverters with switched reluctance drives.* EMD97 Conference Proceedings, pp.351-355, 1997.

[8] Krishnan, R. *Switched reluctance motor drives, modeling, simulation, analysis, design and applications.* CRC Press, 2001.

[9] Miller, T.J.E., *Switched reluctance motors and their control.* Clarendon Press, Oxford, 1993.

[10] Matlab-Version 6.5; The MathWorks Inc., 2002