A HIGH PERFORMANCE 62KW ZCT SVM PFC POWER SUPPLY FOR USE WITH A AC PLASMA TORCH

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Abstract – **This paper describes the concept, the project and simulation of a 62kW three phase ZCT SVM PFC power supply for feed a DC/AC power supply plasma torch used in a waste treatment plant. The power stage is built on an industrial IGBT three-phase bridge rectifier module configured in a boost rectifier topology that supplies the adjustable 550~800V_{DC} output voltage. ZCT soft switching and SVM techniques were simulated to minimize the rectifier structure commutation losses. A DSP unit executes the running sequence, the PFC, the SVM and the main programming parameters as well as the protection function of the associated subsystems. Simulations in Simulink and PSpice were implemented to aid the definition of the boost rectifier topology and predict the results. This paper highlights the PWM boost rectifier, the SVM and the ZCT soft-switching.**

***Keywords* – Power factor correction (PFC), three-phase boost rectifier, ZCT soft switching, PWM power supply, space vector modulation (SVM).**

I. INTRODUCTION

In order to have this work context well situated and to understand the proposed development importance of this project, it is necessary to remind the recent exigencies imposed by the environmental legislation, national agencies of regulation (CONAM, ANVISA, etc.) and other federal, state and municipal inspection orgs demanding the industrial and medical sector to provide the adequate treatment and an appropriate destination for the produced waste [1, 8-11]. Due to the processing, storage and discard high costs produced by the new environmental exigencies, it is important to considerate the aggregated value to the waste. The non-organic components can be recycled or vitrified, and the organic parts can be dissociated in order to generate synthesis gases, thermal and/or electrical energy in co-generation scheme.

The described three-phase with power factor correction (PFC) power supply is destined to have a part of an experimental waste treatment plant using the thermal plasma techniques to destroy industrial waste [12-14]. A three-phase PFC power supply, a non-transferred AC plasma torch, a process reactor and its associated auxiliary systems essentially constitute the main elements plant. This project intends to offer a significant contribution to the research line on electrical power conversion systems, held by the automation and control systems area of the UFRN-PPgEE. Also, it represents an effort to attempt the university-industry integration program [2], by offering effective local solutions for the industrial park demand. Once explained the finality of this project, let's highlight the power supply's technical aspects.

Although many achievements have been made in the design and manufacturing of high power semiconductor devices, high power converters still suffer a lot from low switching frequency due to high switching losses an high switching stress. Poor control bandwidth, large passive components, and high switching noise are the problems associated with low switching frequency. One of the solutions to reduce the switching loss and stress is to use a soft switching technique. This can shape de rising and falling edges of switch current and voltage waveforms. Therefore, *dV/dt* and *di/dt* can be reduced. Meanwhile, switches can be turned on and off under zero current or voltage, which means much less switching loss. The most practical soft switching techniques developed currently are zero voltage transition (ZVT) PWM and zero current transition (ZCT) PWM. In the past several years, various ZVT and ZCT techniques have been proposed. The ZCT technique is more preferred because it can absorb the parasitic inductance along the distributed DC bus while ZVT cannot. The adopted ZCT technique can achieve zero current switching for all of the main and auxiliary switches and theirs anti-parallel diodes. Turn off loss can be almost eliminated. The diode reverse recovery and turn on loss also can be almost removed.

The importance of PFC energy quality can be seen in [15-19].

The topology for the presented three-phase PFC rectifier is shown in figure 1. Snubbers are totally removed in this soft switching scheme.

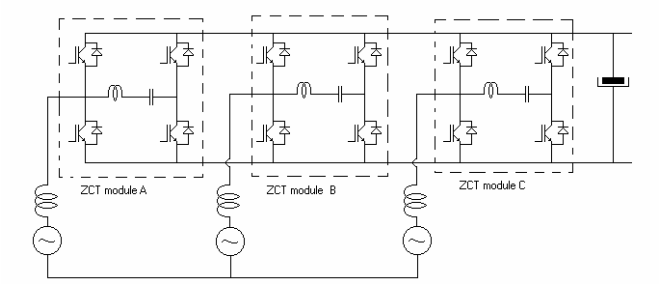


Fig. 1. Topology of three-phase ZCT boost rectifier

II. SYSTEM OVERVIEW

The whole system is comprised of the power stage, digital controller and interface as shown in figure 2.

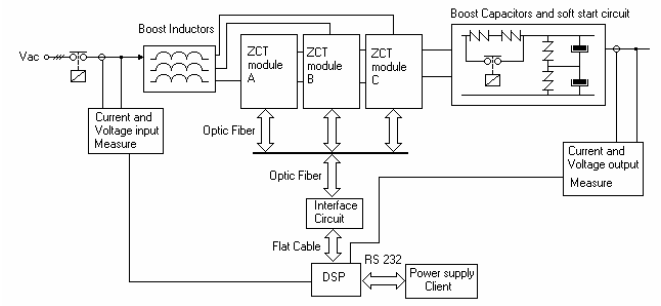


Fig. 2. Over all system structure

The power switch stage includes the main IGBT module (150A/1200V), and auxiliary IGBT module (100A/1200V), IGBT gate drive boards and a sensor board. There are three resonant tanks on the top of each ZCT module. The elements design follows [18-22] recommendations.

The input and output voltage sensors will be based on the opto-coupler 4N25 linear bandwidth and the current measurements will use a Hall Effect sensor that garanties the galvanic decoupling between the control circuit and the power stage. A soft-start circuit on the capacitor will be need due to the high currents in the transitory provoked by the capacitor's DC bus uncharged initial state as can be shown in figure 2. Two 320K resistors were projected as to maintain the charge balance between the capacitors as to provide a discharge way when the power supply is turned off.

The main booster's inductors and capacitors were designs in agree with [4] to produce a current ripple less then 3% and a voltage ripple less then 1%. The inductor's value are 1mH, built on a I/C alloy core with 0,5 mm width boards. The two 3.3mF and 450V electrolytic capacitors will be serie connected as shown in figure 2. The resonant tank was designed to make the peak resonant current I_{pk} exceed the instantaneous maximal boost inductor current in order to achieve ZCT operation. However, the trade-off has to be made when choosing I_{pk} and the resonant period T_o. If T_o is long and I_{pk} is high, the conduction loss and duty cycle loss caused by the soft switching will be high. If T_o is short and I_{pk} is low, they will have a negative effect on switching loss and stress reduction. The resonant period is chosen as *3us* because the minimum dead band that the driver allows is *3,25us*. Based on equations (2.1)-(2.3), the resonant inductor L_r and resonant capacitor C_r can be selected. V_o is the dc bus voltage in equation (2.3). In this ZCT rectifier, the resonant tank was designed to *Lr=2,89uH* and *Cr=145nF*.

$$T_0 = 2\pi\sqrt{L_r C_r} \qquad (2.1)$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \qquad (2.2)$$

$$I_{pk} = \frac{V_0}{Z_0} \qquad (2.3)$$

As this rectifier will produce an adjustable output voltage from 550 to 800 V_{DC}, the soft switching isn't possible in the whole operation band. When the desired output voltage is close to 550V, the pulse width tends to be short and this obliges to overlap the auxiliary arm's waveforms, so overlapping the turn-on and turn-off cycle. Thus, it was necessary design snubber's circuits.

There is an interface board that acts as a connector between the PWM electrical signals from the DSP and the optical signal to the IGBT gate driver boards such as collecting fault signals from IGBT gate drivers.

This effectively can make the controller much more immune to noise. Another potential benefit brought by optic fibers is to minimize the number of wires between the controller and power stage.

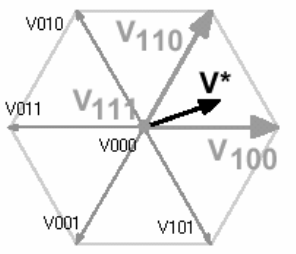
The digital signal processor (DSP) will be a TMS320F2812. The DSP will perform the control algorithms, timing control, A/D D/A data flow control such as the voltage space vector synthesizer. Due to the flexibility of the digital controller, this converter can be configured as a rectifier or inverter, with hard switching or with soft switching in a minute.

The interface board acts as a relay for distributing PWM signals from the controller to the ZCT modules and collecting fault signals from IGBT gate drivers.

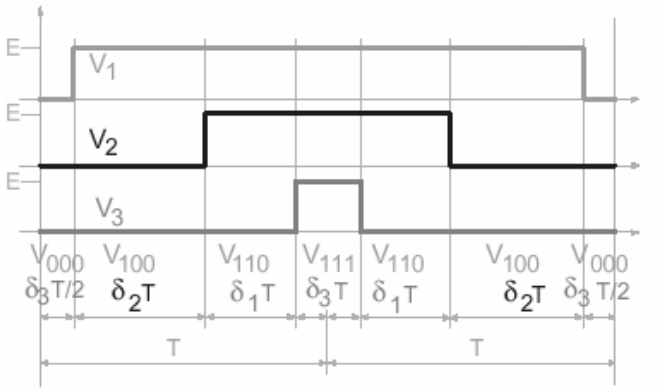
III. SVM SCHEME AND ZCT OPERATION PRINCIPLE

A. PWM Space Vector Modulation Scheme [5-6]

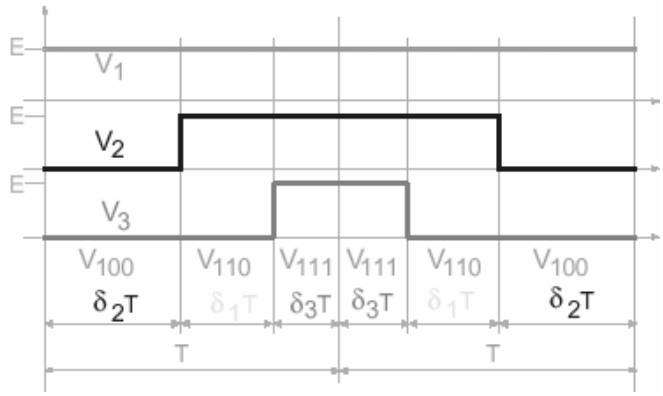
A vector can represent three-phase variables. A voltage vector *V** is used here to represent the three-phase voltages after the boost inductors of the rectifier, which are generated by switching the DC link voltage. There are eight valid switching combinations available for this topology, which are called space vectors, shown in figure 3. There are enormously different SVM schemes. Different SVM schemes can cause different switching losses and total harmonic distortion (THD).



(a)



(b)



(c)

Fig. 3. (a)Voltage Space Vector Hexagon; (b) SVM for low THD; (c) Proposed SVM

For the PFC rectifier, it is critical to improve the control bandwidth to achieve high performance. First, adjacent vectors are selected to synthesize the reference voltage vector and minimize the circulating energy as shown in figure 3(a). Second, the phase carrying the highest current does not switch at all via a properly selected zero vector as shown in figure 3(c). This method can save 33,33% of switching loss compared with the SVM normally used to get the low THD as shown in figure 3(b). Thus, switching loss can be reduced significantly while not introducing much distortion. Third, the sequence of the output vectors is arranged to double the sampling frequency while keeping the switching frequency the same. In every two consecutive sampling cycles, the sequence of the output space vectors flips. Each phase leg only has one switching action at most in every two sampling cycles. In the real setup the sampling frequency can be set do 40kHz while the switching frequency is 20kHz. Therefore the control bandwidth of this PFC can be pushed to several kilohertz. Additionally, the duty cycle of the second sampling cycle does not change much in steady state. The symmetry of the PWM signals means less THD. This space vector modulation scheme is easy to implement by a digital controller. It is suitable for three-phase inverters as well.

B. Improved ZCT Operation Illustration

The operation of each ZCT module is exactly the same. For the purpose of simplification, here we use phase A ZCT module as an example of the soft switching operation analysis, shown in figure 4. The relationship between the main switch and its corresponding auxiliary switch in one module topology is diagonal. This means the timing control of S2 is related with S2x. On the other hand, S1 is related with S1x.

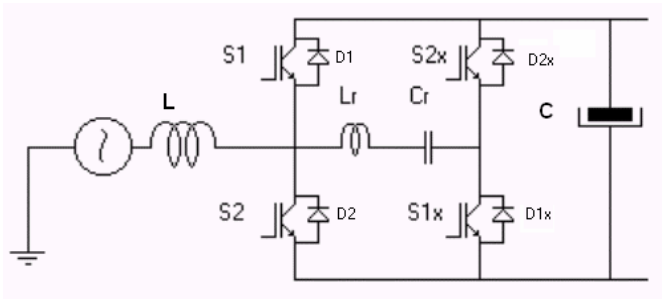


Fig. 4. Topology of one ZCT stage

Two sampling cycles are enough for soft switching operation analysis in this system. Assume the location of voltage vector *V** is as shown in Figure 3(a). The amplitude of phase A current (positive) is the largest because of the PFC operation. Only the phase B and C are switching. The space vector chosen should be V_{111}, V_{110} and V_{100}, which is shown in Fig 3(c). The key waveforms and the control timings are shown in Figure 5, where we can see a complete soft switching cycle. These waveforms were achieved by PSpice® simulation. The graphs of the elements that haven't current were suppressed.

Assume the current in boost inductor *L* and the voltage across output capacitor *C* is constant due to their large values.

The demonstration period, from *65us* to about *71us* is the turn-on transition. The resonant inductor controls the *di/dt* of the main switch current. Therefore, *di/dt* is less than in a hard switching scenario.

The demonstration period, from *90us* to about *100us* is the turn-off transition. After *97us* V_{Cr} is charged to positive, and is then ready for the next turn-on transition.

Note in Figure 6 that the turn-on and turn-off transition occurs under very low current, this reduce a lot the switching loss in S2. Now we will explain this sample period step by step and you can keep the idea for the rest of the time.

At the beginning D1 is conducting all the 143A imposed by the boost inductor that works as a current source. This happens because of the dead time. *Cr* is charged with the output voltage (V_0 *=800V).* In Figure 5 we can see those initial conditions.

At *67us* S2x is turned on, so the resonant tanks start to resonate. The positive voltage on *Cr* imposes a current that pass by *Lr*, D1 and S2x. This current increases until *68us* when start to decrease.

After *68us* the current across *Lr* flips and start to oppose to the current across D1. At *70us* the current across D1 is almost zero and we can switch S2 under ZCT. Now, the current across S2 increases very fast. At the same time the current across *Lr* decrease at the same proportion. At *70us* S2x is turned-off what obliges D2x to conduct due to the energy in *Lr*.

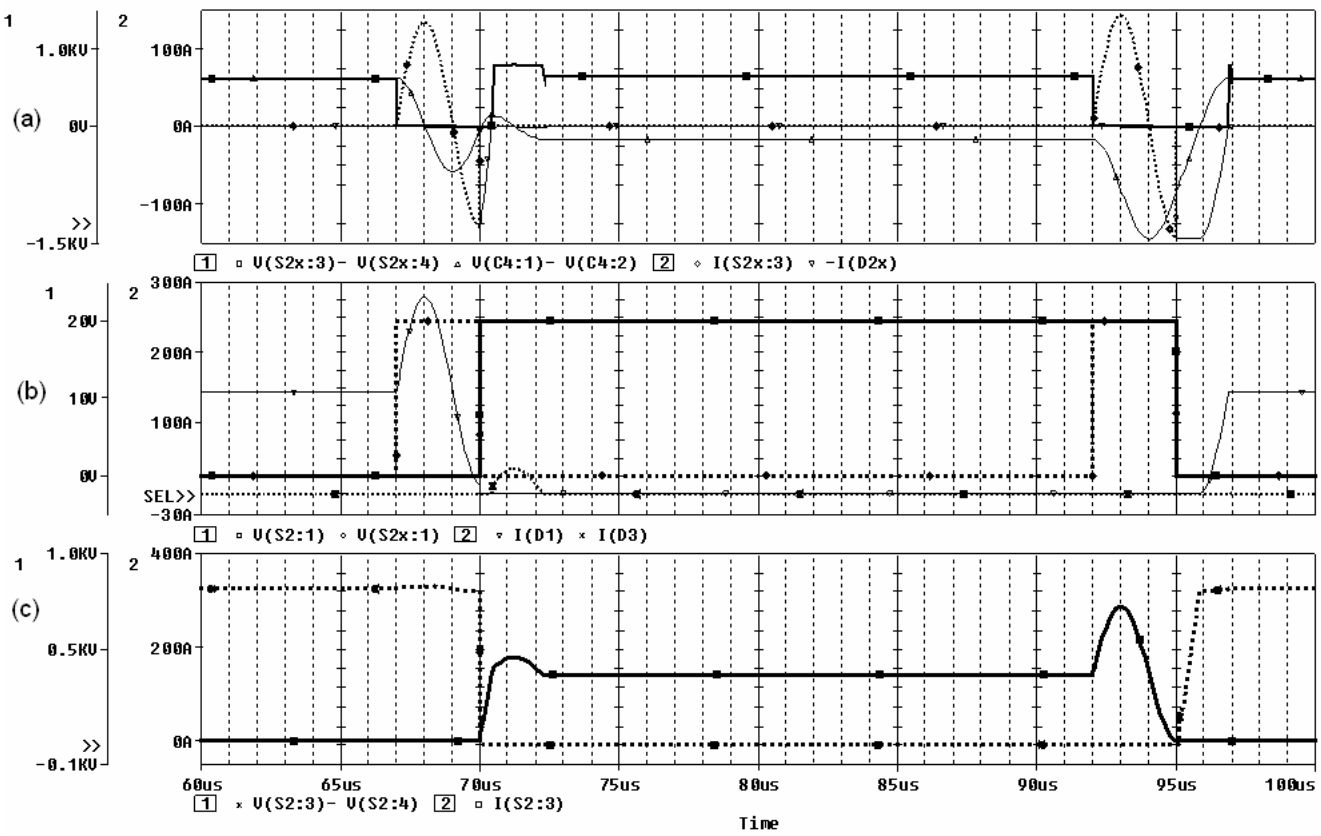


Fig. 5. Soft-switching dynamics. (a) Voltage over resonant capacitor, voltage and current across S2x and current across S2x freewheeling diode. (b) S2 and S2x gate signals, current across S1 and S1xfreewheeling diode. (c) Current and voltage across S2 main switch.

When the current across *Lr* reaches zero it still has sufficient power to oblige D1x to conduct and produce over voltage on S2x and over current on S2. At *72us* the energy on *Lr* is only sufficient to provoke a little ripple on S2x voltage. The same thinking can be shown at turn-off period.

It can be noted that the edges of the main switch PWM signal occur at exactly the same instant as the falling edge of the auxiliary switch gate signal. This kind of timing arrangement facilitates the real implementation.

Note in Figure 5 that when it's desirable a regulated voltage close to 550V (the lower value proposed), the pulse width on S2 gate will be minim and consequently the S2x gate pulses tend to overlap. However, the DSP turn-off the auxiliary circuit and the rectifier start to work as a hard-switch power supply.

IV. CONTROL SIMULATION AND PRELIMINAR RESULTS

Since ZCT PWM soft switching is only to help the switching transitions, the controller analysis is almost the same as a hard switch rectifier. The d-q average model of a three-phase boost rectifier is used in the controller design.

In the Figure 6 we can see the output DC Bus voltage, the current waveforms and the input voltage. Note that the current has the same phase that the voltage, which means that we have achieved PFC.

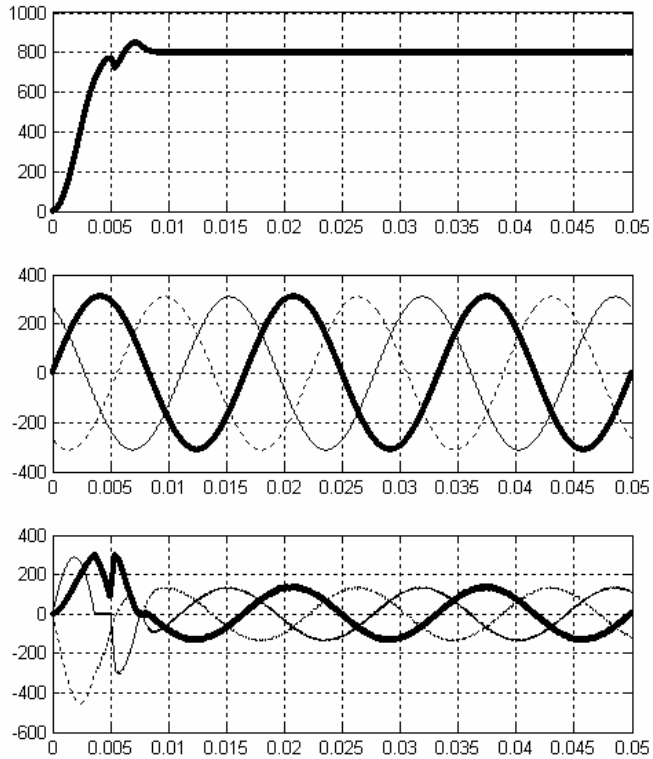


Fig. 6. DC bus voltage, three phase currents and three phase voltages.

In figure 7 we highlight the positive gate pulses on phase A and the respective current. So we can see that the IGBT simply don't switch during 33,33% of the output period and that the current ripple is very low.

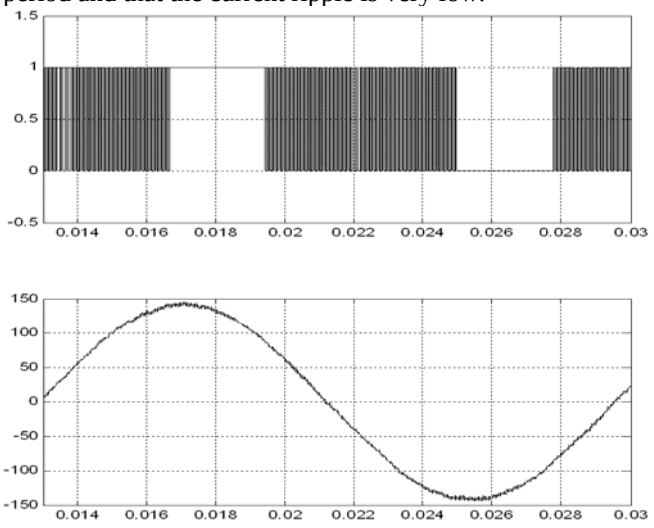


Fig. 7. Highlight on phase A current and S1 gate signal.

A two loop control scheme is adopted in this system. The inner loop is a current loop with wide band width to achieve unity power factor. The outer loop is a voltage loop to regulate the dc bus voltage tightly. All the control is performed by the DSP.

In the Figure 8 we can see all the main blocks used in simulating. In the Figure 9 we highlight the SVM scheme.

All this results were achieved by Matlab/Simulink® simulations

V. CONCLUSIONS

A 62kW modular rectifier with power factor correction is been built. It was chosen the 60º-clamping space vector scheme to obtain lower switching loss. Will be used soft-switching with zero current transition when the duty cycle allow. Wide control bandwidth can be achieved due to the proposed SVM. Satisfactory PFC waveforms are been obtained. We intend as soon as possible to present experimental results and details about the control implementation in the DSP.

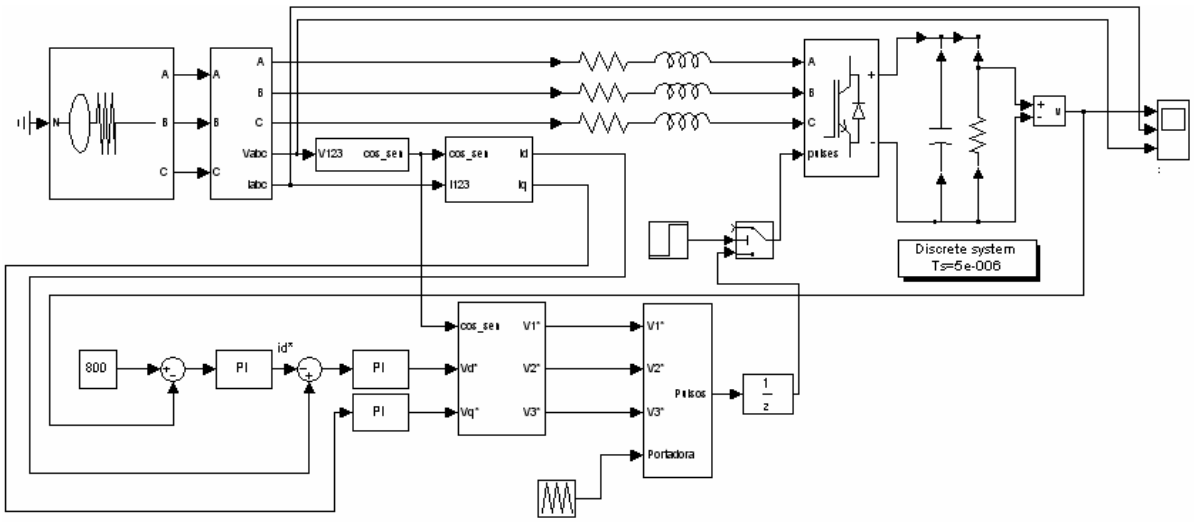


Fig. 8. Rectifier's complete simulation model

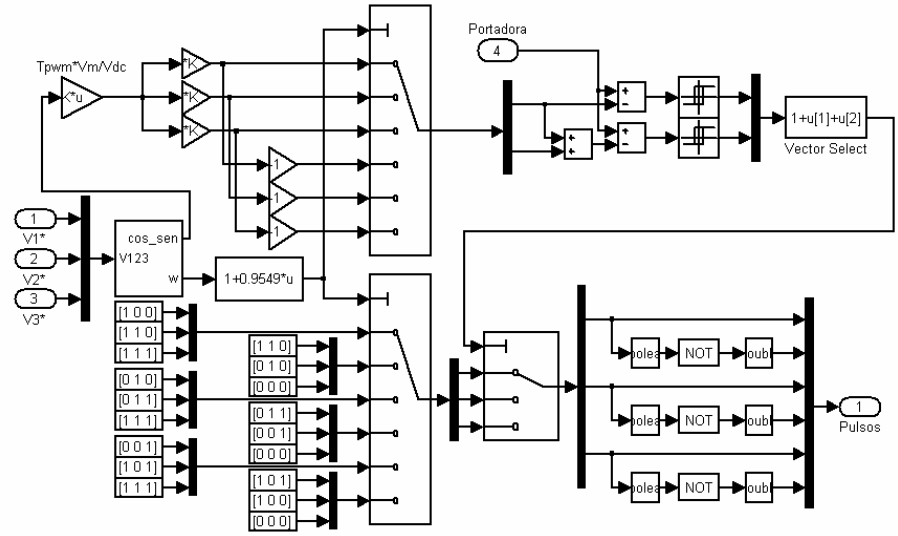


Fig. 9. SVM scheme model

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