DIGITAL CONTROL OF SINGLE-PHASE VSI FOR TRANSFORMER-BASED UPS

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***Abstract* – This paper discusses the problems related to the implementation of single-phase transformer-based UPS. Therefore, a multi-loop linear control strategy is proposed in order to ensure appropriate output voltage regulation, minimize the voltage THD and avoid transformer saturation by means of controlling the primary UPS current. Details about the applied linear controllers and the required synchronization algorithm have been presented and experimental results using a 3kVA prototype validate the performance of the applied control strategy.**

***Keywords* – Uninterruptible power supplies, UPS, digital control, transformer-based VSI, single phase UPS.**

I. INTRODUCTION

Uninterruptible power supplies (UPS) have become widely used for ensuring emergency power to critical or sensible loads fed through unstable or low power quality systems. Generally, this power-conditioning device consists of a DC power supply or battery stage, a pulse width modulation (SPWM) inverter and an output low-pass filter (RLC). The main goal of an UPS is to provide a very well regulated output voltage.

However, considering the UPS application to non-linear load systems, which has been the typical condition, the main drawback is related to the total harmonic distortion of the SPWM output inverter voltage, which can result bigger than the international standards [1]. In order to solve this problem, several digital control techniques have been proposed by different authors. Most interesting solutions are based on repetitive [2,3,4,5] or selective harmonic [6] controllers or multi-loop control based on resonant regulators and feedback of the output filter capacitor current, as discussed in [7].

Indeed, these techniques are able to ensure a high-quality performance of the UPS regulation, as well as limited voltage harmonic emission. Nevertheless, the overall proposed methods have been focusing transformerless UPS topologies and rare literature can be found about transformer-based UPS [7], especially considering single-phase devices [9].

Figure 1 illustrates a single-phase UPS system supplying a critical (sensible) non-linear load. In such case, as well the harmonic control problem, it is very important to avoid transformer saturation due to possible DC currents on the primary side. So, this paper deals with the achievement of a multi-loop digital control, which keeps the RMS output voltage through an integral-based control strategy, assures the output voltage waveform through a basic proportional control and controls the primary transformer current by means of a proportional-integral control. Possible origins of the saturation are also discussed and auxiliary recommendations to minimize its effect have been drawn.

II. UPS SYSTEM DESCRIPTION

A. Power Circuit

The power circuit of the implemented 3 kVA single-phase UPS is described in Fig.1. A low-pass output filter is comprised of the transformer leakage inductance and the output capacitor. As can be seen, the transformer primary current and the output voltage must be measured, preferentially by means of high-precision opto-isolated, Hall Effect or differential sensors.

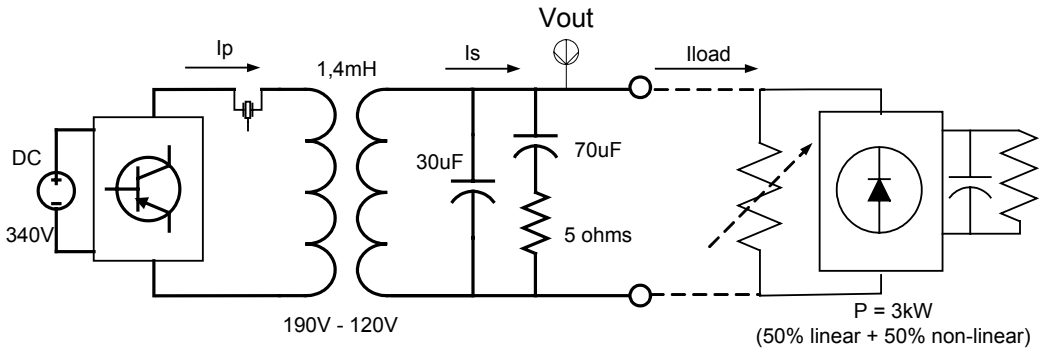

Fig. 1 – UPS power circuit.

B. Mulit-loop Digital Controller

The foremost goals of the proposed digital control are to ensure a good regulation and low distortion (THD) of output voltage, while avoiding flux imbalance problem in the transformer. This problem arises when the magnetic core drifts off center of the hysteresis loop into saturation due to volts-duty cycle products differ from each other (in the inverter arms), even by only a few percent. Figure 2 illustrates the implemented control strategy. In order to provide the regulation of the output voltage (RMS), an integral controller (I) adjusts the amplitude of the sinusoidal reference waveform (Vsin*) as can be seen in Fig. 2. Then, a proportional controller on the instantaneous output voltage controls the voltage waveform conditions and a proportional-integral controller on the output inverter current is applied to over current protection and to minimize possible DC level effects on the transformer.

Considering Fig. 2 it is also recommended that the pre-estimated value of the overall measured DC level should be take out of the steady state measured voltage (Vout) and current (Ip). Such DC levels possibly arise from:

- Asymmetries on the power converter modulator (the aforementioned flux imbalance problem);
- Offset from the analog signal conditioning circuits, as well as sensor elements;
- Shift level circuits;
- Asymmetries on the DC power sources, which fed the DSP and auxiliary analog interface;
- Noise from ground wire;
- Asymmetries on the analog-digital conversion, etc.

In order to eliminate possible DC current components, a detector of the average value of the analog-converter digital registers (offsetAD), before the UPS initialization, should be used. An additional primary current DC level detector should be implemented in order to enforce that the reference of the current (Ip*) should never present DC value. Based on circular buffer arrays, the implemented DC level detector is based on a moving average filter.

III. CONTROL STRATEGY

As previously mentioned, the multi-loop control strategy is based on different controllers, which can be summarized as following:

A. RMS Output Voltage Integral Controller

The performance of RMS voltage controller is defined by the K_I constant and represents a compromise between the required transient response to this kind of the application and a good regulation in steady state. The controller implemented for the experimental activity has been designed to a dynamic response of approximately 200ms. Expression (1) represents the digital implementation of the applied integral controller.

$$V_I[k] = \left(V_{rms}{}^*[k] - Vout_{rms}[k]\right)K_I + V_I[k-1]. \quad (1)$$

It is important to point out that the RMS value is also calculated based on a moving average filter.

Thus, the output of the RMS controller (V_I) multiply by a sinusoidal waveform is the reference voltage (V_{sin}^*):

$$V_{sin}^*[k] = V_I[k].V_{sin}[k] \quad . \quad (2)$$

Note that if necessary, a digital PLL could be applied to ensure synchronization with the utility voltages. The basic rules of a suitable software-based PLL are depicted in the appendix and details can be found in [10].

B. Output Voltage Waveform Proportional Controller

The proportional controller is used to reproduce the output voltage waveform on the terminals of the output low pass filter. The reference amplitude is provided by the RMS controller that compared with the measured voltage results in the output voltage error, which is multiplied by K_P to produce the reference current (3). K_P should be the highest value that synthesizes the sinusoidal voltage and ensures the system stability.

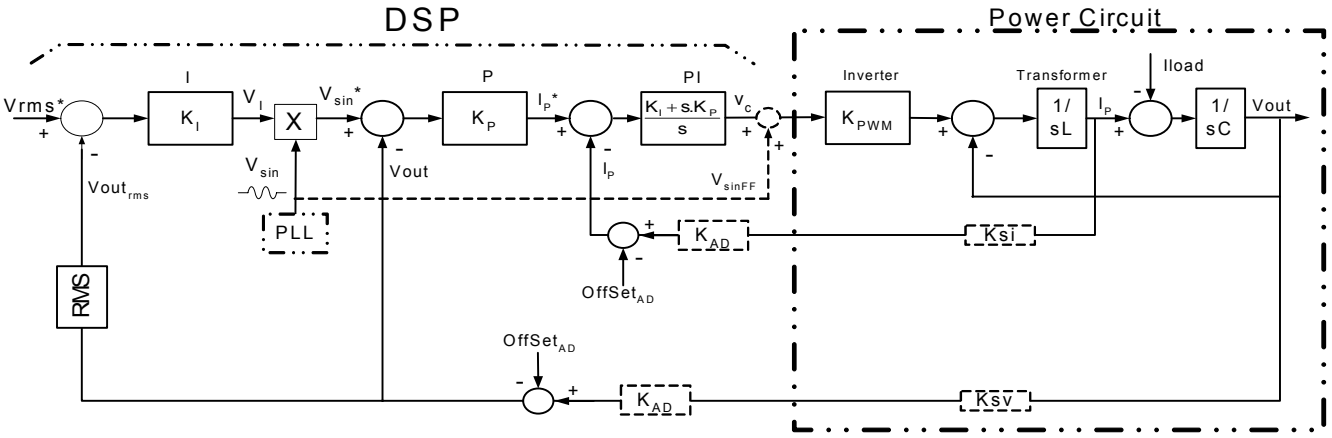

Fig. 2 – Block diagram of the control strategy.

$$I_p^*[k] = \left(V_{sin}^*[k] - Vout[k]\right).K_P \quad . \tag{3}$$

C. PI Current Controller

A PI controller has been used for the primary transformer current control (4-6).

$$V_C[k] = V_{CP}[k] + V_{CI}[k] \tag{4}$$

$$V_{CI}[k] = \left(I_P^*[k] - I_P[k]\right).K_I + V_{CI}[k-1] \tag{5}$$

$$V_{CP}[k] = \left(I_P^*[k] - I_P[k]\right).K_P \quad , \tag{6}$$

where V_C is VSI modulation signal (PI output), V_{CP} represents the proportional part of the PI controller and V_{CI} its integral part.

The designed criterion is based on the classical control, on which the main idea consists in calculating the modulus of the PI regulator multiplied by the plant open loop gain (G_{OLi}) equal to unity.

$$G_{OLi} = 2.\mathrm{V_{DC}}.k_{si}.\frac{1}{L}, \tag{7}$$

where $2.V_{DC}$ is the power gain of the VSI, k_{si} is the scale factor of the applied current sensor and L is the transformer inductance. Thus,

$$\mathrm{K_p}.\frac{G_{OLi}}{\omega_{\mathrm{CLi}}} = 1, \tag{8}$$

$$\mathrm{K_p} = \frac{F_{\mathrm{CLi}}}{G_{OLi}}.2.\pi, \tag{9}$$

where F_{CLi} is the desired closed-loop frequency (in this case, approximately 1 kHz).

On the other hand, the integral constant of the PI depends on the desired phase margin (*mf*) and sampling time (T_s).

$$K_I = \frac{K_P.2\pi.F_{CLi}}{\tan(mf)}.T_s = \frac{\left(2\pi.F_{CLi}\right)^2}{\tan(mf)}.\frac{L}{2.\mathrm{V}_{DC}.k_{si}}.T_s. \tag{10}$$

In order to improve the PI transient response, a dynamic anti-windup PI controller has been implemented, as shown in Fig. 3. Note the integral action is limited accordingly the output of the proportional controller. The normalized scale factors (2^n) are included to ensure correct operation in fixed-point Digital Signal Processors using 1.15 formats.

D. Feed-Forward Loop

Considering Fig. 2, it is possible to note that if necessary, a feed-forward loop could be included to improve the overall UPS performance.

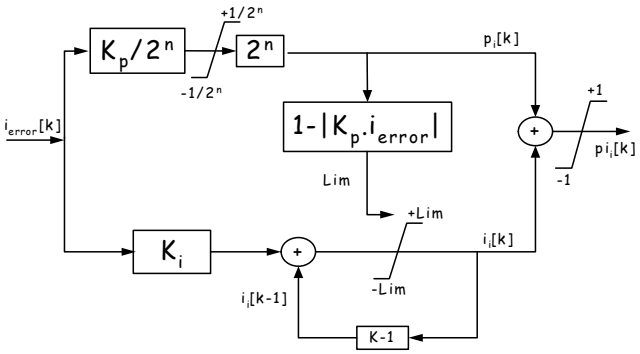

Fig. 3 – Dynamic anti-windup PI controller.

IV. EXPERIMENTAL RESULTS

The control strategy has been implemented in a 16-bit fixed-point DSP, the ADMC 401 from Analog Devices. A 3kVA prototype was built to verify the UPS performance under different load conditions. Steady state and dynamic response were evaluated in the following situations: without load, predominant linear load, non-linear and linear combined load and predominant non-linear load.

The tests were performed using a commercial 3.7kW single-phase inverter and a step-down transformer with windings turns ratio of 0.63. The main power was supplied through a step-up autotransformer allowing a higher voltage in DC link (about 340V). Although the relatively high costs, in this prototype the voltage and current measuring were performed by means of Hall Effect sensors (LV25P and LA 55P).

A. Without Load

Considering the proposed control strategy, Fig. 4 shows the performance of the single-phase UPS under non-load conditions. From top to bottom, it is possible to observe the primary (CH4) and secondary (CH1) voltages and the internal DSP voltage reference (CH2) aside to the internal output voltage (CH3 - secondary voltage inside DSP, after A/D conversion).

In this case, the value of the RMS voltage was adjusted to 108.5 V and the resulting THD (Total Harmonic Distortion) was 1.7%.

The THD has been calculated by means of a Power Harmonics Meter (model 40) by Fluke Instruments.

Main Model 40 specifications are:

- ❖ Volts measurements (true RMS)

Input Range: 0.0V to 600V rms (ac+dc)

- ❖ Amps measurements (true RMS)

(1mV/A) Isolated Input

Input Range: 1.00mV (A) to 1000mV rms (A) (ac+dc)

- ❖ Harmonics Measurement accuracy

Volts:

- ○ Fundamental to 13th Harmonic → ± (2%+2 digits). Phase ± 2 degrees (harmonic>5%)
- ○ 13th to 31st Harmonic → 13th (± (2%+2 digits)) ----------31st (± (8%+2 digits)). Phase ± 10 degrees (harmonic>5%)

Amps and Watts

- Fundamental to 13th Harmonic → Amps or Watts: ± (3%+3 digits) + probe specs. Phase ± 2 degrees + probe specs (harmonic>5%)
- 13th to 31st Harmonic → Amps or Watts: 13th (± (3%+3 digits) + probe specs) ----------31st (± (8%+2 digits)+probe specs). Phase ± 10 degrees + probe specs (harmonic>5%)

❖ Other measurement specifications

Input Bandwidth: (-0.5dB) DC, 5Hz to 2.1kHz
Crest Factor (CF) range: 1.00 to 5.00

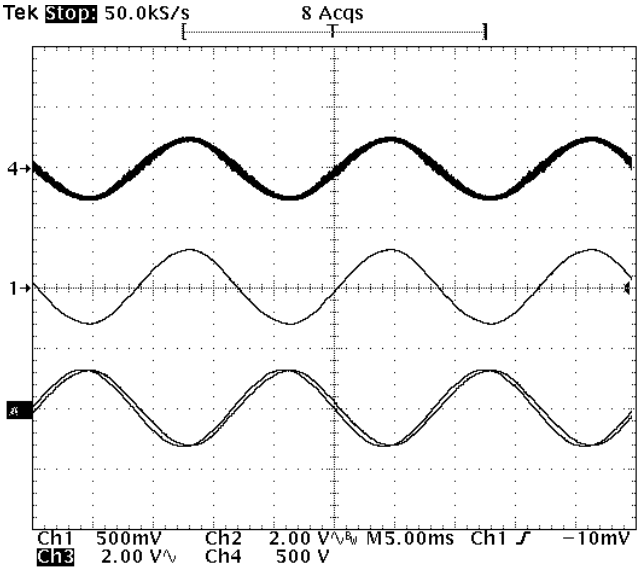

Fig. 4 – From top to bottom: primary and secondary transformer voltages (500V/div) and DSP internal voltage reference aside the resulting output (secondary) voltage.

B. Linear Load

Figure 5 shows the UPS voltage and current signals when feeding a linear load of 1.12kW. In this case the achieved RMS output voltage was 108.3V, while the load current was 10,3A. The voltage and current THD were, respectively, 2.5% and 2.7%.

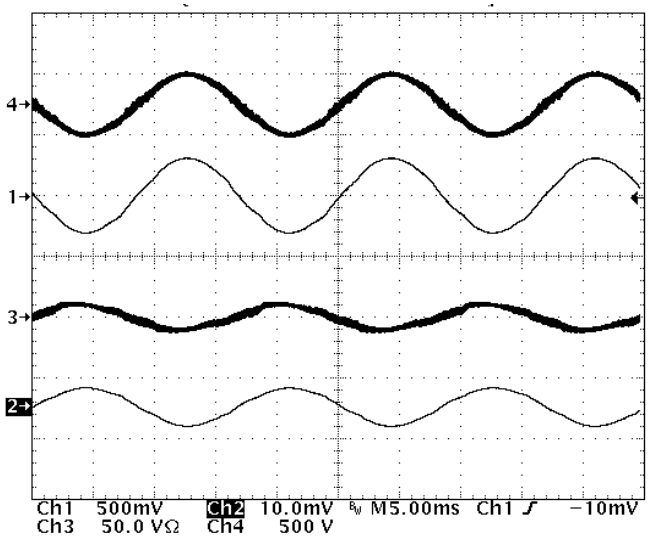

Fig. 5 – From top to bottom: Voltages (CH4, CH1, 500V/div) and currents (CH2, CH3, 50A/div) on high and low side of the transformer.

C. Combined Linear and Non-linear Load

A single-phase rectifier was added to the previous load setup. As a result, the load starts drawing 2.8kW of active and 3.3kVA of apparent power. The non-linear characteristics of the load can be observed in the load current, as shown in Fig. 6.

The peak distortion at high side is due to the saturation problems in the current probe. A TCP202 50MHz current probe containing a Hall effect device was used. The TekProbe interface allows TCP202 probe to be directly connected to Tektronix's oscilloscope. The TCP202 probe has a maximum peak current of 50A with a pulse width ≤ 10μs (500μAseconds). As the frequency decreases, the maximum current rating increases, limited to 15A (DC + peak AC).

In this test the resulting load current THD was 50%, with a crest factor of 2.4 (30 and 70A respectively to RMS and peak values). The load voltage has stabilized in 108,9V, performing a suitable regulation, even though the voltage THD has been increased to 5%.

Dynamic tests were performed under this load setup as shown in Fig. 7. Toward achieving the nominal operating power the RMS loop control may be adjusted by tailor, according the load or system's requirements. As seen in Fig. 7 the output voltage loop assures a soft start feature to the system, if necessary.

It is important to point out that this condition (50% linear, plus 50% non-linear load) is a general test condition, recommended for several national and international standards [1].

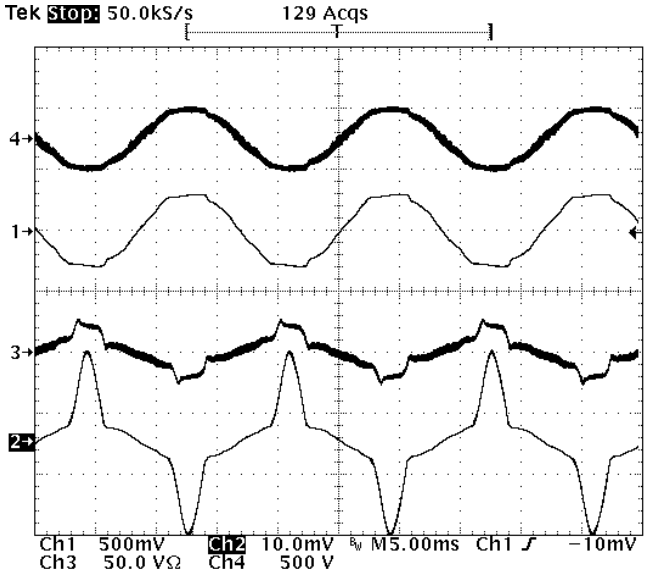

Fig. 6 – From top to bottom: Voltages (CH4, CH1, 500V/div) and currents (CH3, CH2, 50A/div) on high and low side of the transformer.

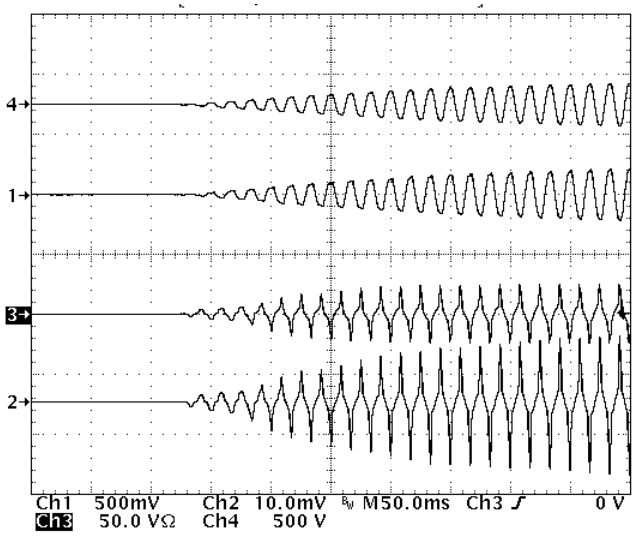

Fig. 7 – Startup test under combined linear and non-linear load condition (2,8 kW / 3.3 kVA). From top to bottom: Voltages (CH4, CH1, 500V/div) and currents (CH3, CH2, 50A/div) on high and low side of the transformer.

D. Non-linear Load

Considering the worst condition, pure non-linear load, only the single-phase rectifier was connected to prototype output. As can be seen in Fig. 8, the resulting current and voltage distortions were about 69% and 9%, respectively. The peak distortion at high side is due to the saturation problems in the applied current probe. The output RMS and peak current values were 21A and 54.9A, respectively. Accordingly, the crest factor reached the value of 2.7.

It can be noted that the tests for a non-linear load of 1.6kW (2.3kVA) demand higher instantaneous current, thus clamping the output voltage to that in the bulk capacitor. The conclusion to be drawn from this evidence is that the overall control strategy should be explicitly improved when supplying predominant non-linear load, e.g., by means of repetitive or selective controllers [5,6]. In the other hand, the regulation has been satisfactory to a stable RMS value of 108.2V.

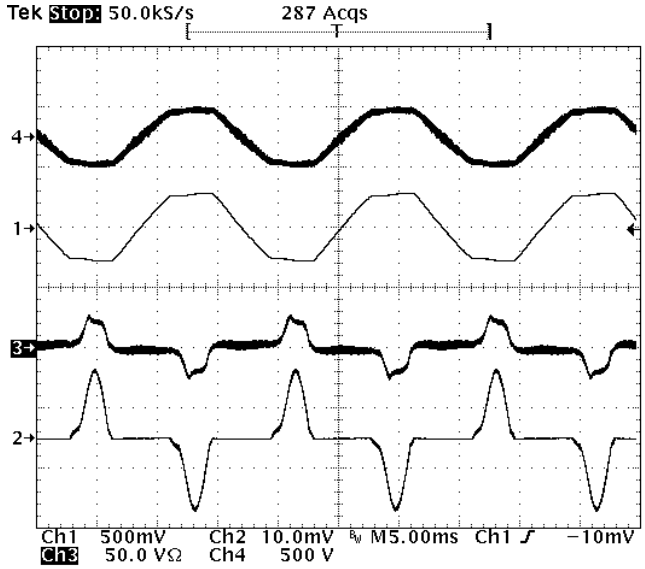

Fig. 8 – – From top to bottom: Voltages (CH4, CH1, 500V/div) and currents (CH3, CH2, 50A/div) on high and low side of the transformer.

V. CONCLUSIONS

This paper discusses the problems on implementing a single-phase transformer-based UPS. It is particularly focused on the output voltage regulation and THD minimization, as well as the control of primary DC current levels in order to avoid the transformer flux imbalance. The proposed digital control strategy is based on multi-loop linear controllers (very well known and widely applied in industrial applications) and attention has been directed to the measurement of the average value of digital and analog offsets. The implemented prototype and experimental results show that the proposed strategy is able to ensure a good regulation to the output voltage and compensate possible DC currents, while maintaining an acceptable distortion in the output voltage.

APPENDIX

A. Sinusoidal reference generator based on digital PLL

Considering the requirements of voltage synchronization with the utility mains, a simple digital PLL is proposed, as shown in Fig. 9. The central idea is to synthesize a unitary sinusoidal function ($u_{\perp}$), which is orthogonal to the input voltage (v) under steady conditions. Thus, the dot product result (dp) of this digitally synthesized function with the input voltage must converge to zero mean value. The instantaneous argument θ, used to synthesize the sinusoidal function $u_{\perp}$, is obtained by integrating the PI regulator output ω. While the PLL algorithm seeks to synthesize the unitary

sinusoid to satisfy the orthogonal condition with the input voltage *v*, the PI controller converts the product error (dp_{error}) into a varying correction term ($\Delta\omega$) that leads to the desired input signal frequency ω, rendering the argument function θ by simple integration.

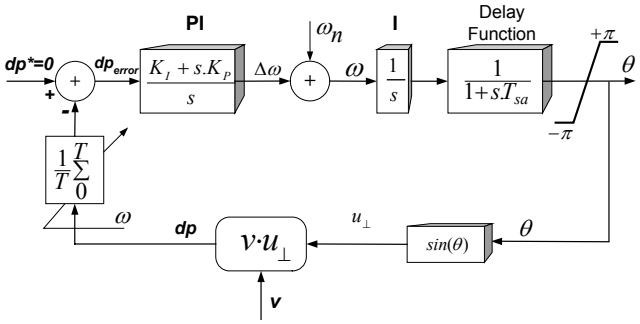

Fig. 9 – Generalized 1ϕ -PLL Model.

A feed-forward reference ($\omega_n = 2\pi f_n$) is included to improve the initial dynamic performance, where f_n is the utility nominal frequency. Since the interest is to develop a digital PLL, a sampling delay function may be added to the PLL model in order to represent the sampling process (sampling time T_{sa}). The PI regulator reaches a constant output ω if the mean input error is zero ($\overline{dp}_{error} = 0$). At this condition $\theta=\omega.t$, and the PLL tracks the input voltage frequencyω, with a phase-angle delay of $(-\pi/2)$, which guarantees the orthogonality condition. Hence, the PLL is able to provide the utility's varying frequency (ω) and the synchronizing angle ($\phi = \theta + \pi/2$) to be used in the UPS sinusoidal reference generator, as shown in Fig. 2.

ACKNOWLEDGEMENT

The authors would like to thank FAPESP and CAPES Foundations for supporting this research. Special thanks to Texas Instruments and Analog Devices for providing the DSP evaluation boards.

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