THE EQUILIBRIUM MECHANISM IN THE NEW FOUR-SWITCH FORWARD CONVERTER

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***Abstract* - The new four switch forward converter was early presented with a natural equilibrium of the input capacitors. This paper analyzes the way of how this equilibrium occurs. The converter is presented here with an 'artificial delay' in the gate of one switch. Each stage of this 'distorted' way mode of operation is analyzed. The limitations and characteristics in maintained the equilibrium of these voltages is described. The equations, simulations and experimental results are also showed.**

***Keywords* – DC-DC converters, Multilevel converters, auxiliary power supply.**

I. INTRODUCTION

The new patent pending converter described in [1] was stated presenting an effective clamp in the off-voltage on switches. This clamping voltage is half of the input voltage, indicating that this converter is useful for applications with high input voltage. The great similarity of this converter with the very well known forward topology was also presented as a great advantage, performing an easy understand of its power transferring mechanism. Another great advantage of this converter is the natural equilibrium of the voltage on the input capacitors.

This paper presents the way of how this natural equilibrium occurs. The possibilities of how the differences on the gate times could cause the non equilibrium and the stages of operation when the converter naturally comes back to the equilibrium state are shown. The analysis, equations and experimental results of these operations, and the conclusions about the limits of the operation of this converter are also presented.

II. THE DC-DC FOUR-SWITCH FORWARD CONVERTER

A. CIRCUIT DESCRIPTION

The double-ended forward converter proposed in [1] is shown in Figure 1, drawn in a different manner as the input capacitors C_1 and C_2 are connected in the midpoint of the primary side of the transformer. The four switches are indicated by the S_1, S_2, S_3 and S_4 MOSFETs. The input capacitors with the voltages V_{C1} and V_{C2} split the input voltage E. The clamping diodes D_{C1} and D_{C2} certify the voltage on the switches S_1 and S_4 to be half of the input voltage. The diodes D_1 and D_2 permit the core reset on the input supply.

The output stage is composed by the rectifiers diodes D_{O1} and D_{O2}. The output filter is indicated by L_O and C_O. The load is represented by the resistance R_O.

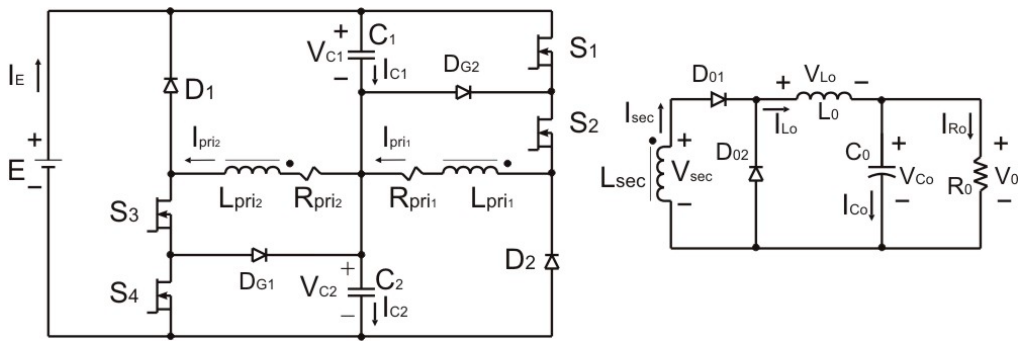

Figure 1 – Four-switch forward converter.

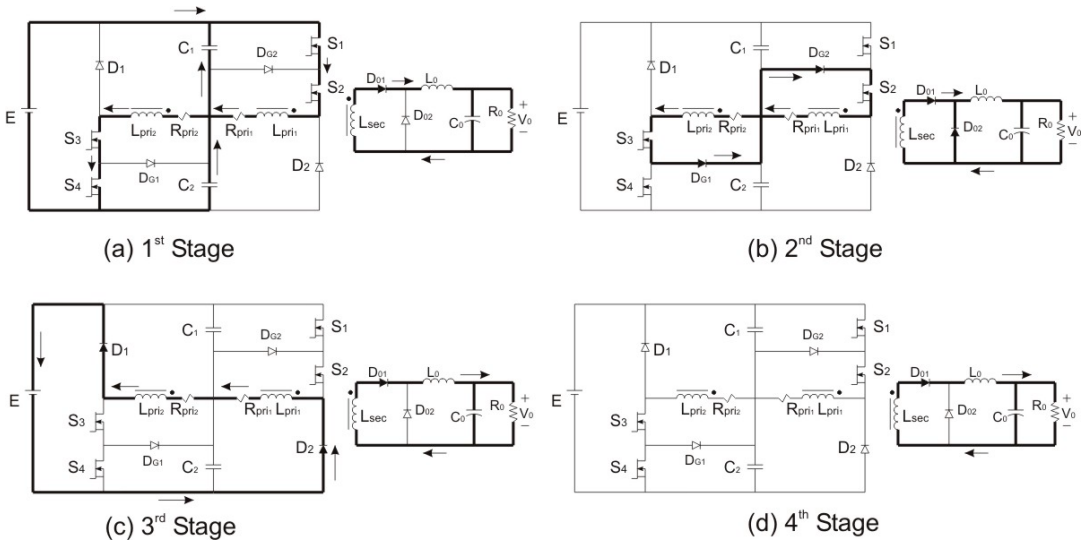

Figure 2 – The simplified topological stages of operation: (a) first stage; (b) second stage; (c) third stage; (d) fourth stage.

B. SIMPLIFIED PRINCIPLE OF OPERATION

To simplify the analysis some suppositions are made: 1) the circuit operates in steady state; 2) all power semiconductors are ideal; 3) the intrinsic capacitances of the MOSFETs are neglected.

The four stages of operation are presented in Figure 2. The main waveforms that correspond for each stage can be observed in Figure 3. The operation is described forward:

First stage (t_0, t_1): This is the stage when the energy is transferred to the load. The switches S_1, S_2, S_3 and S_4 are allowed to conduct.

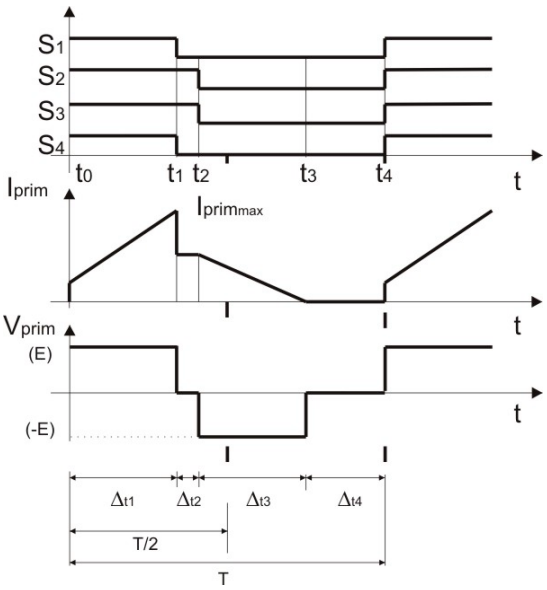

Figure 3 – Main theoretical waveforms.

Second stage (t_1, t_2): The switches S_1 and S_4 are gated off in t_1. The magnetizing inductance make the current roll in freewheel on the primary side. As the voltage on the primary windings is null, the second side of the transformer is also zero, with the L_O inductance keeping the output current continuity. This stage is very short in time, and is used only to guarantee the clamping voltage on the external switches S_1 and S_4 in $E/2$.

Third stage (t_2, t_3): The switches S_2 and S_3 are gated off in t_2. The voltage over S_2 and S_3 reaches $E/2$. The diodes D_1 and D_2 are willing to conduct, resetting the core magnetizing energy on the input supply E. The voltage on the primary side of the transformer is now (-E).

Fourth stage (t_3, t_4): In this stage the voltages over the switches are $E/4$. The voltage on the primary side is zero, as the current. This is a stand by stage, but it is an important stage, as the operation of the converter must reach this stage to be stable and guarantee the $E/2$ voltage on all the switches.

III. THE INPUT CAPACITORS EQUILIBRIUM

The input capacitors equilibrium is critical. Any difference in commutation times, or in intrinsic characteristics of the switches will lead to split voltage on the input capacitors in one unequal division. The connection of the primary winding midpoint to the C_1 and C_2 capacitors was stated to solve this problem. But how will the voltage on these capacitors converge to an equal value?

To perform this analysis, lets considerate that one switch, S_1 for example, stay in conduction mode for a little time after S_4 is turned off. The converter will have now six stages of operation. Figure 4 shows these stages and the main waveforms are presented in Figure 5.

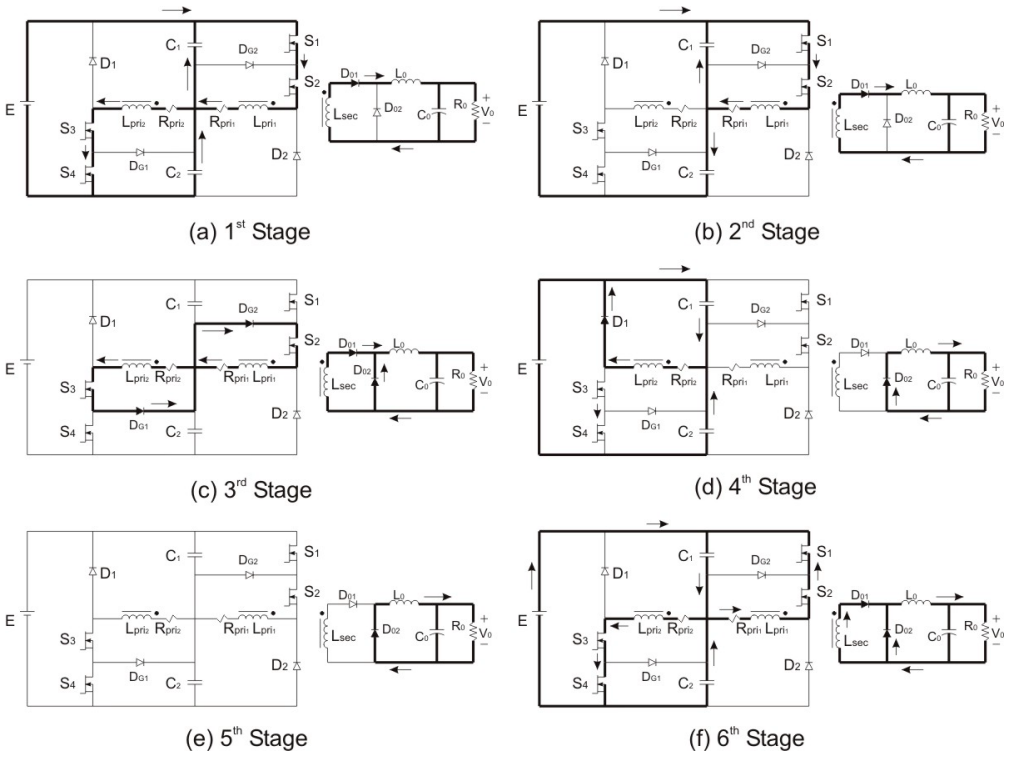

Figure 4 – The topological stages of operation: (a) first stage; (b) second stage; (c) third stage; (d) fourth stage; (e) fifth stage; (f) sixth stage and (g) seventh stage.

First stage (t_0, t_1): This is the stage when the energy is transferred to the load. The switches S_1, S_2, S_3 and S_4 are allowed to conduct.

Second stage (t_1, t_2): The switch S_4 is gated off in t_1. As S_1 is acting like having a little delay in gating off, it continues to conducting. The other switches S_2 and S_3 continue to conducting also. The voltage on capacitor C_1 begins to drop as the voltage on capacitor C_2 begins to rise. To obey the N.i relation, the current delivered to the load from the C_1 capacitor is twice its previous current to supply the same current on the load.

Third stage (t_2, t_3): Now S_1 is finally blocked. This stage is the freewheel stage on the primary, with the same manner as previous described in normal operation. But the voltages on C_1 and C_2 capacitor are no more equal.

Fourth stage (t_3, t_4): In this stage S_2 and S_3 are gated off. The magnetizing inductance will reset the core trough the capacitor C_1 only because of its lower voltage in relation to C_2.

Fifth stage (t_4, t_5): After the core reset, all the currents on the primary goes to zero. The load current is supported by the output inductor. Depending on the capacitor voltages difference, in this stage these voltages could be already balanced. Lets consider that this difference still exists, even being in a lower level.

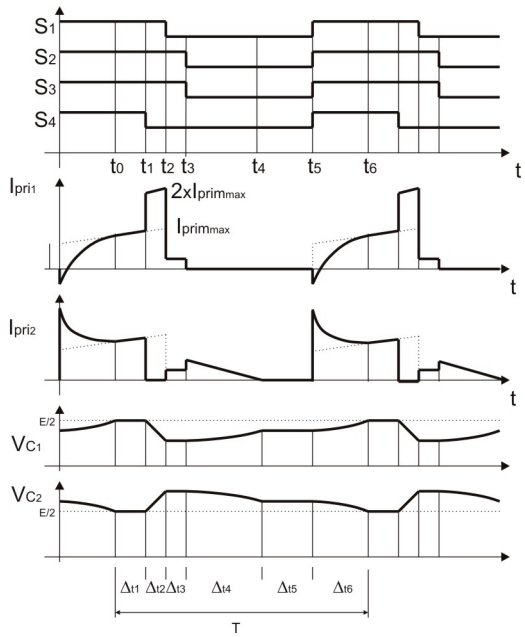

Figure 5 – Main waveforms when considering a delay in the S_1 gate off time.

Sixth stage (t_5, t_6): In this stage all the switches S_1, S_2, S_3 and S_4 are gated on. As the relation between the two primary windings is an 1:1 relation, the

capacitors C_1 and C_2 are now connected in parallel through the primary side of the transformer. The voltages on these capacitors will reach the equilibrium state, with their current being limited by the series resistance of the windings.

IV. INPUT CAPACITOR VOLTAGE BALANCE ANALYSIS

At a first glance it could be realized that there exists two different ways for the voltage on the input divider capacitors. The analysis that will be made now is the description of which stages the voltage rise or fall, and how this happens.

A. FALL VOLTAGE ON C_1

It could be seen in Figure 4 (b) that when only S_1 is allowed to conduct, the voltage on the input capacitor C_1 will fall. This happens because C_1 will feed the current load with twice its previous current as to obey the N.i relation. As the input voltage E is constant, the voltage on capacitor C_2 will rise in the same rate as C_1 voltage falls. This will happen for a Δt_2 interval, as could be seen in Figure 5. To calculate the rate of how the voltage on capacitor C_1 drops, the equivalent loop in Figure 6 could be taken.

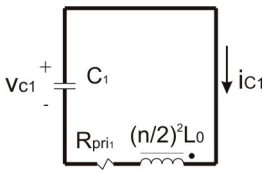

Figure 6 – Equivalent loop for the fall voltage stage on C_1.

The loop solution for the voltage could be described by the follow equation, where $I(t_1)$ is the final current of the first stage.

$$\Delta V_C \quad I4=t(\ _1)C\ \Delta t\ \ _2I4=(\ \ )C_2\ \Delta t_2$$

B. RISE VONLTAGE ON C_1

In the third stage, the currents and voltages will behave in the same manner as described in Figure 2. The only difference is that the voltages on the capacitors are not the same. But they stay as they are, there is no change of its value.

In the fourth stage it will happens the core reset on the primary side. The energy stored in the magnetizing inductance will be delivered back to the primary. This energy will be absorbed by the capacitor with the less voltage, in this case, the capacitor C_1. This is the first contribution to the balanced voltage state, but it could not be sufficient.

In the sixth stage is when the balanced state most probably comes back. With all the four switches being allowed to conduct, a parallel circuit will appear on the primary side. The 1:1 relation between the primary winding put the C_1 and C_2 capacitors in parallel. An equivalent circuit on the primary side could then be taken in account for this analysis. Figure 7 shows this equivalent circuit.

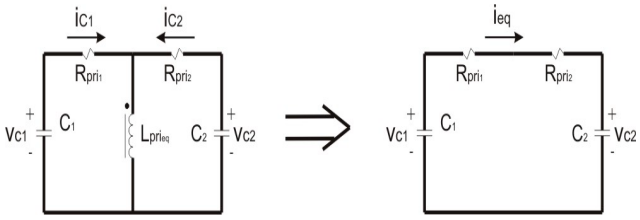

Figure 7 – Equivalent loop for the primary side on the sixth stage.

The parallel configuration with two capacitors with different voltages could lead to a short circuit current. This is in true a short circuit. But the high currents are limited by the series equivalent resistance of the windings. The equation (2) shows the result for this current.

$$i_{C_{eq}}(\ ) = \frac{\Delta V}{2R_{pri_1}} e^{-\frac{t}{R_{pri_1}C_1}}$$

V. SIMULATION RESULTS

Figure 8 shows the main waveforms for a 600V input, 100W project.

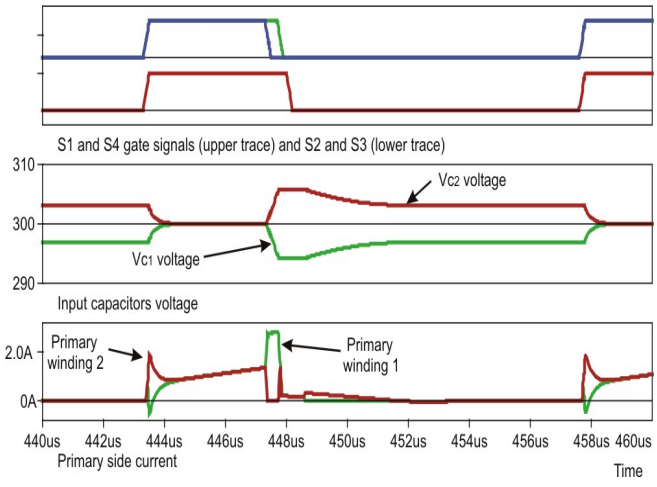

Figure 8 – Simulation results – main waveforms.

VI. EXPERIMENTAL RESULTS

An acquisition depicting the primary currents is shown in Figure 9. Channel 1 shows the current in the primary winding 1. This winding is connected in the same loop of the capacitor C_1. It's easy to identify the tendency of the current going to the double of its original value on the end of the first stage. The

current on the primary winding 2 goes to almost zero in the same time.

The voltage balance could be evidenced by the area under the current traces. It could be noted visually that these areas tend to be the same.

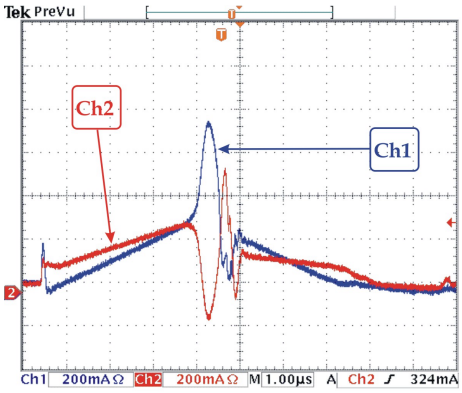

Figure 9 – Primary winding 1 (Channel 1) and primary winding 2 (Channel 2) currents.

Another figure shows these balanced voltages directly over the C1 and C2 capacitors. Figure 10 presents also one channel with the mathematical operation where C1 and C2 voltages are subtract one from another. This math channel is zero, representing an equilibrium state with no difference between these voltages.

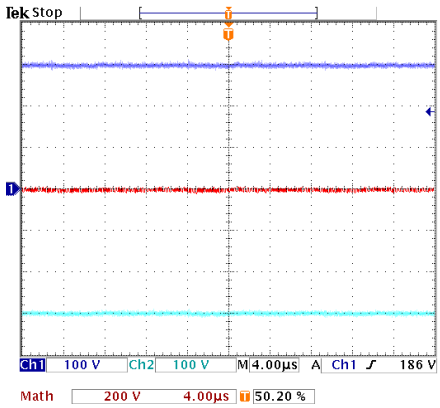

Figure 10 –Balanced voltages: voltage on capacitor C1 (Channel 1), negative voltage on capacitor C2 (Channel 2), and the sum of the tow voltages (Math).

VII. CONCLUSION

The new three level forward converter presented early is now analyzed in its equilibrium mechanism. Its main characteristic of being stable in maintained the balanced voltage on the input capacitors is showed. It was demonstrated that this converter could goes out from its equilibrium input voltage capacitors balance state, but it has a natural 'come back' stage for these voltages.

The simulation results and the experimental results were showed also. It could be seen that the converter has to have enough time to operate with balanced voltages on the input capacitors. It was demonstrated also that the peak currents caused by the 'comes back' stage could be estimated.

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