AN ISOLATED THREE-LEVEL ZVS-PWM DC-TO-DC CONVERTER WITH WIDE LOAD RANGE

Artur Krauss Neto Bruno Sens Chang Altamir Ronsani Borges Eduardo Deschamps*
Universidade Regional de Blumenau
Departamento de Engenharia Elétrica e de Telecomunicações
Caixa Postal 888 – CEP 89.010-971 Blumenau - SC – Brasil
*e-mail: edudes@furb.br

***Abstract* – This paper presents the analysis of an isolated three-level dc-to-dc converter operating in wide load range, which presents half of the input voltage across the main switches. A commutation auxiliary circuit is used in order to assure ZVS for all active switches in the whole load range. The commutation auxiliary circuit operates at lower current than the rated current, and the conduction losses of this converter are almost in the same order of those present in the converter without the auxiliary circuit. This converter is suitable for applications in power supplies that have power factor pre-regulators in their input stage. Principle of operation, and theoretical analysis along with experimental results are presented.**

KEYWORDS

Multilevel converters. DC-to-DC converters. Soft switching.

I. INTRODUCTION

In order to reduce the voltage stress across the switches of dc-to-dc converters, many techniques are being used such as: series connection of the switches, multilevel commutation cells association and multilevel converters association.

The three-level dc-to-dc converter based on the flying capacitor multilevel cell presented in [1] assures half of the input voltage across its active switches with ZVS commutation and pulse-width modulation. However, in order to ensure soft-commutation, a minimum value of load current is necessary. Thus, for this converter, it can be observed that the wider the load range with ZVS, which implies smaller minimum load current, the higher is the reactive voltage drop across the commutation inductor of the converter. Therefore, a good design involves sacrificing the soft-commutation at low load, where the conduction losses are low, to obtain high-efficiency at full-load. [1]

In this paper, a commutation auxiliary circuit (CAC) is introduced in the three-level dc-to-dc converter based on the flying capacitor multilevel cell (figure 1) to obtain ZVS for all active switches in a wide load range. This circuit was previously proposed for the full-bridge ZVS PWM dc-to-dc converter in [2], and for the three-level ZVS PWM dc-to-dc converter based on the neutral-point clamped multilevel cell in [3].

An analysis of a three-level isolated dc-to-dc converters based on the flying capacitor cell with CAC, as well as experimental results obtained with a 1.5kW, 60V output voltage, 600V input voltage and 50kHz prototype are presented and discussed in this paper.

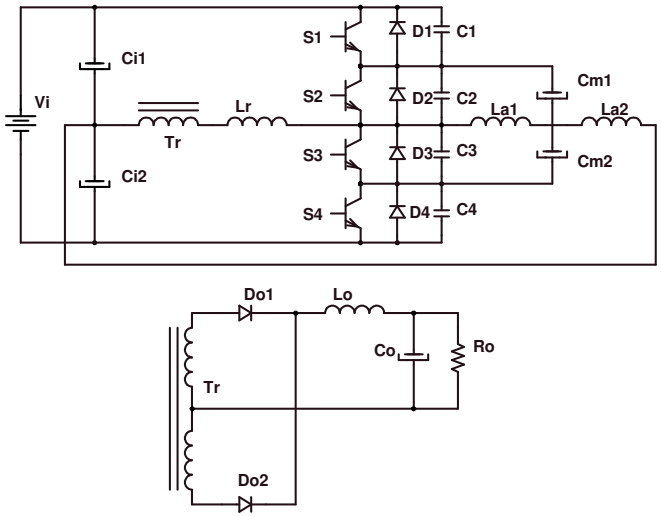

Fig. 1 – The proposed isolated three-level ZVS PWM DC-to-DC converter with CAC.

II. CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

In the converter of figure 1, the switches S_1 to S_4 form the main commutation leg. The diodes D_1 to D_4 conduct inverse polarity current and clamp the switch voltage at reverse voltage (-1V). The capacitors C_{m1} and C_{m2} are responsible for the voltage clamping across the main switches to half of the input voltage (Vi/2). The inductance L_r (which incorporates the leakage inductance of the isolation transformer T_r) and the capacitors C_1 to C_4 provide a resonant transition permitting zero-voltage turn-on and eliminating turn-on switching power losses. Capacitors C_1 to C_4 also provide capacitive turn-off snubbing reducing the commutation losses. The transformer T_r provides galvanic isolation and voltage transformation between the source and the load. The output stage of the converter is formed by the rectifiers D_{o1} and D_{o2} and an output filter, composed of L_o and C_o.

The commutation auxiliary circuit proposed in this paper is obtained by the connection of the inductances La_1 and La_2 in the middle point of the clamping capacitors C_{m1} and C_{m2} and input capacitors C_{i1} and C_{i2}.

Figure 2 shows the stages of operation of the converter for

half period of operation, assuming that all switches are ideal, a transformer turns ratio equal to one, and replacing the output stage by a current source. The output stage is referred to the primary.

Fig. 3 shows the key waveforms for one switching period.

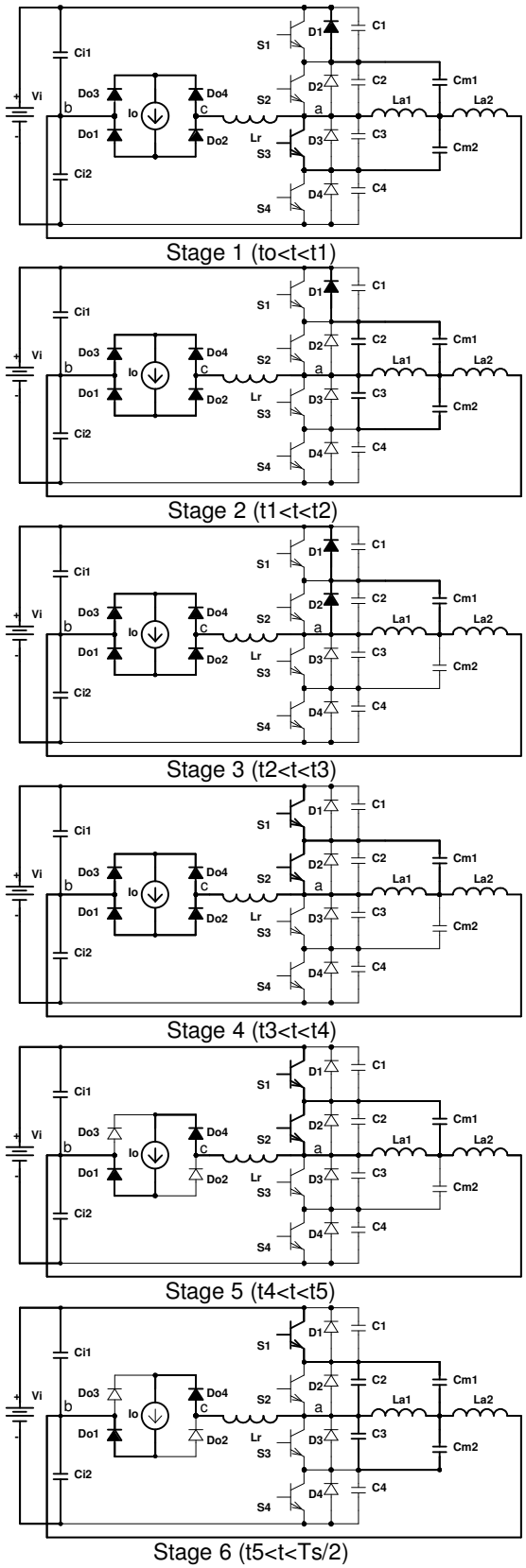

Fig. 2 – Stages of operation.

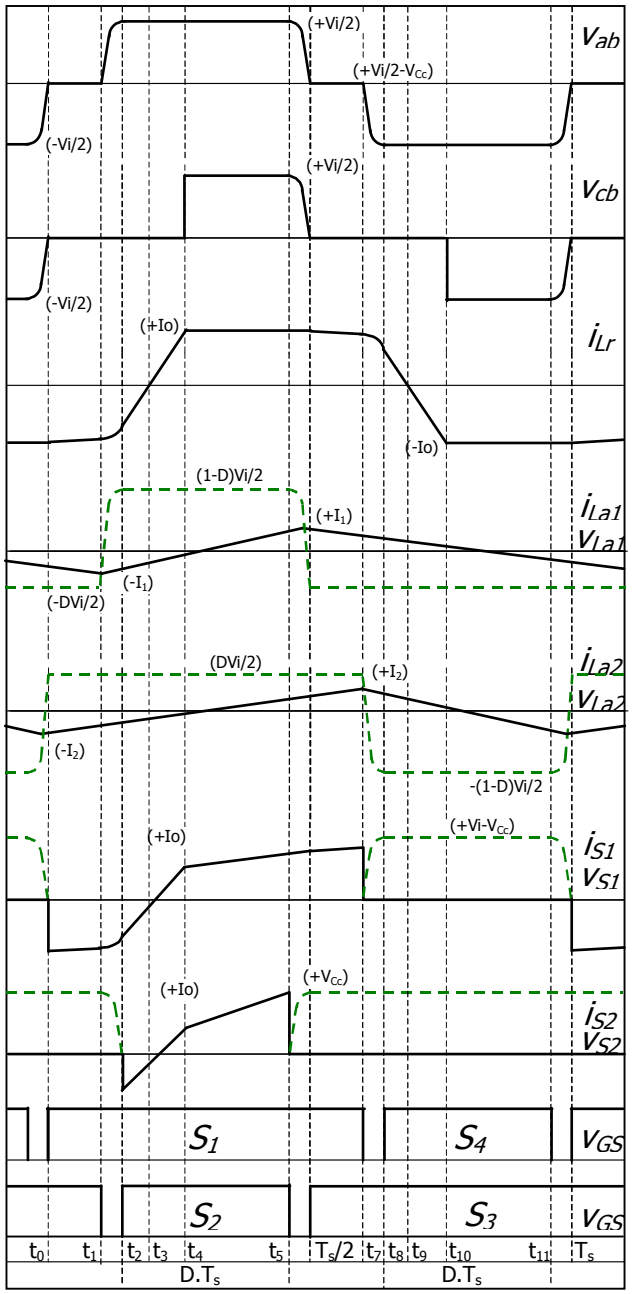

Fig. 3 – Key waveforms.

The stages of operation are described as follows:

a) Stage 1 (t_0, t_1)

During this stage the current flows through switch S_3, capacitors Cm_1 and Cm_2 and diode D_1. The voltage across Cm_1 is (1-D)Vi and across Cm_2 is (D)Vi. The voltage *vab* is null. All output rectifiers are conducting and the output voltage is zero. The voltage across La_1 is –(D)Vi/2 and across La_2 is (D)Vi/2. The current i_{La1}, which is negative, flows through the switch S_3, and the current i_{La2}, also negative, flows through diode D_1.

b) Stage 2 (t_1, t_2)

When S_3 is turned-off, the voltage v_{C3} increases from zero to Vi/2, while v_{C2} decreases from Vi/2 to zero, with the help of current i_{La1}. This stage ends at the instant *t2*, when D_2 is directly polarised and starts conducting.

c) Stage 3 (t_2, t_3)

In this stage the current i_{Lr} is negative and flows through the diodes D_1 and D_2. During this period of time S_2 is gated on at zero-voltage and zero-current. The voltage *vab* is Vi/2 and the output voltage is zero because all output rectifiers are conducting. The voltage across the inductor La_1 reaches (1-D)Vi/2.

d) Stage 4 (t_3, t_4)

When the current i_{Lr} becomes positive, it starts to flow through the switches S_1 and S_2. The voltage *vab* remains Vi/2 and the output voltage is zero.

e) Stage 5 (t_4, t_5)

During this stage, power is transferred from the input source Vi to the load through the switches S_1 and S_2 and the diodes Do_1 and Do_4. During this stage the current across the auxiliary inductors La_1 and La_2 becomes positive.

f) Stage 6 (t_5, $T_s/2$)

This stage begins when S_2 is turned-off. The capacitor C_2 begins to charge and C_3 begins to discharge linearly with time, with a constant current. This stage finishes when v_{C2} reaches Vi/2 and v_{C3} becomes null. The voltage across La_2 goes from (1-D)Vi/2 to –(D)Vi/2.

The second half-period, which is identical to the first one, is omitted in this paper.

III. COMMUTATION ANALYSIS

To ensure ZVS commutation at wide load range, it is necessary to have enough energy to charge and discharge the capacitances C_1 to C_4.

Two different commutations take place in this converter. During stage 6, the switches S_2 and S_3 commutate while the current through the inductance L_r is equal to the output current Io. Even if this current is null, the current trough auxiliary inductance La_1, which is positive, provides the energy necessary to perform the commutation.

However, at stage 2, the switches S_2 and S_3 commutate when the output current is in a free-wheeling mode through the output rectifiers. Since the resonant inductor L_r can not provide enough stored energy to guarantee the zero-voltage commutation. Thus, the current that flows through auxiliary inductor La_1 must be used to charge and discharge the capacitors in parallel with the switches that are commutating.

Therefore, the following condition must be respected to ensure soft commutation:

$$Io + I_{Lapk} \geq \frac{Vi}{2}.\sqrt{\frac{2.C}{Lr}} \qquad (1)$$

where I_o is the load current referred to the transformer primary side, and I_{Lapk} is the peak value of the current in the auxiliary inductances L_{a1} and L_{a2}.

From equation (1), one can observe that even for no load situation, the zero-voltage switching can be obtained if an appropriate value of peak current in the auxiliary inductances is calculated.

The inductance L_r is determined by the maximum allowed reduction in the duty-cycle, and the auxiliary inductances must be large enough to avoid a significant increase in the conduction losses.

IV. OUTPUT CHARACTERISTICS

The currents provided by the two auxiliary inductors of the CAC does not flow through the inductor Lr and the output rectifiers. So, the output characteristics obtained for the converter with CAC, proposed in this paper, is the same that the one obtained to the ZVS PWM dc-to-dc converter with the flying capacitor cell without the CAC [1].

According to the waveforms shown in figure 3, and considering that the commutation time is much smaller than the switching period, the average output voltage is given by (2), where *n* is the transformer turns ratio.

$$Vo = \frac{Vi}{n}.\left[D - \frac{4.Io.Lr.fs}{Vi}\right] = \frac{Vi}{n}.Deff \qquad (2)$$

It can be noticed that the larger Lr is, the larger is the reduction of the output voltage caused by the reactive voltage drop.

V. SIMPLIFIED DESIGN

The design procedure of the converters studied in this paper is similar to the one presented in [1] for the converter without CAC.

Table I present the input data used in the design procedure.

TABLE I
Input Data

Input voltage – Vi (V)	600
Output voltage – Vo (V)	60
Output power – Po (kW)	1.5
Switching frequency – fs (kHz)	50
Input voltage ripple - ΔVi (V)	15
Output current ripple - ΔIo (A)	2.5
Output voltage ripple - ΔVo (V)	0.06
Clamping voltage ripple - ΔV_{Cc} (V)	3
Maximum duty-cycle – D_{max}	0.4
Maximum nominal duty-cycle reduction (%)	15

a) Transformer turns ratio, resonant inductance, output filter and output rectifiers

The transformer turns ratio, resonant inductance Lr, the output filter Lo and Co, and the output rectifiers are calculated in the same manner as in [1].

b) Auxiliary inductances La_1 and La_2

The minimum current necessary to assure soft commutation is calculated using (1), considering the output current null.

$$I_{Lapk} = 1.723A$$

The auxiliary inductances are calculated by (3).

$$La_1 = La_2 = \frac{Deff.(1 - Deff).Vi}{4.fs.I_{Lapk}} = 390\mu H \qquad (3)$$

c) Clamping capacitances $Cm_{1\text{-}2}$: The clamping capacitances $Cm_{1\text{-}2}$ must be large enough to be considered as a voltage sources. Thus the required value of $Cm_{1\text{-}2}$ is

calculated as a function of the maximum allowable ripple voltage (ΔV_{cc}) using the following expression:

$$Cm_1 = Cm_2 = \frac{Io.(1-2.D_{max})}{n.\Delta Vc.fs} \quad (4)$$

Limiting the voltage ripple to 1% of its average value, yields

$$Cm_1 = Cm_2 = 10\mu F$$

d) Switches Voltage and Current Stresses

1) Active Switches: The maximum voltage across the blocking switches is

$$V_{S\,max} = Vi = 300V \quad (5)$$

From a computer simulation analysis, it was observed that in the converter with the proposed CAC, the current through switches S_1 and S_3 increased their rms value in 7%, and the current through switches S_2 and S_4 increased their rms values in 4%, in comparison with the same converter without CAC.

Therefore, the rms current through switches S_1 and S_3 and through switches S_2 and S_4 can be calculated by (6) and (7) respectively.

$$I_{S13rms} = \left[\frac{Io}{n}.\sqrt{\frac{1}{2}-\frac{\Delta}{6}}\right] x1.07 = 5.44A \quad (6)$$

Through switches S_2 and S_4 the rms current is

$$I_{S24rms} = \left[\frac{Io}{n}.\sqrt{\frac{D}{2}-\frac{\Delta}{6}}\right] x1.04 = 4.71A \quad (7)$$

VI. EXPERIMENTAL RESULTS

In order to analyse experimentally the behaviour of the converter, a prototype was built with the input data presented in Table II. The power stage of the converter is shown in figure 7.

TABLE II
Converter Components

S_1-S_4	IRFP460 – 500V, 20A (Harris)
L_r	16µH –ferrite core E42/15 IP12 (Thornton)
$C_{i1} – C_{i2}$	2µF/400V – polyester (Icotron)
$C_{m1} – C_{m2}$	7 x 1µF/400V – polyester (Icotron)
$L_{a1} – L_{a2}$	390µH –ferrite core E30/14 IP12 (Thornton)
T_r	2 ferrite cores E65/26 - IP12 (Thornton) Prim.: 17 esp. Sec.: 5+5 esp. - 22AWG
D_{o1} - D_{o2}	MUR1560 – 600V, 15A (Motorola)
L_o	89µH – ferrite core E55/21 - IP12 (Thornton)
C_o	220µF/100V - electrolytic (Icotron)

MOSFETs were used to implement switches S_1, S_2, S_3 and S_4. The diodes D_1, D_2, D_3 and D_4 are the MOSFET´s body diodes and the capacitors C_1, C_2, C_3 and C_4, are the MOSFET´s C_{oss} capacitances.

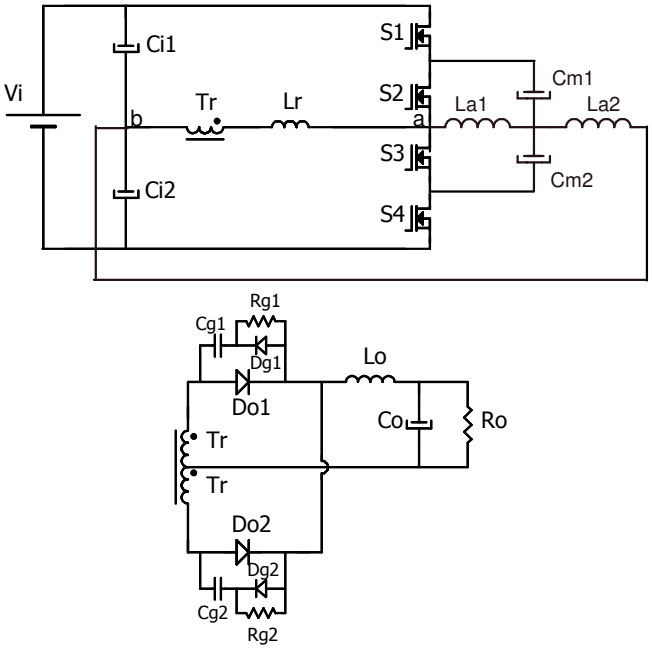

Fig. 4 – Power stage diagram of the implemented converter.

Figure 5 presents the three-level voltage of the inverter stage, the current through the resonant inductor. The waveforms are similar to those obtained for the converter without CAC, as predicted.

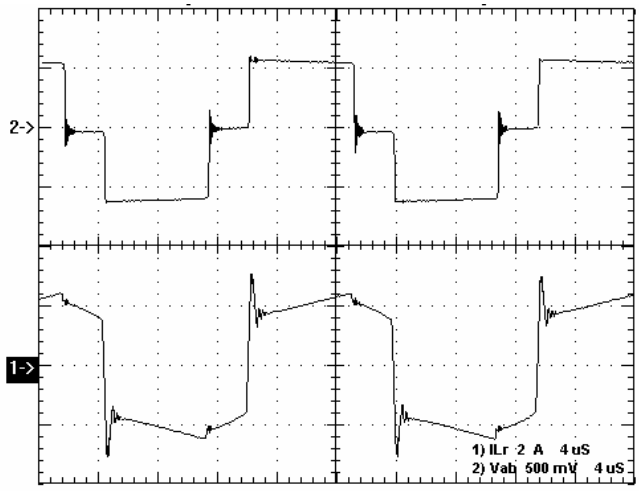

Fig. 5 – Experimental waveforms.
upper trace: voltage v_{ab} (250V/div)
lower trace: current i_{Lr}(2A/div)
Time scale: 4µs/div

The currents and voltages in the auxiliary inductors La_1 and La_2 are presented in figures 6 and 7. The peak current in each inductor is around 1.6A.

Figures 8 and 9 present the voltage and current of switch S_4 for load currents of 18A and 1.7A respectively. It can be observed the zero voltage commutation in the switch even if the load current is lower than the minimum value expected to guarantee soft commutation in the converter without CAC which is 5.8A[1].

Figures 10 and 11 present the same waveforms for switch S_1 on the same load current conditions.

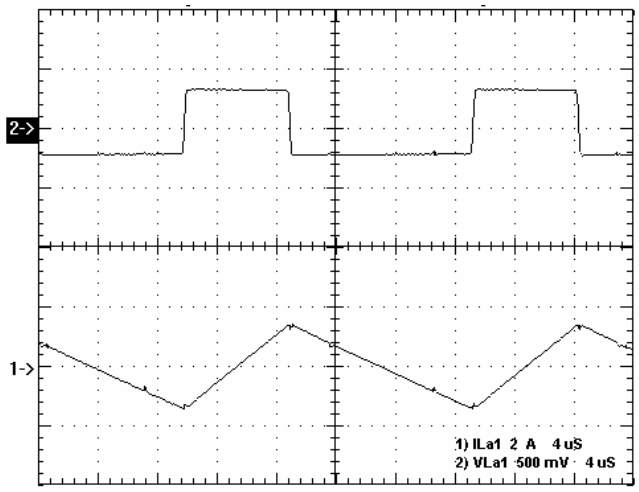

Fig. 6 – Experimental waveforms.
upper trace: voltage v_{La1} (250V/div)
lower trace: current i_{La1}(2A/div)
Time scale: 4µs/div

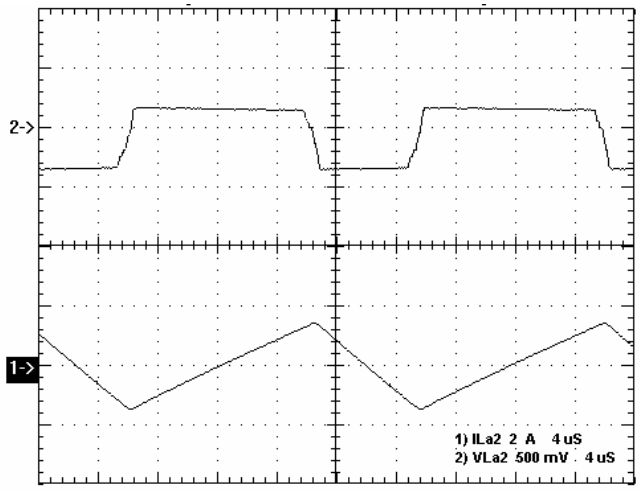

Fig. 7 – Experimental waveforms.
upper trace: voltage v_{La2} (250V/div)
lower trace: current i_{La2}(2A/div)
Time scale: 4µs/div

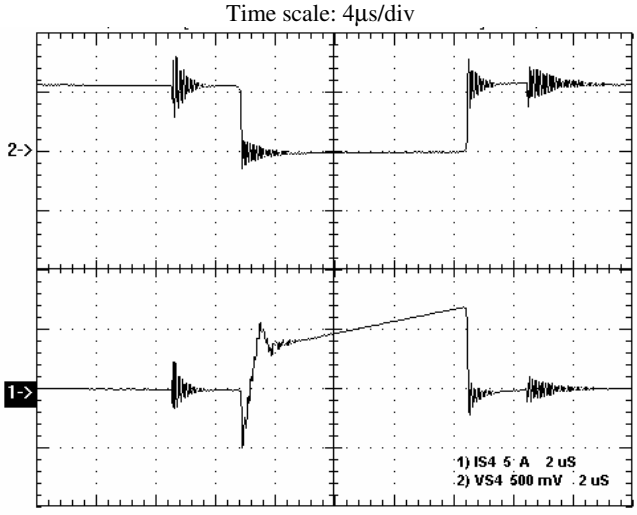

Fig. 8 – Experimental waveforms – Load current = 18A.
upper trace: voltage v_{S4} (250V/div)
lower trace: current i_{S4}(5A/div)
Time scale: 2µs/div

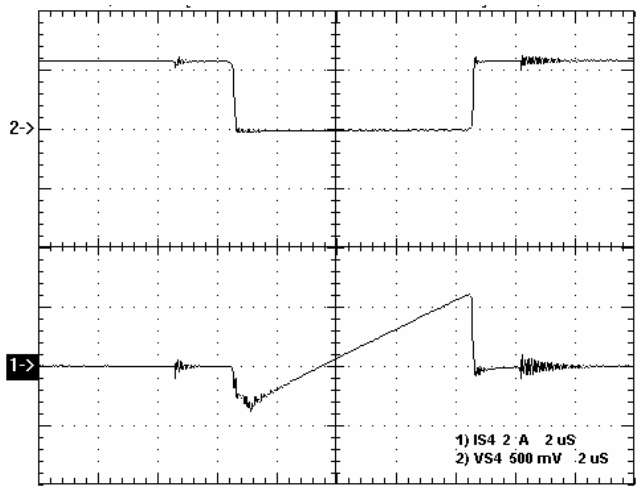

Fig. 9 – Experimental waveforms – Load current = 1.7A.
upper trace: voltage v_{S4} (250V/div)
lower trace: current i_{S4}(2A/div)
Time scale: 2µs/div

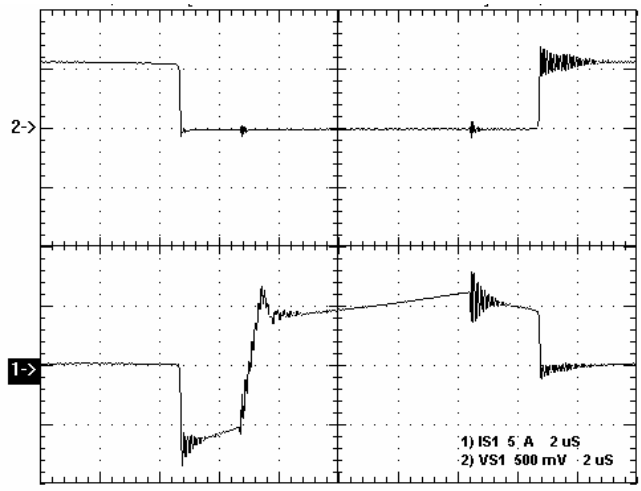

Fig. 10 – Experimental waveforms – Load current = 18A.
upper trace: voltage v_{S1} (250V/div)
lower trace: current i_{S1}(5A/div)
Time scale: 2µs/div

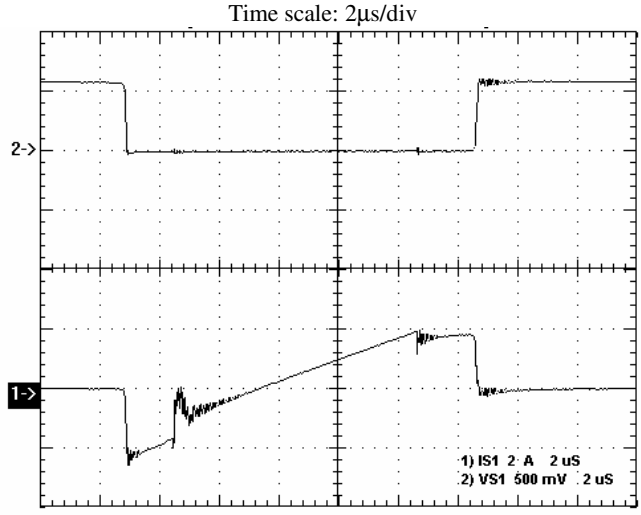

Fig. 11 – Experimental waveforms – Load current = 1.7A.
upper trace: voltage v_{S1} (250V/div)
lower trace: current i_{S1}(2A/div)
Time scale: 2µs/div

It is important to emphasize that the peak voltage across the switches is 300 V, half of the 600 V dc input voltage.

Figure 12 presents the measured efficiency of the converter as a function of the output current, experimentally obtained for constant input voltage equal to 600 V and constant duty-cycle.

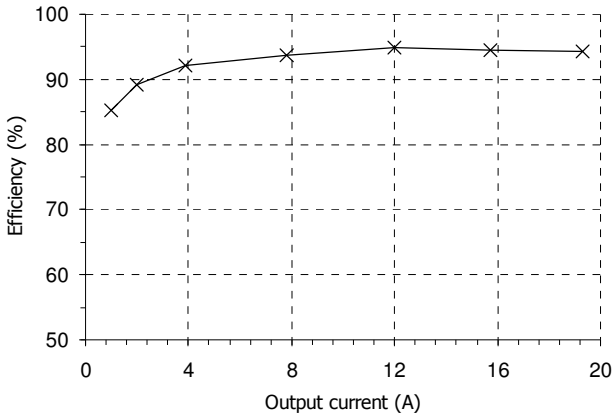

Fig. 12 – Efficiency x output current with CAC.

The main source of losses are diode and MOSFET conduction losses, magnetic and snubber losses. The switching losses at full load are practically null.

In comparison with the results obtained for the converter without CAC [1], the efficiency for output currents below 5A (when the ZVS commutation is lost and the converter starts to operate with hard-switching for the circuit without CAC), the efficiency of the proposed converter is slightly higher.
For currents next to the nominal current, the efficiency of the proposed converter is lower than the efficiency of the converter without CAC [1].

VII. CONCLUSIONS

The proposed isolated ZVS-PWM DC-to-DC converter with the commutation auxiliary circuit presents identical characteristics to the three-level DC-to-DC converters based on the flying capacitor cell [1], on the NPC cell [5], and to FB-ZVS-PWM converter [4], such as:

- high-efficiency due to ZVS commutation on the switches;
- half of the input voltage across the blocking switches makes this converter suitable for high-input voltage applications.

Soft switching can be guaranteed in a wide load range. To achieve that it is necessary to include two inductors only, since the capacitors needed to build the commutation auxiliary circuit are already present in the original three-level dc-to-dc converter based on the flying capacitor multilevel cell.

The raise of the conduction losses caused by the additional current provided by the commutation auxiliary circuit are not significant and can be minimised with a proper design of the auxiliary inductors.

VIII. ACKNOWLEDGMENTS

This work was developed with the financial support of FUNCITEC (Technology and Science Foundation of the Santa Catarina State Government) and FURB.

The authors would like to thank the Electrical Enginering Departament technician, Mr. Márcio Nagel for his support in the prototype building. Special acknowledgemnets are due to the Electrical Engineering Student Gustavo Klitzke, whose help in the laboratory made possible to obtain the experimental results.

REFERENCES

[1] E. Deschamps and I. Barbi, “A Three-Level ZVS PWM DC-to-DC Converter Using the Versatile Multilevel Commutation Cell”, *COBEP’97 Brazilian Power Electronics Conference Record*, pp. 85-90.

[2] J.L.F. Vieira and I. Barbi, “High Power Full Bridge Zero Volateg Switching PWM Off-Line Power Supply with Wide Load Range”, *COBEP’91 Brazilian Power Electronics Conference Record*, pp. 14-20.

[3] J.R. Pinheiro and I. Barbi, “Wide Load Range Three-Level ZVS-PWM DC-to-DC Converter”, *PESC´93 Conference Record*, pp. 171-177.

[4] J.A. Sabaté, V. Vlatkovic, R.B. Ridley, F.C. Lee and B.H. Cho, “Design considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter”, *APEC’90 Conference Records*, pp. 275-284.

[5] J. R. Pinheiro and I. Barbi, “The Three-Level ZVS PWM DC-to-DC Converter”, *IEEE Transactions on Power Electronics*, vol. 8, no. 4, Oct. 1993, pp. 486-492.

[6] T.A. Meynard and H. Foch, “Multilevel Conversion: High-Voltage Choppers and Voltage-Source Inverters”, *PESC’92 Conference Records*, pp. 397-403.