A LOW POWER DYNAMIC VOLTAGE RESTORER WITH VOLTAGE HARMONIC COMPENSATION

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***Abstract* – The increasing use of voltage sensitive loads in industrial applications nowadays has brought a real concern about interruption costs and damages in complex production lines. This paper presents a power-electronic–based device which compensates voltage sags, swells and voltage harmonic distortion, restoring the load voltage to acceptable values through a series connected injection transformer. The ratings and power requirements of a low-power Dynamic Voltage Restorer (DVR) are derived, as well as its deadbeat control algorithm implemented in a Digital Signal Processor (DSP). Finally, simulation and experimental results of a 5-kVA prototype are presented.**

***Keywords* - DSP controlled converter, Dynamic Voltage Restorer (DVR), Power Quality, Voltage Sags.**

I. INTRODUCTION

Disturbances within the power systems can affect sensitive devices present in most of the production lines. According to [1], a Voltage Sag is defined as a decrease in the rms voltage magnitude between 0.1–0.9 per unit (p.u.) at the fundamental frequency and duration from 0.5 cycles to 1 min. Voltage sags are commonly caused by faults on adjacent lines of the power system or by large motors startup, and may cause misoperation or fails. A Voltage Swell is defined as an increase in the rms voltage magnitude at the fundamental frequency and duration from 0.5 cycles to 1 min, which may lead sensitive devices to be permanently damaged. Typical magnitudes are between 1.1 and 1.8 p.u.

The interruption costs of industrial processes depend on the load sensibility and on the process itself. Typically a four-hour outage costs US$74,835.00, while a voltage sag of 0.1 p.u. or 0.2 p.u. which lasts only 15 cycles may cost US$7,694.00 [2], proving that these power quality phenomena are real concerns nowadays in industrial facilities.

In order to mitigate these problems, a possible solution, based on power-electronic devices is the Dynamic Voltage Restorer (DVR), which is series connected to the load by means of injection transformers and restores the load voltage magnitude during voltage sags. DVRs add to the mains voltage a pre-defined voltage synthesized by a power inverter in order to keep the load voltage within acceptable values.

The main advantage of a DVR is, as the device injects the difference between the remaining mains voltage and the reference voltage only during voltage sags or swells, there is no need to store the energy to supply full load, as it happens for Uninterruptible Power Supplies (UPSs). However, DVRs are not designed to work when an outage occurs, as UPSs devices do, which is the major disadvantage of the adopted solution.

This paper describes the rating of a DVR that compensates voltage sags, swells and voltage harmonics. The control technique, phase-locked-loop (PLL) algorithm, voltage reference generation and power converter modeling are discussed. Simulations results of the device in a power utility are also presented. Finally, the proposed approach is implemented in a Digital Signal Processor (DSP) in a 5-kVA/220V prototype and its validity is evaluated through experimental results.

II. TOPOLOGY

The single-phase diagram of the DVR is shown in Fig. 1. A pulse-width-modulated (PWM) full bridge single-phase inverter is connected to a LC filter and a single-phase series transformer. Three equal arrangements allow zero sequence voltage injection.

It is important to note that the energy required to charge DC-link capacitors comes from the mains where the device is installed, by means of a non-controlled three-phase bridge rectifier and a delta-wye transformer. As a consequence, in order to avoid voltage collapse during voltage sags, charging limitation is introduced through resistors in the output of the AC/DC converter. On the other hand, during voltage swells, a DC/DC converter and discharging resistors are operated in order to limit DC-link voltage and to satisfy load voltage specifications.

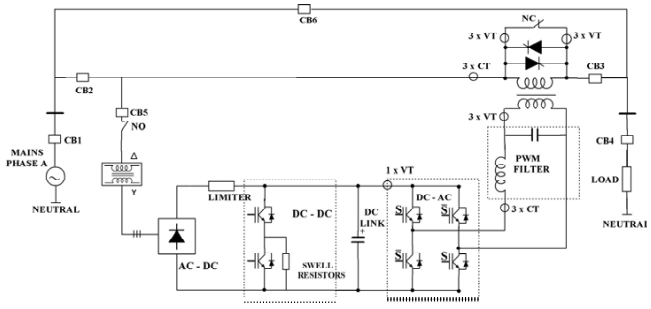

Fig. 1. Single-phase diagram of the DVR

It is well known that the DVR shall not interfere in the protection coordination of the considered load. Moreover, when faults as short-circuits occur in the load connected

mains, the DVR must be isolated from the mains circuit in order to protect its power electronics and other internal sensitive devices. Thus, fast solid-state switches and normally closed contactors are placed in parallel with the injection transformer's primary windings. It was foreseen the inclusion of auxiliary circuit breakers in order to allow DVR replacement or maintenance without interrupting the load.

Fig. 1 also shows Current and Voltage Hall-Effect transducers (CT and VT, respectively) for control and monitoring purposes.

III. DVR RATING DERIVATION [3]

A. Initial Assumptions

The proposed DVR can compensate a maximum single-phase voltage sag magnitude $v_{sag1\phi} = 0.5pu$, maximum three-phase voltage sag magnitude $v_{sag3\phi} = 0.65pu$, maximum voltage sag duration $\Delta t=500ms$ for a maximum three-phase load apparent power $S_{3\phi load} = 10\ kVA$ and nominal line-to-line rms voltage $v_{L\text{-}L} = 220V$.

Assuming the load power factor equal to unity and that the injected voltage is in phase with the mains voltage, the maximum power transfer from the DVR to the load occurs for the maximum three-phase voltage sag specification, where the relation between the DVR apparent power and load apparent power is $S_{DVR} / S_{3\phi load} = 0.35$.

B. Transformer and Inverter Ratings

Taking the load side as the primary and the inverter side as the secondary of the injection transformer, its turns ratio is derived from the relationship between the peak values of the minimum inverter voltage, that is approximately equal to the minimum DC-link voltage v_{CCMIN} , and the maximum rms primary voltage of the DVR v_{DVR}:

$$\frac{N_S}{N_P} \cong \frac{v_{CCMIN}}{(1+k_L)\cdot\sqrt{2}\cdot v_{DVR}} \tag{1}$$

where k_L is the inductor voltage drop in p.u. assuming the inverter voltage as base, N_P is the primary turns number and N_S is the secondary turns number. Writing v_{DVR} as a function of the maximum single-phase voltage dip $\alpha_{1\phi}$:

$$\frac{N_S}{N_P} = \frac{v_{CCMIN}}{0.8165\cdot v_{L-L}\cdot\alpha_{1\phi}\cdot(1+k_L)} \tag{2}$$

The inverter current is equal to the secondary current of the injection transformer plus the filter capacitor current:

$$i_{inv} = \frac{0.8165\cdot(1+k_C)\cdot(1+k_L)\cdot v_{L-L}\cdot i_{LOAD}\cdot\alpha_{1\phi}}{v_{CCMIN}} \tag{3}$$

where k_C is the capacitor current in p.u. considering the inverter current as base and i_{LOAD} is the load current. Multiplying the inverter current by the inverter single-phase voltage, the three-phase inverter apparent power may be written as:

$$S_{inv3\phi} = \frac{S_{3\phi load}\cdot\alpha_{1\phi}\cdot(1+k_C)\cdot(1+k_L)}{\gamma} \tag{4}$$

$$\gamma = \frac{v_{CCMIN}}{v_{CCMAX}}, \qquad 0 \le \gamma \le 1 \tag{5}$$

where γ is the maximum DC link voltage dip and v_{CCMAX} is the maximum DC link voltage.

C. DC Link Capacitor Derivation

The DC-link capacitor bank energy is given by:

$$\varepsilon = 1/2\cdot C\cdot\Delta v_{CC}^2 \tag{6}$$

$$\varepsilon = 1/2\cdot C\cdot v_{CCMAX}^2\cdot\left(1-\gamma^2\right) \tag{7}$$

The capacitor dimensioning is based on the maximum injected active power of the DVR that occurs for the three-phase voltage sag case:

$$\varepsilon = P_{load}\cdot\alpha_{3\phi}\cdot\Delta t \tag{8}$$

where P_{load} is the load active power and $\alpha_{3\phi}$ is the maximum three-phase voltage dip. Substituting (7) into (8):

$$C = \frac{2\cdot P_{load}\cdot\alpha_{3\phi}\cdot\Delta t}{v_{CCMAX}^2\left(1-\gamma^2\right)} \tag{9}$$

D. Output Filter Design

The PWM filter is designed as a second order LC-low-pass filter whose resonance frequency is approximately one decade below the switching frequency and one decade above the fundamental frequency. Setting $k_L = 0.1$, $k_C = 0.1$, the fundamental frequency $f = 60Hz$ and the resonance frequency of the filter $f_r = 1kHz$, the filter inductance is $L_F = 3.947mH$. Consequently, the PWM filter capacitance is equal to $C_F = 6.417\mu F$.

E. Final Dimensioning Considerations

As can be noted from (1), (4) and (9), the injection transformer turns ratio, the inverter apparent power and the DC-link capacitor are strictly related to γ. For instance, fig. 2 shows that a small value of γ implies smaller DC-link capacitor size and higher inverter KVA ratings. Thus, there must be a compromise solution considering these three variables.

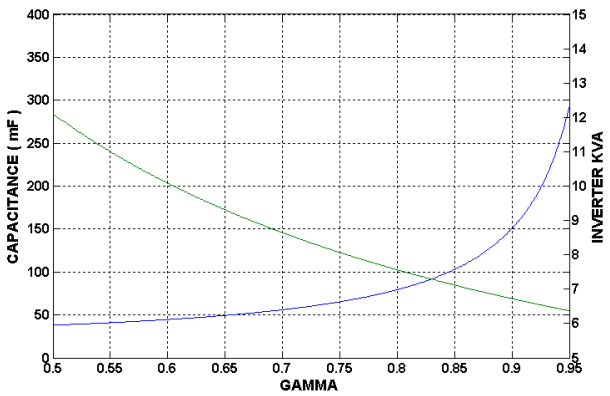

Fig. 2. Inverter KVA rating and DC-link capacitance as function of γ (gamma)

Assuming $P_{load} = 10\ kW$, $v_{CCMAX} = 350V$, $\gamma = 0.7$, $k_L = k_C = 0.1$, $\alpha_{1\phi} = 0.5$, $\alpha_{3\phi} = 0.35$ and $v_{L\text{-}L} = 220V$, the injection transformer turns ratio is $N_S/N_P \approx 2.50$, the DC-link capacitance is $C = 56mF$ and $S_{INV3\phi} = 8.642\ kVA$.

The apparent power of a single-phase transformer is $S_{TR1\phi} = 1.67\ kVA$. As stated in [4], depending on DVR starting instant and on the transformer load, the flux linkage can be as much as the double of its maximum rated value for the worst

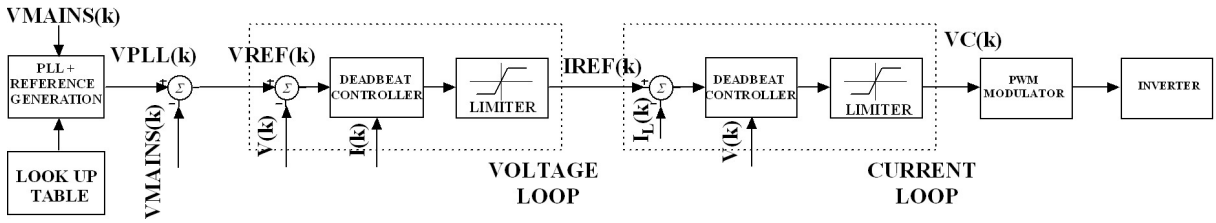

Fig. 3. DVR Control System Block

case and the transformer may saturate. Thus, in order to avoid saturation, the apparent power of each transformer shall be multiplied by two, resulting in $S_{TR1\phi} = 3.33\ kVA$. This solution is cost-effective for low-power DVRs[4].

As the proposed DVR is designed to compensate voltage harmonics in steady-state, it will be always connected to the load, except when faults as short-circuits occur in the grid. The disadvantage of continuous operating mode is essentially the inverter switching losses. The main advantages are speed of response of the device, since there is no standby (idle) mode. The choice of steady-state DVR with harmonic compensation can be determined by the load sensibility, which is analyzed during project development.

IV. CONTROL SYSTEM

A. Control algorithm

Fig. 3 shows a simplified block diagram of the discrete time control algorithm of the DVR under analysis. The algorithm is essentially composed by three blocks: Reference Generation and Phase Locked Loop (PLL), Voltage Loop and Current Loop.

Referring to fig.3, where k is the k-th sample, the PLL reference voltage $v_{PLL}(k)$ is compared to the mains voltage $v_{MAINS}(k)$ in order to determine the input reference voltage of the voltage loop block $v_{REF}(k)$, that is, the voltage to be synthesized by the power converter.

Since the tracking error after a certain number of modulation periods must be zero and a simple design and implementation as well as a fast dynamic response is always achievable, deadbeat response controllers are adopted in current and voltage loops. However, a reasonable model of the system under control must be employed for a good performance of digital predictive controllers [6], [7].

The output of the voltage controller establishes the filter inductor current reference $i_{LREF}(k)$. The current controller is responsible for tracking the reference current, forcing the error to zero. The current controller also provides overload protection by limiting the inductor current. Finally, the output of the current loop $v_C(k)$ is the voltage reference of the PWM modulator.

B. Reference Generation and Phase-locked-loop (PLL)

The magnitude and the phase angle of the reference voltage $v_{PLL}(k)$ are generated by means of an internal normalized sinusoidal signal obtained from a look up table. The frequency of $v_{PLL}(k)$ is given by the PLL.

The Phase Locked Loop (PLL) is based on a rising zero-crossing detection of the sinusoidal reference in order to generate synchronization signals with the same frequency of the mains voltage. The algorithm is implemented in a discrete-time model and consists in forcing the first sample of the next mains period to be coincident with the zero crossing of the internal reference voltage $v_{PLL}(k)$, by inserting equally spread samples (fig.4).

At the first time the algorithm runs, it detects the first zero-crossing and calculates the voltage reference phase angle. From the second zero-crossing on, as a new detection occurs, a new computation of the sampling period $\Delta(k)$ is made, taking into account the previous mains period $\Delta_{MAINS}(k-1)$, the last cumulative number of samples $n'(k-1)$, the total number of samples per mains period n and the current zero-crossing error $\Delta_{ERR}(k)$, according to (10):

$$\Delta(k) = \frac{\Delta_{MAINS}(k-1) - \Delta_{ERR}(k) - \Delta(k-1)}{2n - n'(k-1) - 1} \quad (10)$$

It shall be noted that the zero crossing calculation is based on a linear interpolation, since a sinusoidal signal is approximately linear near zero-crossing region.

The PLL and reference generation algorithms are applied only for a reference phase A. The voltage references for the remaining phases (B,C) are calculated by displacing a pre-defined number of samples in order to obtain a balanced three-phase system, i.e., load voltage unbalances compensation can be achieved. Load voltage harmonic and sag-swell compensation is implemented by calculating $v_{REF}(k)$.

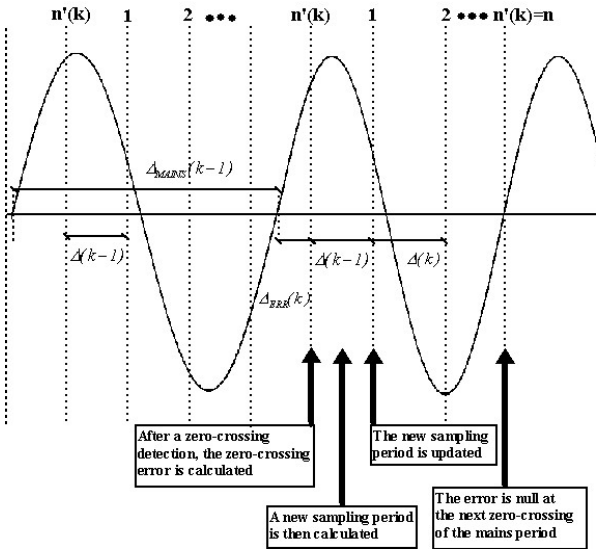

Fig. 4. PLL algorithm graphical description

C. Current and Voltage Loops

Considering the averaged model of fig.5, the inverter is represented by a controlled voltage source. In order to keep

the inverter voltage and output current constant between two sampling periods [7], a zero-order hold sampling of the PWM reference voltage must be assured. Assuming that the sampling frequency is much greater than the resonance frequency of the output filter, the control system discrete time dynamic equations are:

$$x(k+1) = \Phi \cdot x(k) + \Gamma_1 \cdot v_{REF}(k) + \Gamma_2 \cdot i(k) \quad (11)$$

$$y(k) = D \cdot x(k) \quad (12)$$

where:

$$\Phi = \begin{bmatrix} 1 & \Delta/C_F \\ -\Delta/L_F & 1 \end{bmatrix}, \ \Gamma_1 = \begin{bmatrix} \Delta/C_F \\ 0 \end{bmatrix}, \ \Gamma_2 = \begin{bmatrix} 0 \\ \Delta/L_F \end{bmatrix}$$
$$D = \begin{bmatrix} 1 & 0 \end{bmatrix} \qquad x(k) = \begin{bmatrix} v(k) \\ i_L(k) \end{bmatrix} \quad (13)$$

where $v(k)$ is *k-th* output voltage at the inverter side, $i_L(k)$ is the *k-th* filter inductor current and $i(k)$ is the *k-th* load current at the inverter side of the DVR.

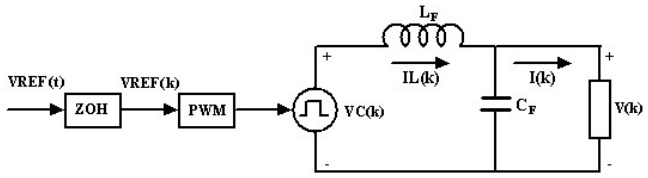

Fig. 5. Inverter averaged model

Rearranging (11), (12) and (13), the current and voltage loops are described by (14) and (15), respectively:

$$v_C(k) = \frac{i_L(k+1) - i_L(k)}{\Delta} \cdot L_F + v(k) \quad (14)$$

$$i_{LREF}(k) = \frac{v(k+1) - v(k)}{\Delta} \cdot C_F + i(k) \quad (15)$$

The control technique consists in making the current error equal to zero by the end of the following sampling period, that is:

$$i_L(k+1) = i_{LREF}(k) \quad (16)$$

$$v(k+1) = v_{REF}(k) \quad (17)$$

Substituting (16) in (14), considering the output voltage samplings as disturbances in the current loop and applying the z-transform to the resultant equation, the closed loop poles in z-plane are [8]:

$$z_{1,2} = \frac{1}{2} \pm \frac{j}{2}\sqrt{4\alpha - 1} \quad (18)$$

where α is a constant that represents a mismatch between the modeled and real filter inductances. As can be seen in (18), deadbeat response is not achieved in the current loop, since the closed loop poles are not at the origin. Moreover, if $\alpha = 1$, a low-order frequency equal to *1/6* of the sampling frequency will be present in the inductor filter current [8], but according to the classical definition of stability, the system is not unstable. As a consequence, care must be taken when designing the output LC filter and detuning shall be considered as an option to avoid undesirable resonances.

As a fixed number of samples per cycle of the mains voltage is adopted [5], the sampling frequency, which is equal to the switching frequency, is not constant in order to achieve synchronization. Indeed, this does not change the relationship between the damping and switching frequency in the current loop, but the controller dynamic response becomes slower.

V. SIMULATION RESULTS

The DVR control system was simulated with PSIM (v.5.01) for a two-phase voltage sag to 58% (remaining voltage) with 17.5% of the nominal load current for a resistive load and simulation parameters of Table 1. Referring to section III.D, the filter inductance, switching frequency and the filter capacitor were modified during project development.

TABLE 1
DVR simulation parameters

Mains Voltage Harmonic Content: 3rd (4%); 5th (3.7%); 9th (1.25%)	
Mains voltage phase-to-neutral magnitude	$127V_{RMS}$
Load current percentage	17.5%
DC-Link Voltage	350V
Output filter inductance	5mH
Output filter capacitance	7.5μF
Switching frequency	6667kHz
Series transformer turns ratio (Ns/Np)	2.51
Series transformer pri.winding leakage inductance *	0.0667 mH
Series transformer sec.winding leakage inductance*	0.1234 mH
Series transformer magnetizing inductance	3.8411H
Series transformer pri.winding resistance *	56.6mΩ
Series transformer sec.winding resistance *	44.24m Ω

* Referred to primary side

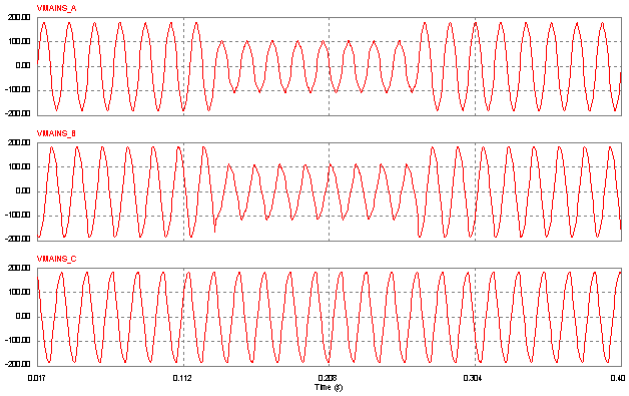

Fig. 6. Two-phase voltage sag to 58% (simulation), mains voltages. Phase A (top), phase B (center), phase C (bottom)

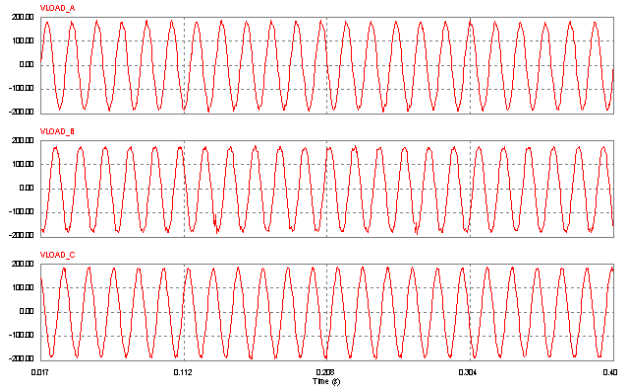

Fig. 7. Two-phase voltage sag to 58% (simulation), load voltages. Phase A (top), phase B (center), phase C (bottom)

The PLL and reference generation block was represented by a sinusoidal, 60Hz voltage-source. Fig. 6 and fig. 7 show the mains and load voltages, respectively.

The DVR injected voltage can be seen in fig. 8 (center). It is important to note that in steady-state the DVR compensates voltage harmonics with relatively low active power requirements when compared to the voltage sag interval of fig.8.

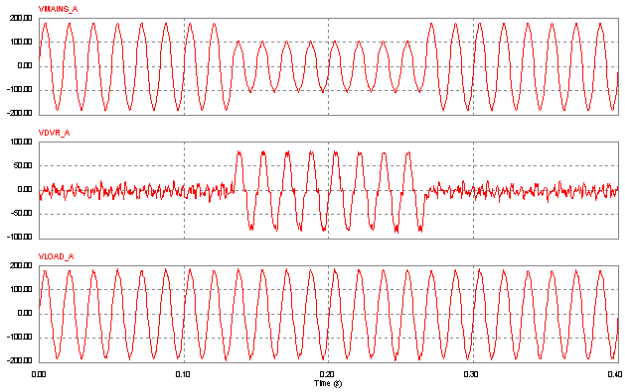

Fig. 8. Two-phase voltage sag to 58% (simulation), phase A. Mains Voltage (top), Injected Voltage (center), Load Voltage C (bottom)

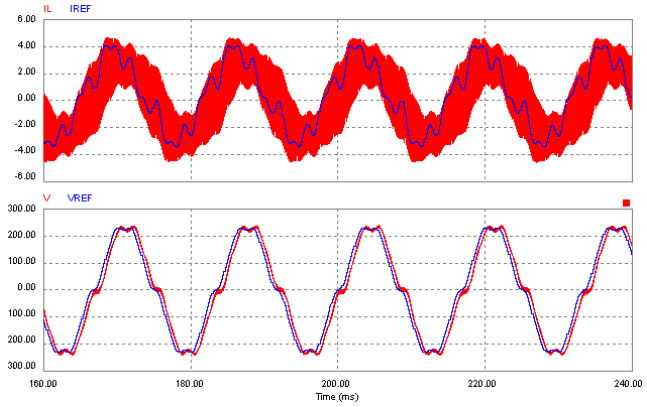

Fig. 9 . Control loop during voltage sag to 50% (simulation). Reference current (top blue), Inductor current (top red), Output capacitor reference voltage (bottom blue), Output capacitor voltage (bottom red)

In Fig. 9, current and control loops behavior during voltage sags is evaluated. It can be observed that the controllers have reasonable tracking performance with the presence of voltage harmonic distortion and even with low load current levels, when inductor current ripple is quite high. Further improvements on control are under study.

VI. EXPERIMENTAL RESULTS

The control algorithm was implemented in a 16-bit fixed-point Analog Devices ADSP21992 DSP in the 5-kVA/220V prototype of fig.10.

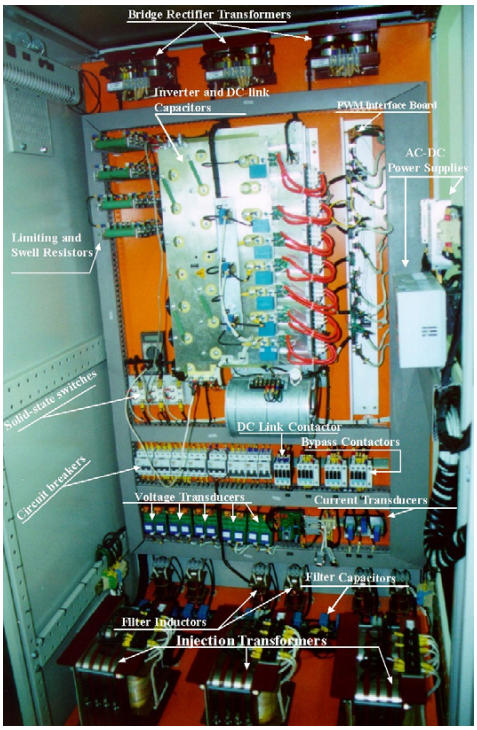

Fig. 10 . 5kVA/220V-DVR-prototype

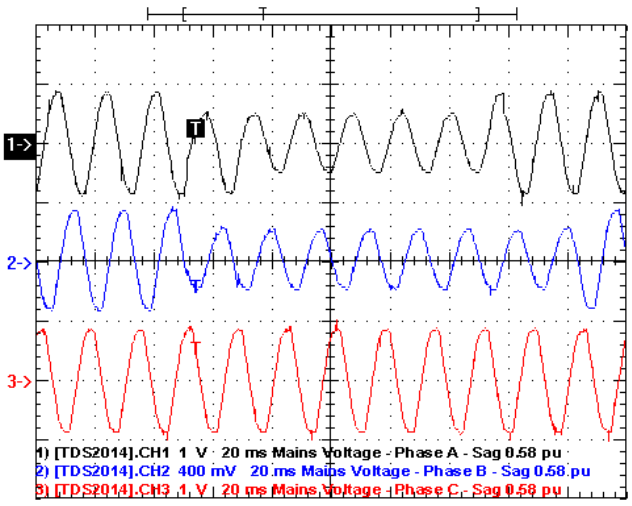

Fig. 11 . Mains Voltages – Two-phase voltage sag to 58% (measured) -Top: Phase A, Center: Phase B, Bottom: Phase C

The prototype was tested with parameters of Table 1 for a two-phase voltage sag to 58%. Voltage sags were generated by using 0.05 p.u. series resistors in the mains circuit and by inserting 0.075 p.u. parallel resistors for voltage sags., taking as base the line-to-neutral load voltage and the load current. Fig. 11 and fig. 12 show the mains and load voltages, respectively, obtained with differential oscilloscope probes. The injected voltage during voltage sags and steady-state for Phase A can be noted in Fig. 13.

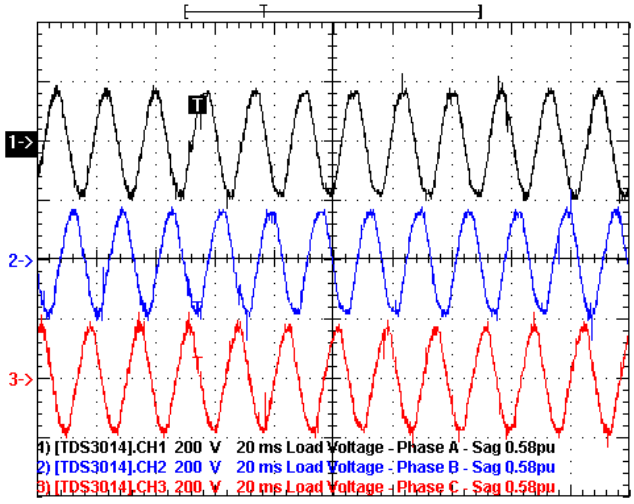

Fig. 12 . Load Voltages – Two-phase voltage sag to 58% (measured) –Top: Phase A, Center: Phase B, Bottom: Phase C

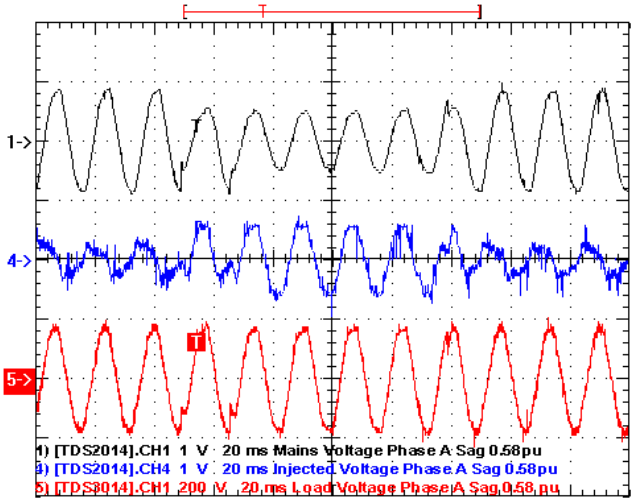

Fig. 13 . Two-phase voltage sag to 58% (measured), phase A. Mains Voltage (top), Injected Voltage (center), Load Voltage C (bottom)

VII. CONCLUSION

This paper has presented the simplified design and power requirements as well as the control algorithms derivation of a low-power Dynamic Voltage Restorer (DVR) which compensates voltage harmonics and voltage sags/swells. The algorithms were analyzed through computer simulation and implemented in a Digital Signal Processor (DSP). Finally, experimental results of a 5-kVA/220V prototype have been presented in order to validate the proposed approach.

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