PROPOSAL OF A SWITCH-MODE POWER SUPPLY BY THE ASSOCIATION OF AN INTERLEAVED BOOST-FLYBACK CONVERTER AND AN INTERLEAVED FORWARD TOPOLOGY

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Abstract — **This work presents the analysis of a switch-mode power supply operating at high switching frequency with high efficiency. An almost unity input power factor is obtained when an interleaved Boost-Flyback converter associated with a nondissipative snubber is used as a preregulator stage. An interleaved Forward converter is used as DC-DC stage, as the combination of both topologies results in the proposed SMPS. Theoretical background on each one of the converters is presented, and analytical results on the proposal are discussed in order to validate the proposal.**

Keywords — power factor correction, SMPS, soft switching.

I. INTRODUCTION

Power supplies are very important units for electronic devices, because they provide the necessary voltages for their accurate operation. The evolution of such equipment has demanded the reduction of the size, weight and volume of power supplies. Generally, they employ AC voltages as primary power source, which must be converted to DC voltages [1].

Linear power supplies are adequate for low power applications, but are uneconomical and inefficient when more power is required. The alternative lies in the use of switch-mode power supplies (SMPS), which present multiple output DC voltages, constant switching frequency and reduced size and weight when compared with linear units [2].

However, the input stages of switch-mode power supplies are well known to be harmonic sources. Recently, there has been great interest about the reduction of the input current harmonic content and also power factor correction (PFC) [3]. Moreover, in many single-phase applications, the power levels can reach several kilowatts and, in some cases, the input voltage can be quite high as well. For such types of application, conventional Boost PFC converters have been intensively used as preregulator stages due to the characteristics of DC-voltage gain, lower inductor volume and weight, and reduced losses on the power devices, which will affect converter cost, efficiency, and power density [3]-[5]. Conventional resonant and quasi-resonant converters [6]-[9] provide Zero-Current Switching (ZCS) and/or Zero-Voltage Switching (ZVS) [10]-[11], as they can operate at high frequency. However, such techniques have load limitation, because there are current and/or voltage stresses over the switches, and the control frequency range is restricted, complicating the design of the filter components. Interleaving techniques consist in the interconnection of multiple switching cells for which the operating frequency is the same, but the internal switching instants are sequentially phased over fractions of the switching period. The converter described in [12] employs this strategy with power factor correction IC UC3854, although the switching frequency is 100kHz. Within this context, this paper employs an interleaved Boost-Flyback converter to be used as a preregulator stage. Two switching cells operate at 100kHz each, as the design of the filter inductors and filter capacitors is performed with a switching frequency equal to 200kHz. It means that the sizes of the filter elements are substantially reduced if compared with the case studied in [13]. Further information about this converter can be found in [14].

Switch-mode power supplies are employed in DC voltage step-up or step-down. A DC-DC interleaved Forward converter [15] using a nondissipative snubber [16] that can reach high frequencies and high power levels is used in the proposed SMPS. This topology also presents some prominent advantages i.e. soft switching for a wide load range and reduced conduction losses.

II. THE PROPOSED SMPS

As mentioned above, PFC is a desirable feature in power supplies, and a preregulator stage is necessary. Therefore an AC-DC stage is supposed to be associated with a DC-DC converter. The AC-DC and DC-DC converters are shown in Fig. 1 and Fig. 2, respectively, and Fig. 3 depicts the proposed SMPS.

To simplify the analysis, the converters will be presented separately.

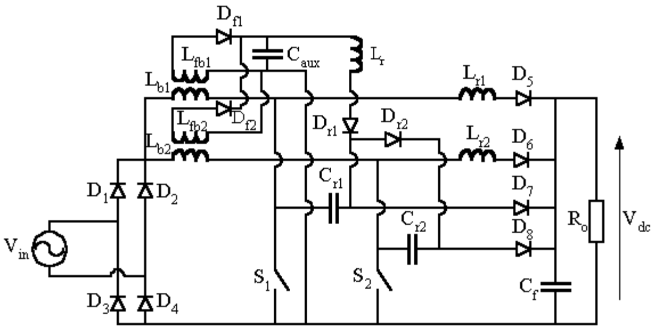

Fig. 1. AC-DC Interleaved Boost-Flyback Converter associated with a nondissipative snubber.

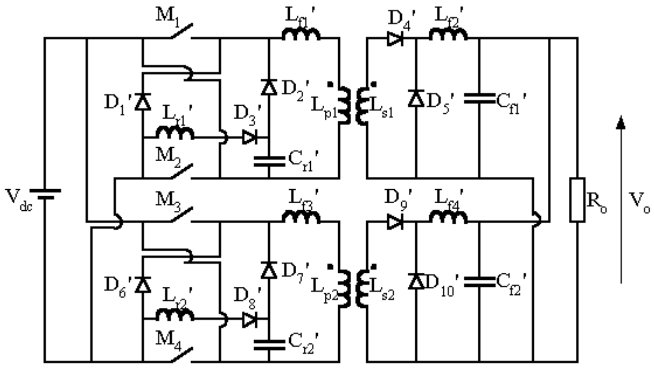

Fig. 2. DC-DC Interleaved Forward converter using a soft-switching cell.

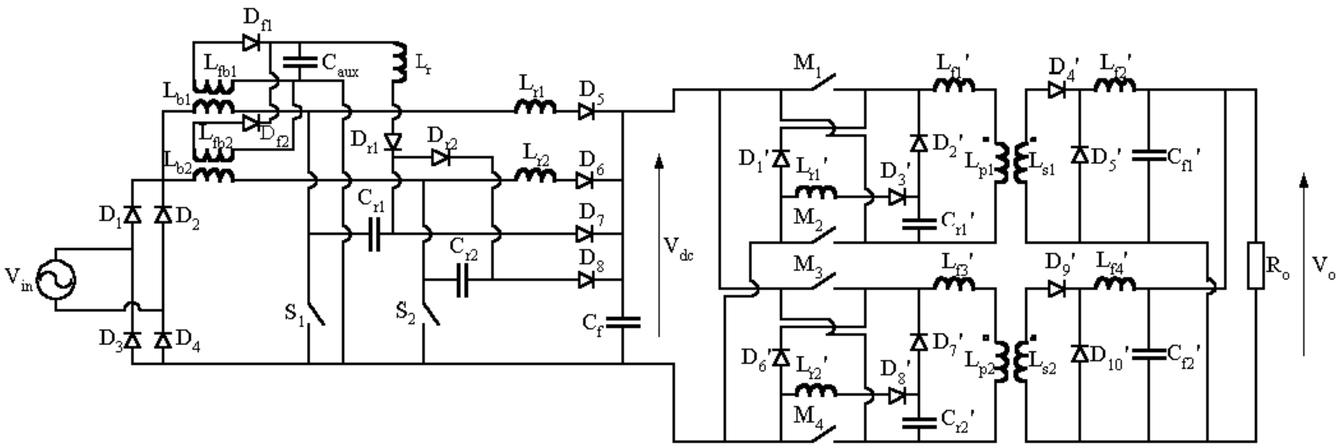

Fig. 3. Proposed high power factor switch-mode power supply.

III. AC-DC INTERLEAVED BOOST-FLYBACK CONVERTER AND POWER FACTOR CORRECTION

Fig. 1 shows the interleaved converter associated with a nondissipative snubber to be used as a preregulator stage. The study of the converter is available in [14], and design guidelines on the circuit parameters are given in [17].

This stage operates with constant switching frequency and high power factor, using the average current mode control [18]-[19], illustrated in Fig. 4, which eliminates many serious problems, such as poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain can not correct. However, the strategy demands current sensors and multipliers, increasing control complexity. In Fig. 4, T_{on} is the on-time of the switch driven by UC3854 and T_s is the switching period.

The control strategy represented in Fig. 5 monitors the input current, which is supposed to follow a reference signal. It is created when the rectified line voltage (A and C) is multiplied by the output voltage (B). Hence the input voltage waveform is supposed to be nearly sinusoidal, which implies nearly unity displacement power factor and reduced harmonic distortion. In this case, this process is implemented by UC3854 [18].

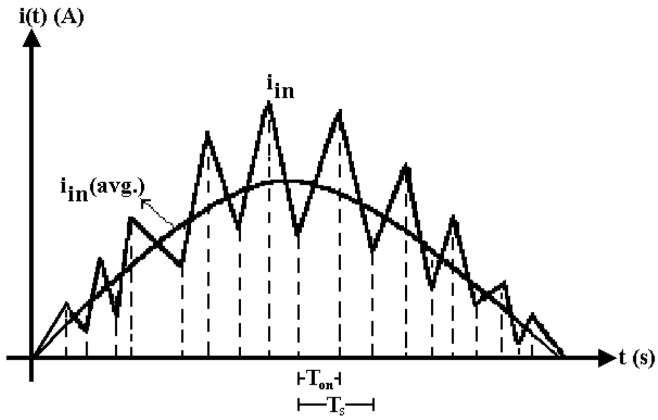

Fig. 4. Principle of the average current mode control.

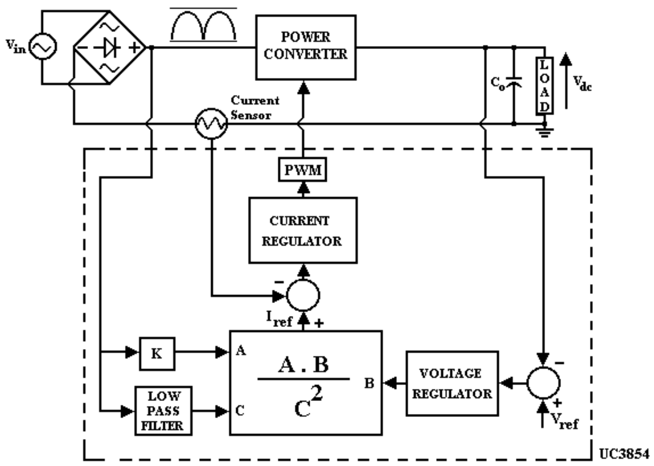

Fig. 5. Control strategy employed by the preregulator stage.

IV. DC-DC INTERLEAVED FORWARD CONVERTER

Fig. 2 shows the interleaved Forward converter associated with a nondissipative snubber, representing the DC-DC stage of the SMPS. The switches are turned on and off in ZCS and ZVS modes, respectively, due to the resonant cell [20] [21]. The PWM converter operates using IC UC3525A, according to the block diagram shown in Fig. 6. Additional information on this approach can be found in [15].

The transfer function between output voltage V_o and DC voltage V_{dc} is given by (1) [15].

$$G' = D' - \frac{F_S'}{2\omega_{04}}\left(\alpha_1 - \frac{1}{\alpha_1}\right) \tag{1}$$

By definition [15], parameter K_f' is:

$$K_f' = \frac{f_s'}{\omega_{04}} \tag{2}$$

Substituting (2) in (1), it results:

$$G' = D' - \frac{K_f'}{2}\left(\alpha_1 - \frac{1}{\alpha_1}\right) \tag{3}$$

Expression (3) can be plotted as a function of parameter α_1, as shown in Fig. 7. From [15], one can obtain the waveforms shown in Fig. 8.

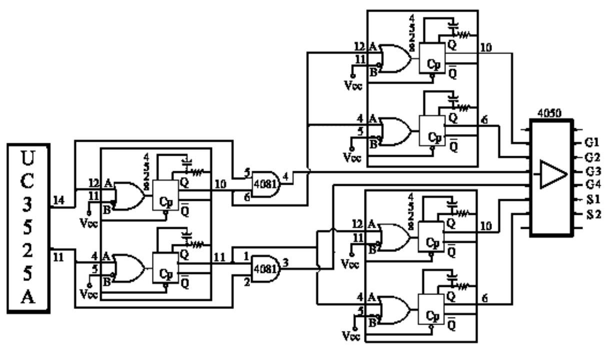

Fig. 6. Control circuit employed in the DC-DC converter.

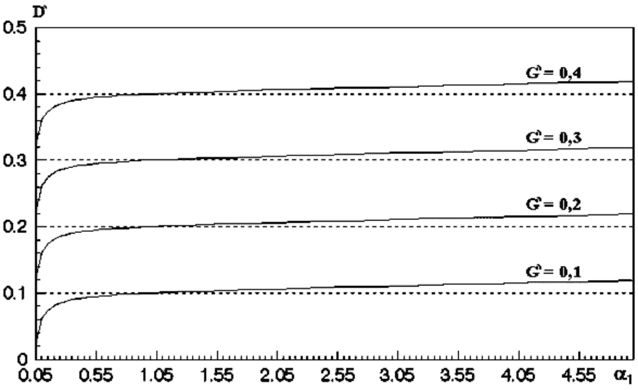

Fig. 7. Output characteristic of the interleaved Forward converter.

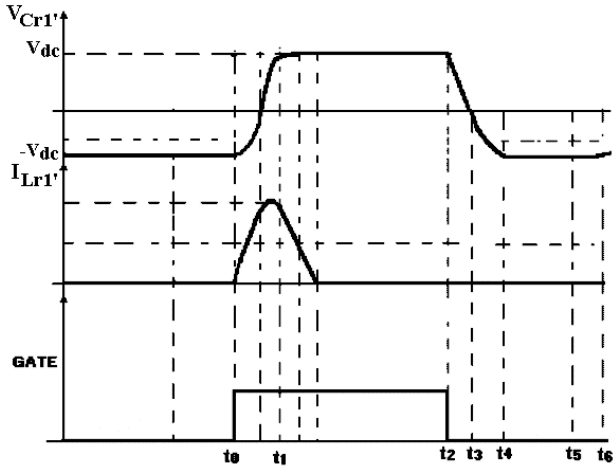

Fig. 8. Theoretical waveforms of the interleaved Forward converter.

V. EXPERIMENTAL RESULTS

An experimental prototype of the switch-mode power supply was built and evaluated using the parameters shown in Table I.

In Fig. 9, power factor correction at nominal load is evidenced, where the displacement power factor is above 0.995.

Fig. 10 demonstrates that the use of the average current mode control is efficient causing the reduction of the input current harmonic content.

Fig. 11 and Fig. 12 present experimental results regarding switches M_1 and M_2, which are both turned on and off under ZCS and ZVS conditions, respectively.

Fig. 13 corresponds to diodes D_4' voltage and current waveforms.

Finally, Fig. 14 shows the efficiency curve of the switch-mode power supply. It can be seen that the efficiency at nominal load is quite high i.e. about 85%.

Table I
Parameters set used in experimental tests

Parameter	Value
AC-DC Stage	
Parameter	**Value**
Input voltage	V_{in}=127/220V
All switches	IRFP460
Switching frequency	f_s=100kHz
Diode bridge $D_1 \ldots D_4$	TB258
Remaining diodes	HFA15TB60
Boost inductors	L_{b1}=L_{b2}=400μH
Flyback inductors	L_{fb1}=L_{fb2}=100μH
Auxiliary capacitor	C_{aux}=270nF
Resonant inductors	L_r=5μH L_{r1}=L_{r2}=2.5μH
Resonant capacitors	C_{r1}= C_{r2}=100nF
Filter capacitor	C_f=1mF
DC-DC Stage	
Parameter	**Value**
DC voltage	V_{dc}=350V
Diodes D_4', D_5', D_9', D_{10}'	MBR245CT
Remaining diodes	HFA15TB60
All switches	IRFP460
Switching frequency	f_s=30kHz
Resonant inductors	L_{r1}'=L_{r2}'=5μH
Resonant capacitors	C_{r1}'=C_{r2}'=270nF
Input filter inductors	L_{f1}'=L_{f3}'=7.5μH
Output filter inductors	L_{f2}'=L_{f4}'=100μH
Primary number of turns	N_{p1}=N_{p2}=20
Secondary number of turns	N_{s1}=N_{s2}=4
Output filter capacitors	C_{f1}'=C_{f2}'=30mF
Output power	P_0=2kW
Output voltage	V_o=12V
Output current	I_o=166A

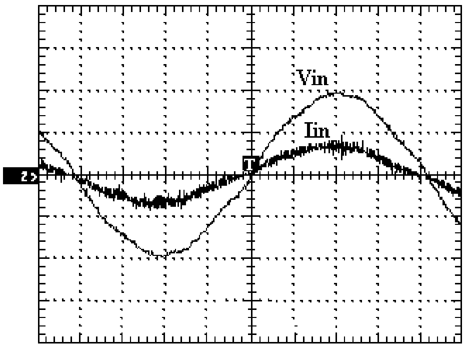

Fig. 9. Input voltage and input current at nominal load
Scales: I_{in} – 100V/div.; V_{in} – 20A/div.; time – 2ms/div.

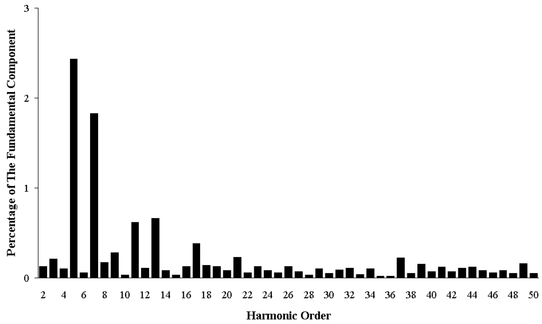

Fig. 10. Harmonic spectrum of the input current (THD_I=3.85%).

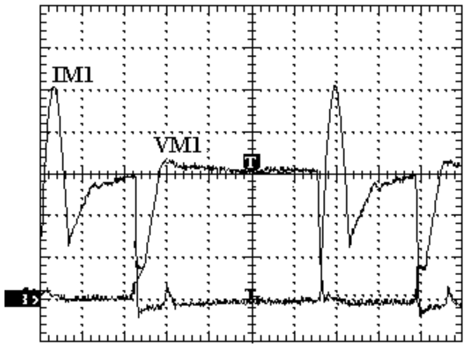

Fig. 11. Drain-to-source voltage and drain current waveforms of switch M_1
Scales: V_{M1} – 100V/div.; I_{M1} – 5A/div.; time – 5μs/div.

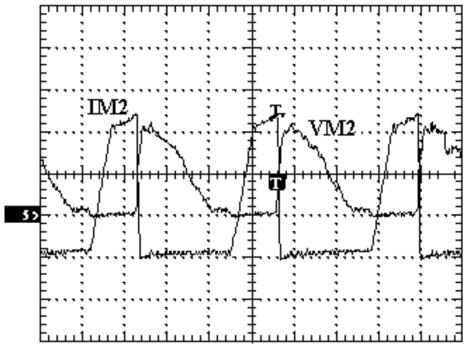

Fig. 12. Drain-to-source voltage and drain current waveforms of switch M_2
Scales: V_{M2} – 100V/div.; I_{M2} – 5A/div.; time – 10μs/div.

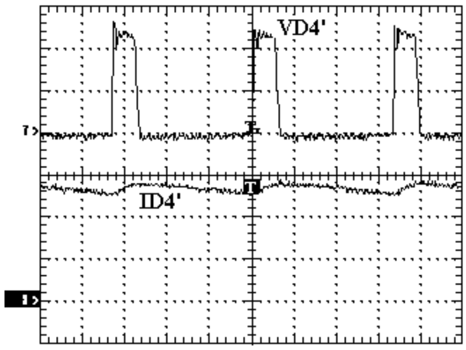

Fig. 13. Voltage and current waveforms of diode D_4'.
Scales: $V_{D4'}$ – 20V/div.; $I_{D4'}$ – 50A/div.; time – 10μs/div.

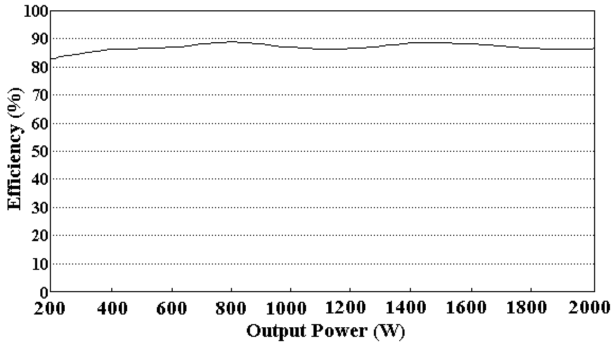

Fig. 14. Efficiency versus output power.

VI. CONCLUSION

This paper has reported the analytical, simulation and experimental developments of a SMPS composed of two stages. The first stage is a soft-switched Boost-Flyback converter, and the second one is an interleaved Forward converter. The use of the average current control technique implies highly efficient power factor correction without commutation losses. The proposed approach also provides an optimum performance at high switching frequencies.

The objective initially proposed was achieved as a switch-mode power supply with unity input factor, high efficiency, low harmonic distortion and also regulated output voltage was analyzed theoretically, designed, evaluated and implemented successfully.

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