THREE-PHASE TO SINGLE-PHASE UPS TOPOLOGIES

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***Abstract* – This paper describes two three-phase to single-phase UPS topologies. The first one is characterized by a double function three-phase input stage. The second one uses a 12-pulse rectifier at the input. Both UPS significantly reduce the input currents make it easier the installation in the customer premises, reducing the EMI as well as losses in the power network where the UPS is connected. As a result, these UPS topologies are strong candidates to feed single-phase critical loads in the range of 7.5kVA to 50 kVA. Design curves are given to select the passive components of the input stage such that the input power factor, unbalance factor and total harmonic distortion (THD) of the input current are kept under desired levels. Simulation and experimental results on a 10 kVA prototype are given to demonstrate the performance of the proposed circuits.**

***Keywords* – UPS, Flux Imbalance, 12-pulse rectifier.**

I. INTRODUCTION

Single-phase UPS are used in a wide range of power, typically form 150VA to 75 kVA [1], to feed single-phase critical loads. It is worth mentioning that as the power increases, in UPS with single-phase input stage, the input neutral current increases as well. One problem associated with this overloading of the neutral wire and the distribution transformer is that it poses a fire hazard, as well as an increase in the EMI. For instance, let us consider single-phase UPSs with single-phase input stages operating from a 127V line to neutral network with nominal power of 5kVA, 10kVA and 25kVA. These UPS will draw neutral currents of 40A, 80A e 200A, respectively, which are considerably high. Single-phase UPS with three-phase input stage is a feasible solution to eliminate the input neutral current and to reduce the input line currents. Three-phase rectifier stage can be divided into controlled and uncontrolled ones. Three-phase PWM rectifiers can operate with high power factor, low THD of the input current and regulated dc bus voltage. However, PWM rectifiers require a larger number of active switches with can lead to a lower reliability and possibly to a higher cost. On the other hand, uncontrolled rectifiers are simpler and rugged, however the dc bus voltage is not regulated and they requires larger passive filter to keep the input current with acceptable performance

In this paper two three-phase to single-phase UPS topologies are proposed. The first one is shown in, Fig. 1 (a). It is comprised of a double function input stage. In the normal mode of operation the input stage operates as a three-phase PWM rectifier ensuring unity power factor while keeping the dc bus voltage at the desired level. During the storage energy mode the AC input is disconnected and the input converter now steps up the battery voltage keeping the dc bus voltage at the desired value. The second topology is characterized by an uncontrolled 12-pulse rectifier input stage. This topology is shown in fig. 1 (b). In this topology with an adequate passive filter design the input currents can have acceptable THD and unbalance factor.

This paper presents the details of the transitions between operation modes for the topology with double function input stage. The impact of the filter design (input inductors and DC bus capacitor) on the THD and unbalance factor of the input currents as well as in the input power factor for the topology of fig. 1 (b) are also given. In addition, the main issues associated with the digital control of the output inverter are addressed and feasible solutions are presented to keep the output dc component at acceptable values.

II. INPUT STAGES OF THE UPS TOPOLOGIES

This section describes the two input stages consider in this paper.

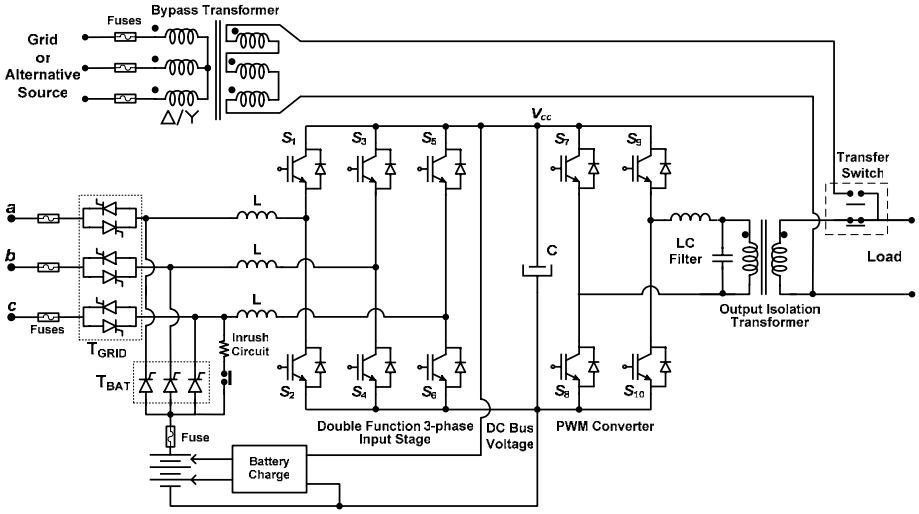
A. Double function three-phase PWM converter

The topology of Fig. 1(a) presents an input stage with double function. The input stage operates in the normal mode when the utility grid is inside of its acceptable limits. In this case, the T_{GRID} interrupters are closed while the T_{BAT} interrupters are open. In the normal mode of operation the input stage operates as a three-phase PWM rectifier ensuring high power factor and draining grid current with appropriate amplitude to keep the dc bus voltage at the desired value. This three-phase rectifier performance is well known in the literature [2]. When the grid voltages are not acceptable, the input stage operates in backup mode. In this case, the T_{GRID} interrupters are open and the T_{BAT} interrupters are closed. In the backup mode each leg of the three-phase rectifier operates as three step-up (boost) converter [3], dividing the battery current equally and keeping the DC bus voltage at desired value.

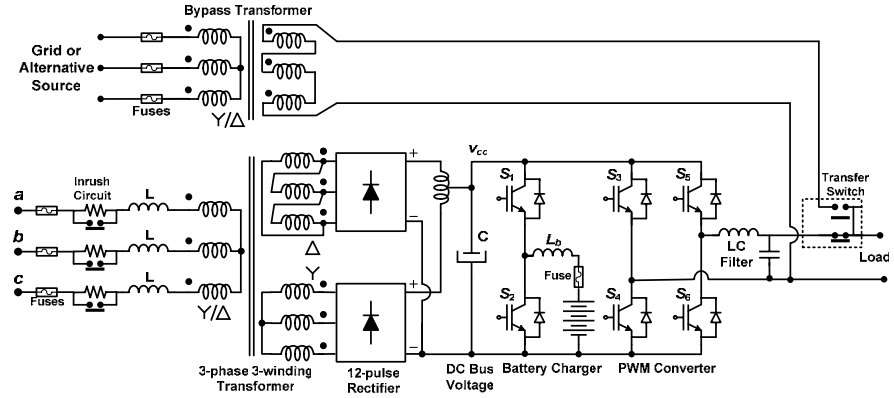
The control structure of the three-phase rectifier has an inner loop to control the input currents and an outer loop to control the dc bus voltage. The current controllers ensure high power factor in the normal mode of operation, while in the backup mode the battery current is shared among three legs of the rectifier. In addition, in the backup mode, three controllers are required to regulate inductors currents once they are linearly independent.

The dc bus voltage controller must have the following characteristics:

(i) Fast response to minimize over and under voltage during transients resulted from: (a) the change between operation modes, and (b) abrupt variations of the load current;



(a) Three-phase to single-phase UPS with double function input stage



(b) Three-phase to single-phase UPS with 12-pulses rectifier

Fig. 1. The two three-phase to single-phase UPS proposed topologies.

(ii) To limit currents in the inductors in acceptable values in both modes of the operation.

The transient behavior of the double function PWM rectifier due to transitions between operating modes as well as due to load variations is shown in Fig. 2.

At *t*=0ms, the circuit starts in backup mode. The DC bus voltage starts at 311 V that is the peak of the input ac line to line voltage. At *t*=2ms the dc bus voltage reaches its nominal value, 467 V. The currents in the inductors are limited in the established value, 40A. As soon as the voltage reaches the expected value, the inductor currents are reduced to the value required by the load.

At *t*=55ms starts the transfer to the normal mode. Initially, the inductors reference currents are brought to zero. The currents in the inductors quickly follow their references.

At *t*=58ms, the normal mode of operation is initiated and within one grid cycle the DC bus voltage returns to its nominal value

At *t*=150ms starts the transfer from the normal mode to the backup mode. The inductors reference currents are brought to zero and in less than 5ms the currents in the inductors also reach zero. Note that the duration of this stage depends on the amplitude of the grid voltage and on the amplitude of the current in the inductors.

At *t*=158.3 ms, the backup mode starts. The inductor currents are limited and the DC bus voltage increases up to its nominal value.

At *t*=200ms, the load is reduced to zero. The transient of the DC bus voltage is well damped and the voltage is stabilized in 508V. Finally, at *t*=250ms, the load is connected again. The minimum value of the voltage is above 446V.

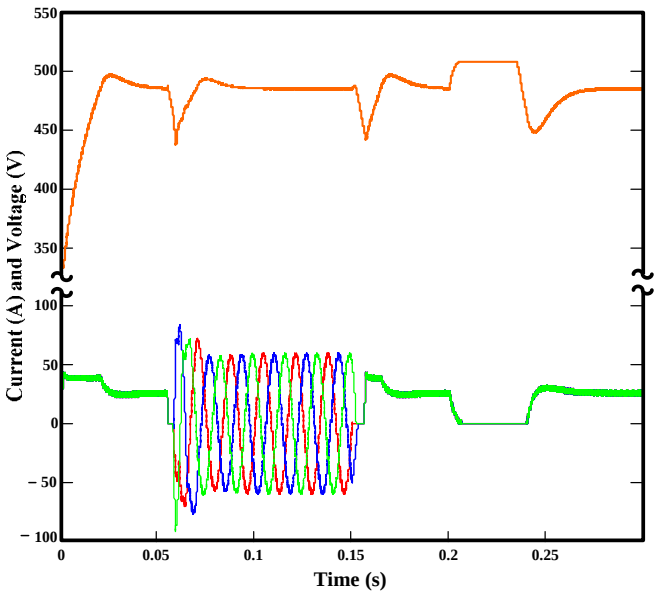


Fig. 2. Currents in the inductors and DC bus voltage, v_{in}=127Vrms, P_o =15kW, v_{bat}=196V, C=6800uF.

B. Uncontrolled 12-pulse diode rectifier

The behavior of the uncontrolled 12-pulse diode rectifier is well known in the literature, where it is usually considered that the DC bus current is constant [4]. However, in the circuit of Fig. 1(b) the current in the DC bus presents an alternate component with the double of the output fundamental frequency (120 Hz) of confineable amplitude. Is as result the DC bus voltage also has a 120Hz ripple. This in turn causes the input current to be unbalance, as shown in Fig. 3.

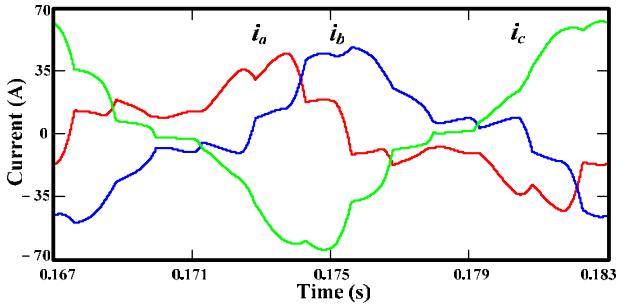


Fig. 3. Input currents of the 12-pulse rectifier feeding a single-phase inverter. L=0.5mH, C=4700uF, P_o=10kVA, v_{ab}=380V

The effect of the 120 Hz voltage component of the dc bus in the input current is minimized with an adequate selection of the input inductors and the DC link capacitors, as shown in Fig. 4.

The abacus given in Fig 5, Fig. 6 and Fig. 7 show the impact of the input inductors and the filter capacitor on the input currents imbalance, power factor and total harmonic distortion (THD), respectively. These performance quantities are defined by the equations, (1), (2) and (3).

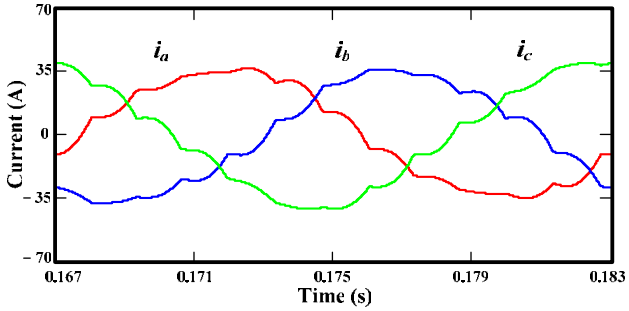


Fig. 4. Input currents of the 12-pulse rectifier feeding a single-phase inverter. L=3mH, C=4700uF, P_o=10kVA, v_{ab}=380V.

***Rectifier input current unbalance factor*:** Current unbalance can be defined as the maximum deviation from the average of the three-phase current, divided by average of the three-phase current, as defined in the *IEEE Std.*1159-1995, that is:

$$Unb\ \% = \left(\frac{\left| I_{frms} - I_{avg} \right|_{\max}}{I_{avg}} \right) 100 \qquad (1)$$

Displacement power factor (DF): The displacement component of power factor; the ratio of the active power of the fundamental wave, in watts, to the apparent power of the fundamental wave, in volt-amperes, according to IEEE Std. 100-1996, that is,

$$DF = \frac{P}{S} \qquad (2)$$

***Harmonics in the input currents of the rectifier*:** for this the *THD* of currents are used. It is defined in the *IEEE Std.* 519-1992, as follow:

$$THD_i\ \% = \left(\sqrt{\sum_{h=2}^{\infty} I_h^2} \Big/ I_1 \right) 100 \qquad (3)$$

It can be observed in the Fig. 5 and Fig. 7 that the increase of the input inductors and the DC bus capacitor reduces the input current unbalance and THD. However, by increasing the inductors the input power factor decreases, as shown in Fig. 6. For example, by selecting an input inductor of 3 mH the input current unbalance is less than 6%, with a power factor of the 0.96 and a THD less than 10%. These results are satisfactory for most applications. Fig.10 shows the experimental setup implemented.

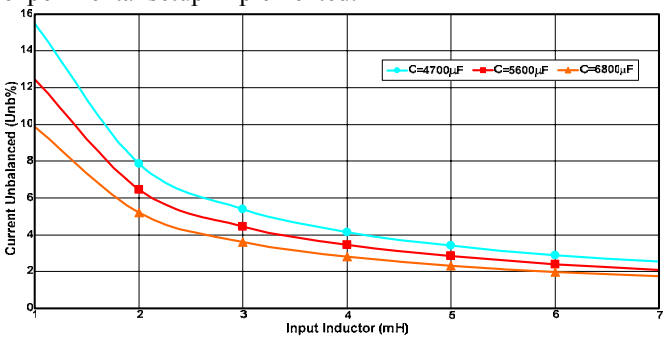


Fig. 5. Current Unbalance versus Input Inductor value. P_o=10kVA, v_{ab}=220V/380V

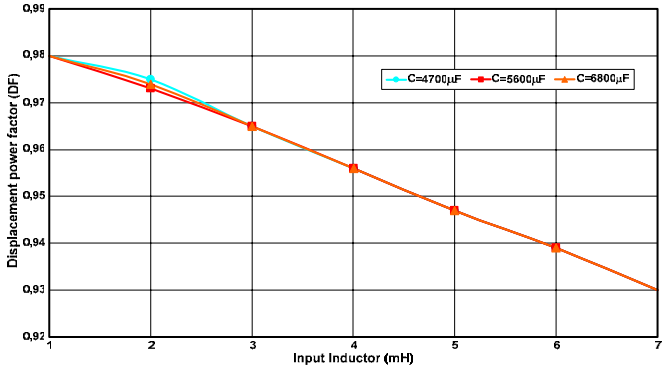


Fig. 6. Displacement Power Factor versus Input Inductor value, P_o=10kVA, v_{ab}=220V/380V.

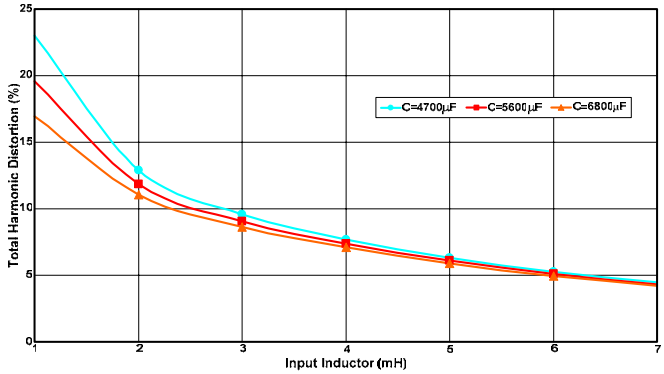
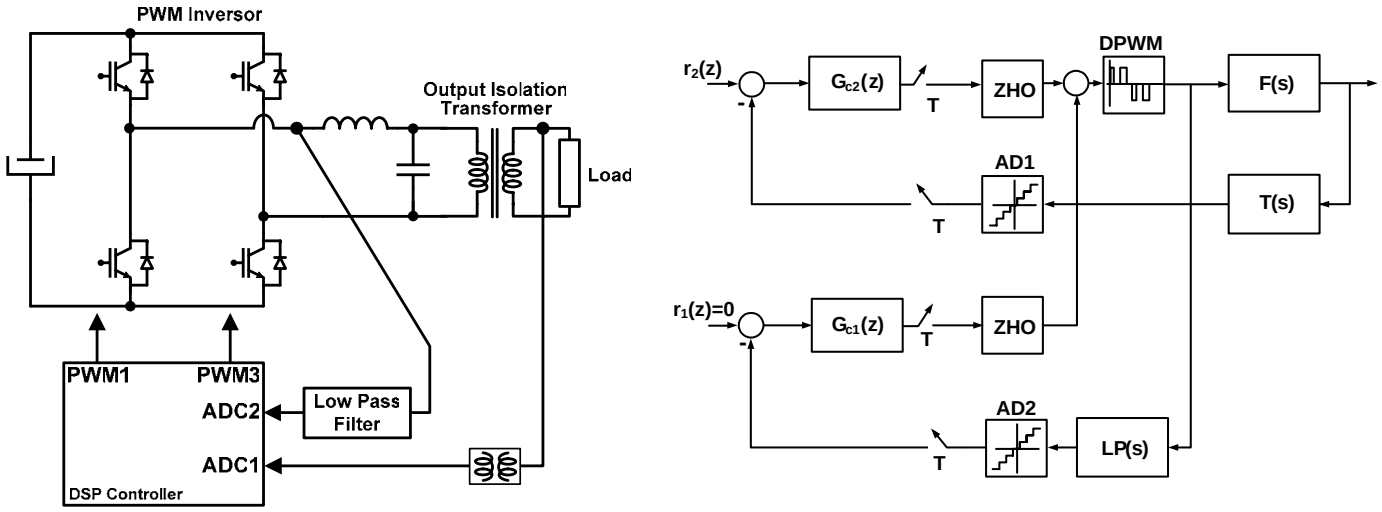


Fig. 7.Total Harmonic Distortion versus Input Inductor value, P_o=10kVA, v_{ab}=220V/380V



(a) (b)

Fig. 8. (a) Two layer Controller. (b) Block Diagram of the two layer controller.

III. OUTPUT STAGE OF THE UPS TOPOLOGIES

The output stage is a full bridge single-phase PWM inverter for both proposed topologies. However, the first one requires an output isolation transformer as shown in fig. 1 (a). In either case the dc component generated by the inverter should be kept as small as possible. The IEC62040-3 standard [5] recommends that the output voltage DC components shall be less than 0.1 % of its rms rated value.

Many factors contribute for the existence of DC component at the inverter output. Among them are: asymmetry of driving signals, different characteristic of switches and the quantization error of both PWM and AD converters [6,7].

This represents a challenge for digitally controlled inverters. Aiming to overcome this problem here it is used a two layer controller as shown in Fig. 8.

The two layers digital controller allows to reduce significantly the dc components present at output of digitally controlled PWM inverters. Fig. 8(b) shows the proposed controller. The first layer consists of an analog low pass filter that reduces significantly the dynamic range of the ADC voltage input followed by a digital controller that keeps the inverters output dc component close to zero. The second layer makes the inverter or transformer output voltage to track a sinusoidal reference with low total harmonic distortion as shown in Fig.9. It is also shown in Fig. 9 the low pass filter output voltage that feeds the ACD2 as well as the transformer magnetizing current. It is seen that the magnetizing current is symmetric indicating that the inverter dc component is small or even zero.

Fig. 11 and Fig. 12 shows the experimental results of the three-phase input currents of the input stage of Fig. 1 (b). Even though these results are not under nominal load, the

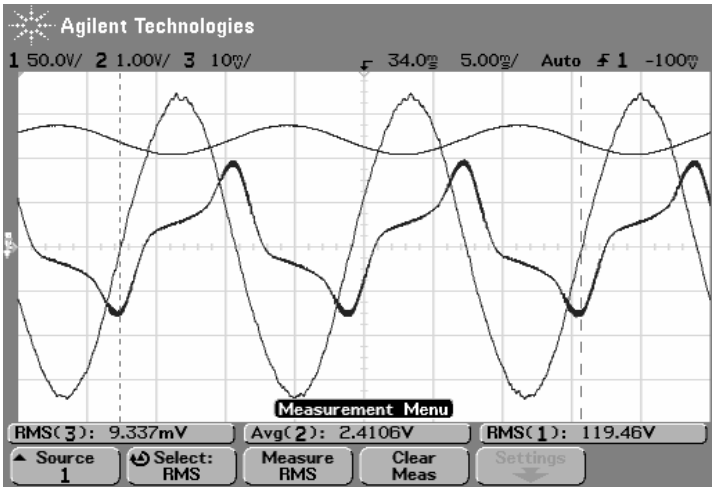


Fig. 9 Experimental Results. Steady-state. Filter output voltage, magnetizing current and low pass filter output voltage.

Fig. 10 10 kVA experimental setup of the input stage of Fig. 1 (b). Three-phase transformer, input inductors, interphase transformer and 12-pulse diode rectifier

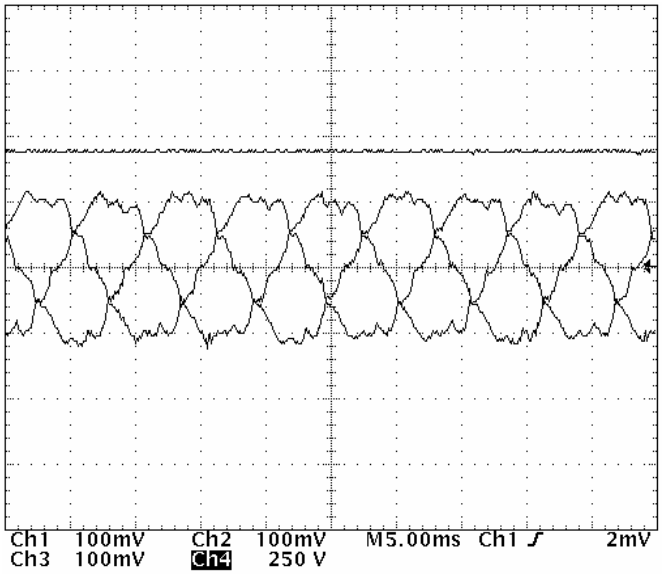


Fig. 11 Experimental Results. Three phase input currents with output inverter. L=3mH, C=4700uF, vab=380V.

Current scale:10A/div.

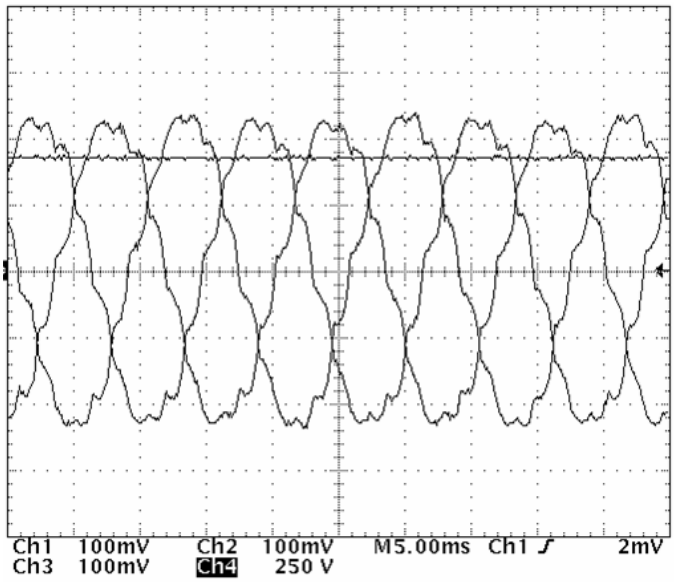


Fig. 12. Experimental Results. Three phase input currents with output inverter. L=3mH, C=4700uF, vab=380V, P_o=10kVA.

Current scale:10A/div..

current unbalance factor is 4%, the THD is 9% and the power factor is 0.97.

IV. CONCLUSIONS

Three-phase to single-phase UPS reduces significantly the input current if compared with single-phase UPS with single-phase input stage and eliminates the problem associated with this overloading of the neutral wire and the distribution transformer that poses fire hazard, as well as the EMI. This paper proposes two three-phase to single-phase UPS topologies. The first one has a double function three-phase input stage. The second one is more attractiveness due to its ruggedness and simplicity. However, it requires a special attention to the passive filter design. The impact filter design on the input current unbalance, THD, and power factor is investigated and guide lines for its selection are given. Finally, experimental results are given in order to validate the analysis carried out.

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