BUCK PWM DC-TO-DC CONVERTER WITH THREE-STATE SWITCHING CELL

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Abstract: **This paper presents a new PWM DC-to-DC non-isolated buck converter. The converter is generated using the three-state commutation cell, comprising two active switches, two diodes and two coupled inductors. The main advantages over the classical buck converter are: lower conduction losses, low input and output current ripples and reduced weight and size, due to the double frequency in the reactive components. Due to these features, the new converter is suitable for low voltage and high current applications. Theoretical analyses with a complete operation description, simulation and experimental results are presented in this paper.**

Keywords **– Buck Converter, PWM, Three-state switching cell, dc-to-dc converter,**

I. INTRODUCTION

Pulse-width modulated (PWM) converters are currently used in a majority of DC-DC conversion applications [1-3]. Widespread applications of DC-DC converters include power supplies for a countless variety of electronic systems, telecommunication energy systems, solar energy applications, DC motor drivers and satellite energy systems. Also, DC-DC converters are often found as basic building blocks for other types of power converters [4-6].

The conventional PWM converters (at hard commutation) present a low power density, even though by using the power mosfets associated with commonly large heatsink, and because the capacitor and inductor filters operating in lower switching frequency. Although the possibility of the mosfet to operate in higher switching frequencies (some MHz) the operation with high power becomes impossible in this frequency range, whereas increasing the switching losses also reduce the efficiency and the switches become tired. In addition, the leakage inductances of the circuit and the transformer and the capacitances of the semiconductor junctions affects in a strongly way the converter performance.

The effects of the leakage inductances are shown in the turn-off (inductive), occurring high voltage stresses. The intrinsic capacitances affect the turn on of the semiconductors, because the energy stored in the junctions are all dissipated in the semiconductors. The written facts before limit the switching frequency to increase in the PWM converters, with hard commutation.

The proposed buck converter, using the three states switching cell [4], is able to process higher power than the conventional topology because it operates the switches with lower switching frequency. The volume of the power reactive elements (inductors and capacitors) is also decreased since the ripple frequency on the output is a double of the switching frequency. Another advantage of this converter is the smaller region to operate in discontinuous mode when compared to the classical buck converter. Generally, the region of discontinuity is undesirable because it presents a non-linearity and becomes difficult to control the converter system.

II. PROPOSED CIRCUIT AND PRINCIPLE OF OPERATION

The proposed buck converter can be seen in Fig 1. The circuit is composed of the input DC voltage source (V1), two switches (S1, S2), two diodes (D1, D2), one transformer formed of two coupled inductors (T), one inductor (L), one output filter (Co), and the load (Ro).

This topology presents two mode of operation. The first mode is for duty-cycle lower than 0.5 ($0 < D < 0{,}5$), i.e., when the command of the switches are non-overlapping. The second mode is for duty cycle greater than 0.5 ($0.5 < D < 1$), i.e., when the command of the switches are overlapping.

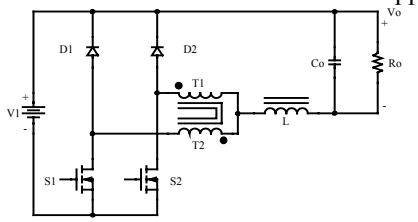

Fig. 1 – Proposed buck converter.

With respect to the inductor current shape, three conduction modes are defined: The continuous conduction mode (CCM), the discontinuous conduction mode (DCM) and the critical conduction mode that is a boundary between CCM and DCM. These conduction modes are considered to find the output characteristic of the converter.

A. Operation For Duty-Cycle Lower Than 0.5 ($0 < D < 0.5$)

1) Continuous Conduction Mode - CCM

Stage 1 ($t_0<t<t_1$): at instant t=t0, switch S1 is turned on and switch S2 is turned off. Since, the turn ratios of both

windings of the center-taped transformer are the same and the current IL is equally divided between these windings. Half of the current IL flows through diode D2 to the load, and half flows through switch S1. In this stage, current IL grows linearly and energy is stored in L. The voltages across the transformer windings T1 and T2 are equal to V1/2. The current paths can be seen in Fig 2a. The differential equation of the current in the inductor L, is expressed by (1).

$$L \cdot \frac{dI_L}{dt} + V_0 - \frac{V_1}{2} = 0 \qquad (1)$$

Stage 2 (t_1<t<t_2): at instant t=t1, switch S1 is turned off, while switch S2 remains blocked and diodes D1 and D2 are forward biased. In this stage, only the energy stored in inductor L is transferred to the load through T1, T2, D1 and D2. The voltage across the transformer windings is zero while their currents are equal with opposite directions. The current paths are shown in Fig. 2b. The differential equation of current in the inductor L, in this stage, is expressed by (2)

$$-L \cdot \frac{dI_L}{dt} + V_o = 0 \qquad (2)$$

Stage 3 (t_2<t<t_3): due to the topological symmetry of the circuit, this stage is similar to the first one (see Fig. 2c).

Stage 4 (t_3<t<T): This stage is identical to the second one (see Fig. 2d).

2) Discontinuous Conduction Mode – DCM

The operation of the DCM is similar to the CCM. The basic difference between DCM and CCM is in the final of the stages 2 and 4. For discontinuous conduction mode, the inductor current becomes zero. The main idealized waveforms can be seen in Fig 4.

3) Voltage Gain - GV

The voltage gain for CCM is calculated during a switching period looking toward the magnetic flux variation in the inductor, as shown in (3) and (4).

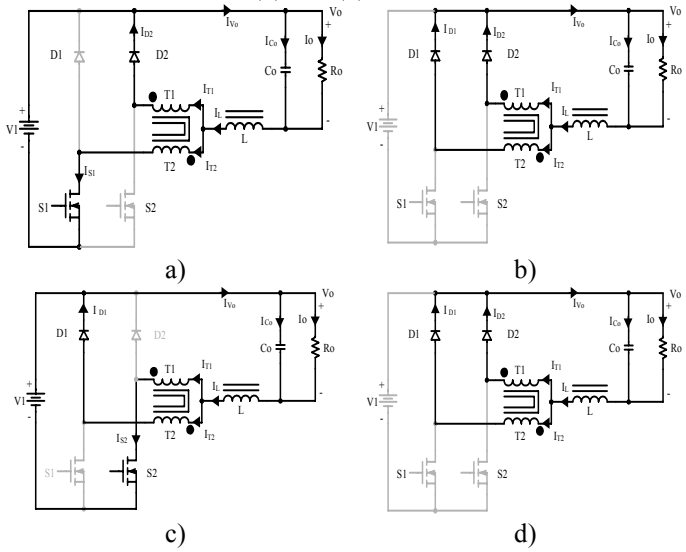

Fig. 2 – Operation modes for CCM.

$$\Delta\phi_{(t1-t0)} = \Delta\phi_{(t2-t1)} \qquad (3)$$

$$G_V = D \qquad (4)$$

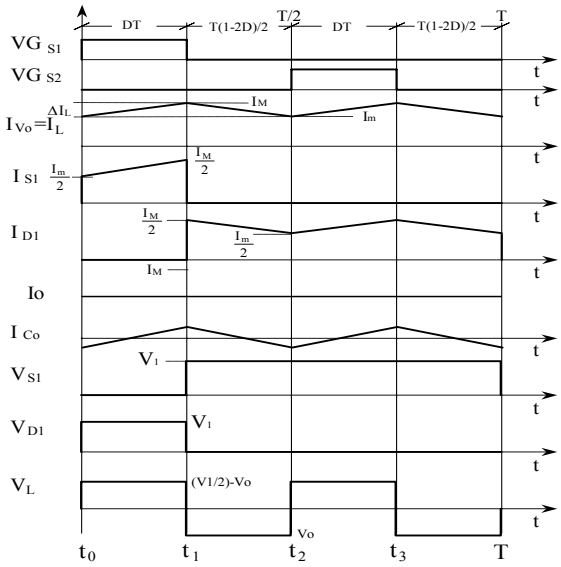

Fig 3 – Main waveforms for CCM.

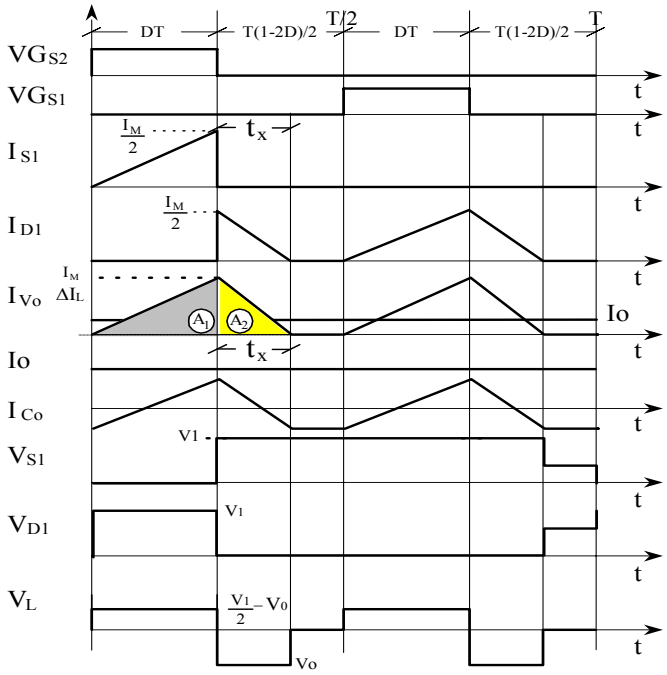

Fig. 4– Main waveforms for DCM.

The voltage gain for DCM (6) is defined from the current average through the diodes D1 and D2 (5).

$$Io = \frac{1}{T} \cdot \int_0^T I_{Vo}(t)dt = \frac{2 \cdot (A1 + A2)}{T} \qquad (5)$$

$$G_v = \frac{D^2}{\gamma + 2 \cdot D^2} \qquad (6)$$

B. Operation for Duty Cycle Greater Than 0.5 (0.5 < D < 1)

1) Continuous Conduction Mode - CCM

Stage 1 (t_0<t<t_1): at instant t=t0, switches S1 and S2 are turned on and diodes D1 and D2 are reverse. In this stage, current IL grows linearly and the energy is stored in L through T1, T2, S1 and S2. The voltages across the

autotransformer windings are zero while their currents are equals, but with opposite directions. The current paths are shown in Fig. 5a. The differential equation of current in the inductor L, is expressed by (7).

$$V_1 - V_0 - L \cdot \frac{dI_L}{dt} = 0 \qquad (7)$$

Stage 2 (t_1<t<t_2): at instant t=t1 switch S2 is turned off, while switch S1 is on. Since, the turn ratios of both windings of the center-taped transformer are the same and the current IL is equally divided between these windings. One half of the inductor current flows through diode D2 to the load, and another half returns to the power supply through switch S1. The voltages across the transformer windings T1 and T2 are one half of the voltage V1. The current paths are shown in Fig 5b. The differential equation of the current in the inductor L is expressed by (8).

$$\frac{V_1}{2} - V_o - L \cdot \frac{dI_L}{dt} = 0 \qquad (8)$$

Stage 3 (t_2<t<t_3): this stage is identical to the first one (Fig. 5c).

Stage 4 (t_3<t<T): due to topological symmetry of the circuit, this stage is similar to the second one (Fig. 5d).

2) Discontinuous Conduction Mode – DCM

The operation of the discontinuous conduction mode is similar to the operation of the continuous conduction mode. The main idealized waveforms can be seen in Fig 7.

3) Voltage Gain - GV

The voltage gain for CCM is calculated during a switching period looking toward the magnetic flux variation in the inductor, as shown in (3) and (4).

The voltage gain for DCM (9) is determined from the current average through the diodes D1 and D2 (5).

$$G_v = \frac{\gamma + 4 \cdot D^2 - 4 \cdot D + 1}{2 \cdot \gamma + 4 \cdot D^2 - 4 \cdot D + 1} \qquad (9)$$

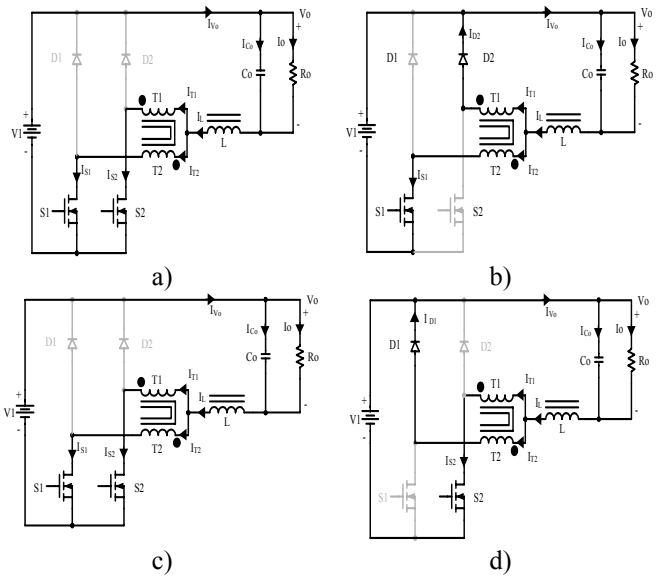

Fig. 5 – Operation modes for CCM**.**

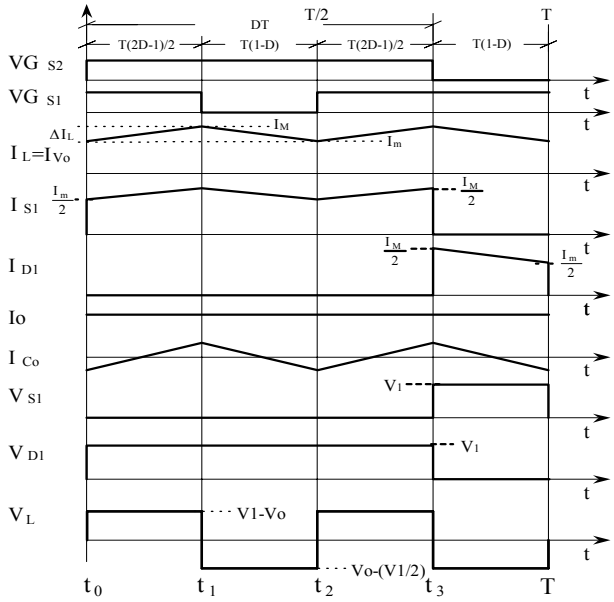

Fig 6 – Main waveforms for CCM.

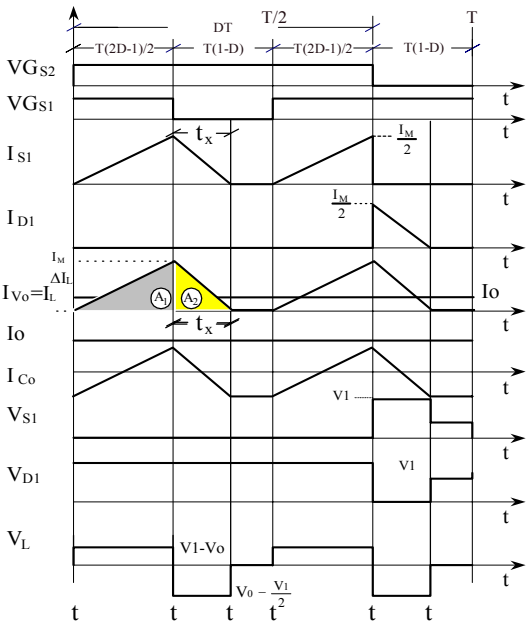

Fig.7 – Main waveforms for DCM.

C. Static Gain and Output Characteristic

For the proposed converter, the maximum value of the normalized load (γ) for critical conduction mode (boundary between the CCM and DCM) is only γ=0.125. In this load condition, the duty-cycles are 0.25 and 0.75 for D lower than 0.5 and D greater than 0.5, respectively, as shown in Fig. 8. To the classic buck converter, the normalized load is the double (γ=0.25) when the duty-cycle is 0.5. This is an advantage of the proposed converter. In the other words, it can be said that the calculated inductance of the proposed converter is reduced to one half of the inductance of the classic buck.

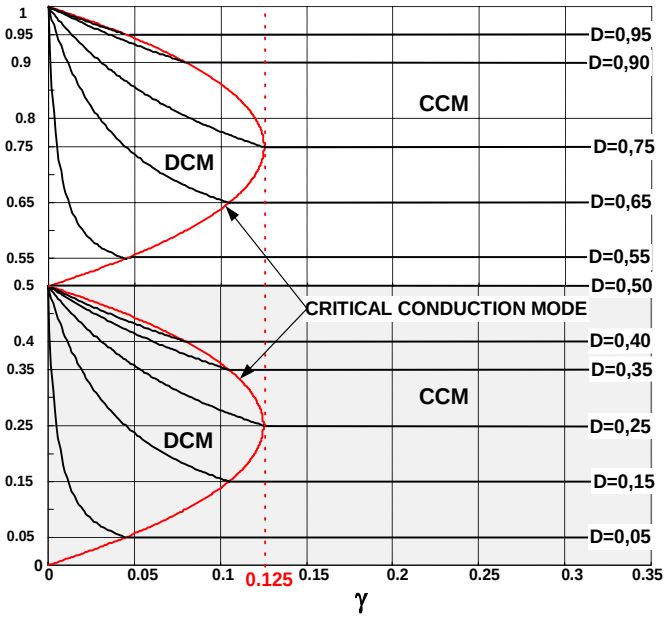

Fig. 8 – Output Characteristic (voltage gain x normalized load).

III. SIMULATION RESULTS

In this section, simulation results obtained to the proposed buck converter are presented for duty-cycle lower than 0.5 and greater than 0.5.

The main parameters used for D<0.5 are shown bellow and the simulation results can be seen in fig 9.

Po=2kW output power
V1=220V input voltage
Vo=60V output voltage
fs=25kHz switching frequency
Co=50µF output filter capacitor
L=10µH storage inductor

The main parameters used in the second simulation (D>0.5) that are different from the first simulation, are shown bellow and the simulation results can be seen in fig 10.

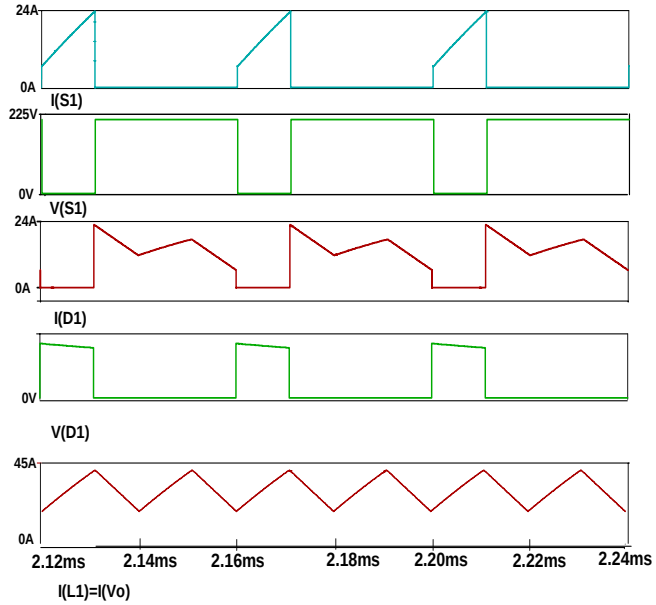

Fig.9 - Simulation results for duty cycle lower than 0.5.

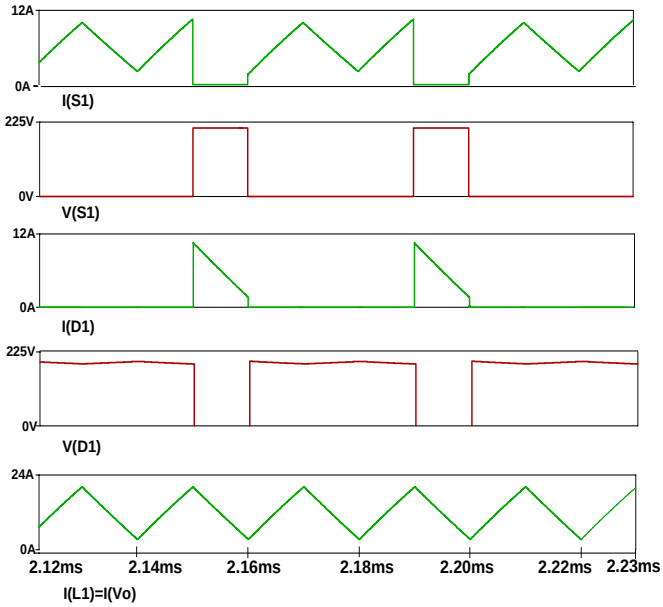

Fig.10 - Simulation results for duty cycle greater than 0.5.

L=32µH storage inductor
Co=50µF filtering capacitor

It can be observed in Fig. 9 and Fig.10, witch the current through the switch S1 and the current through the diode D1, are no more than one half of the current through the inductor (load). The same happen to the switch S2 and the diode D2.

IV. DESIGN PROCEDURE

In this section, the design procedure of the proposed buck converter are presented for duty-cycle lower than 0.5. The design is accomplished in base the proposed converter of Fig. 1.

A. Specifications

Input date:
Po = 1kW output power;
V1 = 200V input voltage;
Vo = 60V output voltage.
For the design the following parameters are adopted:
D = 0.3 duty cycle
fs = 30kHz switching frequency;
ΔIL = 3,33A ripple current (20% of the I1p);
ΔVo = 0,6V output ripple voltage (1% of the Vo).

B. Equations to calculate the passive components

Inductance L:

$$L = \frac{(1 - 2 \cdot D) \cdot Vo \cdot ta}{2 \cdot \Delta IL} = 120uH \qquad (10)$$

Capacitance Co:

$$Co = \frac{\Delta IL}{4 \cdot \pi \cdot fs \cdot \Delta VCo} = 3.684uF \qquad (11)$$

1) Inductor

$$IM = Io + [\frac{V_1 \cdot D \cdot T \cdot (1 - 2 \cdot D)}{4 \cdot L}] \qquad (12)$$

$$\mathrm{Im} = Io - [\frac{V_1 \cdot D \cdot T \cdot (1-2 \cdot D)}{4 \cdot L}] \quad (13)$$

Where:

IM – maximum current in the inductor L

Im - minimum current in the inductor L

$$iL_1(t) = \mathrm{Im} + [\frac{V_1 \cdot (1-2 \cdot D) \cdot t}{2 \cdot L}] \rightarrow 0 < t < t_1 \quad (14)$$

$$iL_2(t) = IM - [\frac{V_1 \cdot D \cdot t}{L}] \rightarrow t_1 < t < t_2 \quad (15)$$

$$iL_1(t) = \mathrm{Im} + [\frac{V_1 \cdot (1-2 \cdot D) \cdot t}{2 \cdot L}] \rightarrow t_2 < t < t_3 \quad (16)$$

$$iL_2(t) = IM - [\frac{V_1 \cdot D \cdot t}{L}] \rightarrow t_3 < t < t_4 \quad (17)$$

$$Irms_L = \sqrt{\frac{2}{T} \cdot \int_0^{D.T} (iL_1(t))^2 dt + \frac{2}{T} \cdot \int_0^{(1-2.D)\frac{T}{2}} (iL_2(t))^2 dt} = 17.19(A) \quad (18)$$

$$IpL = IM = 18.33(A) \quad (19)$$

Where:

IrmsL – rms current in the inductor L

IpL - peak current in the inductor L

2) Transformer

$$V_{T1} = \frac{V_1}{2} = 100(v) \quad (20)$$

$$Irms_{T1} = \sqrt{\frac{2}{T} \cdot \int_0^{D.T} (\frac{iL_1(t)}{2})^2 dt + \frac{2}{T} \cdot \int_0^{(1-2.D)\frac{T}{2}} (\frac{iL_2(t)}{2})^2 dt} = 8.35(A) \quad (21)$$

$$Ip_{T1} = \frac{IM}{2} = 9.18(A) \quad (22)$$

Where:

VT1 – Voltage on the transformer windings

IrmsT1 – rms current in the transformer windings

IpT1 - Peak current in the transformer windings

3) Switches S1 and S2

$$Vs = V_1 = 200(V) \quad (23)$$

$$Irms_s = \sqrt{\frac{1}{T} \int_0^{D.T} (iL1(t))^2 dt} = 4.57(A) \quad (24)$$

$$Ips = \frac{IM}{2} = 9.18(A) \quad (25)$$

Where:

V_S – Voltage on the switch

$Irms_S$ – rms current in the switch

Ip_S - Peak current in the switch

4) Diodes D1 and D2

$$V_D = V_1 = 200(v) \quad (26)$$

$$Irms_D = \sqrt{\frac{1}{T} \cdot \int_0^{D.T} (\frac{iL_1(t)}{2})^2 dt + \frac{2}{T} \cdot \int_0^{(1-2.D)\frac{T}{2}} (\frac{iL_2(t)}{2})^2 dt} = 6.98(A) \quad (27)$$

$$Ip_D = \frac{IM}{2} = 9.18(A) \quad (28)$$

Where:

V_D – Voltage on the diode

$Irms_D$ – rms current in the diode

Ip_D - Peak current in the diode

With these calculated values, the voltage and current limits on the components can be specified.

V. EXPERIMENTAL RESULTS

In this section, experimental results obtained with the proposed buck converter circuit are presented. Intending to verify the principle of operation, a laboratory prototype was implemented, as shown in Fig. 11. The preliminary results were obtained for reduced input voltage (V1=100V) because the snubber circuit was not implemented yet. The duty cycle was 0.3 to rate 30V and 10A on the output. Fig. 12 to 16 show the principal results obtained with the prototype. Fig. 13 shows the current ripple in the inductor is two times the switching frequency.

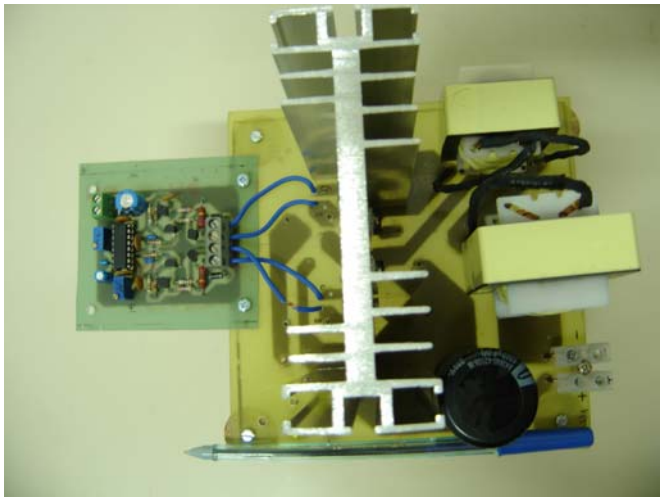

Fig. 11 – Photograph of the prototype.

VI. CONCLUSION

From the study presented in this paper, we can draw the conclusions as follows:

- The new DC-to-DC converter performs as predicted theoretically;
- The converter shows suitable for commercial and industrial applications, when low voltage and high current DC-to-DC conversion is required;
- It is enable to transfer more power quantity because it submits the switches to a lower frequency. In addition, the volume of the reactive elements (inductors and capacitors) is lower because they operate with higher ripple frequency (the double frequency of the switches);

This proposed converter processes through the active switches only part of the load energy. Furthermore, it has an important feature that another part of the energy from the power supply is delivered to the load, just through passive components (by the diodes and the transformer).

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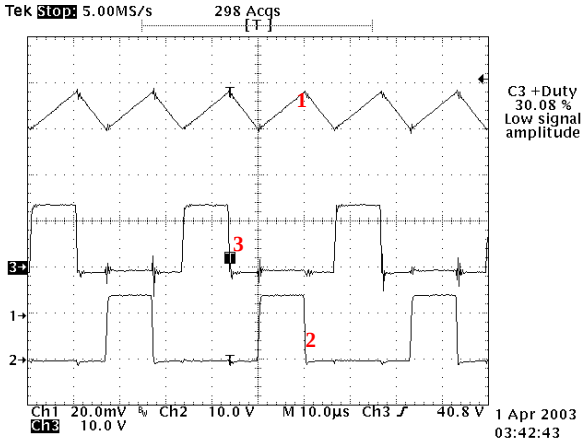

Fig. 12. Curves 2 and 3 are the gate voltages of the switches S1 and S2. Curve 1 is the current in the inductor.
Scale: 10V/div., 2A/div. and 10µs/div.

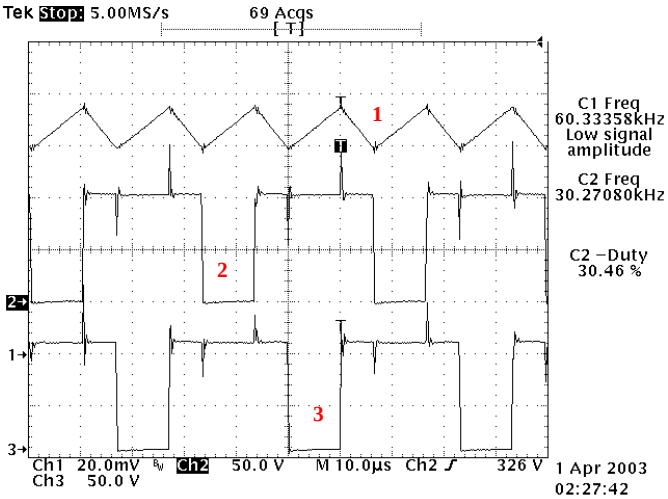

Fig. 13. Curves 2 and 3 are the voltages on the switches S1 and S2. Curve 1 is the current in the inductor.
Scale: 50V/div., 2A/div. and 10µs/div.

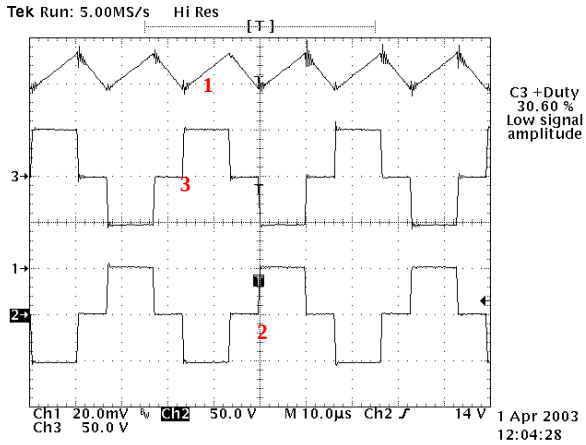

Fig. 14. Curves 2 and 3 are the voltages on the transformer windings. Curve 1 is the current in the inductor.
Scale: 50V/div., 2A/div. and 10µs/div.

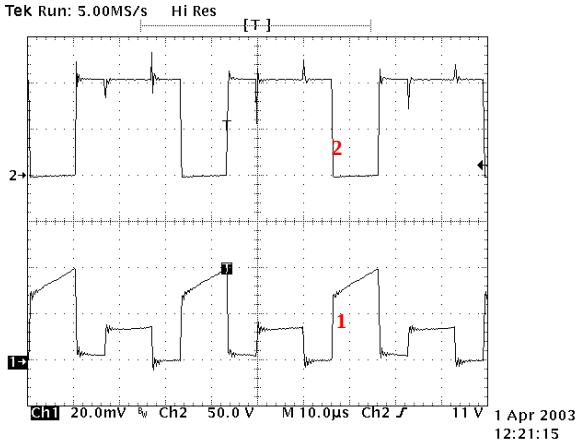

Fig. 15. Voltage (curve 1) and current (curve 2) in the switch S1.
Scale: 50V/div., 2A/div. and 10µs/div.

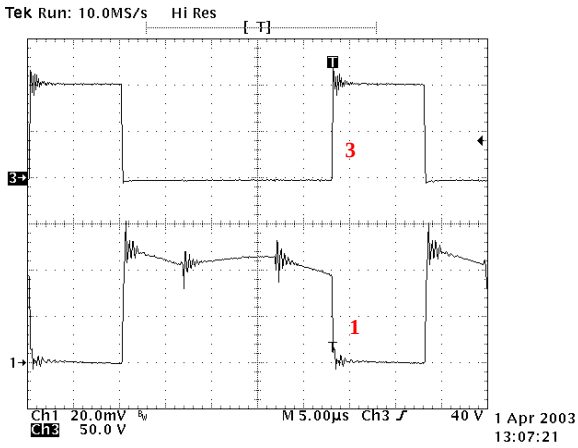

Fig. 16. Voltage (curve 1) and current (curve 2) in the diode D1.
Scale: 50V/div., 2A/div. and 5µs/div.

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