COMPARISON AMONG THREE TOPOLOGIES OF MULTILEVEL INVERTERS

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Abstract **- This paper compares three distinct topologies of multilevel inverters to drive an induction motor of 500 kVA/4.16 kV. The multilevel inverters analyzed are: a neutral point clamped, a symmetrical cascaded multilevel inverter and a hybrid asymmetrical cascaded multilevel inverter. The performance indexes used in the comparison are semiconductors power losses distribution, total harmonic distortion and first order distortion factor. The comparisons are developed in three ways; in the first comparison the switching frequency is found. It guarantees that the converters present the same efficiency. In the second comparison the objective is finding the maximum switching frequency that it is gotten in each topology. And in the third comparison, the efficiency which both systems present the same output filter is found.**

Keywords **- Multilevel inverter, adjustable speed drives, induction motor.**

I. INTRODUCTION

The reliability of medium voltage drive systems has increased significantly in the last years. It has occurred due to the improvements in the semiconductors devices and refrigeration systems, mitigation of the harmonic distortion, improvements in the design of the power stage (rectifier/inverter) and control systems. Therefore, Adjustable Speed Drives (ASDs) present a better performance and the cost to adopt them has became more attractive, as evidenced by the increase in the use of these systems, [1].

The ASDs have been used in several industry sectors as petrochemicals, mining, water/waste, pulp & paper, cement, chemicals, power generation, metals and marine, in equipments as pumps, fans, compressors, blowers, extruders, conveyors, crushers & mills, rolling mills, mixers, propulsion, test beds, synchronous condensers, gas turbine starts, hoists and winders, [2].

In this context, it has been verified an increasing interest by the cascaded multilevel inverter. This interest occurs because this inverter presents some advantages, such as: it has cells operating in low-frequency, uses low-voltage switches, uses smallest number of components to generate the same numbers of levels in the output voltage and presents modular characteristic. It has as main disadvantage the necessity of using isolated DC sources, [3]. This inverter was presented for the first time by [4]. This hybrid topology applied to the drive of electric machines was shown by [5]. A generalized design methodology to define the main parameters of a hybrid multilevel inverter was presented in [6].

Cascaded multilevel inverter can be classified in two groups. The first one refers to the amplitude of isolated DC sources destined to supply each H-bridge cell. If the amplitude of all sources is equal, then the inverter is called symmetrical, otherwise, if at least one of the sources present different amplitude, then it will be called asymmetrical. The second classification label the multilevel inverter whether hybrid or not. If the converter is implemented with different technologies of semiconductor devices (IGBTs, SCRs, GTOs, IGCTs), if it presents a hybrid modulation strategy and/or it is compound by distinct topologies connected in series or parallel, then it is classified as hybrid, otherwise, not.

Some comparative studies regarding multilevel inverter topologies had already been considered in literature, as the comparison of the power losses between diode-clamped multilevel inverters of three and four levels presented by [7], and involving an inverter with H-bridge cells and a two-level inverter shown in [8]. In addition, there are comparisons among diode-clamped, flying-capacitor and cascaded multilevel inverters [9], and between hybrid multilevel inverters with the same number of cells connected in series [10]. However, literature still lacks a comparison among cascade multilevel inverters with the same number of levels in the output voltage and the neutral point clamped, which is the most used multilevel inverter.

In this paper a comparison among a neutral point clamped, an asymmetrical and a symmetrical multilevel inverter will be developed. This paper will be divided as follows: Section II presents the drive systems. Section III shows the performance indexes that will be used in the comparison. Section IV displays the comparison methodology and its results. Section V presents some experimental results and Section VI presents the final conclusions.

II. DRIVE SYSTEMS

The drive systems shown hereinafter are designed to supply an induction motor with line-voltage of 4160V, phase-current 68.4A, apparent power of 500kVA, frequency of 60 Hz and power factor of 0.85.

A. Nine-level hybrid asymmetrical inverter

One phase of a nine-level hybrid asymmetrical inverter can be seen in Fig. 1. This configuration is known as 1-1-2 and receives this name because the amplitude of the

normalized voltage that supplies the cell 3 is twice the amplitude of cells 1 and 2.

The DC voltage sources of cells 1 and 2 are equal to 850 V, while the DC voltage source of cell 3 is 1700V. The devices used to implement the inverter are the GTOs/diodes DG408BP45/DSF8045SK ([11] and [12]) for the highest power cell (cell 3) and for the lower power cells (cells 1 and 2) the module of IGBTs/diodes BSM200GB170DLC, [13].

The hybrid multilevel modulation technique is used to guarantee that some cells operate in low-frequency and other in high-frequency. This strategy associates the stepped voltage waveform synthesis in higher power cells with high-frequency PWM modulation for the lowest power. The diagram that describes this modulation strategy can be verified in Fig. 2, where V_3, V_2 and V_1 are the normalized amplitude of DC sources that supply each cell, Ψ_3 and Ψ_2 represents the comparison levels of cell 3 and 2, $r_3(t)$, $r_2(t)$ and $r_1(t)$, are the reference signals, $v_3(t)$, $v_2(t)$ and $v_1(t)$ are the output voltage of each cell and $v_{out}(t)$ is the output phase-to-neutral voltage.

The comparison levels employed in the comparison were obtained in [14], to guarantee minimum power losses for the converter. When the amplitude modulation index is equal to 1, for which the comparison analysis presented in the paper was developed, the comparison levels are $\Psi_3 = 0$ and $\Psi_2 = 1$.

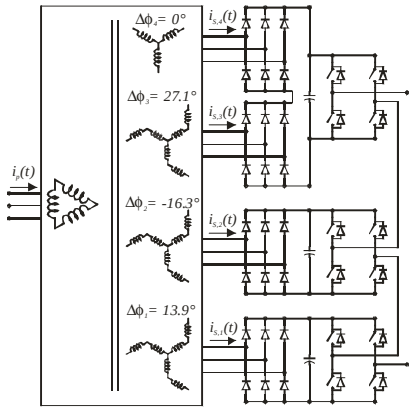

Fig. 1. Nine-level hybrid asymmetrical system

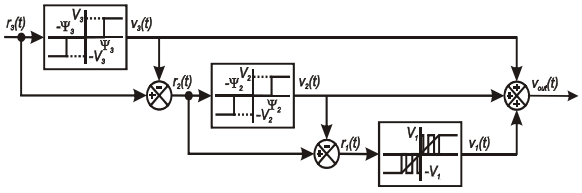

Fig. 2. Hybrid multilevel modulation technique

B. Nine-level symmetrical inverter

One phase of a nine-level symmetrical inverter can be seen in Fig. 3. This inverter is known as 1-1-1-1, because it presents four H-bridge series-connected cells with the same DC input voltage source.

To generate a phase-voltage with peak value of 3400V, the DC sources must be equal to 850V. The device used to implement the H-bridge cells is the module of IGBTs/diodes BSM200GB170DLC, [13].

The phase-shift PWM modulation technique was used [15], [16]. To generate a phase-voltage with *m* levels, this strategy uses (*m–1*) carriers with the same amplitude, but with *360/(m–1)* degrees phase-shift among themselves. For a *m*-level converter, the most significant harmonics will be located in lateral bands around $(m-1)f_p$, where f_p is the carrier frequency. For even values of the modulation frequency index (m_f), the waveforms synthesized present quarter-wave symmetry, resulting only even harmonics [16]. Therefore, for a nine-level inverter, this strategy uses eight carriers with 45º phase-shift among themselves, as can be seen in Fig. 4.

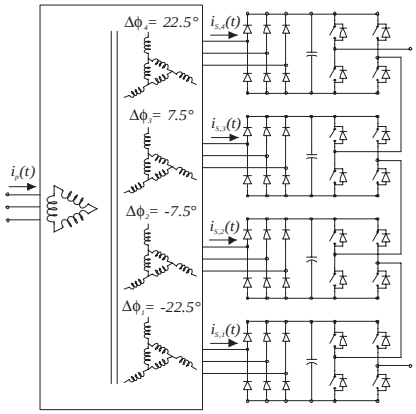

Fig. 3. Nine-level symmetrical system

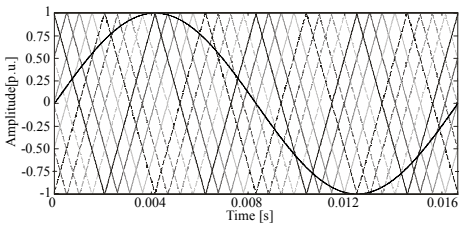

Fig. 4. Phase-shift modulation technique

C. Neutral point clamped system

One phase of a neutral point clamped inverter can be seen in Fig. 5. The other phases of this inverter use the same DC link.

The maximum voltage in the semiconductors is 3400V. Therefore, the devices used in this topology are the modules of IGBTs/diodes FZ200R65KF1, [17].

The phase disposition PWM modulation technique was used. The reference signal and the two carriers can be verified in Fig. 6. In this strategy, the most significant harmonic appear around the carrier frequency. However, this component does not appear in line voltage. This technique guarantees only odd harmonics for odd values of m_f [16].

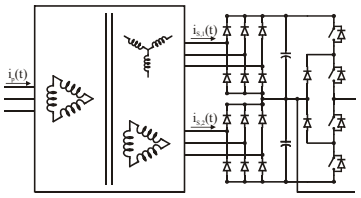

Fig. 5. Neutral point clamped system

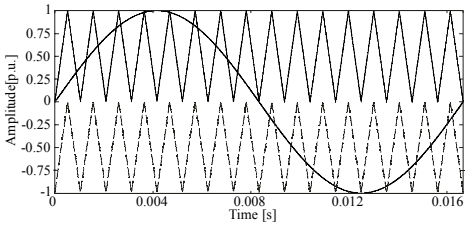

Fig. 6. Phase disposition modulation technique

III. PERFORMANCE INDEXES

The performance indexes used in the comparative analysis are total harmonic distortion (THD), first order distortion factor (DF1) of the output voltages and semiconductors power losses.

A. Total harmonic distortion

The total harmonic distortion of a signal is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency (1).

$$THD\% = \frac{100}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} \tag{1}$$

B. First order distortion factor (DF1)

In induction motors applications, the leakage inductances provide first order attenuation [15]. Therefore, the DF1 represents the first order attenuation of the harmonics in the output voltage of the inverter. The DF1 is given by (2):

$$DF1\% = \frac{100}{V_1}\sqrt{\sum_{h=2}^{\infty} \frac{V_h^2}{h}} \tag{2}$$

C. Semiconductors power losses

Although there is a significant development in the semiconductors technology, there is not one power device that simultaneously have: large breakdown voltages, low on-state voltages and resistances, fast turn-on and turn-off and large power dissipation capability. For all devices, there is a trade-off between breakdown voltages and on-state losses. In bipolar devices, there is also a trade-off between on-state losses and switching speeds. These trade-offs specify which type of device is more adequate for a specific application.

Semiconductor devices employed in each configuration were defined from their characteristics and they were presented in section II.

The semiconductors power losses can be estimated from the curves ($v_{sat}(\theta)$ x $I_{load}(\theta)$) and ($E(\theta)$ x $I_{load}(\theta)$), presented in the datasheet of each device, where: v_{sat} is the on-state saturation voltage ($v_{ce}(\theta)$ for the IGBT, $v_F(\theta)$ for the diode and $v_{TM}(\theta)$ for the GTO); $E(\theta)$ represent the energy losses in one commutation ($E_{on}(\theta)$ if it is a turn-on commutation, $E_{off}(\theta)$ if it is a turn-off commutation and $E_{rec}(\theta)$ if it is a diode reverse recovery process).

These curves are used in a Matlab script developed to determinate the power losses. This software uses the mathematical modes that better represent the functions $v_{ce}(i_{load}(\theta))$, $v_F(i_{load}(\theta))$, $E_{on}(i_{load}(\theta))$, $E_{off}(i_{load}(\theta))$ and $E_{rec}(i_{load}(\theta))$ for each semiconductor device. The mathematical models are found using the points extracted of datasheets of each semiconductor and using the Matlab tool identified as *cftool* (curve fitting tool).

The mathematical models obtained for module BSM200GB170DLC are given by (3)-(7), for the GTO DG408BP45 and diode DSF8045SK are given by (8)-(11) and for the module FZ200R65KF1 are given by (12)-(16).

$$v_{ce_{BSM}} = 0.27.I_{load}(\theta)^{0.47} + 0.025 \tag{3}$$

$$v_{F_{BSM}} = 0.29.I_{load}(\theta)^{0.38} - 0.057 \tag{4}$$

$$E_{on_{BSM}} = \left(98.93.e^{(0.004.I_{load}(\theta))} - 95.77.e^{(0.002.I_{load}(\theta))}\right).10^{-3} \tag{5}$$

$$E_{off_{BSM}} = \left(63.57.e^{(0.002.I_{load}(\theta))} - 63.78.e^{(-0.003.I_{load}(\theta))}\right).10^{-3} \tag{6}$$

$$E_{rec_{BSM}} = \left(55.87.e^{(0.0002.I_{load}(\theta))} - 63.31.e^{(-0.011.I_{load}(\theta))}\right).10^{-3} \tag{7}$$

$$v_{TM_{DG}} = -0.26.I_{load}(\theta)^2 + 2.32.I_{load}(\theta) + 1.47 \tag{8}$$

$$v_{F_{DSF}} = -2.79.10^{-6}.I_{load}(\theta)^2 + 0.005.I_{load}(\theta) + 1.19 \tag{9}$$

$$E_{on_{DG}} = \left(4.10^{-5}.I_{load}(\theta)^2 + 1.43.I_{load}(\theta) + 220\right).10^{-3} \tag{10}$$

$$E_{off_{DG}} = \left(-8.10^{-4}.I_{load}(\theta)^2 + 4.I_{load}(\theta) - 189.1\right).10^{-3} \tag{11}$$

$$v_{ce_{FZ}} = 3.78.e^{(0.002.I_{load}(\theta))} - 2.70 + c.e^{(-0.015.I_{load}(\theta))} \tag{12}$$

$$v_{F_{FZ}} = 2.9.e^{(0.002.I_{load}(\theta))} - 2.35 + c.e^{(-0.015.I_{load}(\theta))} \tag{13}$$

$$E_{on_{FZ}} = \left(1058.e^{(0.004.I_{load}(\theta))} - 1011.e^{(-0.004.I_{load}(\theta))}\right).10^{-3} \tag{14}$$

$$E_{off_{FZ}} = \left(1051.e^{(0.002.I_{load}(\theta))} - 1097.e^{(-0.005.I_{load}(\theta))}\right).10^{-3} \tag{15}$$

$$E_{rec_{FZ}} = \left(211.e^{(0.004.I_{load}(\theta))}\right).10^{-3} \tag{16}$$

Based on the models for each device, the conduction and switching power losses are calculated for each semiconductor of the output inverter. The sum of all results is computed to obtain the total power losses

The conduction power losses are those that occur while the semiconductor device is conducting current. The conduction power losses are given by (17) for the main switch (IGBT or GTO) or given by (18) for the diode.

$$P_{cond_{SW}} = \frac{1}{2.\pi}\int_0^{2.\pi} v_{sat}(\theta).i_{load}(\theta).v_{cmd_{SWX}}(\theta)\,d\theta \tag{17}$$

$$P_{cond_D} = \frac{1}{2.\pi}\int_0^{2.\pi} v_F(\theta).i_{load}(\theta).v_{cmd_{SWX}}(\theta)\,d\theta \tag{18}$$

$$i_{load}(\theta) = m_a.\mathrm{I}_{m\acute{a}x}.sen(\theta - \phi) \tag{19}$$

Where $i_{load}(\theta)$ is the load current (19), m_a is the modulation amplitude index, ϕ is the load displacement angle and $v_{cmd_{SW_X}}(\theta)$ is the command signal of the switch SW*x*.

The total conduction losses are obtained by:

$$P_{cond_{TOTAL}} = P_{cond_{SW}} + P_{cond_D} \tag{20}$$

The switching losses are obtained by identifying every turn-on and turn-off instants during one reference period. Therefore, the turn-on, turn-off and reverse recovery losses are given by (21), (22) and (23), respectively.

$$P_{on} = \frac{1}{T}\sum E_{on}\left(i_{load}(\theta)\right) \tag{21}$$

$$P_{off} = \frac{1}{T}\sum E_{off}\left(i_{load}(\theta)\right) \tag{22}$$

$$P_{rec} = \frac{1}{T}\sum E_{rec}\left(i_{load}(\theta)\right) \tag{23}$$

The total switching losses are the sum of turn-on, turn-off and reverse recovery losses of all semiconductor devices:

$$P_{comut_{TOTAL}} = P_{on} + P_{off} + P_{rec} \quad (24)$$

The total losses are the sum of all conduction and switching power losses:

$$P_{TOTAL} = P_{comut_{TOTAL}} + P_{comut_{TOTAL}} \quad (25)$$

IV. COMPARISON METHODOLOGY

This section presents three comparisons for the drive systems described in Section II.

A. Inverters with same efficiency

The first comparison is developed to obtain the carrier frequency in which the three systems present an efficiency of 99%, which is a typical efficiency for medium voltage converters [9].

The performance indexes are presented in Table I and the power losses distribution for each topology is shown in Fig.7

This comparison shows that the converter 1-1-2 can use a filter with volume, weight and cost equal half of the filter used in the converter 1-1-1-1 and 28 times smaller than the filter used in NPC converter, without decrease the converter efficiency.

B. Inverters with maximum switching frequency

The second comparison is developed to obtain the maximum carrier frequency for each inverter. The maximum switching frequency result from the losses of the highest stress device, where the maximum junction temperature is reached ($T_{j,max}$=125°C).

The performance indexes are presented in Table I for maximum switching frequency and the power losses distribution is presented in Fig. 7.

The highest carrier frequency obtained is with the converter 1-1-1-1. In this system the filter will be minimized, however the efficiency will be penalized. In the configuration 1-1-2 the carrier frequency increases the power losses of the cell 1, because only this cell operates in high frequency. In the NPC inverter the maximum carrier frequency is limited by the switching power losses of the IGBTs 1 and 4. At this maximum frequency, the DF1 of NPC inverter is significantly higher than in topologies 1-1-2 and 1-1-1-1.

TABLE I
Compendium of the comparison

Comparison	Equal efficiency			Maximum switching frequency			Equal output filter		
Topologie	1-1-2	1-1-1-1	NPC	1-1-2	1-1-1-1	NPC	1-1-2	1-1-1-1	NPC
Total number of devices/phase	12	16	6	12	16	6	12	16	6
Number of phase-voltage levels	9	9	2	9	9	2	9	9	2
Carrier frequency [Hz]	9060	720	1020	39000	20880	6540	1860	240	5580
Frequency of first harmonic band [Hz]	9060	5760	1020	39000	167040	6540	1860	1920	5580
THD [%]	13.84	13.90	53.17	13.86	13.89	56.47	13.90	13.57	56.47
DF1 [%]	0.085	0.162	2.4518	0.0432	0.0307	0.4077	0.4613	0.4697	0.4686
Total power losses/phase [W]	1575	1629	1646	3823	12999	8047	1027	1383	6910
Performance [%]	99.06	99.02	99.012	97.71	92.01	95.17	99.38	99.18	95.25

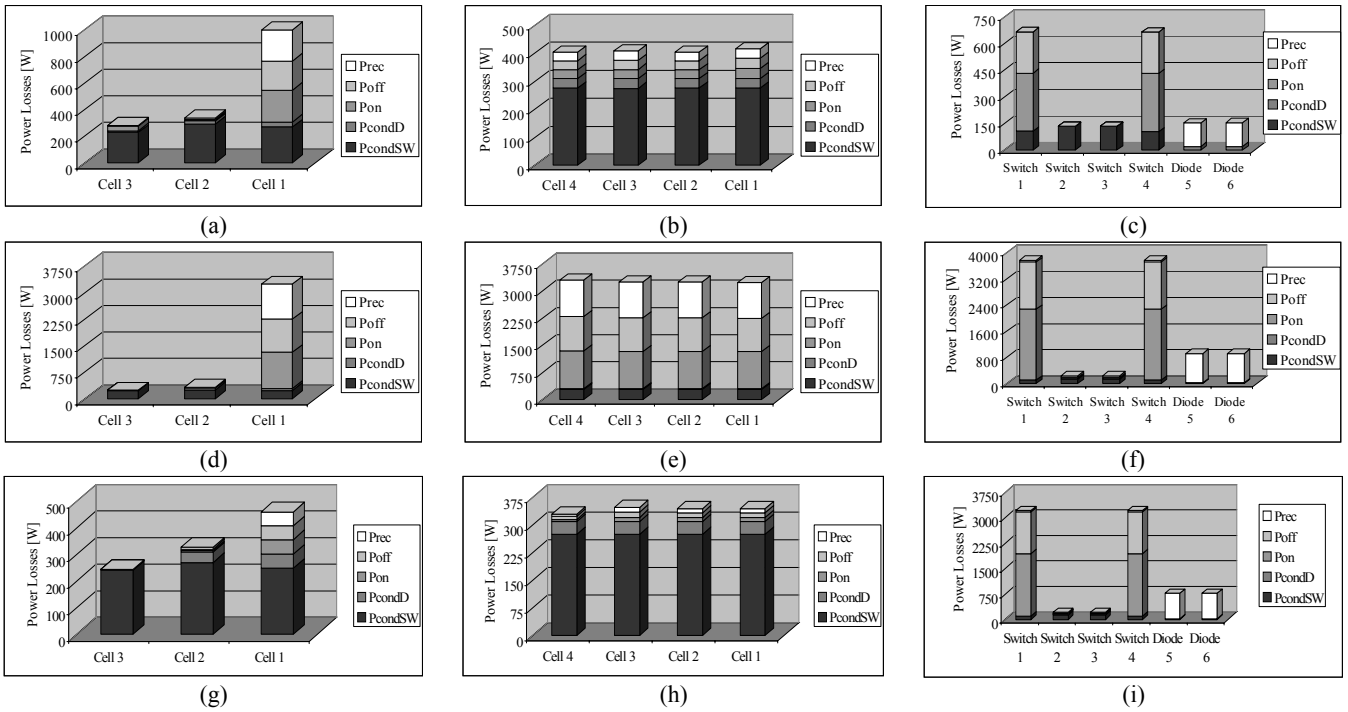

Fig. 7. Power losses distribution: Same efficiency (a) 1-1-2, (b) 1-1-1-1, (c) NPC; Maximum switching frequency (d) 1-1-2, (e) 1-1-1-1, (f) NPC; Equal output filter (g) 1-1-2, (h) 1-1-1-1, (i) NPC

C. Inverters with same output filter

The third comparison has the purpose of obtaining the carrier frequencies in which the three systems will present the same output filter, with the same volume, weight and cost. These frequencies are obtained when the DF1 is equal for all systems.

The performance indexes for this comparison are presented in Table I and the power losses distribution is shown in Fig. 7.

In this comparison, the topologies 1-1-2 and 1-1-1-1 present approximately the same indexes, however the topology 1-1-2 still presents better performance. The NPC inverter presents power losses higher than in inverters 1-1-2 and 1-1-1-1, in other words the efficiency is penalized to use the same output filter.

V. EXPERIMENTAL RESULTS

This section presents the experimental results obtained with a low-power prototype of one phase of a hybrid asymmetric nine-level inverter. This multilevel inverter uses three H-bridge cells in series and its nominal output power is 1 kW. The isolated DC voltage sources are: V_{DC1}=85V, V_{DC2}=85V and V_{DC3}=170V. These DC voltage sources are implemented using a multipulse transformer and 4 three-phase rectifiers, where the nominal load of each rectifier is: P_1=133W, P_2=230W, P_3=318,5W and P_4=318,5W. The voltage DC source of the cell 3 is obtained with two series-connected rectifiers (rectifiers 3 and 4). Details about the multipulse transformer design can be verified in [18]

All H-bridge cells are implemented using the IGBT module SK45GB063 (600V/30A). The mathematical models of the SK45GB063 semiconductor curves $v_{ce}(i_{load}(\theta))$, $v_F(i_{load}(\theta))$, $E_{on}(i_{load}(\theta))$, $E_{off}(i_{load}(\theta))$ and $E_{rec}(i_{load}(\theta))$ were extracted from datasheet of the manufacturer. They are given respectively by (26), (27), (28), (29) and (30).

$$v_{ce_{SK\,45}}(\theta) = 1.6.e^{0.008.I_{load}(\theta)} - 1.6.e^{-0.097I_{load}(\theta)} \quad (26)$$

$$v_{F_{SK\,45}}(\theta) = 3.3.e^{0.058.I_{load}(\theta)} - 1.0.e^{-0.129I_{load}(\theta)} \quad (27)$$

$$E_{on_{SK\,45}}(\theta) = \left(3.3.e^{0.058.I_{load}(\theta)} - 2.9.e^{0.059.I_{load}(\theta)}\right).10^{-3} \quad (28)$$

$$E_{off_{SK\,45}}(\theta) = \left(10.3.e^{-0.004.I_{load}(\theta)} - 10.1.e^{-0.008I_{load}(\theta)}\right).10^{-3} \quad (29)$$

$$E_{rec_{SK\,45}}(\theta) = \left(-2.6.e^{-0.012.I_{load}(\theta)} + 2.7.e^{-0.006.I_{load}(\theta)}\right).10^{-3} \quad (30)$$

The power losses of each cell are computed from the mathematical model of each semiconductor. The total power losses of the cells 3, 2 and 1 are 2.89W, 3.02W and 4.87W, respectively. Then, the efficiencies of the cells 3, 2 and 1 are 99.54%, 98.68% and 96.3%, respectively. The total power loss of the inverter is 10.78W. Therefore, the total efficiency is 98.9%. The power losses distribution in each cell can be verified in Fig. 8.

Fig. 9 presents the experimental results obtained with the prototype. The measures were made with the Digital Power Meter WT1600 (Yokogawa). Fig. 9(a) presents the results of the cell 3. Channel 3 is applied to the DC voltage source of the cell 3 ($Urms3$, $Irms3$ and $P3$ represents, respectively, the voltage, current and active power measured at the input of this cell) and channel 6 is used to measure the output variables of this cell. Fig. 9(a) shows the output voltage of the cell 3. In Fig. 9(b), channel 2 presents the input measurements of the cell 2 and channel 5 shows the output measurements of this cell. The waveform presented in Fig. 7(b) is the output voltage of the cell 2. In Fig. 9(c), channel 1 includes the input measurements of the cell 1 and channel 4 presents the output measurements of this cell. The waveform shown in Fig. 9(c) is the output voltage of the cell 1. Finally, Fig. 9(d) presents the input measurements of all cells (channels 1, 2 and 3) and channel 6 shows the output measurements of the hybrid asymmetric inverter. In addition, Fig. 9(d) shows the output phase voltage waveform. In Fig. 9(a), (b) and (c), the parameter η is the efficiency of cells 3, 2 and 1, respectively. In Fig. 9(d), η is the total efficiency of the multilevel inverter.

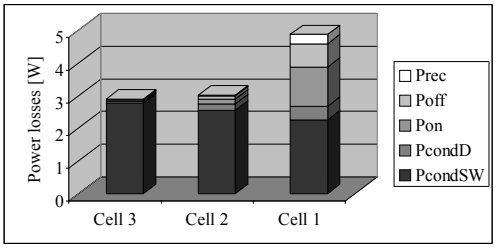

Fig. 8. Power losses distribution in the setup

The power losses of the cells 3, 2 and 1 are, respectively, 8.7W, 9.5W and 11.5W. The efficiency of the cells 3, 2 and 1 are, respectively 99.13%, 97.9% and 97.68%. The total power losses of the inverter are 29.7W. Therefore, the total efficiency is 97.29%.

There is a difference between the theoretical and experimental results obtained from the prototype. However, this difference can be caused by the gate resistance. The theoretical efficiencies are similar to the experimental efficiencies. The difference between the theoretical and experimental results not affects the conclusion of this paper because the errors that occur for one topology also happen in the other.

The experimental results were obtained using a hybrid multilevel modulation. These results prove that the highest power cell presents the lowest power losses because it operates at low frequency. Also, they show that the lowest power cell presents the highest power losses because it operates at high frequency.

VI. CONCLUSION

This paper presents the comparison among three topologies of multilevel inverters. Among two nine levels inverters with H-bridge cells connected in series, one configuration is hybrid and asymmetrical (1-1-2) and the other is symmetrical (1-1-1-1) and the NPC inverter. The comparison was developed in three forms, for same performance, for maximum switching frequency and for same output filter. When the objective is to obtain the same performance or the same output filter, the topology 1-1-2 presents more advantages. When the objective is obtaining the maximum switching frequency the configuration 1-1-1-1 is more indicate, however, in this case the performance will be penalized. Then, the hybrid asymmetrical topology presents better performance that the topology symmetrical and the NPC inverter.

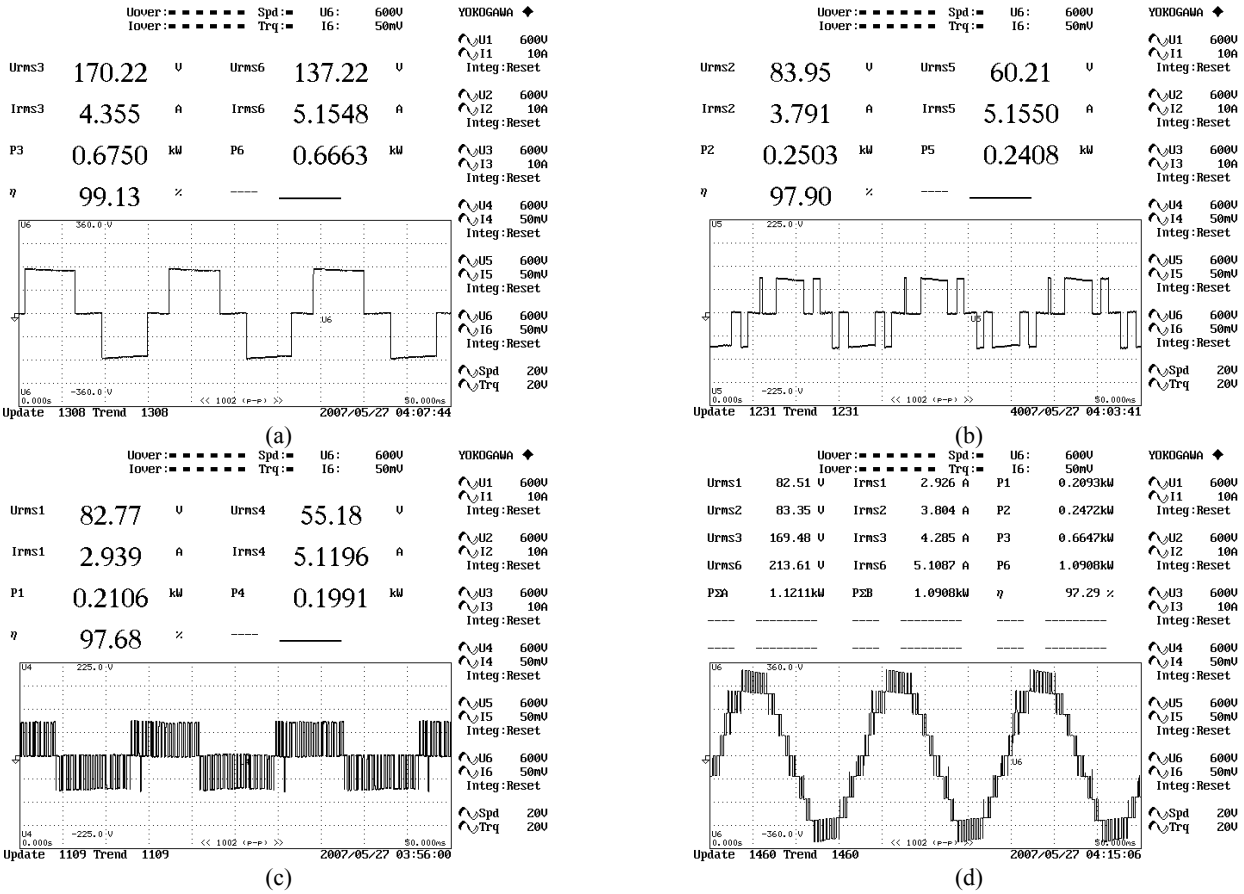

Fig. 9. Experimental results: (a) Cell 3; (b) Cell 2; (c) Cell 1; (d) Total

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