LOW COST IEC61000-4-4 COMPATIBLE PULSE GENERATOR

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***Abstract* – This paper presents a Low Cost Pulse Generator compatible with the test equipment presented in the IEC61000-4-4 standard. The presented circuit is able to handle continuous switching frequencies up to 1 kHz and 100 kHz on burst applications. Due to the high voltage involved, up to 5kV, and the need for ultra-fast turn-on, a High Voltage Fixed On-time Switch is briefly presented. The series connection of power MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) is reviewed and practical considerations are discussed. Safety considerations involving the printed circuit board, cables layout and magnetics assembly are also discussed. Experimental results and pictures of the prototype itself are presented in order to validate the specifications and give a better idea about the simplicity of the presented generator.**

***Keywords* – Burst Generator, Fast Transient, Flyback Mosfet Driver, Fixed On-time Switch and IEC61000-4-4.**

I. INTRODUCTION

The last decade was a decade of big changes regarding to Electronics, Power Electronics and Power Systems. The amount of equipments generating random or harmonic noise has increased so significantly that in order to ensure safe operation to the end user it became necessary to run tests of equipment behavior under noisy operational conditions before releasing a product on the market. The IEC61000 standard family is one of the standards package responsible for specifying test setups and test equipments to carry many different tests that ensure the safe operation of an Equipment Under Test (EUT). In 2004 the International Electrotechnical Commission (IEC) released the second edition of the IEC61000-4-4 standard [1]. It is the standard that specifies the Testing and Measurement Techniques for the Electrical Fast Transient/Burst Immunity Test. This standard is the base document for the work presented in this paper. The Fast Transient test ensures the correct operation of the EUT under operational conditions that present high voltage high frequency pulses on the power supply line and on the Inputs and Outputs (I/Os) of the system. These operational conditions may exist during the occurrence of voltage arcs during switches operation in power stations, inductive related spikes and so on.

The studies of Fast Transient Generators started many years ago. For the reason that this generators are mostly built by companies specialized in Electromagnetic Compatibility (EMC) tests, it is difficult to find articles that analyze and/or present design techniques about them.

It is small the number of publications regarding to generators used on Fast Transient Immunity Tests. Some studies [2][3] deal with the analysis of the test itself but not with the design of generators. In addition to the IEC61000-4-4, the most important articles found over the Electrical Engineering community that relate to the presented project are the ones that discuss the analysis of the series connection of power switches. Series connected switches are necessary to built an ultra-fast switch that fulfill the speed and voltage requirements of the pulse generator under analysis.

In the early 90's Baker and Johnson presented the Capacitive Coupling method [4] for series operation of MOSFETs. It was the first structure capable of handling higher voltages using series connected MOSFETs that allowed ultra-fast turn on. As mentioned in other articles like [5] and verified by the authors during a previous attempt to accomplish the specifications of this project, the Capacitive Coupling method was found difficult to experimentally trim the theoretical capacitance distribution and was left behind.

Following the timeline, many structures and methods [7][8][9][10][11][12] for achieving voltage balance on series connected IGBTs were presented but none of them achieved ultra-fast turn on.

Even most of the articles regarding the series connection of power switches relate to the series connection of IGBTs, the authors opted to use MOSFETs in this application due to the fact that, in general, MOSFETs are faster than IGBTs and the ultra-fast turn-on would be easier to accomplish.

The Flyback MOSFET Driver that is briefly presented in this article is in fact a Flyback converter that uses the switch capacitance as its output capacitor, a zener diode to protect the gate input and a load resistor in parallel with the output (gate input) to quickly discharge the switch gate input after the inductor discharge.

A 5kV switch with a fixed on-time about 300ns capable of turn on faster than 10ns was built and successfully tested on the Fast Transient Generator that is the main object of this study. Experimental results using the developed generator are also presented in order to validate the study.

II. TRANSIENT GENERATOR SPECIFICATIONS

The IEC61000-4-4 standard clearly specifies the Fast Transient/Burst Generator. The standard proposes a simple circuit capable of generating the necessary pulse shape and specifies the magnitude, rise time and duration of the pulses.

Fig. 1 shows the circuit proposed by the standard in which:

- U - High voltage source.
- R_C - Charging resistor.
- C_C - Energy Storage capacitor.
- R_S - Impulse Duration Shaping resistor.
- R_M - Impedance Matching resistor.
- C_D - DC blocking capacitor.
- R_{out} - Theoretical Load.
- vC_C - Energy storage capacitor voltage.

iC_C - Energy storage capacitor current.
vS_1 - Switch voltage.
vR_{out} - Test load voltage.
S_1 - High voltage power switch.
iS_1 - Switch current.
Ton - Switch fixed on time.
R_{S1} - Switch S_1 on resistance.

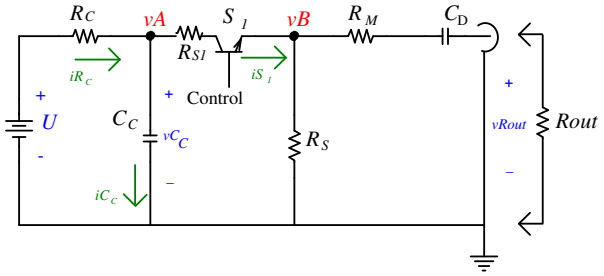

Fig. 1. IEC61000-4-4 Pulse Generator.

The specified pulse profile is presented in Fig. 2.

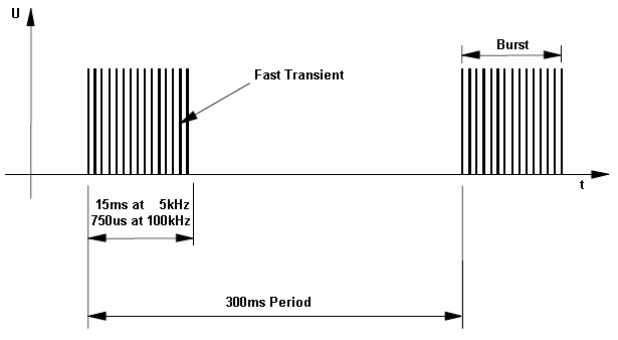

Fig. 2. Pulse profile.

The standard specifies the pulse shape presented in Fig. 3. Its shape must to be verified using testing loads of 50Ω and 1kΩ. The rise time is specified to be 5ns ± 30% to both test loads. Using the 50Ω load, the duration time should be 50ns ± 30% and the maximum voltage half the selected voltage ±10% tolerance. It is half the set voltage because the output impedance should also be 50Ω. Using a 1kΩ test load the duration time should be 50ns (-15 +100ns) and the maximum voltage must be the selected voltage multiplied by (100/105) ±20% tolerance.

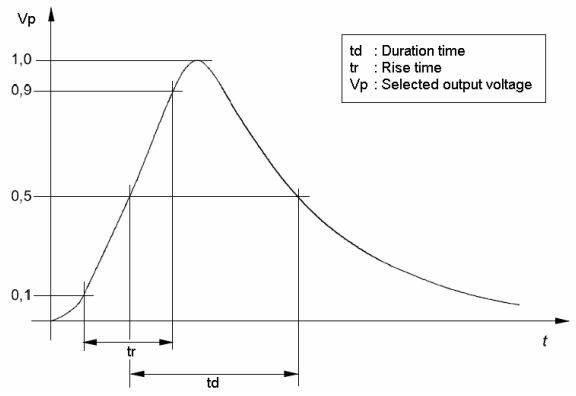

Fig. 3. Specified pulse shape.

III. TRANSIENT GENERATOR ANALISYS

A. Operational stages

The circuit has 2 main operational stages. The first one, presented in Fig. 4, starts when the switch is closed. The energy previously stored on the Energy Storage capacitor is sent to the output through the Impedance Matching resistor and the DC Blocking capacitor. The discharge of the Energy Storage capacitor and consequently the pulse shaping is performed mostly by the Impulse Duration Shaping resistor.

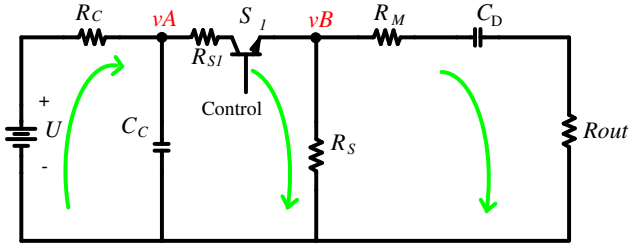

Fig. 4. First operational stage.

The second operational stage begins when the switch is opened. The equivalent circuit for this operational stage is presented in Fig. 5. The Energy Storage capacitor is recharged with the high voltage provided from the High Voltage power source and a small current flow on the output loop due to the energy stored on the DC Blocking capacitor.

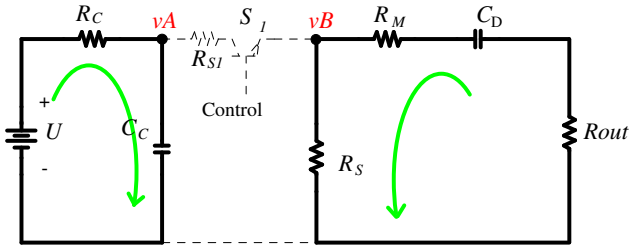

Fig. 5. Second operational stage

IV. MATHEMATICAL ANALYSIS

Fig. 6 presents the theoretical transient behavior of the most important variables. This figure is not drawn on scale in the time axis. Some variables are much faster than the others and the experimental results will give a better idea of the variables behavior.

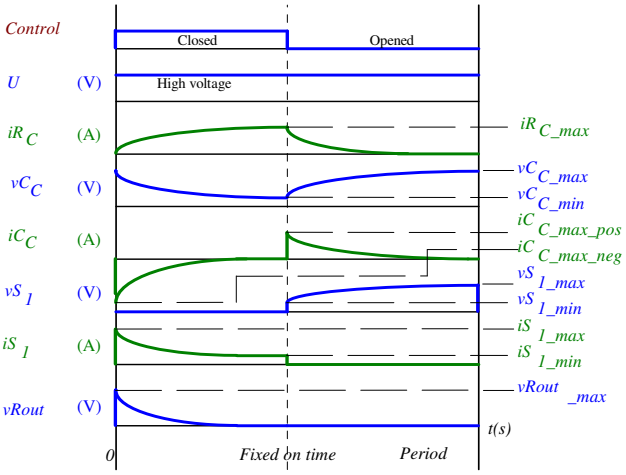

Fig. 6. Transient behavior of the most important variables.

The solution for the output voltage of the pulse generator and the specification of the components is done through the nodal analysis of the nodes A, presented in equation (1), and B, presented in equation (2), in the frequency domain using the appropriate mathematical tools. This analysis is done for the first operational stage considering the initial condition of voltage on the Energy Storage capacitor. It means that the design of the Transient Generator is mostly done through the Energy Storage capacitor discharge behavior.

$$\frac{V_A(S)-U/S}{R_C}+\frac{\left(V_A(S)-U/S\right)}{\frac{1}{C_C\cdot S}}+\frac{V_A(S)-V_B(S)}{R_{S1}}=0 \qquad (1)$$

$$\frac{V_B(S)-V_A(S)}{R_{S1}}+\frac{V_B(S)}{R_S}+\frac{V_B(S)}{R_M+R_{out}}=0 \qquad (2)$$

$$vRout(t)=\frac{vB(t)\cdot R_{out}}{R_{out}+R_M} \qquad (3)$$

Equation (4) presents the output voltage on a resistive load found using (1), (2) and (3).

$$vRout(t)=U\left(\delta e^{-\frac{\alpha t}{C_C R_C \beta}}+\lambda\right)\frac{R_S}{\alpha\beta}\left(\frac{R_{out}}{R_{out}+R_M}\right) \qquad (4)$$

Where:

$$\alpha=R_{S1}\left(R_M+R_{out}+R_S\right)+R_S\left(R_M+R_{out}\right)+R_C\left(R_M+R_{out}+R_S\right)$$
$$\beta=R_{S1}\left(R_M+R_{out}+R_S\right)+R_S\left(R_M+R_{out}\right)$$
$$\delta=\left(R_M+R_{out}+R_S\right)\left(R_M+R_{out}\right)R_C$$
$$\lambda=R_M R_{S1} R_S+R_{out}\cdot\left(2R_M\left(R_{S1}+R_S\right)+R_{S1}R_S\right)+\left(R_{S1}+R_S\right)\left(R_{out}{}^2+R_M{}^2\right)$$

V. FAST TRANSIENT GENERATOR DESIGN

Due to the amount of variables in (4), it is necessary to use some information presented in the standard to obtain one more mathematical relationship that allow the designer to find the component values. The standard specifies an output impedance of 50Ω. Analyzing the circuit it is possible to verify the relation presented in (5).

$$R_M=50\Omega-\frac{R_{S1}R_S}{R_{S1}+R_S} \qquad (5)$$

First design step: The Energy Storage capacitor and the Charging resistor specification should be done in such way the Energy Storage capacitor voltage raises to the input voltage at the end of each switching period. At this point it is necessary to specify the maximum switching frequency and the fixed on time of the switch in order to know how much time the input circuit will have to fully charge. The capacitor value should be arbitrarily chosen but some values will not allow the circuit to fully satisfy the standard specifications. It means the presented design process is iterative and should be verified at the end. During numerous specifications, it was found that a capacitor value of 680pF is a very good option. It is easily found at voltages about 5kV, allow all the specifications to be achieved and the losses are minimized.

Second design step: Using the switch on resistance that should already be known from its previous design, the value of R_M that was found using (3), the component values found on the first design step and (4), all other component values can be calculated. Since (4) represents the discharge of a capacitor, it is possible to find the value of R_S using the information the standard provides about the duration time for the 1kΩ test load. Since the discharge time depends on the test load resistance and the other test load is 50Ω, it is recommended to use the greater tolerance allowed by the standard.

Third design step: As previously stated, the presented design process is iterative, resulting that the duration time for the second specified test load should be confirmed. Plotting or just mathematical evaluation of (4) using the calculated component values and the 50Ω test load should confirm the duration time for this test setup. As known, the duration time obtained from the previous calculus should match the duration time range specified by the standard. It is worth nothing that the duration time will not match the exact values specified by the standard. By nature, this circuit will just be easily designed if the tolerances presented in the standard were used during the design. If the duration time for the 50Ω load is out of the tolerance range, another capacitor value should be chosen and the calculus executed again until the specifications fulfillment.

Post design considerations: Due to intrinsic characteristics of the circuit under development, it is necessary to increase the input voltage to levels higher than the pulses amplitude. The maximum voltage at the high voltage power source terminals to obtain the highest amplitude for a 50Ω load is calculated using (6). The input voltage for intermediate levels should be proportional to the desired pulse magnitude.

$$U_{\_max}=\frac{\left(\frac{vRout_{\_max}\big|_{50\Omega}}{50}\right)\left(R_M+50\right)}{\left(R_S/\!/\left(R_M+50\right)\right)}\left(R_S/\!/\left(R_M+50\right)+R_{S1}\right) \qquad (6)$$

VI. HIGH VOLTAGE ULTRA-FAST TURN ON FIXED ON TIME POWER SWITCH

Due to the lack of inexpensive high voltage high speed power semiconductors on the market, it was verified the need to build the power semiconductor switch using low voltage power switches that are easily found on the market.

Since the big challenge is to achieve the 5ns rise time specified on the standard for the output pulse, the authors verified the possibility of creating an Isolated Fixed On-Time Ultra-Fast switch using the Flyback power converter topology as the gate driver.

As shown in Fig. 7 the driver is in fact a Flyback converter. The switch gate input capacitance acts as the output capacitance of the converter and the resistance Rload discharges it after the fixed on time.

The ultra-fast turn on is granted by the current injection characteristic of the Flyback converter that occurs during the energy delivery to the secondary side.

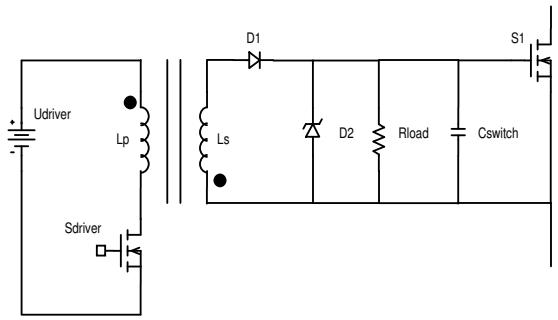

Fig. 7. Isolated Ultra-Fast Flyback MOSFET Gate Driver.

The fixed on time is granted by the fact that the switch capacitance will just be discharged after the energy stored on the Flyback transformer is almost fully discharged.

The discharge time of the energy stored on the Flyback transformer is known due to the fact that the voltage on the inductance of the secondary windings is clamped by a zener diode and results on a fixed negative current slope that can be moved up and down as the energy stored is changed.

The presented driver experimentally achieved the ultra-fast turn on and the results are presented in [14] for a 1500V switch stack.

The feasibility of building a switch stack able to handle higher voltages using the presented gate driver was analyzed. The developed switch stack is partially presented in Fig. 8. As it is shown, the series connected switches are assumed to have their gate drivers equal and series connected on the control side.

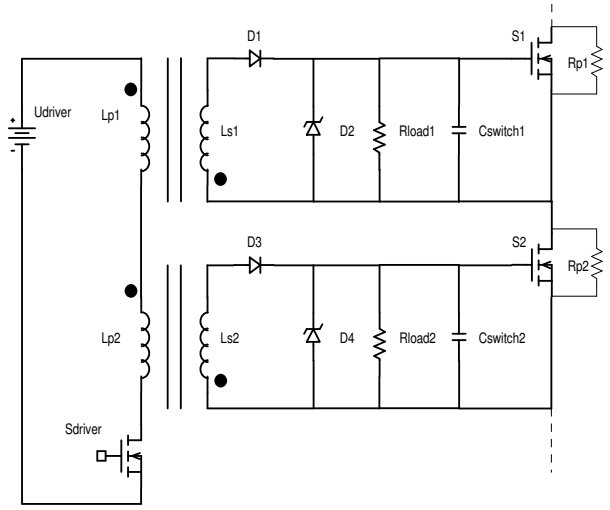

Fig. 8. Series connected MOSFETs using the Isolated Ultra-Fast Flyback MOSFET Gate Driver.

The ultra-fast gate driver do not impose dynamic voltage unbalance to the switches during the turn on process due to the fact that the switches receive the same energy injection granted by the series connection of the primary inductors and they close very fast. This assumption was experimentally verified and the results are also presented in [14].

The turn off process was assumed to impose dynamic voltage unbalance because of variations on the resistances responsible for discharging the gate input capacitances and small variations on the energy stored in the inductors and on the gate input capacitances among the switches, which is common even for switches from the same production batch. In order to control the time constant of each discharge circuit and allow the individual regulation of the voltage transient behavior of each switch in the stack, it was proposed a variable resistance connected in series with the discharge resistance. The variable resistance should be experimentally trimmed and the fixed resistance is necessary to assure a minimum resistance that is necessary to achieve the ultra-fast turn on.

As already mentioned in many papers and manufacturers catalogs, the easiest way to achieve static voltage balance is to connect resistances in parallel to each one of the switches. These resistances are presented on Fig. 8 and were calculated based on the leakage current of the switches.

Further information regarding the High Voltage Fixed On-Time Switch development can be found in [14].

VII. ASSEMBLY CONSIDERATIONS

Innumerous precautions are necessary in order to achieve all the specifications of the standard. The most important are:

A. Low inductance components.

The usage of low inductance resistors for R_S, R_M and R_{out} is necessary to allow high di/dt in the circuit. Switches with low Drain-Source inductance are required for the same reason. A very low leakage inductance gate transformer is necessary to improve driving speed.

B. Safety considerations

Appropriate safety distances between high voltage components should be used. The usage of printed circuit boards with good isolation like FR4 boards should be considered. The isolation between primary and secondary windings of each gate transformer should support the greatest voltage on the switch stack. Resistors that support not just the power specifications but also the high voltage peaks are mandatory. It is recommended to use resistors classified as Surge Resistor because of their very low inductance and voltage capability.

C. Experimental trimming

The presented mathematical analysis was well developed and brought excellent simulation results. However, experimental results revealed that printed circuit board layout, parasitic effects and component values variation have significant influence on the pulse shape and output impedance. In order to fully satisfy the standard specifications it was found necessary that the first prototype had the resistances R_S and R_M experimentally adjusted to correct small deviations and take the generator to the standard specifications.

VIII. EXPERIMENTAL RESULTS

The pulse generator assembly is shown in Fig. 9. Component values are listed below. The developed switch stack uses four STP4N150 power MOSFETs (1500V - 5Ω - 4A). The drivers where built using EE20 Ferrite cores.

R_C - 2000Ω.
R_S - 136Ω.
C_D - 10nF.
C_C - 680pF.
R_M - 30Ω.

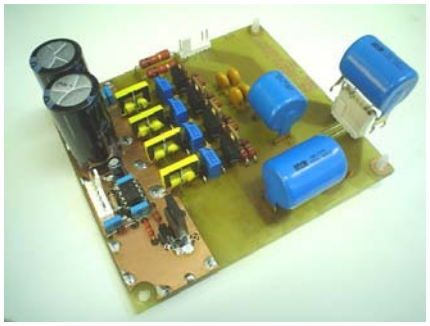

Fig. 9. Fast Transient Generator prototype.

The pulse profile used during the experimental tests was created using a TMS320LF2401A Digital Signal Controller (DSC). The standard specifies two testing frequencies. The lower one is 5 kHz and the higher one is 100 kHz.

Fig. 10 presents the control signal for a 5kHz setup.

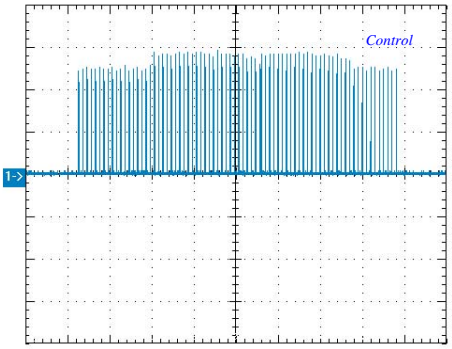

Fig. 10. Driver side switch gate voltage (*Control:* 5V/div, 2ms/div).

Fig. 11 was acquired in order to validate the 300ms period that must exist between generated bursts and the switching frequency of 5kHz. Attention must be taken to the fact that the pulses presented in Fig. 11 (a) are not single pulses but burst packages containing 75 pulses at 5 kHz. Fig. 11 (b) presents in detail the pulses contained in those bursts.

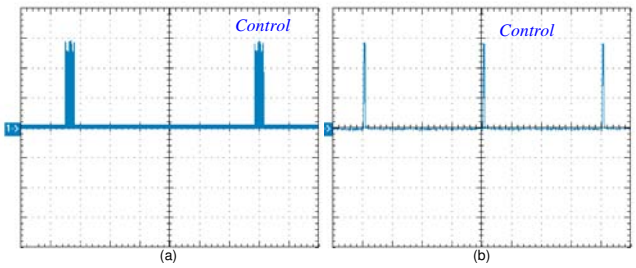

Fig. 11. Driver side switch gate voltage ((a) *Control*: 5V/div, 50ms/div; (b) *Control*: 5V/div, 50us/div).

The pulse presented in Fig. 12 was obtained using a 1kΩ/1kV setup. Fig. 12 (a) present the entire pulse and Fig. 12 (b) the rise time. The peak was measured about 850V and the rise time about 9.12ns.

The pulse presented in Fig. 13 was obtained using a 50Ω/4kV setup. Fig. 13 (a) present the entire pulse and Fig. 13 (b) the rise time. The peak was measured about 660V and the rise time about 16.7ns.

The pulse presented in Fig. 14 was obtained using a 1kΩ/4kV setup. Fig. 14 (a) present the entire pulse and Fig. 14 (b) the rise time. The peak was measured about 2300V and the rise time about 18.66ns.

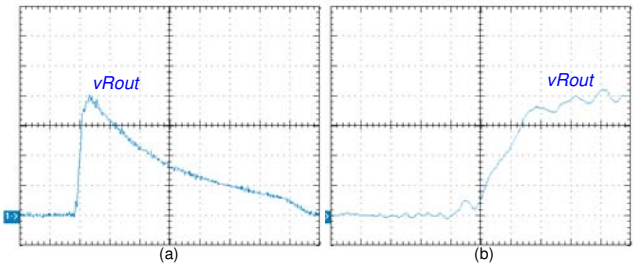

Fig. 12. Pulse profile obtained for a 1kV/1kΩ setup ((a) *vRout:*200V/div, 50ns/div; (b) *vRout:*200V/div, 5ns/div).

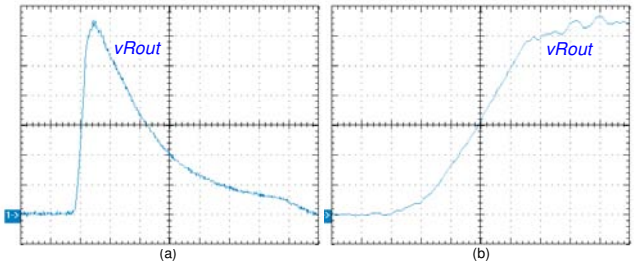

Fig. 13. Pulse profile obtained for a 4kV/50Ω setup ((a) *vRout:*100V/div, 50ns/div; (b) *vRout:*100V/div, 5ns/div).

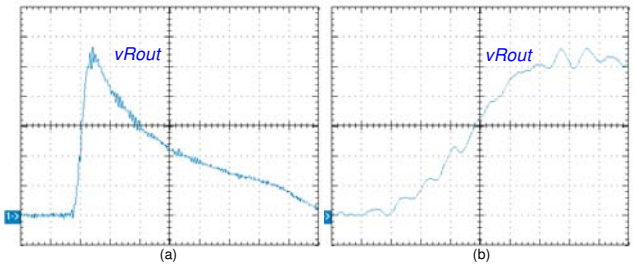

Fig. 14. Pulse profile obtained for a 4kV/1kΩ setup ((a) *vRout:*400V/div, 50ns/div; (b) *vRout:*400V/div, 5ns/div).

The voltage sharing among the switches in the stack for a 100kHz setup is presented in Fig. 15. As previously stated there is no dynamic voltage unbalance during the turn-on and turn-off. This figure shows the drain voltages of the switches in the stack referenced to node B. Fig. 15 (a) present the voltage behavior for the first pulse of a burst and for that reason the static voltage balance (before pulses) is also verifiable. Fig. 15 (b) present the turn-on process confirming the expected behavior.

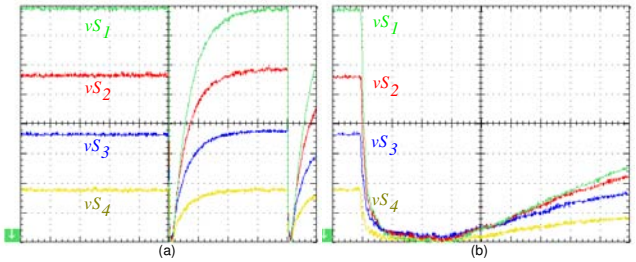

Fig. 15. Voltage sharing in the switch stack at switching frequency of 100kHz ((a) 20V/div, 2.5us/div; (b) 20V/div, 100ns/div).

CONCLUSION

A low cost easy to assemble circuit that partially fulfilled the IEC61000-4-4 test equipment needs was presented. The design steps and experimental results were also presented. Due to the costs involved to assembly the presented circuit and mainly the Fixed On-Time switch, it was verified that it is a good alternative to the equipments that use expensive high voltage semiconductor based switching devices currently found on the market.

The main limitation of the presented circuit lies on the turn-on process of the switches in the switch stack. The increment of the voltage on the switch stack results in slower turn-on transients that compromise the pulse magnitude because the pulses are generated mostly during the turn-on of the switches. The effect most likely to be responsible for this behavior is the Miller effect that will be considered in further analysis. To illustrate the switch behavior Fig. 16 (a, b, c and d) present the voltage in the switch stack for 250V, 500V, 1000V and 2000V setups respectively.

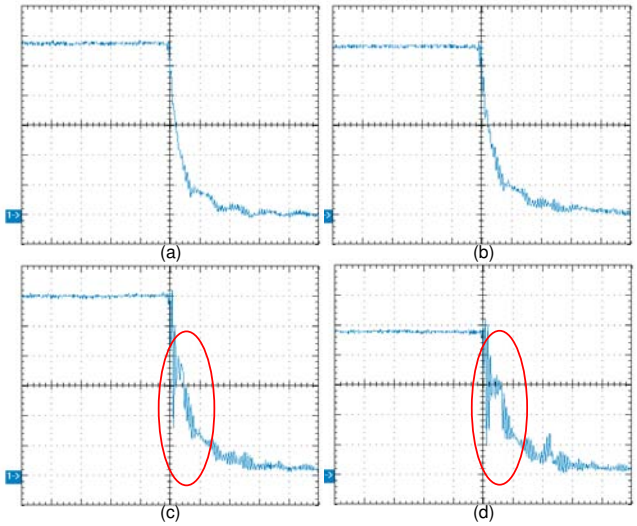

Fig. 16. Switch stack voltage ((a) 50V/div, 50ns/div; (b) 100V/div, 50ns/div; (c) 200V/div, 50ns/div; (d)500V/div, 50ns/div).

This pulse generator can be easily adapted to be used on biomedical research projects. "Cells membrane electroporation for drug delivery in cancer therapy", "Bacterial decontamination of liquids with pulsed electric fields" and "Human cells apoptosis induced by high intensity pulsed electric fields" are some of the research projects that could benefit from the information in this article.

Future studies will focus on semiconductors thermal behavior, the analysis of the Miller effect, the usage of other magnetic core geometries to minimize leakage inductance and on the usage of IGBTs.

ACKNOWLEDGEMENT

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