STUDY AND DESIGN OF A VOLTAGE LINE CONDITIONER WITH SERIAL COMPENSATION AND FED BY LOAD SIDE

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***Abstract* – This work presents the study and design of an *ac* line conditioner operating in closed loop, which can provide energy to linear and non-linear loads. The proposed topology has serial *ac* voltage compensation. This configuration allows operate with only a part of the load power. To provide the conditioning of the output voltage face the system's perturbation a feedback control technique is used. A control technique to avoid the saturation of the transformer is incorporated within the main control loop. Fast response is obtained by using the virtual resistance concept to damp the output voltage oscillations. Experimental results of a 10 kVA prototype are included to show the validity of the proposed study.**

***Keywords* – *ac* line conditioner, *ac-ac* converters, feedback control, virtual resistor.**

I. INTRODUCTION

In voltage-sensitive equipment, requirements on the power quality of *ac* sources are becoming more significant. Power line disturbances on sensitive loads such as computers, process control systems and communication equipments can often lead to valuable data loss, interruption to communication services, and long shutdown of production [1].

The recent increase in the use of sensitive loads results in a greater demand for high-quality voltage sources, concerns about harmonic content and voltage stability in electrical supply systems. Therefore, uninterruptible power supplies (UPSs), voltage regulators (VRs), and voltage or line conditioners (VCs) have been used in various environments to provide regulation and protect loads supplied.

The VCs differ from the VRs, because besides stabilizing the output voltage they correct the harmonic content, working as active filters of voltage.

A line conditioner with voltage up/down capability based in [2] is shown in Fig. 1. It uses eight current bi-directional switches, that represents a high number of active switches. However, its command circuit is simple. It has the advantage of robustness and can use the classical PWM inverters principle. Considering these characteristics this topology was chosen to design a 10 kVA line conditioner, with three-level modulation, operating as active filter and as voltage regulator feeding linear and non-linear loads.

For *dc-dc* converters the modeling and control is widely discussed in the literature [3] and several linear and non-linear techniques are used to implement a robust and fast control loop of the systems variables. On the other hand, the control of *ac-ac* converters is a current research topic and for which no standard control techniques are yet established. One of the difficulties of the control of *ac-ac* converters lies in the complexity of the systems, leading to high order transfer functions. Moreover, both the load and input voltages vary over time, demanding great control effort. If the voltage control loop is too fast, there is good dynamic response, but due to the complexity of the system, it may become unstable.

To provide the conditioning of output voltage a feedback control loop is used. An extra control loop is incorporated in the main loop to control the offset voltage in the transformer input, avoiding its saturation. Fast response is obtained by using the virtual resistance concept to damp the output voltage oscillations. Experimental results of a 10 kVA prototype are included to show the validity of the proposed study.

II. CONVERTER STRUCTURE AND PRINCIPLE OF OPERATION

The circuit of the line conditioner is presented in Fig. 1. This topology has serial *ac* voltage compensation, a configuration that allows operating with only a part of the load power, increasing the total efficiency of the structure.

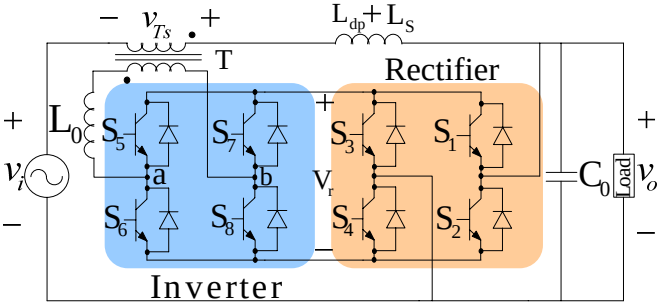


Fig. 1 – Power Circuit of the line conditioner.

The power circuit of the line conditioner is based on [2], where an *ac-ac* indirect converter is used with direct *dc* link. Therefore, there are no energy storage elements between the rectifier stage (S_1/S_2 and S_3/S_4) and the inverter stage (S_5/S_6 and S_7/S_8). Although, due to line impedance and parasitic inductances, it is necessary to use a small capacitor in order to avoid over voltage across the switches. The transformer *T* has the purpose of applying the compensation voltage v_{Ts}, increasing or decreasing the input voltage v_i, to stabilize the output voltage v_0. All the active switches have an anti-parallel diode.

In this topology, the capacitive filter C_0 is positioned on the load side. The transformer's leakage inductance L_{dp} with the line intrinsic inductance L_s are used as a multifunctional filter, acting on the output voltage v_0 and on the output inverter voltage v_{ab}. The inductance L_0 represents the total inductance seen by the primary side of the transformer.

III. MODULATION AND MAIN WAVEFORMS

In order to rectify the output voltage, the bi-directional rectifier operates with low frequency and has two operating stages, which depend on the output voltage v_0 polarity. The full bridge inverter is modulated by a three-level PWM modulation and has five operating stages described in [4].

The modulation waveforms for the rectifier and inverter stage are shown in Fig. 2. It can be noted that, for the inverter, the control voltage v_c is a rectangular voltage, therefore this modulation can be called rectangular PWM (RPWM). RPWM's characteristics were described in [5].

In Fig. 3 the converter's main waveforms are presented, showing its operation in conditions of increasing and decreasing compensation voltage.

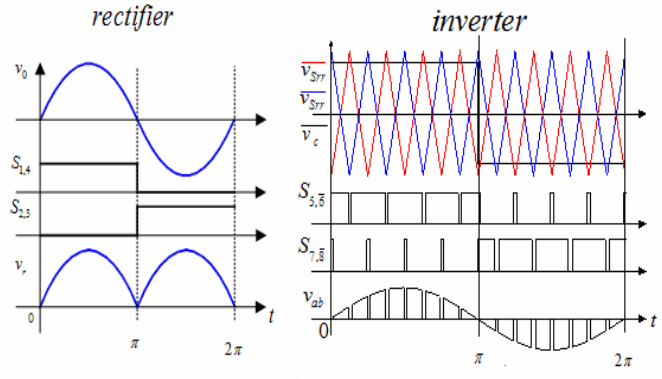


Fig. 2 – Modulation for the rectifier and inverter stage.

IV. CONDITIONER ANALYTICAL STUDY

A. *Main Analytical Expressions*

The mathematical expressions presented in this section are valid for the converter when a three-level PWM modulation is used. The switching frequency is assumed to be much higher than the line frequency, and instantaneous average values are considered.

For the *ac-ac* converter the duty cycle D is obtained as the ratio between the interval when the switches S_5 and S_8 conduct simultaneously and the switching period T_S, on the v_0 positive cycle. On the negative cycle, D is defined as the ratio between the interval when S_6 and S_7 conduct simultaneously and T_S.

The line voltage applied in the conditioner input can have an amplitude variation of ±Δ of the rated voltage and is given by (1). D_{max} is the maximum duty cycle. The expressions (2) and (3) represent respectively the transformation ratio n_1 of the transformer T and the converter static gain.

To design the output filter elements it is necessary to know its voltage and current ripple. All circuit inductances referred to the transformer secondary as L_{eq}, (4) cause the current ripple ΔI_{Leq}, where f_S is the commutation frequency.

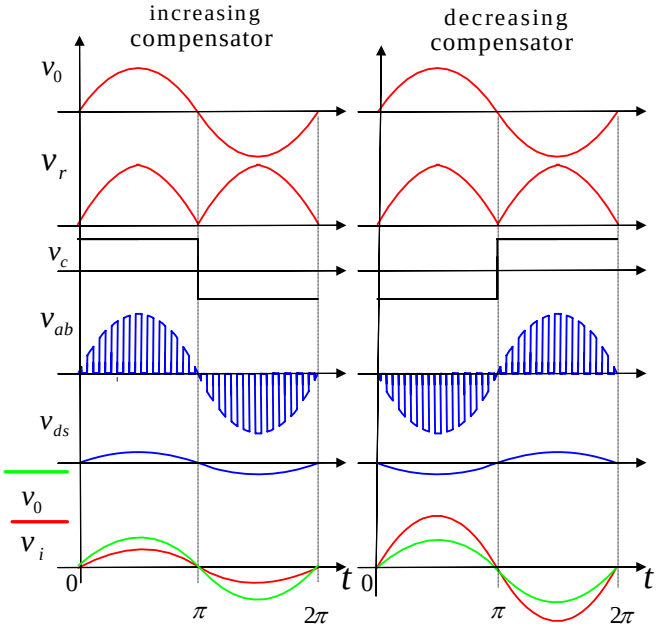


Fig. 3 – Main waveforms for the conditioner.

The C_o voltage ripple ΔV_{Co} can present four distinct forms (Fig. 4), which depend on the circuit's parameters. To optimize its design it is necessary to identify the specific ΔV_{Co}, by analyzing two conditions, (5) and (6), where I_0 is defined as the maximum load current. If both conditions are not satisfied, case *(a)* of Fig. 4, ΔV_{Co} is given by (7); If just (5) is true, case *(b)*, ΔV_{Co} is expressed by (8); If just (6) is true, case *(c)*, ΔV_{Co} is calculated by (9); finally, if (5) and (6) are satisfied, case *(d)*, ΔV_{Co} is calculated by (10).

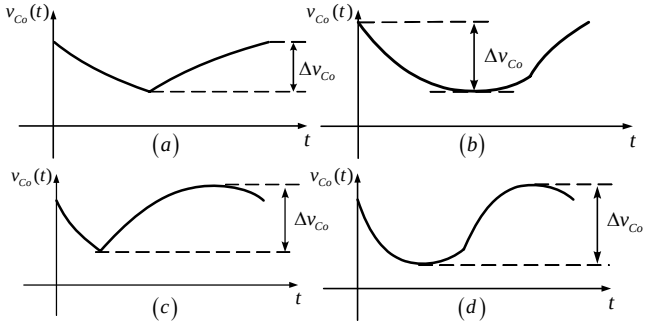


Fig. 4 – C_o voltage ripple.

$$v_i(t) = V_i \cdot \sin(\omega_r \cdot t) \tag{1}$$

$$n_1 = \frac{v_{dp}(t)}{v_{ds}(t)} = \frac{1}{\Delta} \cdot D_{max} \tag{2}$$

$$g(t) = \frac{v_o(t)}{v_i(t)} = \frac{n_1}{n_1 - D} \tag{3}$$

$$\Delta I_{Leq} = \frac{V_0 \cdot D \cdot (1-D)}{2 \cdot n_1 \cdot f_s \cdot L_{eq}} \tag{4}$$

$$\frac{4 \cdot I_0 \cdot L_{eq} \cdot n_1^2}{V_0 \cdot D \cdot (n_1 - 1) \cdot (n_1 - D)} \leq \frac{1}{f_S} \tag{5}$$

$$\frac{4\cdot n_1\cdot I_0\cdot L_{eq}}{V_0\cdot(1-D)\cdot(n_1-D)}\le\frac{1}{f_S} \tag{6}$$

$$\Delta V_{Co}=\frac{I_0 D(1-D)}{2\,f_S C_0\,(n_1-D)} \tag{7}$$

$$\Delta V_{Co}=\frac{\Delta I_{Leq}\,f_S\,(n_1-1)}{n_1 D C_0}\left(\left(\frac{I_0 L_{eq} {n_1}^2}{V_0\,(n_1-1)(n_1-D)}\right)+\left(\frac{D}{4\,f_S}\right)\right)^2 \tag{8}$$

$$\Delta V_{Co}=\frac{V_0 D}{2n_1 L_{eq} C_0}\left(\left(\frac{I_0 L_{eq} n_1}{V_0\,(n_1-D)}\right)+\left(\frac{(1-D)}{4\,f_S}\right)\right)^2 \tag{9}$$

$$\Delta V_{Co}=\frac{\Delta I_{Leq}\cdot(n_1-D)}{16\cdot n_1\cdot f_S\cdot C_o}+\frac{{I_o}^2\cdot D\cdot(1-D)}{4\cdot f_S\cdot C_o\cdot\Delta I_{Leq}\cdot(n_1-D)\cdot(n_1-1)} \tag{10}$$

B. Mathematical Model

The model of the voltage conditioner is obtained by considering the *ac-ac* converter and the transformer as a controlled source (Fig. 5). In this model the average values of the variable within the switching interval are considered. It is assumed that: the switching frequency is much greater than the line frequency; Z_L is a linear load; all the controlled switches and diodes are ideal; and R, in series with the input line, represents all parasitic resistances in the circuit. The mathematical model can be represented by (11).

$$\begin{cases} L_{eq}\dfrac{di_{Leq}(t)}{dt}=v_i(t)+v_0(t)\cdot\left(\dfrac{D-n_1}{n_1}\right)-R\cdot i_{Leq}(t) \\ C_0\dfrac{dv_0(t)}{dt}=i_{Leq}(t)\cdot\left(\dfrac{n_1-D}{n_1}\right)-i_0(t) \end{cases} \tag{11}$$

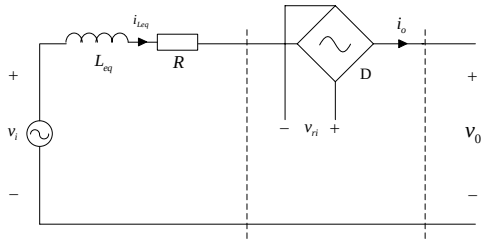


Fig. 5 – The *ac-ac* converter and transformer as a controlled source.

For the analysis of the system's dynamic its small signals model is determined as a *dc-dc* circuit modeled over peak point of the output voltage. This model is represented in (12). Fig. 6 shows the block diagram of the line conditioner, in which the transfer functions *TF* are determined.

$$\begin{aligned} L_{eq}\frac{d\hat{i}_{Leq}}{dt}&=\hat{v}_i+\frac{V_0\cdot\hat{d}}{n_1}-R\cdot\hat{i}_{Leq}+\hat{v}_0\cdot\left(\frac{D+\hat{d}-n_1}{n_1}\right) \\ C_0\frac{d\hat{v}_0}{dt}&=-\frac{I_0\cdot\hat{d}}{n_1-D}-\hat{i}_L\cdot\left(\frac{D+\hat{d}-n_1}{n_1}\right)-\hat{i}_0 \end{aligned} \tag{12}$$

The *TF* for output voltage vs. duty cycle *G(s)* is obtained by disregarding the input line perturbations. The *TF* for output voltage vs. input voltage *F(s)* is found by disregarding the duty cycle perturbations. The system can be modeled by the expression (13), where *G(s)* is given by (14) and *F(s)* by (15).

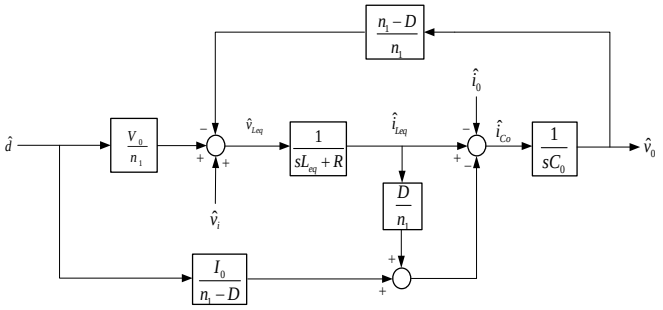


Fig. 6 – Block diagram of the line conditioner.

$$v_0(s)=F(s)\cdot v_i(s)+G(s)\cdot d(s) \tag{13}$$

$$G(s)\Big|_{\hat{v}_i=0}=\frac{-sL_{eq}\dfrac{I_0{n_1}^2}{n_1-D}Z_L+\left(Z_L V_0(n_1-D)-R\dfrac{I_0{n_1}^2}{n_1-D}Z_L\right)}{s^2 C_0 Z_L L_{eq}{n_1}^2+s{n_1}^2\left(L_{eq}+C_0 Z_L R\right)+\left(Z_L(n_1-D)^2+R{n_1}^2\right)} \tag{14}$$

$$F(s)\Big|_{\hat{d}=0}=\frac{Z_L n_1(n_1-D)}{s^2 C_0 Z_L L_{eq}{n_1}^2+s{n_1}^2\left(L_{eq}+C_0 Z_L R\right)+\left(Z_L(n_1-D)^2+R{n_1}^2\right)} \tag{15}$$

Analyzing expression (14), it is noticed that *G(s)* contains a zero right-half-plane (*RHP)*. These kind of systems, often referred to as non-minimum phase systems, have a unique step input response shown in Fig. 7. An incremental step in duty cycle translates as an increase in compensation voltage v_{Ts} and line current i_{Leq}. The current i_{Leq} crosses the line impedance and drops the input voltage. This will cause the output voltage to initially drop during the Δt time interval, rising later and reaching steady state. The lag time Δt from the initial drop until the voltage returns to its initial value is inversely proportional to the positive zero.

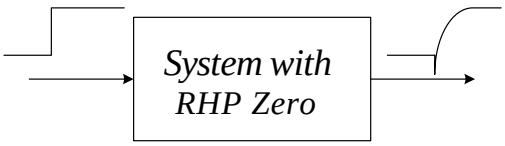


Fig. 7 – Non-minimum- phase-zero characteristic step response.

To further analyze G(s) the conditioner sensibility to load variation is verified, where the critical case is operating without load ($Z_L\to\infty$). To study the load influence over the circuit's dynamic response a resistive load is assumed and Fig. 8 shows a Bode diagram of expression (14) for two different Z_L value.

Analyzing Fig. 8 it is observed that the system's dynamic is more oscillatory and less damped as the load value increases. Therefore, in closed loop the topology has problems feeding non-linear loads. For example, the conditioner feeding a half-bridge rectifier has an abrupt rise or drop of input current and this may cause the system to be unstable. In experimental tests, there are parasitic resistances that lessen this effect since these elements damp the voltage oscillation.

There are some strategies to compensate the absence of load [5], but this work will study just the virtual resistance control strategy.

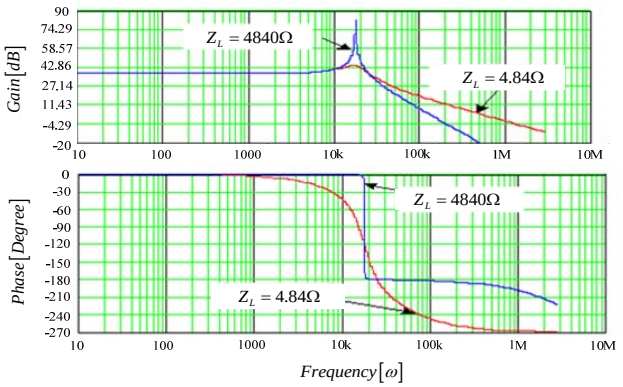


Fig. 8 – Magnitude and phase G(s) Bode diagrams.

V. CONVERTER CONTROL

To study the converter control and its design it is necessary to determine the transfer functions for the output voltage vs. duty cycle and output voltage vs. input voltage.

The converter closed loop control will be implemented in a feedback control strategy with three loops. The main loop will provide the conditioning of output voltage with fast response and its controller will be determined using the classical methodology of design in the frequency domain. The second loop is incorporated in the main loop to control the voltage offset in the transformer input, avoiding its saturation. The last loop incorporates the virtual resistance concept in the main loop to damp the output voltage oscillations. Fig. 9 shows the closed loop converter's complete circuit.

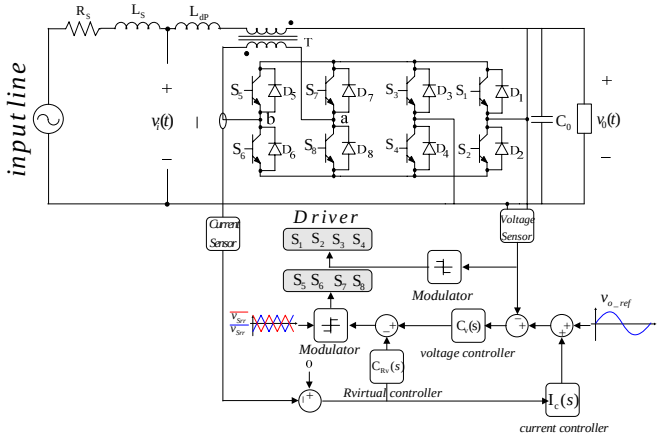


Fig. 9 – Converter's control circuits.

A. Main Loop: Voltage Control

Classical control techniques state that the variable that is to be directly controlled is fed back by means of a sensor and is compared to a reference signal. The error signal is then compensated using proportional, integral and derivative compensators, or a combination of those as shown in the block diagram of Fig. 10. Good results are achieved both in terms of dynamic response and in terms of the output voltage quality [6, 7]. The careful modeling of the plant becomes necessary. Further computer simulations are performed to check the system stability against unknown system parameters such as the line impedance at the input of the line conditioner.

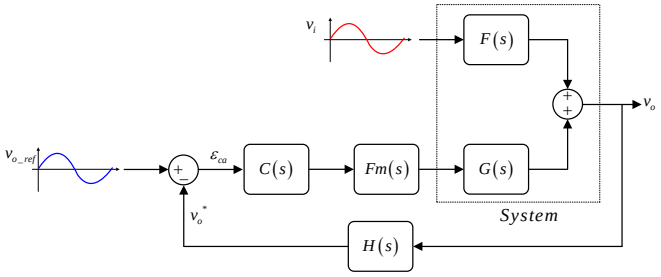


Fig. 10 – Block diagram of the control using the classical method.

The voltage compensator design is done using the classical methodology for the Buck and Forward converters with a PID type compensator. The choice of the crossover frequency is important to avoid instabilities in the closed loop operation of the converter, and so a good phase margin must be guaranteed in the ideal system.

To generate the sinusoidal reference a microcontroller was used in order to facilitate the synchronization procedure that must be performed between the input and output voltages of the converter. Another advantage of digitally implementing the reference signal is the possibility of adjusting its frequency according to small variations in the line frequency.

B. Second Loop: Current Control

The current control loop aims to eliminate the mean voltage values in the *T* transformer, without interfering in the voltage loop. This control is used to avoid the core transformer saturation and to protect the system from modulator or switch faults that cause the voltage loop to saturate.

The control is implemented by monitoring the transformer's current and comparing it to a null reference. The error signal is compensated using a proportional and integral compensator *PI* with crossover frequency around ten times smaller than line frequency to avoid interfering with the working structure. In *PI* controller the output has a *dc* signal that aims to compensate the mean voltage in the transformer. This signal is summed to the voltage loop, causing mean voltage level on the inverter output. Fig. 11 shows the block diagram of the current control.

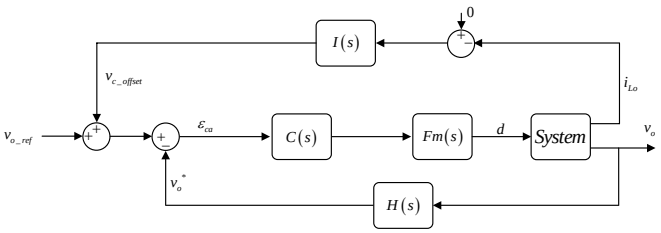


Fig. 11 – Block diagram of the voltage and current control.

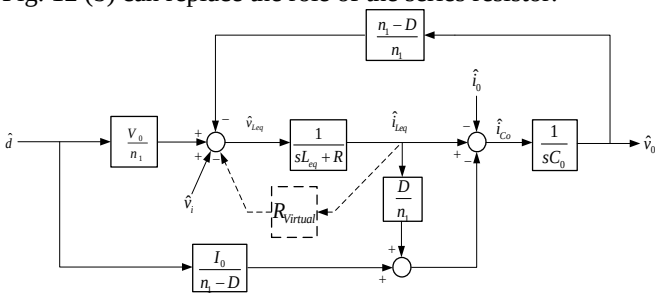
C. Last Loop: Virtual Resistance Control

In normal operation, the conditioner needs a robust and fast dynamic response. In [8], [9] and [10] the virtual capacitor and resistance concepts incorporated in current control loop for a *dc-dc* converter are studied. Virtual capacitor or resistor is a control algorithm that changes the system behavior into the one that has a capacitor or resistor connected to it. A virtual capacitor is used to ensure that the steady-state error of the output current is zero. A virtual

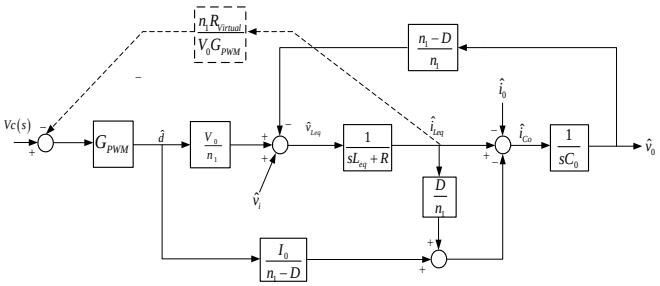
resistor is used to damp overshoot and oscillation in the output filter. How the virtual capacitor and virtual resistor are connected to the circuit will determine how the technique is carried out.

This work presents only the use of a virtual resistance, which can be connected in different ways. While oscillations can be damped effectively by using a real resistor, the power loss will prohibit the application of this method. Thus, a resistor with no power loss is needed.

Fig. 12 (a) shows the block diagram that represents the system when a virtual resistor is connected in series to the output inductive filter (L_{dp} and L_S). It can be noted that the role of the resistor is to reduce the voltage across the filter proportionally to the current through it. The resistance of the series resistor desired determines the proportional gain RVirtual. Using circuit theory a virtual resistor as shown in Fig. 12 (b) can replace the role of the series resistor.



(a)



(b)

Fig. 12 – Development of virtual resistor that is connected in series to the inductive output filter.

The effect of R in the circuit is the same of the virtual resistance $R_{Virtual}$, reducing the voltage across the filter. Thus, the expression of $G(s)$ and $F(s)$ remain unaltered, only replacing the R value by the $R_{Virtual}$ value.

VI. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

A. *Converter specifications*

The following parameters characterized the implemented conditioner:

- V_i = 220 ± 20[V] – input voltage;
- V_o = 220[V] – output voltage;
- S_o = 10[kVA] – output power;
- F_r = 60[Hz] – *ac* mains frequency;
- F_S = 20[kHz] – commutation frequency;
- n_1 = 4 – *T*'s transforming ratio;
- L_{eq} = 150[μH], C_o = 20[μF] – output filter.

B. *Operation with load and input transient*

A +50% load transient was applied to the converter operating with linear load and the results are shown in Fig. 13. It is verified that the output voltage is quickly corrected, showing that the system is practically insensitive to load variations.

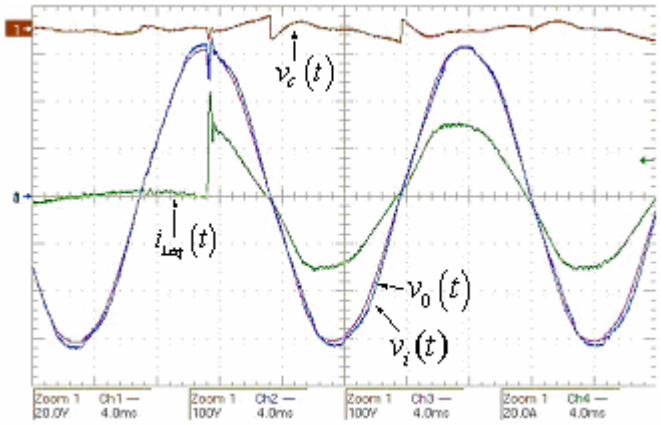


Fig. 13 – +50% load transient output voltage response.

Output voltage and control waveforms for a +20% and -20% transient in input voltage can be observed, respectively, in Fig. 14 and Fig. 15. In both situations, the converter corrects quickly the output voltage, maintaining it within safe values for the load.

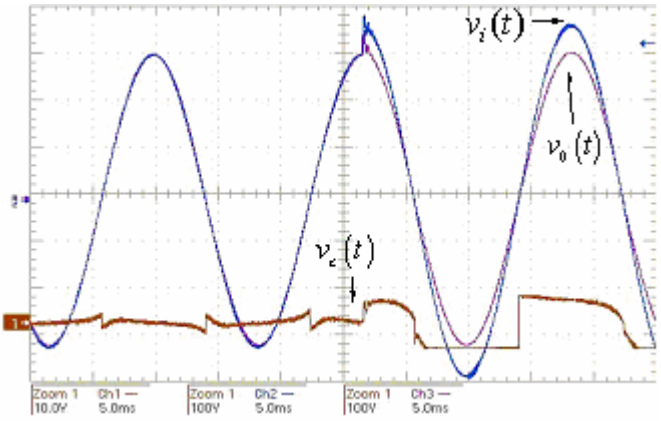


Fig. 14 – +20% input voltage transient output voltage response.

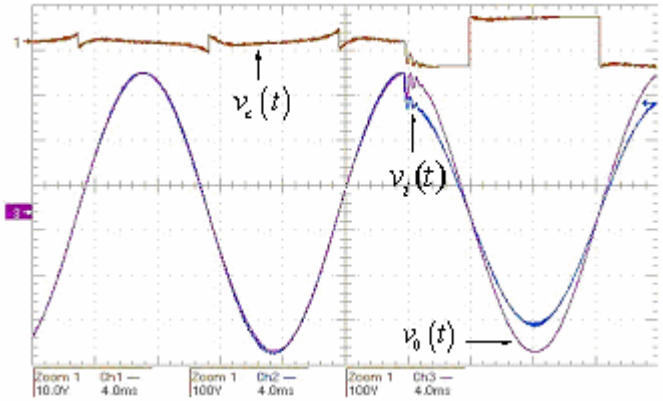


Fig. 15 – -20% input voltage transient output voltage response.

C. *Operation with non-linear load*

The greatest requirements in terms of dynamic response are with non-linear load operation.

To a non-linear load with crest factor of three, the output voltage, input current and control voltage waveforms are presented in Fig. 16. It can be observed that the output voltage is a sinusoid with a low harmonic distortion (3.7%). Then, the total harmonic distortion (THD) of the output voltage was below 5% and no harmonic component had a value larger than 3%, attending the limits of THD of the standard IEEE 519/92 [11].

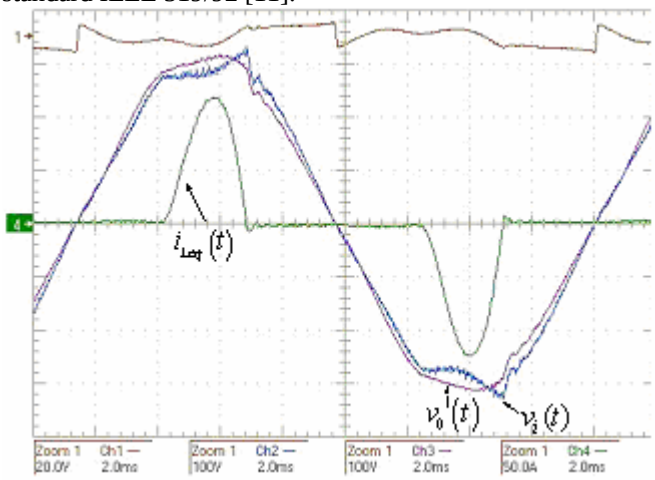


Fig. 16 – Operation with a non-linear load.

VII. CONCLUSIONS

This article studied a 10 kVA indirect line conditioner operating in closed loop and processing only a part of the total load power. The converter's operation, its characteristics, the modulation used and the system control in closed loop were presented.

The experimental results supported the optimal performance operating with a non-linear load and obtaining a sinusoidal output voltage with low harmonic distortion (3.7%). Despite the fact that the conditioner processes only part of the total load power, it presented an excellent efficiency, around 97%.

The voltage conditioner proposed presented close to instantaneous correction of the output voltage, faced to variations in the input voltage and in the load. The output voltage error for input voltage variations is lower than 0.5%.

Line voltage conditioners without power storage elements in the bus have direct coupling between inverter and rectifier, enhancing the problem of line impedance. Using the output voltage instantaneous control with classical controllers plus virtual resistance loop it was possible to impose an output voltage with the desired shape.

Therefore, the presented converter is appropriate for implementation in line voltage conditioners.

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