A BOOST CONVERTER TO IMPROVE THE LOW VOLTAGE RIDE-THROUGH CAPABILITY OF AN ADJUSTABLE SPEED DRIVE

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***Abstract* – This paper presents the application of a boost converter designed to improve the voltage sag ride through capability of an adjustable speed induction motor drive. The boost is a non isolated converter, 200W, 300V of dc output voltage and 150-300V of dc input voltage, operating in continuous conduction mode with average current mode control. The boost converter is added in parallel to a commercially available 220V 250W three-phase Adjustable Speed Drive (ASD), and details are discussed. The boost converter maintains the ASD dc bus voltage at 0.9 pu under voltage sag condition. The ASD low voltage ride-through has changed from 0.7pu to 0.5pu increasing the ASD supportability to voltage sags. Experimental results are presented, which show the effectiveness of the mitigation approach to voltage sags.**

***Keywords* - Adjustable speed drive, Boost converter, Low voltage ride-through capability, Voltage sag.**

I. INTRODUCTION

Adjustable Speed Drives (ASDs) are electronic equipment applied to control the speed of electric machines through the variation of the amplitude and frequency of the supply voltage. ASDs are used in a wide variety of industrial applications. The benefits that might be provided by the ASDs are the reason for their widespread use by the industry. Despite of its importance to the process operation, the ASDs are sensitive to voltage sags. Undervoltage and overcurrent often follow voltage sags which may cause the ASD trip bringing about the halt of the productive process and revenue losses. The ASD may also operate inappropriately resulting on load torque and load speed variations since the control of the current and of the output voltage are dependent on the inverter dc voltage level which decays during voltage sag [1], as shown in (1).

$$V_{dc} C \frac{dV_{dc}}{dt} = \frac{T_L \omega_r}{\eta_{mot} \eta_{inv}} \quad (1)$$

Thus, the decrease rate of the dc bus voltage dV_{dc}/dt depends on the capacitance C, the voltage V_{dc} across the capacitor at the beginning of the voltage sag, the load torque T_L, the motor speed ω_r, the motor efficiency η_{mot} and the ASD efficiency η_{asd}.

Several works related to the ASD performance evaluation under voltage sags have been published [2], [3], [4]. Different approaches to improve the ASD ride through by increasing the average voltage of the dc bus have been proposed [1], [5], [6], [7], [8]. The methods include the addition of capacitors to the dc bus [6], the regenerative mitigation which converts the kinetic energy from the motor and load into electric energy transferring it to the ASD dc bus [1], the connection of the neutral conductor of the supply source to the midpoint of the dc bus through a controlled switch [8], and the application of boost converters [1], [5], [7].

This paper presents a boost converter designed to improve the low voltage ride-through capability of an adjustable speed drive. The voltage sag mitigation based on a boost converter approach is evaluated and test bed results are presented for a system comprising a boost converter of 200W, a three-phase ASD of 250W and a three-phase induction motor of 0,25hp (186W), 60Hz, 220V. The system is tested under symmetrical and asymmetrical voltage sag conditions in order to assess the contribution of the boost converter to improve the ASD operation under voltage sags.

II. ASD VUNERABILITY TO VOLTAGE SAGS

The tolerance of an ASD to voltage sags depends on the characteristics of the voltage sag. Seven different types of voltage sags, classified as A, B, C, D, E, F, G, may come upon the terminals of an ASD as a result of symmetrical and asymmetrical faults. The voltage sags are classified according to the number of phases affected and the phase displacement, which are associated to the fault type. Table I presents the seven categories of voltage sags according to the fault type (3Φ-three phase fault, 1Φ-single phase fault, 2Φ-double phase fault, and 2Φ-G-double phase-to-ground fault) and as seen by the phase voltage and the line voltage terminals. The voltage sag type C* has the same pattern of the voltage sag type C [9]. Voltage sag type A is caused by symmetrical faults, whilst the remaining cases are due to asymmetrical faults.

TABLE I
The categories of voltage sag according to the fault type.

Voltage Type	Fault type						
	3Φ	1Φ	2Φ		2Φ-G		
	Voltage Sag Categories						
phase	A	B	C	D	E	F	G
line	A	C*	D	C	F	G	F

Voltage sag severities are normally measured by their magnitude and duration. The voltage sag magnitude is usually measured by the smallest rms voltage among the sagged phases, while the duration is often measured from the instant the rms voltage of any phase drops to less than 0.9 pu until no phase voltage is under 0.9 pu.

The drive is independent of line voltage sag as long as the dc bus holds up. During a voltage sag or short interruption, the diodes in an ASD rectifier bridge will not conduct if the peak line voltage drops below the dc bus voltage. While the ASD is still controlling the motor and its load, energy is

drawn from the dc-bus capacitors, which will cause the dc-bus voltage to decrease. When the dc-bus voltage drops below a pre defined set point before the line voltage returns, the control circuit will respond according to the drive's program, typically shutting down the drive. If the supply voltage recovers before the dc bus voltage reaches the under-voltage protection level, a high charging current is drawn from the supply which could end up in a shutdown of the drive, due to the activation of the over-current protection [1], [2].

The dc bus will typically trip on under voltage at an equivalent line voltage of 65% to 51% of nominal rated voltage and on over current between 1.3 and 1.5pu. The typical duration of voltage sags are between 0.5 to 30 cycles or 8ms to 0.5s.

Voltage sags, classified as type A, are the most severe ones as they cause the larger amount of energy withdraw from the dc bus, and are more likely to trip the ASD under voltage protection. The asymmetric voltage sags usually have at least one line supply voltage which keeps the dc link voltage above the under voltage protection level. Nevertheless, voltage sag type A is the least severe as far as the over current level is concerned. On the other hand, voltage sags type B, caused by one-phase faults, are accountable for the most severe sags as far as over current are concerned and the least severe as for the dc bus under voltage threshold level [5], [10]. It has been withdrawn from [5] that tests with voltage sag type A can set the under voltage protection level and tests with voltage sag type B can set the over current protection level of an ASD.

A. Voltage Sag Immunity Tests

Immunity to a disturbance is the ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance [11]. Voltage sag immunity test sets minimum immunity requirements for equipment response to voltage sags. Testing procedures for evaluating equipment sensitivity to voltage sags are specified in IEC standards 61000-4-34 [11] and 61000-4-11 [12]. Immunity is specified in terms of voltage sag depth (in percent of nominal voltage remaining during the sag) and voltage sag duration (in cycles or seconds).

Using a power disturbance source tests have been performed on a commercial three-phase ASD of 250W and 230V of nominal line voltage to determine how the drive would respond to voltage sags and short interruptions. The tests were conducted with the ASD under full load condition, and the ASD dc bus voltage was measured for different categories of applied voltage sags.

The power disturbance source is able to generate voltage sag types A (three-phase), B (one phase-to-neutral), and E (two phase-to-neutral) for what there are no phase-angle displacement during the voltage sag.

Voltage sag type A, B, and E are represented by the mathematical expressions given in Fig.1 as a function of the parameter h ($0 \le h \le 1$), whose value determines the voltage magnitude in pu and the phase-angle jump. The magnitudes of sag A, B and E are defined by h figure.

Type A	Type B	Type E
$V_a = h$	$V_a = h$	$V_a = 1$
$V_b = -\frac{1}{2}h - j\frac{\sqrt{3}}{2}h$	$V_b = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$	$V_b = -\frac{1}{2}h - j\frac{\sqrt{3}}{2}h$
$V_c = -\frac{1}{2}h + j\frac{\sqrt{3}}{2}h$	$V_c = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$	$V_c = -\frac{1}{2}h + j\frac{\sqrt{3}}{2}h$

Fig. 1. Equation form to voltage sags type A, B and E.

Fig. 2 shows the low-voltage ride-through of the ASD under voltage sags of type A, B and E. The ASD immunity response is compared with the SEMI F-47 0706 standard [13]. The SEMI F-47 curve sets minimum voltage sag immunity requirements for equipment used in the semiconductor industry. Immunity is specified in terms of voltage sag depth (in percent of nominal voltage remaining during the sag) and voltage sag duration (in cycles or seconds).

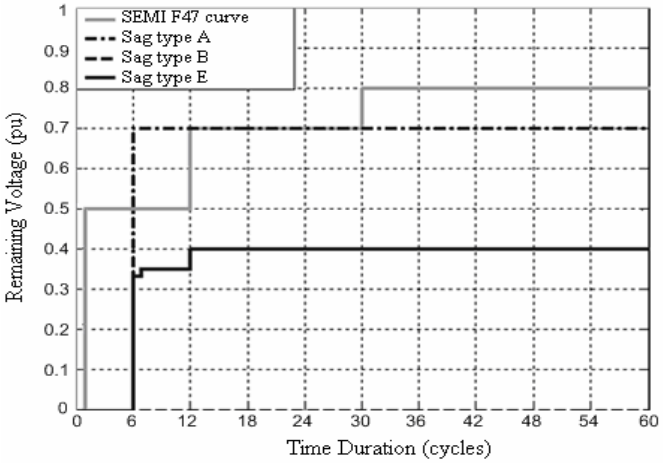

Fig. 2. Low voltage ride-through of the ASD under voltage sag types A, B, E compared with immunity requirements in SEMI F47.

According to the tests only voltage sags types A and E turn the ASD off. It can be observed in Fig.2 that the ASD under test can withstand voltage sag type A and E to 0pu during 6 cycles. However, the ASD does not comply the SEMI F47 standard for voltage sag type A between 6 and 12 cycles - whilst the SEMI F47 standard requires immunity to 0.5 pu the ASD voltage sag ride-through capability is to 0.7 pu.

Based on the ASD immunity test it has been concluded that the ASD can ride-through voltage sags type B even under permanent interruption condition, i.e., when one of the supply line voltages is 0pu. In addition, the ASD supply voltage threshold is 0.7pu to voltage sag type A and 0.4pu to voltage sag type E. For both conditions the dc-bus voltage reaches 0.7pu. Therefore, the immunity of the ASD under test to voltage sag is 0.7 pu.

B. ASD Performance under Voltage Sag

In order to evaluate the response of the dc bus voltage and the output voltage, voltage sags to 0.5pu type A and to 0pu type B and E have been applied to the ASD under test.

Fig. 3 shows the dc-bus voltage and the supply line voltages curves for a voltage sag type A to 0.5pu. The dc link voltage decays until 0.7pu when the undervoltage protection

trips turning the ASD off and then the capacitor at the dc-bus stop discharging.

Fig. 4 shows the ASD ac-output voltage response to voltage sag type A to 0.5 pu. Note that the ac-output voltage follows the dc-bus voltage profile until around 100ms when the undervoltage protection reaches the trip threshold and then the ac-output voltage decays to zero. Only one phase-to-phase output voltage is depicted in Fig. 4 since the behaviour of the other two output voltages are similar.

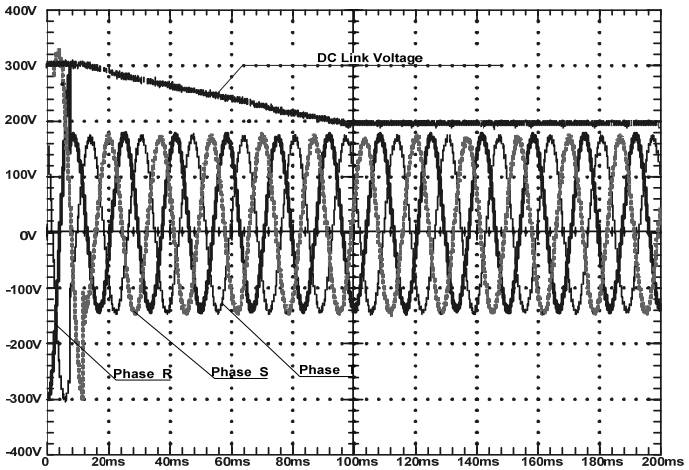

Fig. 3. The ASD three-phase supply voltages and the dc-bus voltage responses to voltage sag type A to 0.5pu.

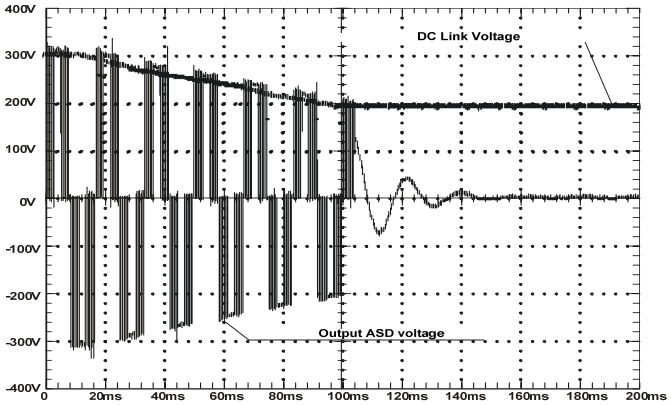

Fig. 4. The ASD output voltage and the dc-bus voltage responses to voltage sag type A to 0.5pu.

Likewise the ASD is tested under voltage sag type B and E to 0pu (short interruption) and the dc-voltage and ac-output voltage responses are evaluated.

Note that under steady state operation the voltage at the ASD dc bus is equal to the peak voltage of the supply line voltage ($V_{dc}=\sqrt{2}.V_{line}$). Therefore, the last row in Table I show the voltage sag type as seen by the dc bus when considering voltage sag phase-to-neutral applied to the ASD.

The ASD responses under voltage sag type B (phase-to-neutral) to 0V are depicted in Figs. 5 and 6. As a matter of fact, the line voltages shown in Fig. 5 represent a voltage sag type C, which means that one of the line voltages remains 1pu and the other two 0.58pu. As a result the dc bus does not drop under 0.95pu with the increase on the dc voltage ripple during the voltage sag. The voltage output shown in Fig.6 denotes that the ASD can ride-through the voltage sag.

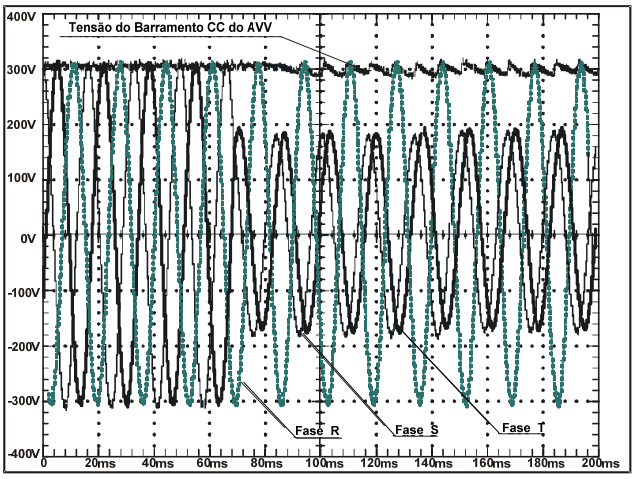

Fig. 5. The ASD three-phase supply voltages and the dc-bus voltage responses to voltage sag type B to 0pu.

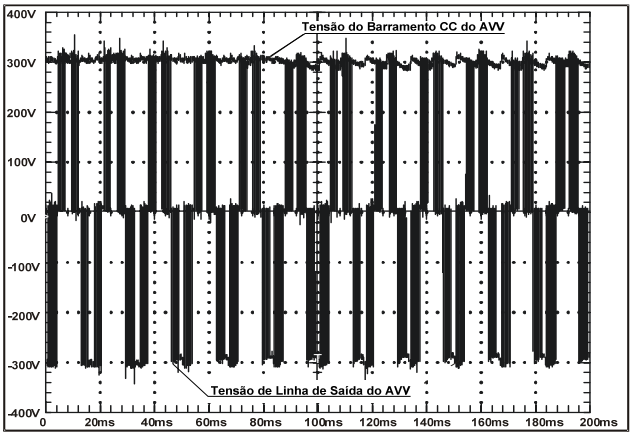

Fig. 6. The ASD output voltage and the dc-bus voltage response to voltage dip type B to 0pu.

For voltage sag type E to 0pu the dc-voltage and ac-output voltage responses are shown in Fig. 7 and 8.

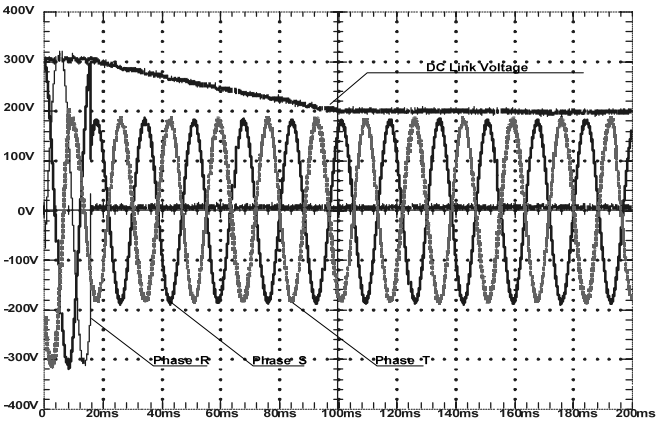

Fig. 7. The ASD three-phase supply voltage and the dc-bus voltage responses to voltage sag type E to 0pu.

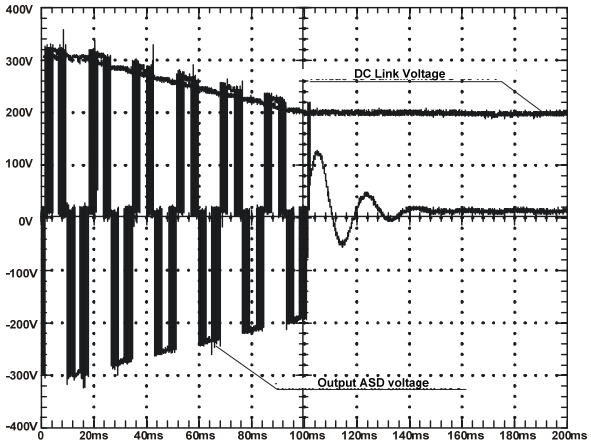

Fig. 8. The ASD output voltage and the dc-bus voltage response to voltage dip type E to 0pu.

The behavior of the ASD is similar to that under three-phase voltage sag. For voltage sag to 0pu type E lasting longer than 6 cycles the dc bus reaches the trip threshold at 0.7pu, then the ASD shuts down preventing the dc bus to discharge further.

It is worthy to note that although experimental tests have been performed to voltage sags type A, B, and E only due to the power disturbance source constraints as aforementioned, simulation tests have been carried out for all seven categories of voltage sag using the Orcad platform.

The simulation tests for the asymmetrical voltage sags type C, D, E, F and G have shown that for the worst voltage sag conditions (i.e., when h=0) the dc bus voltage has decayed to levels not smaller than 0.5pu [14].

Thus, the simulation and the bed test results have indicated that to improve the ASD ride-through capability to the worst condition of asymmetric voltage sag (h=0) and to symmetrical voltage sag to 0.5pu a mitigation approach should be provided.

III. MITIGATION STRATEGY TO IMPROVE THE ASD VOLTAGE SAG RIDE-THROUGH CAPABILITY

A boost converter is a power converter with an output dc voltage greater than its input dc voltage. The basic components of a boost converter are a dc power source, a boost inductor, a power switch, a boost diode and an output capacitor as depicted in Fig. 9. The dc power source may be a battery or a rectifier converter with a dc capacitor to smooth the boost dc voltage input.

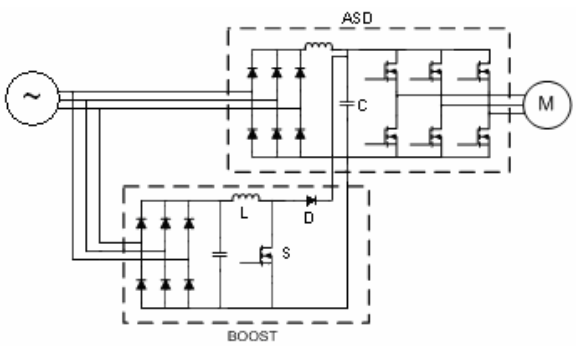

Fig. 9. The basic schematic of a non isolated boost converter.

The input of a boost converter has the feature of a current source due to the boost inductor in series with the supply source, and the boost output the characteristic of a voltage source because of the capacitor across the converter output.

A boost converter has been assembled to mitigate voltage sags up to 0.5pu. The boost converter operates whenever the ASD dc-bus voltage drops to under 0.95pu for a dc base voltage of 300V. The boost is 200W of rated power, connected in parallel to a 250W ASD that drives a 0.25 hp induction motor. All the energy to drive the load flows through the boost converter during the voltage sag.

The boost converter is supplied by the ASD supply source through a three-phase diode rectifier with a capacitor across the boost input. The diodes of the rectifier are 1N4007 with maximum current of 1A and maximum reverse voltage of 1000V and the input capacitor is 470µF.

The boost input voltage ranges between 150V and 300V and the output dc voltage is regulated to 300V. The output voltage of the boost converter has been pre-defined to be smaller than the nominal dc bus voltage (311V) of the ASD in order to assure a reverse biased boost diode during the steady state operation and therefore with no energy flow through the boost converter under this operation condition.

The boost inductance is equal to L=14mH and the inductor has 270 turns wounded on an E type ferrite core. The boost diode CSD0606 is an ultra-fast diode D with fast recovery, 6A and 600V of reverse voltage, and the transistor S is a SiC Mosfet IRFP350, 15A, 400V, with 40 kHz of switching frequency and variable duty cycle.

When applied to improve the ASD voltage sag ride-through capability the capacitor of the ASD dc bus is normally used as the *boost* output capacitor. Thus, by inspection it has been verified that the capacitance of the ASD is equal to C=330µF/400V.

The boost converter operates on continuous conduction mode (CCM) and the control is based on the average current control mode which is suitable to this application. In the CCM topology, there are two control loops called voltage loop and current loop in its transfer function as shown in Fig. 10. The inner loop in the dashed area corresponds to the current control loop whilst the outer loop represents the voltage control loop.

The control strategy provides an output voltage appropriate to the ASD dc bus. Although the boost diode rectifier unit draws high discontinuous currents in order to process the required power under reduced supply voltage, the current control prevents large input current variation that otherwise it might trip the overcurrent protection during voltage sag condition.

A boost converter based on the discontinuous conduction mode (DCM) although presents a lower cost, there is only one control loop, i.e. voltage loop, in its transferring control blocks, and its inherent high current ripple is not controlled.

The current and voltage control in closed loop were designed according to the stability criteria established by the switch mode power supply theory. The voltage control loop provides the reference to the current control loop. The voltage control has a cut–off frequency much smaller than that of the current control in order to take into account the

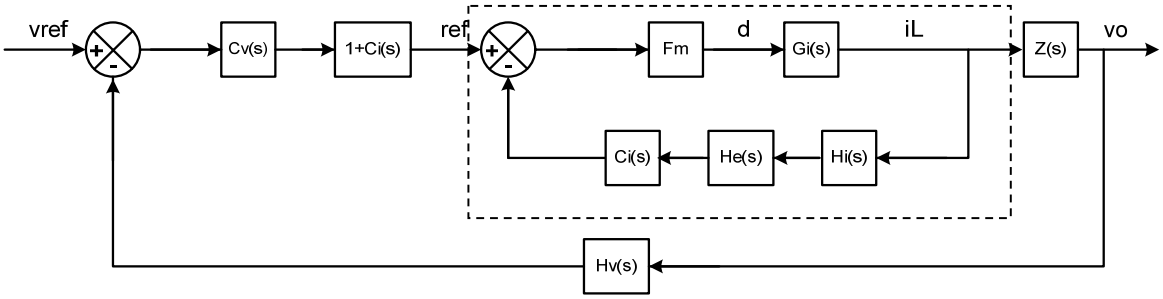

Fig. 10. The block diagram of the average current control mode.

load non linearity [15].

The implemented control strategy has proved to be suitable as far as the dynamic response of the boost converter, the immunity to noises, and the high gains to minimize the steady state error are concerned.

A. Evaluation of the Boost Converter Response

Experimental tests as described in the previous section have been carried out with the boost converter connected to the ASD dc-bus voltage. Voltage sags type A to 0.5pu and type E to 0pu have been applied to the ASD, and the dc-bus voltage and the ASD output voltage evaluated.

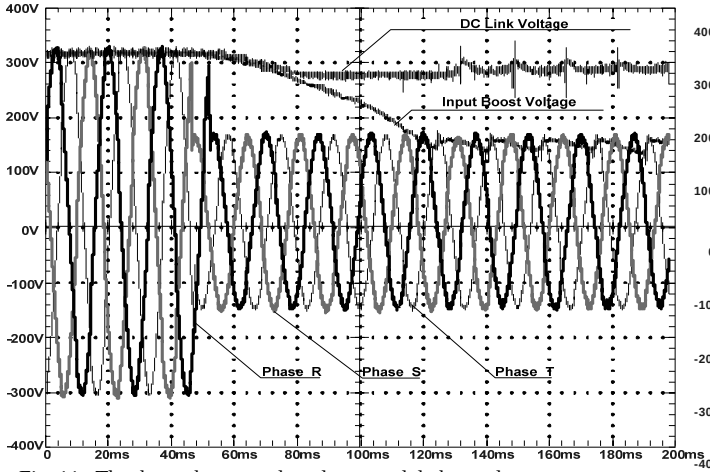

Fig. 11. The three-phase supply voltages and dc-bus voltage response to voltage sag type A to 0.5pu with the boost converter connected to the ASD.

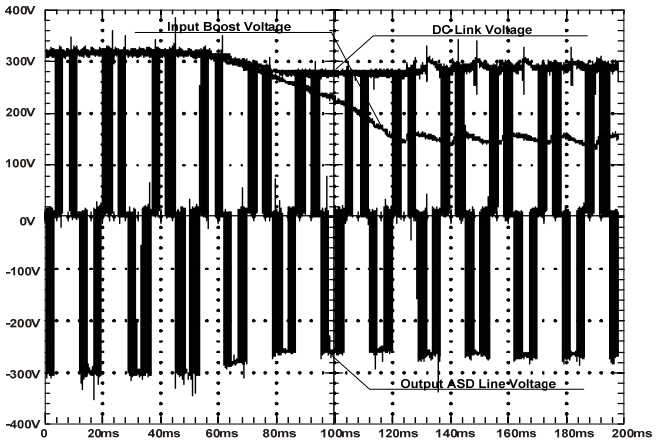

Fig. 12. The ASD output voltage and the dc-bus voltage response to voltage sag type A to 0.5pu with the boost converter connected to the ASD.

When comparing Figs 11 and 12 to Figs 3 and 4, respectively, it can be observed that although the ac-supply voltages and the boost dc-input voltage are below the ASD ride-through capability the dc-bus voltage of the ASD is kept above the trip threshold and the rms output voltage is sustained in 0.94pu.

Test results for the voltage sag to 0pu type E are presented in Figs 13 and 14. Although one of the supply line voltages is 0pu during the voltage sag the dc-input voltage of the boost converter decays to and follows the profile of the ac supply voltages whilst the boost output dc-bus (or the ASD dc-link voltage) is kept above the trip threshold (0.7pu) and the ASD keeps running as it can be seen by the ASD output voltage.

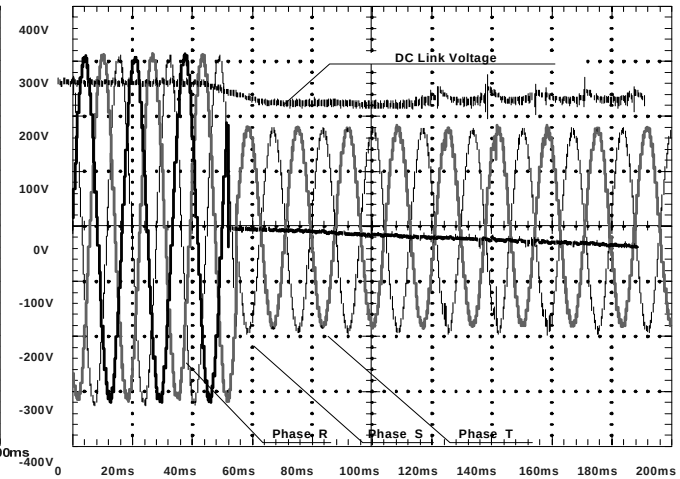

Fig. 13. The three-phase supply voltages and the dc-bus voltage response to voltage sag to 0pu type E with the boost converter connected to the ASD.

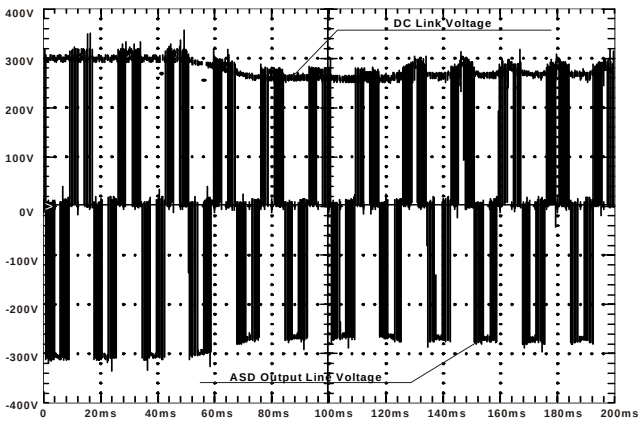

Fig. 14. The ASD output voltage and the dc-bus voltage response to voltage dip type E to 0pu with the boost converter connected to the ASD.

IV. CONCLUSIONS

A boost converter has been designed and implemented to improve the voltage sag ride-through capability of a three-phase adjustable speed induction motor drive. Voltage sag immunity tests have been performed in the ASD and it has been found that the ASD undervoltage protection threshold is equal to 0.7pu.

Test bed results have been presented which show that the boost converter designed to improve the dc-bus voltage threshold from 0.7 pu to 0.5 pu has performed accordingly.

The boost converter maintains the ASD dc bus voltage at 0.95pu to all asymmetric voltage sag events covered by SEMI F47, including total loss of a single phase, with no limitation of the event duration. The boost will also maintain the ASD dc bus voltage at 0.95pu for a permanent symmetrical sag in all three input phases to 0.5pu. Besides, the boost converter can prevent overcurrent under voltage sag condition and as a result the trip of the overcurrent protection. This approach provides ride-through to critical ASD load during voltage sags without any additional energy storage device.

The addition of capacitors to the dc bus of the ASD and also the connection of the neutral conductor of the supply source to the midpoint of the dc bus have been also pointed out as alternative solutions to improve the ASD low voltage ride-through capability. Although the cost of the capacitor addition method is alike to the boost converter alternative the major difficulty is the limitation of the voltage sag duration by the former. The neutral connection on the other hand is a simple solution as long as the neutral points of the supply source and of the ASD dc bus midpoint are accessible. The mitigation nevertheless is limited to 15% increase in the dc-bus voltage threshold.

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