A CONVERTER EMBEDDED AC MAINS VOLTAGE QUALITY ANALYZER

Marco A. de Oliveira, Fernando O. Martinz, Wilson Komatsu, Mauricio Galassi, Lourenço Matakas Jr.
Escola Politécnica da Universidade de São Paulo – Depto. de Eng. de Energia e Automação Elétricas
Av. Prof. Luciano Gualberto, travessa 3 , 158 – CEP 05508-900 – São Paulo - SP - Brazil
wilsonk@usp.br, mauricio.galassi@poli.usp.br

Abstract – **Power electronics converters connected to the AC mains are subjected to voltage disturbances which may cause malfunctioning and operation failures. This paper proposes an AC mains voltage quality analyzer using the existing converter voltage sensors and DSP microprocessor. The purpose is to perform an early diagnosis on the AC mains voltage quality before starting the converter, also with the possibility of doing such diagnosis periodically during the normal converter operation. The analyzer applies three-phase dot product based phase locked loops synchronized on both positive and negative sequences of the mains. Simulation and experimental results are presented in order to validate the proposed system.**

Keywords **– DSP based converter control, Voltage quality analyzer, PLL.**

I. INTRODUCTION

Power electronic converters connected to the AC mains are subjected to malfunctions and failures depending on the mains voltage quality. Usually in an installation start-up procedure one applies dedicated equipment such as multimeters, oscilloscopes and power quality analyzers in order to verify the sanity of the mains and its phase sequence before connecting the equipment. Moreover, after the installation, subsequent AC faults like phase loss, phase sequence inversion and unbalance between phases keep undetected and can lead to operation problems.

The purpose of this paper is to present an AC mains voltage quality analyzer which can employ a DSP (digital signal processor) already present in the converter in order to measure the voltage quality of the mains. This analyzer applies a three-phase PLL (phase locked loop) algorithm based on a dot product [1] to detect the mains phase sequence, phase loss and phase unbalance. The proposed system is presented and explained, and results from simulation and experimental setup are presented to validate the system.

II. PROPOSED ANALYZER OPERATION

The PLL shown in Figures 1 and 2 is based on the dot product of the mains voltages and the VCO (voltage controlled oscillator) which are orthogonal between each other when the PLL is synchronized, resulting in zero mean value for the dot product [1]. As stated in [2], since the PLL closed loop has one integrator at the VCO and other at the PI controller, it is not necessary to filter the output of the dot product. Notice that in the case of Figure 1 the synchronization sequence is RST, which is orthogonal to the ABC sequence generated by the VCO, and considered as the positive sequence in this work. If one changes the sequence generated inside the VCO block the synchronization occurs with the negative sequence as in Figure 2. It also shall be noted that in Figures 1 and 2 an additional normalization gain is required in the control loop to keep the PLL insensitive to mains voltage variations [1].

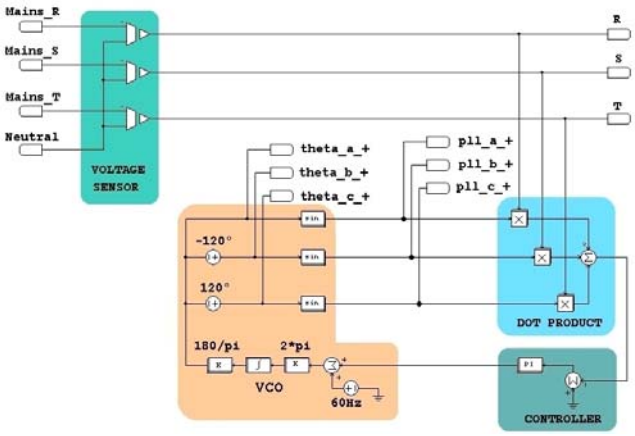

Fig. 1. Proposed three-phase PLL structure, drawn in the graphic environment of the PSIM software. This PLL synchronizes with the positive sequence and is called *PLL(+)* block in this paper.

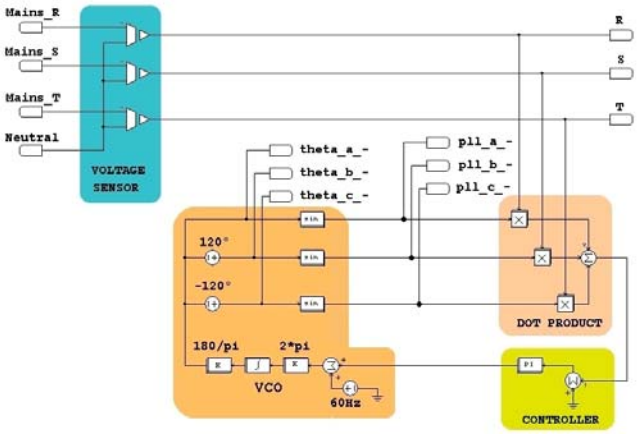

Fig. 2. Proposed three-phase PLL structure, drawn in the graphic environment of the PSIM software. This PLL synchronizes with the negative sequence and is called *PLL(-)* block in this paper.

Figure 3 shows a diagram block implementation for the proposed analyzer. Mains three-phase voltages are fed to both *PLL(+)* and *PLL(-)* blocks, which in their turn synchronize with the positive and negative sequences present in the mains, respectively. In this particular implementation of the PLL the instantaneous values of the angles for each

phase (*theta_a_+*, *theta_b_+*, *theta_c_+* for the *PLL(+)* block and *theta_a_-*, *theta_b_-*, *theta_c_-* for the *PLL(-)* block), generated within the VCO block, are available as seen in Figures 1 and 2. These instantaneous angle values will be transformed to a three-phase system with unitary phase peak value (1 p.u.) per phase and processed with the mains voltage inside the *Dot Product* block of Figure 4. If, for instance, there are only positive sequence voltages in the mains (RST sequence in this analysis), the *PLL(+)* block will synchronize with them and the resulting angles *theta_a_+*, *theta_b_+* and *theta_c_+* (with an abc sequence) submitted to the cosine function will generate three-phase sinusoidal voltages synchronized and in phase with the positive sequence present in the mains. It is important to observe in Figures 1 and 2 that the sine function is applied, instead of the cosine function of Figure 4. In the first case, PLL lock is achieved when instantaneous PLL generated voltages are orthogonal to the mains voltages, resulting in a null dot product [1]. As the PLL is locked, the objective of the dot product block of Figure 4 is to obtain information about the voltages that are in phase with mains positive or negative sequence. The dot product between the *Dot Product* block generated voltages and the mains results in a mean value of 3/2 of the phase peak value of the positive or negative sequence of the mains. By filtering it with a LPF (low pass filter) and multiplying with 2/3, one obtains the phase peak value of the positive sequence at the output PP. The LPF must be implemented to attenuate oscillating components of the dot product which appear, for instance, when harmonics are present in the mains voltages [1],[2]. In the same way, one can take the sequence *theta_a_+*, *theta_c_+* and *theta_b_+* (now with a negative sequence acb) and the mains thru the *Dot Product* block to detect any negative sequence present in the mains and put it in the PN output . In order to address a possible phase sequence inversion, one can run a PLL locked to the mains negative sequence (*PLL(-)* block) and perform an operation between its outputs *theta_a_-*, *theta_b_-* and *theta_c_-* at the two *Dot Product* blocks (one with a phase sequence abc and the other with acb) with the mains, getting NP and NN outputs respectively in this operation.

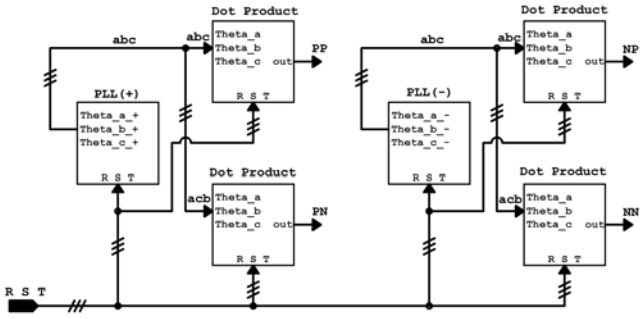

Fig. 3. Block diagram of the implementation for the proposed analyzer.

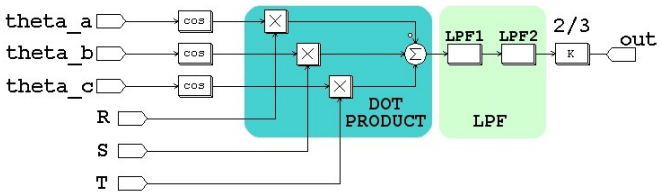

Fig. 4. *Dot Product* block, drawn in the graphic environment of the PSIM software.

In the implementation of the *Dot Product* block for this work, the LPF was implemented with two cascaded first-order filters:

$$f(s) = \frac{1}{0.1s + 1} \qquad (1)$$

Figure 5 shows a possible flowchart for a diagnosis system embedded in a power electronics converter.

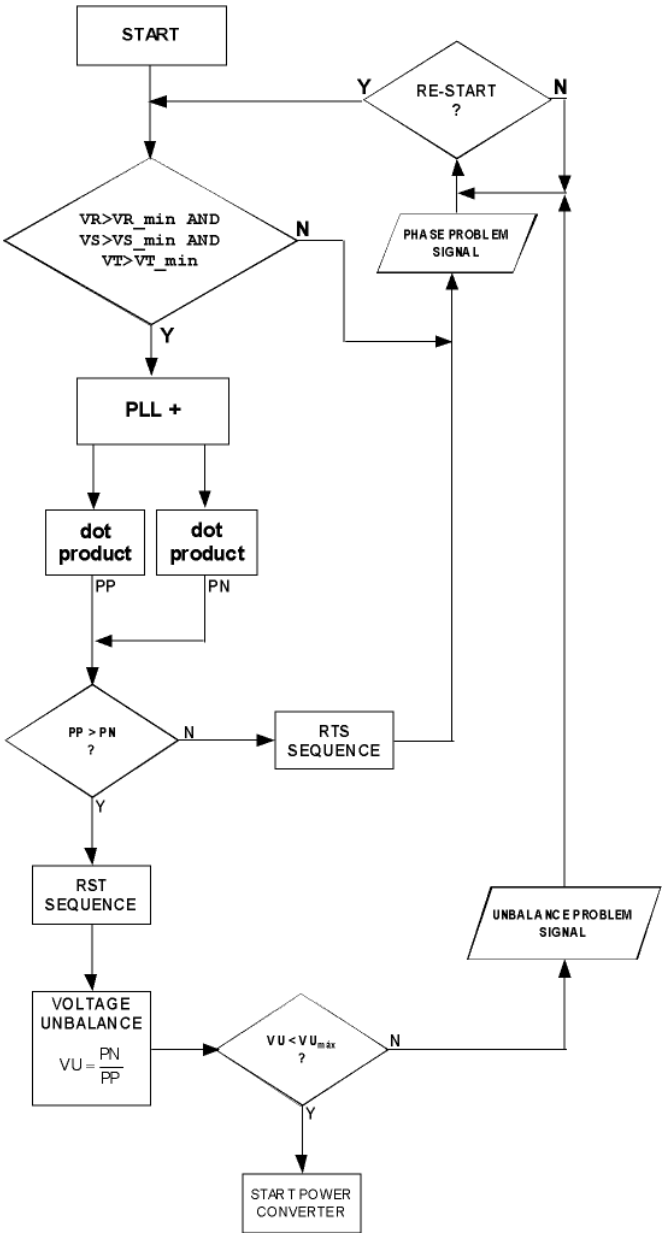

Fig. 5. Flowchart of a possible implementation of the proposed analyzer.

In the particular implementation shown in Figure 5, the phase loss is detected by measuring the phase voltage amplitudes before running the PLL block, in this case only the *PLL(+)* block. Phase loss (or their values below a certain level) and inversion of phase sequence are detected as "Phase Problem", and phase unbalance above limits is detected as "Unbalance Problem", and both problems forbid the operation of the power converter until the problems are solved. Possible variations on this flowchart can include the synchronization with the negative sequence by using the *PLL(-)* block, automatic change of phases in case of detection of phase sequence inversion, definitions of warning and error levels for phase voltages and unbalance etc.

III. SIMULATION RESULTS

The analyzer proposed in Figure 3 was implemented in the PSIM simulation software and six representative cases (from A to F of Table I) were run to verify the system behavior. The proportional and integral gains of the PI controller (ISA model) were 0.5 and 1000, respectively.

A three-phase generator was implemented in the simulation software and allowed simultaneous and independent generation of both positive and negative sequences, as well as harmonics.

TABLE I
Description of test cases ran on the system of Figure 3 with the PSIM simulation software and their corresponding results

CASES	DESCRIPTION	PP (p.u.)	PN (p.u.)	NP (p.u.)	NN (p.u.)
A	Positive Sequence (PS) = 1 p.u.	1	0	0	0
B	Negative Sequence (NS) = 1 p.u.	0	0	1	0
C	PS = 1 p.u., NS = 0.35 p.u., 5th Harm. = 0.2 p.u.	1	0,35	0,35	1
D	PS = 0.35 p.u., NS = 1 p.u., 5th Harm. = 0.2 p.u.	0,35	1	1	0,35
E	PS (R = 1 p.u., S = 0.6 p.u., T = 1 p.u.)	0,86	0,63	0,14	0,43
F	PS (R = 1 p.u., S = 0 p.u., T = 1 p.u.)	0,70	0,16	0,34	0,35

Reference [3] defines the expression of the voltage unbalance factor in equation (2):

$$\%\mathrm{VUF} = \frac{\text{Negative sequence voltage component}}{\text{Positive sequence voltage component}} \times 100 \quad (2)$$

In order to clarify the implementation of the test cases, one can explain that, for instance, Case C was run from a mains generator delivering the sum of a positive sequence three-phase system with 1 p.u. peak value, a negative sequence three-phase system with 0.35 p.u. peak value, and a 5th harmonic of the positive sequence with 0.2 p.u. peak value (figure 6). Case E was run from a mains generator with phases R and T at 1 p.u. peak values and phase S with 0.6 p.u. peak value. One can remember that the classical Fortescue symmetrical components equation [4] clearly relates asymmetry of phase values with the generation of zero sequence voltage (V_0) voltage, positive sequence voltage (V_1) and negative sequence voltage (V_2) at the fundamental frequency:

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \times \begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (3)$$

In (3) the operators $\alpha = 1\angle 120°$ and $\alpha^2 = 1\angle -120°$ are defined and applied. By using (3), one can see that negative sequence voltages can be generated either with phase values asymmetry or with independent generation of complete three-phase systems running simultaneously at positive and negative sequences. Both ways were applied in these simulation test cases.

Case A: A three-phase mains with RST (positive) sequence and 1 p.u. phase peak value was applied at the proposed analyzer. PP output value indicates that *PLL(+)* block is synchronized with the mains. As there is no negative sequence here, all other outputs have null values as expected.

Case B: Mains generator has only negative sequence generation, consequently synchronizing the *PLL(-)* block and exhibiting output NP with 1 p.u. phase peak value. All other outputs have null values.

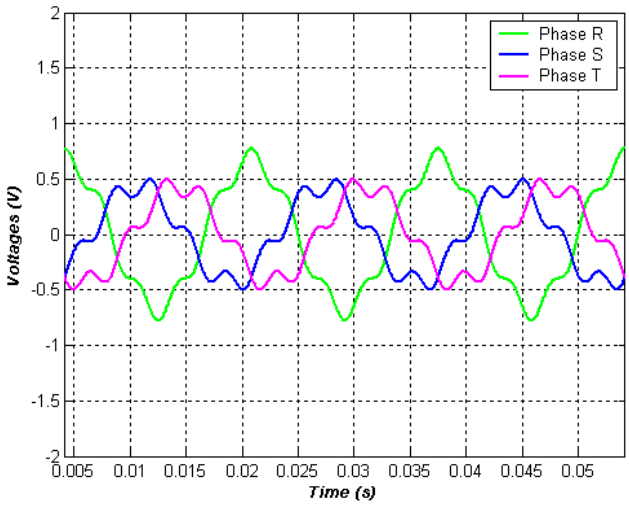

Fig. 6. Case C simulated voltages with positive sequence (1 p.u.), negative sequence (0.35 p.u.) and 5th (0.2 p.u.). Phase R (green), phase S (blue) and phase T (magenta).

Case C: Mains generator delivers the sum of a positive sequence three-phase system with 1 p.u. peak value (500mV in PSIM simulation), a negative sequence three-phase system with 0.35 p.u. peak value, and a 5th harmonic of the positive sequence with 0.2 p.u. peak value (Figure 6). All outputs (PP, PN, NP e NN) exhibit non-zero values, indicating synchronization of both *PLL(+)* and *PLL(-)* blocks. The outputs indicate coherence with the input signals. The harmonic content is filtered by the LFP of the *Dot Product* blocks, as it has zero mean value. Measurement of harmonic content can be done by comparing the RMS values of both voltages, one including harmonics, positive and negative sequences and the other with only the positive sequence, and

taking a decision when the difference is higher than a given level.

Case D: Same as in Case C, but with the inversion of positive and negative sequence generator values. Because of it, the outputs present symmetrically changed values.

Case E: Mains generator with phases R and T at 1 p.u. peak values and phase S with 0.6 p.u. peak value. The results from Table I can be analyzed by applying (3) at the mains voltages:

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \times \begin{bmatrix} 1\angle 0° \\ 0.6\angle -120° \\ 1\angle 120° \end{bmatrix} \quad (4)$$

$$\text{Resulting in} \quad \begin{aligned} V_0 &= 0.13\angle 60° \ \text{p.u.} \\ V_1 &= 0.87\angle 0° \ \text{p.u.} \\ V_2 &= 0.13\angle -60° \ \text{p.u.} \end{aligned} \quad (4.1)$$

One can see that the output NP from Table I corresponds to V_2 and V_1 is present at output PP.

Case F: Three-phase mains without phase S. Application of (3) for this situation leads to:

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \times \begin{bmatrix} 1\angle 0° \\ 0 \\ 1\angle 120° \end{bmatrix} \quad (5)$$

$$\text{Resulting in} \quad \begin{aligned} V_0 &= 0.33\angle 60° \ \text{p.u.} \\ V_1 &= 0.67\angle 0° \ \text{p.u.} \\ V_2 &= 0.33\angle -60° \ \text{p.u.} \end{aligned} \quad (5.1)$$

The difference between values of V_1 from Table 1 and from (5.1) just indicates that in the simulation of Case F it was not given enough (simulation) time to reach steady state.

The drawback of this method is that it is not possible to distinguish if the mains voltages are unbalanced or if there is a phase absence. A better strategy, shown in Figure 5, consists in detecting phase loss directly from phase voltages monitoring, instead of depending on the posterior processing at the analyzer, since these measurements are already available from voltage sensors. The analyzer can be programmed to take decisions, such as disconnecting the power converter from the mains, if the voltage unbalance is higher than a certain level, a phase is missing or if there is a phase sequence inversion.

One can notice that the proposed implementation does not measure individual harmonic levels, as it does not run a FFT (or similar) algorithm, but as the positive and negative sequence voltages are obtained, total harmonic distortion levels can be calculated based on its definition [5] by applying measured RMS voltage and RMS value of PP output.

Figure 7 shows Case C simulation at the PSIM software starting from zero value conditions. One can clearly see that output signals (PP, PN, NP, NN) are converging to the values of Case C at Table I. In a real situation, one has to wait until the transitory state is over in order to process the algorithm and get the results. This time depends on the dynamic of the filters used at the *Dot Product* blocks, as well as on the dynamic of the PLL tracking behavior, which depends, among other factors, on the dynamic of the PI controller [1].

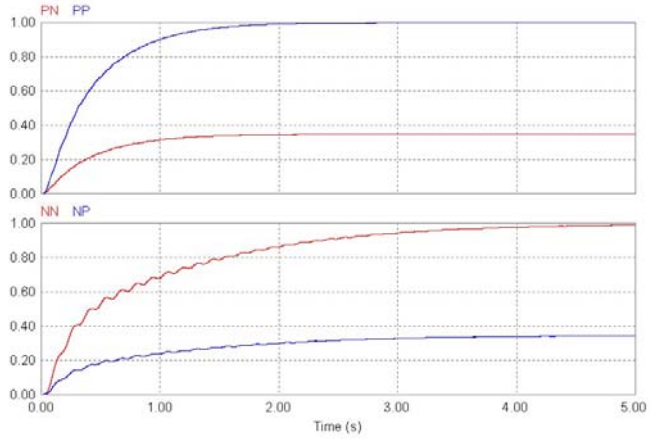

Fig. 7. Transitory behavior for Case C simulation with PSIM software starting from null value conditions.

IV. EXPERIMENTAL RESULTS

Experimental results were obtained from an assembly including a three-phase signal generator with variable frequency, harmonics inclusion and voltage unbalance capabilities [6]. The proposed analyzer from Figure 3 was implemented in the DSP development kit EZ-KIT-ADSP-21992 from Analog Devices.

Fig. 8. Case C generated voltage with positive sequence (1 p.u.), negative sequence (0.35 p.u.) and 5th (0.2 p.u.). Phase R (green), phase S (blue) and phase T (magenta). Scales: 0.5 V/div and 5 ms/div.

Figure 8 shows three-phase generated phase voltages including distortions, referring to Case C. All outputs were obtained directly from the DA (digital/analog) output of the DSP, and are affected with a 1V offset.

Figure 9 shows the resulting output voltages PP, PN, NP and NN from the experimental setup. As can be seen, the positive sequence peak voltage is equal to 500 mV and the negative sequence peak voltage is 192.5 mV, corresponding to 35% of the positive sequence. One can verify that the experimental results agree closely with the simulation ones.

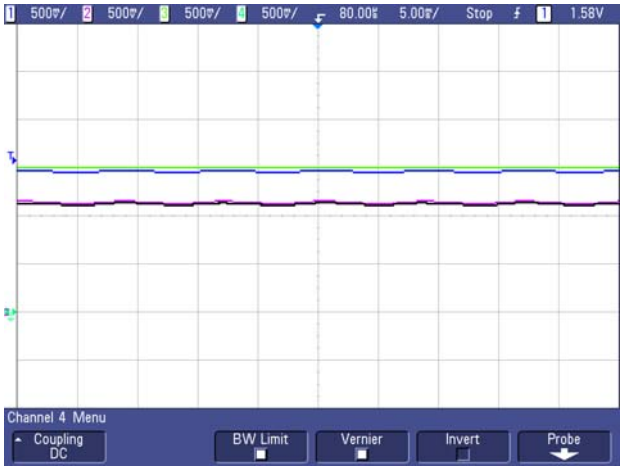

Fig. 9. Case C DSP generated outputs PP (green), PN (black), NP (red), NN (blue). Zero volts (discounting offset) appear at the central (middle) horizontal line. Scales: 0.5 V/div and 5 ms/div.

V. CONCLUSION

This paper has presented an AC mains voltage quality analyzer which employs existing voltage sensors and an embedded DSP intelligence of a digitally controlled power electronic converter connected to the mains. The purpose of this system is to perform an early diagnosis on the AC mains voltage quality before starting the converter, also with the possibility of doing such diagnosis periodically during the normal converter operation. The analyzer uses three-phase dot product based PLL loops that can be synchronized simultaneously on both positive and negative sequences of the mains. An implementation flowchart is also proposed, which detects and acts on previously established phase loss situations and levels of unbalance for this system.

Simulation and experimental results were presented, confirming the validation of the proposed system.

REFERENCES

[1] L. Matakas Jr., F. O. Martinz, A. R. Giaretta, M. Galassi, W. Komatsu, “Uma Abordagem Gráfica para um Algoritmo de PLL Baseado em Sequência Positiva”, *in Congresso Brasileiro de Automática*, pp. 2081-2086, 2006.

[2] V. Kaura, V. Blasko. Operation of a Phase Locked Loop System Under Distorted Utility Conditions, in *IEEE Transactions on Industry Applications*, Vol. 33, No. 1, pp. 58-63, Jan/Feb 1997.

[3] IEEE Std. 141-1993 “IEEE recommended practice for electric power distribution for industrial plants”.

[4] C. C. B. Oliveira, H. P. Schmidt, N. Kagan, E. J. Robba, *Introdução a sistemas Elétricos de Potência – Componentes Simétricas*, Edgard Blücher, 2ª edição, São Paulo, SP, Brasil, 2000.

[5] IEEE Std. 519-1992 “IEEE recommended practices and requirements for harmonic control in electrical power”.

[6] W. Komatsu, A. R. Giaretta, L. Matakas Jr., “A Didactic Microcontrolled Three-Phase Signal Generator”, *in Oitavo Congresso Brasileiro de Eletrônica de Potência (COBEP 2005)*, Vol. 1, pp. 169-174, 2005.