DESIGN AND IMPLEMENTATION OF A POWER CONTROL UNIT FOR THE SOLAR ARRAY OF THE ITASAT UNIVERSITY SATELLITE

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***Abstract* – This article describes the modeling, simulation, design and experimental results of a shunt regulator used in the power control unit (PCU) for the solar array of the ITASAT university satellite. The Sequential Switching Shunt Series Regulator (S^4R) topology with a microcontroller is used and simulation and experimental results are shown. The proposed solution is evaluated as suitable for its purposes.**

***Keywords* – Power Control Unit, Shunt Regulator, Shunt Series Regulator, Direct Energy Transfer, Satellite Power Supply.**

I. INTRODUCTION

The ITASAT university satellite has demanded research about several satellite subsystems, such as the power supply unit. Several spacecraft power subsystem architectures were studied, with special attention to the specific power requirements of this mission [2]. Some of these requirements are bus power and voltage, thermal control, reliability and availability of radiation hardened components. It was then decided to use solar energy by means of photovoltaic (PV) conversion as the primary energy source. To achieve that, several PV cells have to be stacked to form a large solar array (SA) and the array is divided into parallel circuits called strings. The SA will be assembled on the satellite body.

However, the satellite will not be illuminated all the time, so it is indispensable to store energy for eclipse and load peak periods. A rechargeable battery will be used to store the energy provided by the solar array.

In photovoltaic-battery systems the two main power control architectures are called Peak Power Tracking (PPT) and Direct Energy Transfer (DET) [7][8].

II. STUDY AND MODELING OF THE SHUNT REGULATOR

Two unregulated power supply units are shown in Figure 1, with a battery directly connected to the bus. In the PPT architecture, shown in Figure 1a, a series regulator is placed between the load and the SA. In the DET architecture, shown in Figure 1b, the energy from the solar array is directly transferred to the load and a shunt regulator (SR) is connected in parallel with the SA.

Figure 2 shows a switching shunt regulator without dissipative resistor. When the switch T is closed the solar array, Ip source, is short-circuited and the diode D prevents the load (RC circuit) to be also short-circuited. When the switch T is open the SA provides power to the load through the diode D. The switching frequency is controlled using the ripple of the output voltage. This method is called ripple control [6][9]. Another possibility is to use a microcontroller to command the switch T using pulse width modulation (PWM) with a fixed switching frequency.

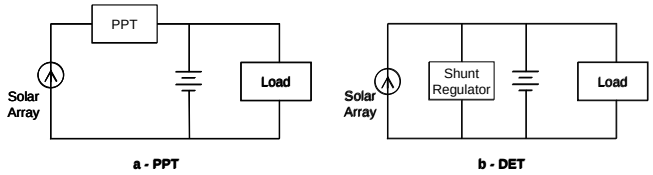

Fig. 1. Power control architectures: a) PPT, b) DET.

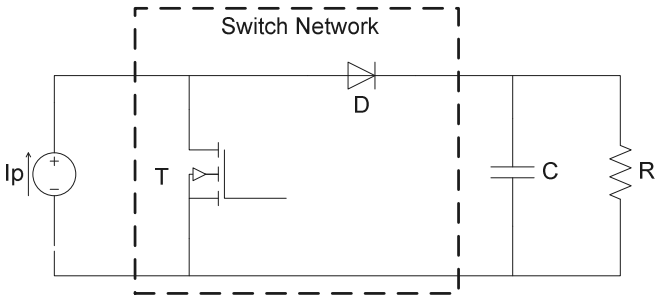

Fig. 2. A Switching Shunt Regulator without dissipative resistor.

The state-space averaging approach [3][4] was employed to model the SR. The control-to-output transfer function, the output and the input average voltage were obtained as follows:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{I_P R(1+sCr_C)}{1+sC(R+r_C)} = G_{vd}(s) \quad (1)$$

$$V_O = I_P R D \quad (2)$$

$$V_P = I_{Pcc} R_{on}(1-D) + D(V_D + I_P r_D + V_O) \quad (3)$$

where:

- $\hat{v}_o$ Output voltage perturbation, AC component,
- $\hat{d}$ Diode duty cycle perturbation, AC component,
- C Output capacitor,
- r_C Equivalent series resistance of the capacitor C,
- I_p Solar array average current,
- R Load,
- V_O Output average voltage, DC component,
- D Diode average duty cycle, DC component,

I_{pcc} Solar array short circuit current,
R_{on} Switch on resistance,
V_D Diode forward voltage,
r_D Diode forward resistance.

The non-linear devices shown in Figure 3, Switch Network, were modeled to allow AC simulations using the SPICE software. The values between "< >" are the averaged values for the switching period, d(t) is the diode duty cycle and d'(t) is the switch T duty cycle, d'(t) = 1 – d(t).

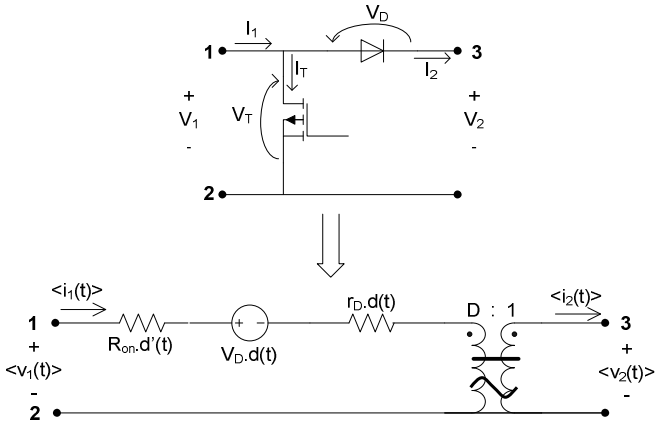

Fig. 3. Switch network model for the shunt regulator.

The analysis of SR model (1) shows that the steady-state error (4) would be 50% if the load, R, was the nominal value (R_{nom}) and the solar array was supplying exactly its nominal current, I_{pnom}, ($V_{O\_nom} = I_{pnom}.R_{nom}$).

$$e_{ss} = \frac{V_{O\_nom}}{V_{O\_nom} + I_p.R} \tag{4}$$

In this case, if output current feedback is added, Figure 4, a new transfer function is obtained (6) and the steady-state error becomes 0% (there is system pole at 0, an integrator).

$$\frac{V_O(s)}{e(s)} = G_i(s) = \frac{k_n.G_{vd}(s)}{1 - k_n.S_c.H_i.G_{vd}(s)} \tag{5}$$

$$V_d = V_{O\_nom} - I_p.R_{nom}$$

$$G_i(s) = \frac{I_p.R.V_{O\_nom}.(1 + s.C.R_C)}{V_d + s.C.\left[R.V_{O\_nom} + R_C.V_d\right)} \tag{6}$$

However, even with output current feedback, if the solar array current is not I_{pnom} the steady-state error (7) will not be zero ($V_{O\_nom} \neq I_p.R_{nom}$).

$$e_{ss} = \frac{V_{O\_nom} - I_p.R_{nom}}{V_{O\_nom} - I_p.R_{nom} + I_p.R} \tag{7}$$

Since the SA current and voltage values change with temperature, life time, angle, radiation and distance to the sun [5], a controller for the switch T is needed if a zero steady-state error is desired. A simple proportional and integral (PI) controller was used for that.

The SR models were simulated, without the PI controller and with nominal solar array current, using SPICE and MATLAB/SIMULINK software and these results were compared with the experimental results obtained in laboratory. Figure 4 shows the system block diagram used to model the current and voltage output feedback loops, where:

V_R Reference for the output voltage,
$e(s)$ Output voltage error,
H_i Current feedback gain, (R_{nom}/V_{O_nom}),
S_c Current sensor ($1/R$),
k_n PWM gain, convert voltage into pulse width,
H_v Voltage feedback gain, ($1/V_{O\_nom}$).

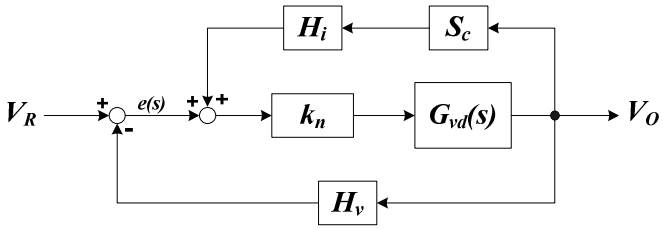

Fig. 4. Block diagram of SR control loop.

Figures 5 and 6 show the block diagram used in the SIMULINK software and the electrical schematic used for the frequency-domain analysis in the SPICE software. The parameters used were: I_{pnom} = 0,47 A, C = 780 uF, R_C = 65 mΩ, $R = R_{nom}$ = 29,79 Ω and V_{O_nom} = 14 V. A table with the values of voltage and current obtained from solar array simulator was used to simulate the solar array.

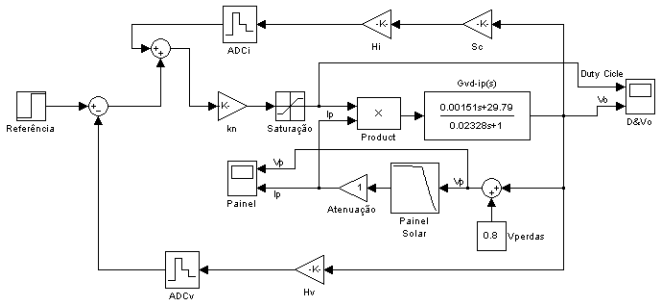

Fig. 5. Simulink block diagram.

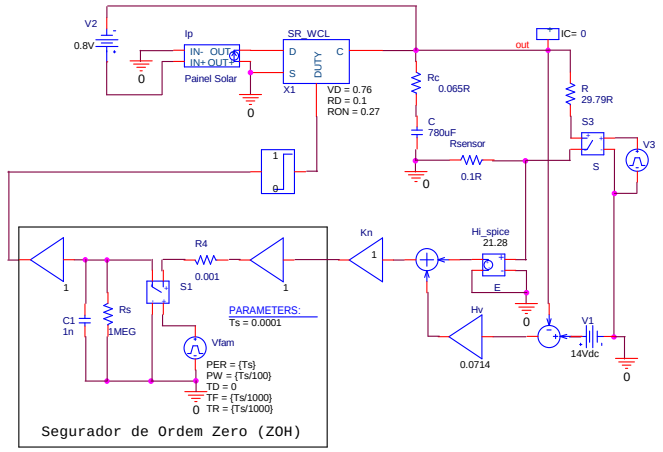

Fig. 6. Electrical circuit for frequency-domain analysis in SPICE.

Figure 7 shows the electrical circuit used to simulate the load step and other simulations in *switched mode* and to perform time-domain and DC analysis.

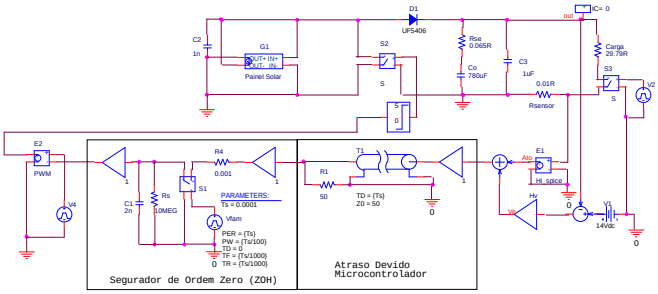

Fig. 7. Circuit for *Switched mode* simulation in SPICE.

III. EXPERIMENTAL AND SIMULATED RESULTS

The simulation results for the steady-state analysis of the SR with MATLAB and SPICE software and the experimental results are shown in Figures 8, 9 and 10 for the same resistive load. The output voltage ripple is shown in Figure 11. Every experiment was made using a solar array simulator (which has a similar static response to a real SA), a MC68HC908GP32 Freescale microcontroller, a IRLZ24N mosfets and a UF5402 diode. In the next figures, I_O is the output current.

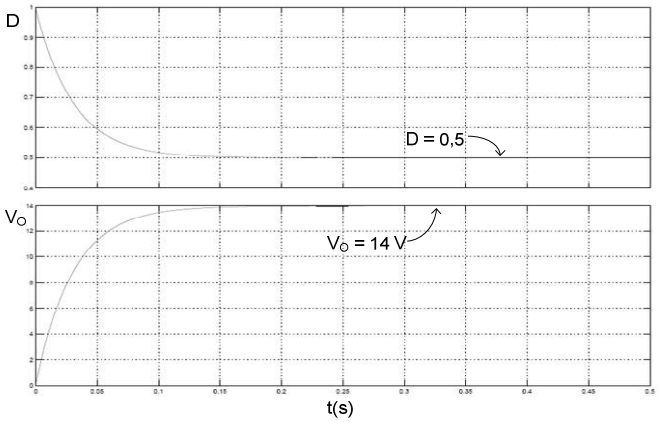

Fig. 8. MATLAB simulation results for I_O = 0,22 A: duty cycle and output voltage.

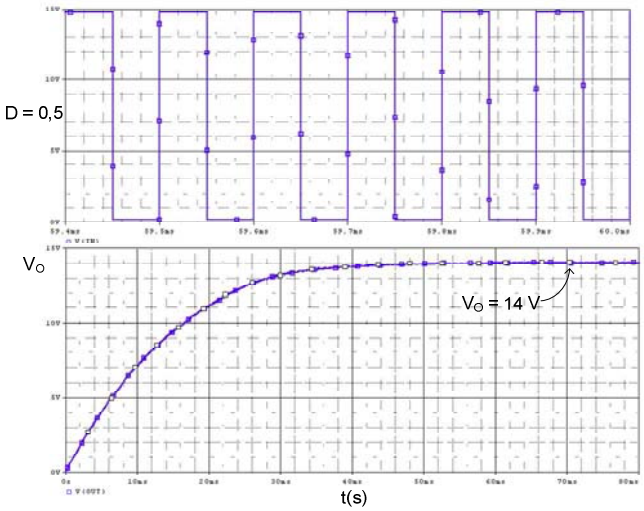

Fig. 9. SPICE simulation results for I_O = 0,22 A: duty cycle and output voltage.

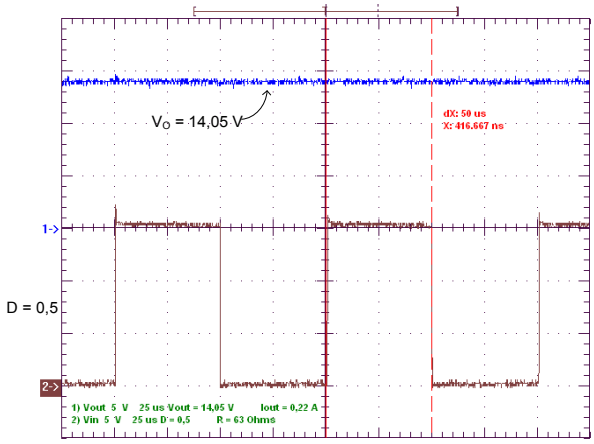

Fig. 10. Experimental results for I_O = 0,21 A: duty cycle and output voltage.

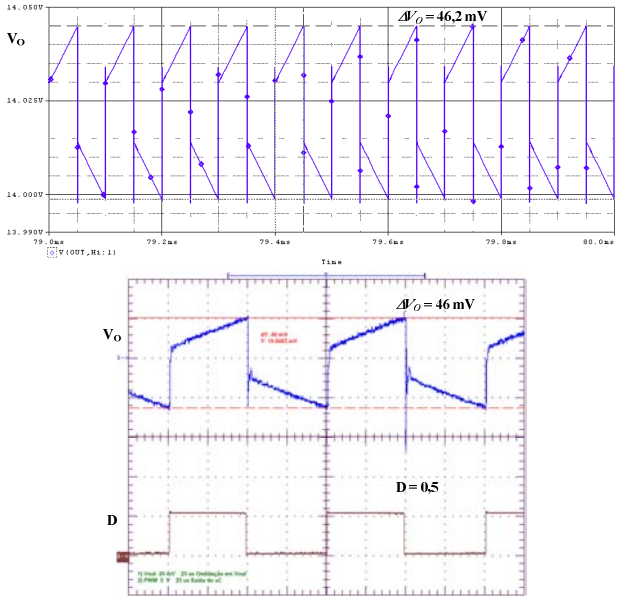

Fig. 11. Output voltage ripple.

The simulated and the experimental time response of the output voltage for the full load step are shown in figure 12.

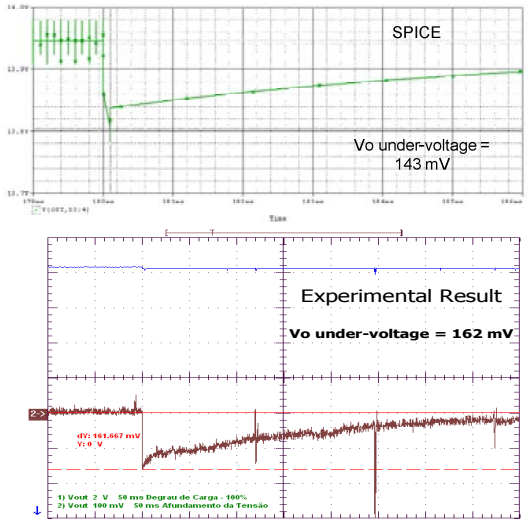

Fig. 12. Dynamic response for 100% load step.

The simulated and the experimental time response of the output voltage are shown in Figure 13. The values are similar, despite of the difficulties to simulate the microcontroller and the switching delays. The results shown in Figure 13 were obtained using half load.

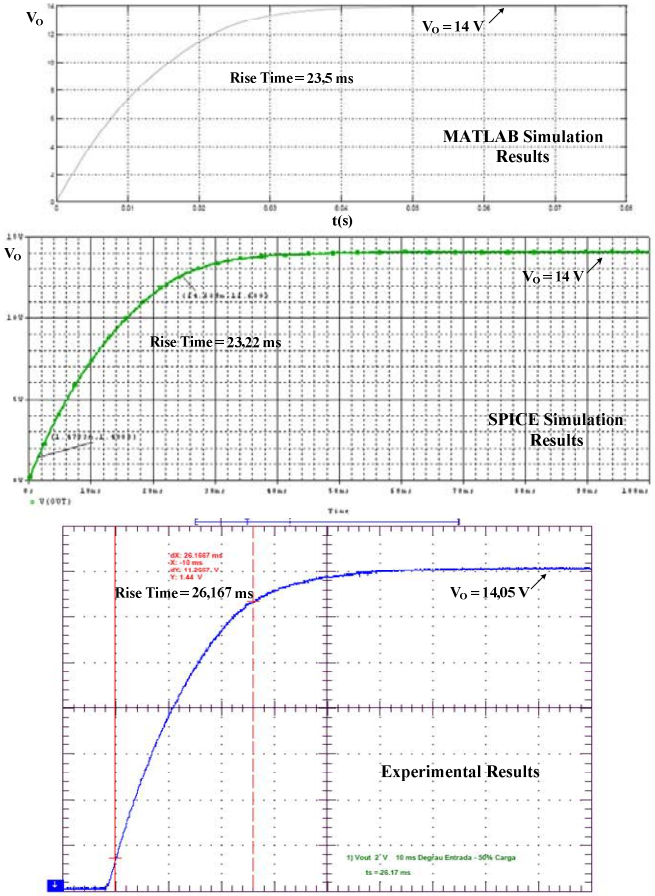

Fig. 13. Simulated and experimental time response for the output voltage.

IV. SEQUENTIAL SWITCHING SHUNT SERIES REGULATOR (S^4R)

A power unit with just one SR would not be practical because it would not be reliable and would need a large bus capacitance, C, in order to have a low output voltage ripple.

Figure 14 shows a practical solution, the Sequential Switching Shunt Regulator (S^3R) topology, where the SA is divided into parallel sections and each section has a SR which acts independent of the others. In this topology, some sections are not needed when the current required by the load and the battery is low. If these unneeded sections are connected to the bus, its voltage will be higher than the desired value. Therefore, the bus voltage is kept regulated by controlling the state of the switches (S_1, S_2,…) that connect the SA sections to the bus. For the sections unneeded the switches are closed, and they are short-circuited. A finer control of the bus voltage is achieved by switching just one of the sections using PWM. The remaining SA sections connected to the bus are not switched by PWM. In the S^3R would be used a battery charger regulator (BCR).

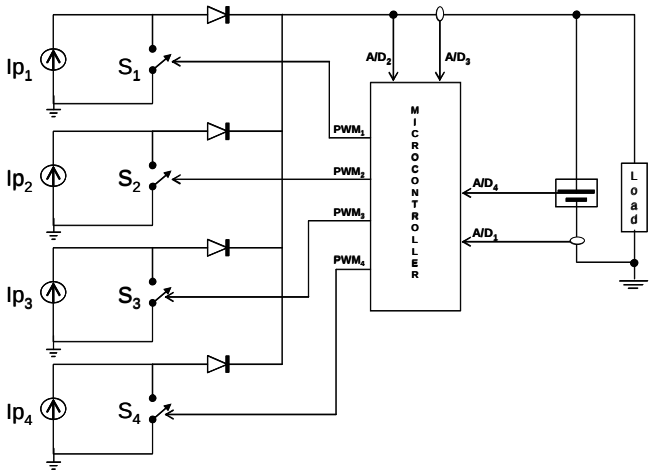

Fig. 14. Sequential Switching Shunt Regulator (S^3R) with microcontroller and PWM switching.

Another solution is the Sequential Switching Shunt Series Regulator (S^4R) topology, shown in figure 15. In the S^4R topology the battery is not directly connected to bus and power is transferred to the battery through the series module (switches S_{Bx} and diode D_{Bx}) [1][2].

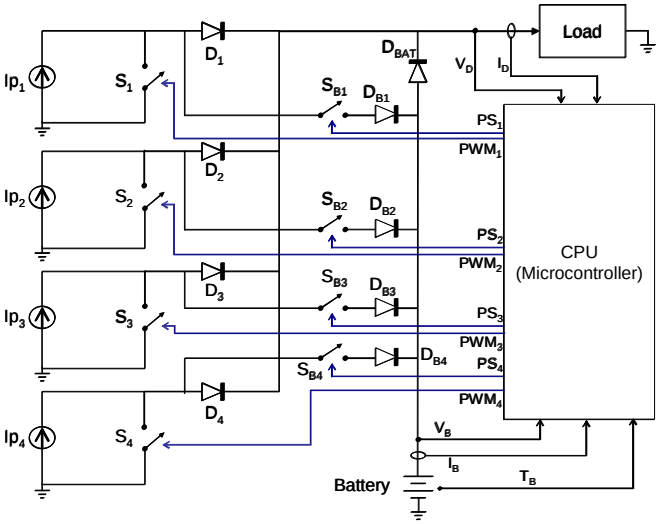

Fig. 15. Sequential Switching Shunt Series Regulator (S^4R) proposed to be used at the ITASAT.

In the S^4R topology each SA section can independently provide power to the load, to the battery, to both or it can be short-circuited.

In the S^4R topology the battery voltage must be lower than bus voltage. Therefore, in the SA sections which are used to charge the battery, the switch S_{Bx} is closed and the diode D_x is blocked, allowing the current to flow to the battery.

When the load requires more power than the capacity of the solar panel, the battery is used to provide power to the load. In this case, a battery discharger regulator (BDR) can be used to keep the bus voltage regulated during battery discharge. If it is not necessary to keep the bus voltage regulated, a diode can be used instead of a BDR (D_{BAT} in Figure 15). However, the bus voltage will vary according to the battery discharge cycle.

A simplified flow chart for the computation of the pulse width and the number of SA sections is shown in Figure 16.

The number of SA sections connected to the bus is defined by the division of the sum (S) of output voltage error after compensation ($u(k)$) and the load current (I_{BUS}) by the current of one solar array section (I_{pnom}). The fraction of the load current (I_{pn}) provided for the section which will be modulated and the output voltage error after compensation ($u(k)$) defines the pulse width (LP).

The number of SA sections connected to the battery and the pulse width are computed using a recharge algorithm that depends of the type of the battery used. The algorithm has current, voltage and temperature of the battery to control the recharge. Then, it is verified if there are enough SA sections. If the answer is affirmative, the SA sections which will be used are selected and the remaining sections are short-circuited, the pulse width is then computed. If the answer is negative, all available sections are selected and the pulse width is computed to share the bus section that is modulated, if its duty cycle is not one.

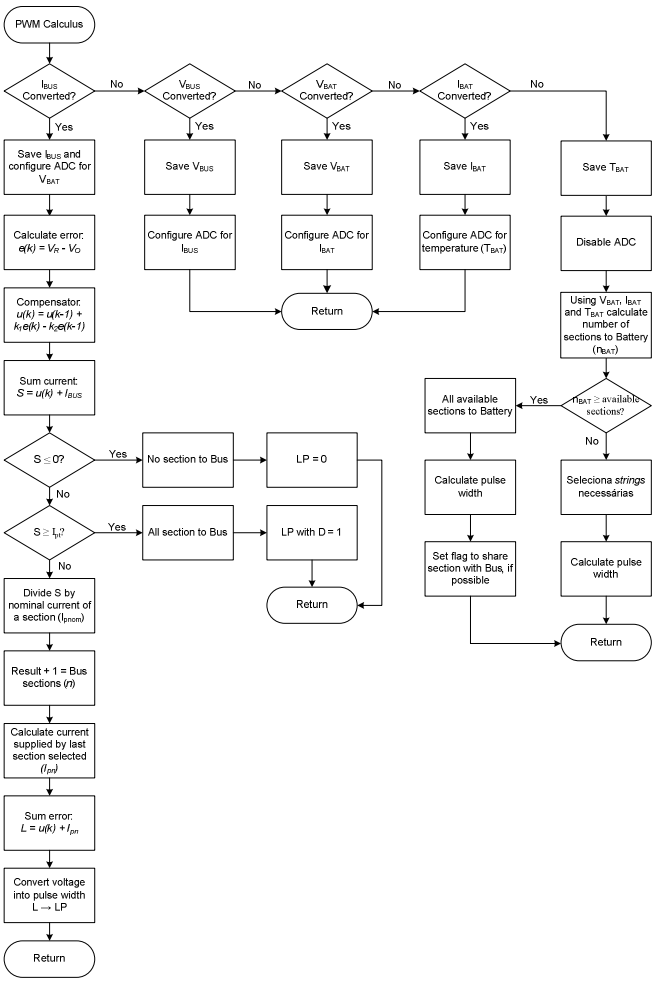

Fig. 16. Simplified flow chart to compute the pulse width and the number of SA sections for the bus and for the battery.

Figure 17 shows the beginning of the pulse interrupt. The switches are commanded and the PWM counters are updated. If a section is shared: a) all others sections are connected to the bus or to the battery; b) the battery PWM counter is updated with the pulse width used for the bus; c) the bus PWM counter takes the sum of bus and battery pulses; and d) the end of the pulse interrupts are enabled.

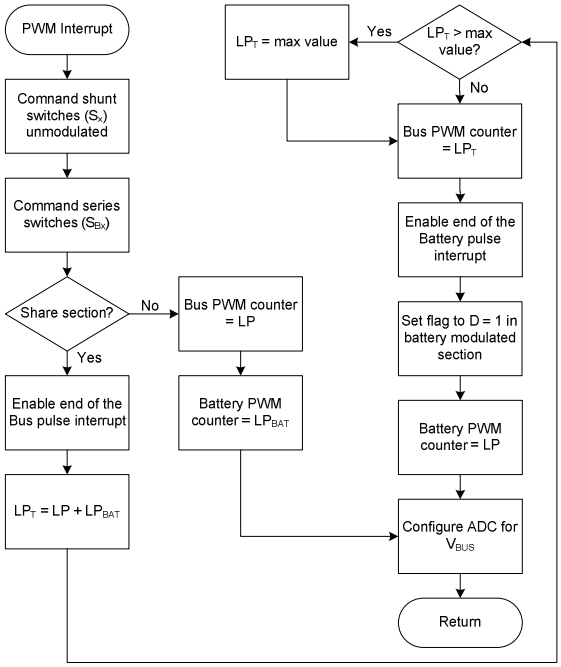

Fig. 17. Simplified flow chart of pulse width updating.

If a section is shared, when the bus pulse finishes the series switch is closed and the SA section is connected to battery. When the battery pulse finishes, the shunt switch is closed so the section is short-circuited. Then the series switch is closed.

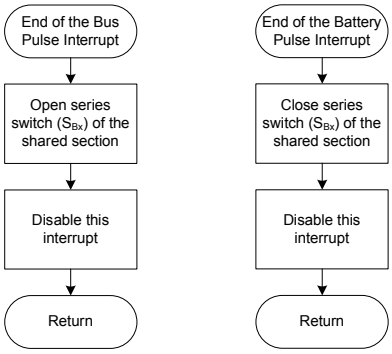

Fig. 18. End of pulse interrupts.

The experiments results of the next figures were obtained using IRF9Z34N mosfets and UF5402 diodes in the series module (S_{Bx} and D_{Bx}). Also, the battery was replaced by a resistive load or by a constant-current load in order to provide a better evaluation of the S^4R operation. Figure 19 shows the experimental load step response in the bus. In this figure the load varies from 1% to 100%, approximately. The output voltage is 14 V and the output current for full load is 2.82 A, divided in 6 SA sections of 0.47 A each one. In figure 19 the waveforms are:

- (1) The bus output voltage;
- (2) The battery voltage: there was a load, 400 mA, connected to the bus instead of the battery. All SA sections were used by the load bus, then no power was supplied to the battery and therefore its voltage was zero.
- (3) The bus output current: it varies from 28 mA to 2.82 A. In the waveform shown there is an offset of 200 mA

approximately caused by a measurement error in current sensor.

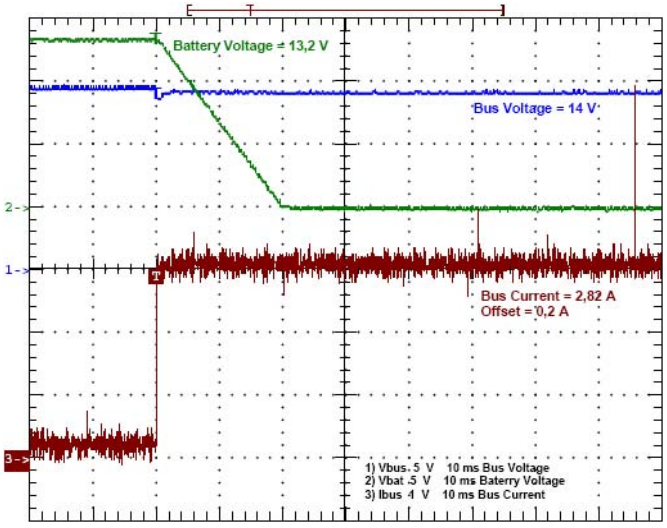

Fig. 19. Load step, full load, in the bus.

Figure 20 shows the load step response to a 50% of the full load. In this case the battery voltage was not zero since not all sections are needed by the load. The bus output current varies from 28 mA to 1.41 A, approximately.

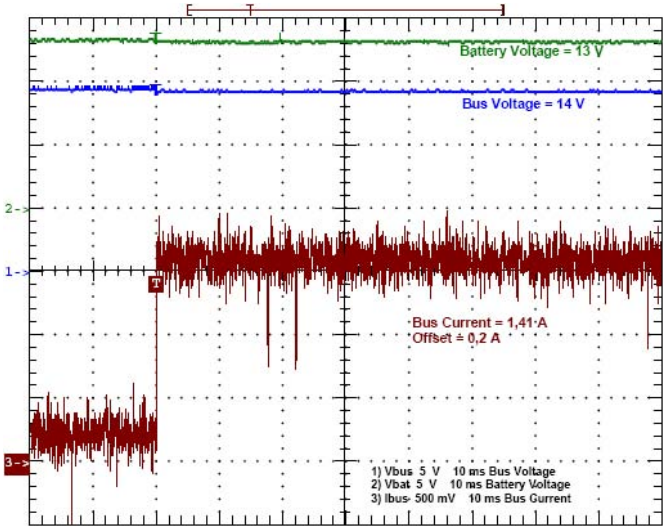

Fig. 20. Load step, half load, in the bus.

Figure 21 shows the waveforms when the battery is replaced by a load and there is a step in this load. After the step, there were not enough sections to provide power to the load which replaced the battery. Therefore the voltage for this load dropped, but it did not reach zero because some SA sections were available. Since the bus has higher priority, its voltage did not vary. In Figure 21 the battery current is the waveform 1.

The shared section commands are shown in Figure 22. Waveform 1 shows the pulse command of the shunt switch of section 1 (the sum of bus and battery pulses). Waveform 2 shows the pulse command of the series switch of section 1, after bus pulse section 1 is connected to the battery. Waveform 3 shows shunt command of the section that was modulated to charge the battery (it is not modulated in this case).

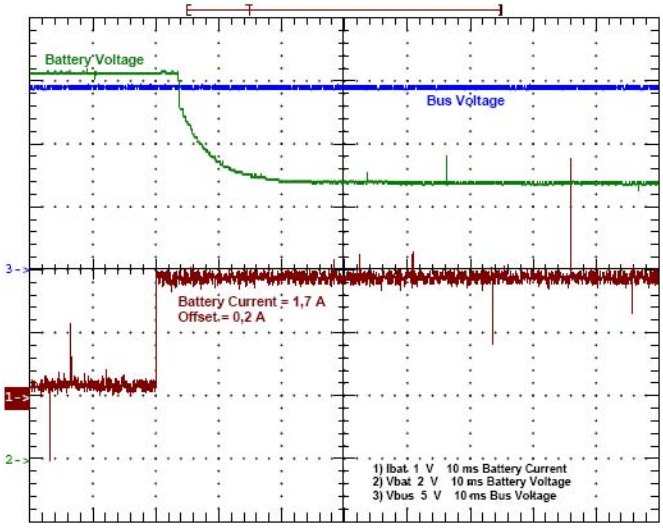

Fig. 21. Load step in the battery module.

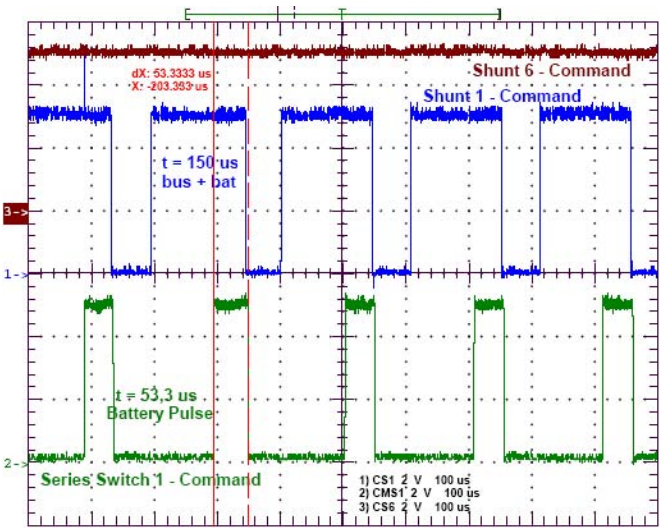

Fig. 22. Shared section commands.

V. CONCLUSION

From the simulations and experimental results it was possible to validate the models used and conclude that the S^4R topology is a viable and efficient solution to be used in the ITASAT.

The greatest advantage of S^4R topology is the elimination of BCR that in general is heavy and has lower efficiency. In this topology the battery is recharged by solar array sections without the need of a DC-DC converter.

Another important advantage is that the S^4R topology is modular and therefore can be used in a wide power range keeping high efficiency and without the need of considerable changes.

The use of microcontroller is also a great advantage of this topology since it allows a more “intelligent” and flexible control solution.

The proposed solution allows efficient control of the battery charge and the bus regulation independently,

although the bus has higher priority and can limit the battery charge. It was possible to obtain steady-state error zero and satisfactory dynamic response without using complex circuitry or a complicated algorithm.

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