Neutral Point Potential Balancing Algorithm at High Modulation Index for Three-Level Medium Voltage Inverter

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***Abstract* — Three-level Neutral-Point-Clamped (NPC) inverter needs a point at half potential of the full dc-link voltage (neutral point). A practical implementation of this neutral point is to use two capacitor banks series connected. Normally at steady-state operation this inverter topology produces a natural balancing of the two capacitor voltages, however, at some operation conditions, voltage differences may appears and must be controlled to keep safe and correct operation.**

This paper describes the use of redundant vectors applied together with a synchronous optimal pulse width modulation technique to achieve the voltage balance between dc-link capacitors. Practical measurements, performed with a medium voltage motor drive using a 1.8 MW-4160V three-level inverter are showed validating the strategy.

Index Terms— **Medium voltage inverter, three-level inverter, synchronous optimal modulation, neutral point control, redundant vectors.**

I. INTRODUCTION

Of particular interest for medium voltage inverter applications is the neutral-point clamped (NPC) topology [1], the circuit diagram as shown in Fig. 1.

It permits to use power semiconductors that may be rated at half of the full dc-link voltage. With the latest available high voltage IGBT (6.5 kV) it allows to have a drive for motor voltage of 4160V without series connection of semiconductors. Also the three-level inverter topology offers reduced harmonic distortion of the output current for the same switching frequency when compared with a two-level topology. Or in another way it offers reduced harmonic distortion of the output current with a low switching frequency reducing semiconductor losses and improving overall efficiency.

The three-level Neutral-Point-Clamped (NPC) inverter needs a point at half potential of the full dc-link voltage (neutral point). A practical implementation of this neutral point is done using two capacitor banks series connected. Static voltage distribution is obtained by using sharing resistors parallel connected to each capacitor bank. To keep losses low these sharing resistor draw only a small current.

Normally at steady-state operation and using symmetric semiconductor switching sequences this inverter topology

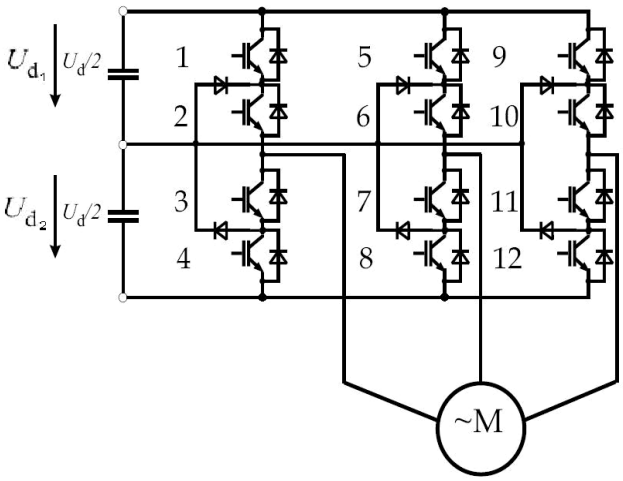

Fig. 1. Three-level Neutral-Point Clamped (NPC) inverter topology

produces a natural balancing [2] of the two capacitor voltages over a complete cycle of the output frequency, however, at some transient conditions, voltage differences may occur and must be controlled to keep safe and correct operation.

During operation depending on the switching status of the semiconductors and during a transient condition a combination of the three output phase currents charge or discharge each individually capacitor bank (upper or lower) differently. The small currents of the sharing resistors can not overcome the voltage unbalance introduced and then some kind of control of the semiconductors switching sequence must be employed to return to a balanced condition as soon as possible without disturbing operation of the motor load.

At low motor speed, what means low output voltage low output frequency and also low modulation index the Space Vector Modulation offers low output current distortion either at low switching frequency and can be used efficiently. Making use of the redundant vectors the three-level Neutral-Point-Clamped (NPC) inverter offers a closed loop control can bring the voltage of the capacitor banks to a balanced condition [3]. This technique is easily understood and implemented when looking at the three-level Neutral-Point-Clamped (NPC) inverter topology and decomposing it into two sub-bridges (positive and negative). Both can be used applying voltage to the load, but they change the way the upper and lower capacitor bank are charged or discharged.

Choosing how much time we use each of the sub-bridges, and also taking in account if the inverter is in motoring or regenerating condition, we may control the balancing.
As the modulation index increases using Space Vector Modulation causes the inverter output current distortion to increase and another modulation strategy must be used.
Performance improvement for medium voltage applications is achieved by employing synchronous optimal pulse width modulation (PWM) techniques for inverter control [4] [5] at high modulation index. Assuming steady-state operation, the switching angles within a fundamental period are determined such that an optimization criterion is satisfied. A preferred objective is minimizing the harmonic distortion of the output current. Although the technique of redundant vector to balance the dc-link neutral point may be used with synchronous optimal PWM and this implementation is not so clear and easy as for Space Vector Modulation. This paper discusses the neutral point potential balancing problem in the higher modulation range using synchronous optimal PWM.

II. Optimal synchronous PWM

The method of optimal synchronous PWM is the most effective approach to minimize harmonic distortion, especially for PWM inverters of higher power rating operating at high modulation index [4].
The optimal pulses tables are calculated off-line on a personal or mainframe computer and the sets of switching angles are stored in the memory of the control processor. The stored angles or optimal pulse patterns (OPP) are accessed in real time to determine the optimized switching angles.

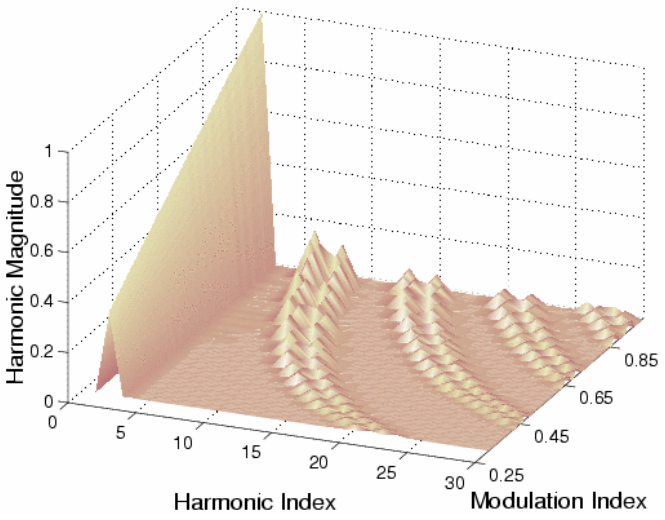

Fig. 2. Inverter output voltage harmonic magnitudes in SVM at different modulation index.

Since these angles always are synchronized to the fundamental component, the harmonic spectrum is free of sub-harmonics components. The switching angles operate in synchronism, so that the number of pulses per cycle must be changed in discrete fashion as the fundamental frequency decreases in order to maintain a good quality waveform and also to keep the switching frequency bellow a maximum [6]. The inverter output voltage harmonic magnitudes for SVM and optimal synchronous PWM are showed at figures 2 and 3 at different modulation index. Switching frequency is around 333 Hz for both modulation methods. Comparing both figures we can see that SVM can provide low harmonic magnitudes at low modulation index and optimal synchronous PWM gives a lower total harmonic distortion at high modulation index.

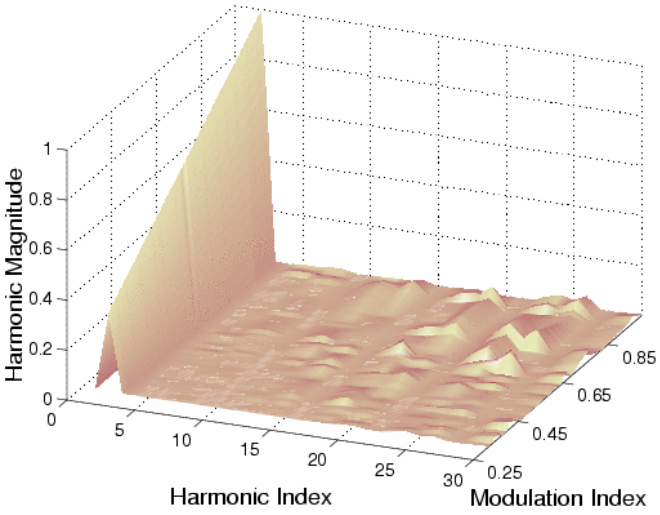

Fig. 3. Inverter output voltage harmonic magnitudes in optimal synchronous PWM at different modulation index.

III. Redundant vectors

The Fig. 4 indicates all the possible switching states of a three-level inverter. The inverter can assume a total of 27 switching states.

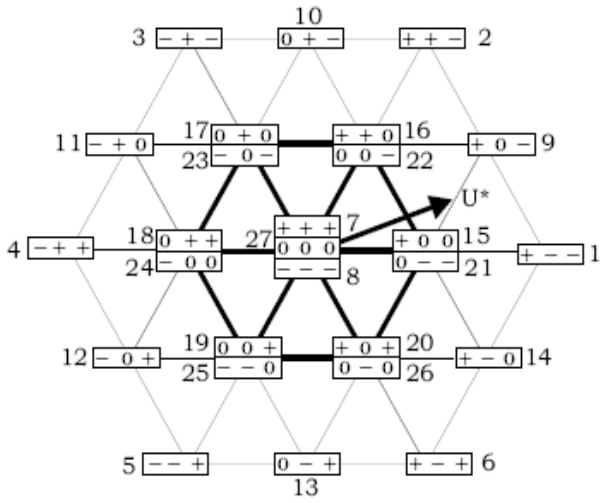

Fig. 4. Switching state vectors of a three-level inverter.

The notation, e.g. $\mathbf{u}_9$(+ 0 –), indicates that phase *a* is connected to the positive dc rail, phase *b* to the neutral point, and phase *c* to the negative dc rail. The switching state vectors can be associated to four groups [3]:

1. The zero vectors $\mathbf{u}_7^+$ (+ + +), $\mathbf{u}_{27}^0$ (0 0 0) and $\mathbf{u}_8^-$(– – –) do not cause a current flow through the neutral point. Hence the neutral point potential is not affected.

2. Large vectors, such as $\mathbf{u}_1$ (+ – –), connect the phase terminals either to the positive or the negative dc-rail. They do not cause a current flow through the neutral point which leaves the neutral point potential unaffected.

3. Medium vectors, such as $\mathbf{u}_9$ (+ 0 –), connect one of the three phase terminals to the neutral point. The resulting neutral point current changes the neutral point potential.

4. Small vectors exist in redundant pairs: Each positive small vector, such as $\mathbf{u}_{15}^+$ (+ 0 0) has a corresponding negative small vector $\mathbf{u}_{21}^-$ (0 – –) that generates the same output voltage vector. Although the neutral point current has the same magnitude in either case, its sign reverses depending on which one of the two redundant vectors is activated. The neutral point potential then changes either to higher or to lower values.

It is therefore the small and the medium switching state vectors that can be used to balance the dc-link capacitor voltages. For example the 16 and 22 switching state at Fig.4. both produce the same inverter output voltage without affecting the motor load ($\mathbf{u}_{16} \bullet \mathbf{u}_{22}$). If we use voltage vector $\mathbf{u}_{16}$ instead of $\mathbf{u}_{22}$ we use the positive upper bridge and do not use the negative lower bridge.
This property may be used to control capacitor bank voltage unbalance by choosing one or the other of these switching state vectors.

IV. Unbalance Problem Origin

The dc-link unbalances may be produced by the presence of asymmetries as for example differences between the capacitance of the dc-link capacitors [5] [7] or PWM modulation pattern.

The dc-link unbalance problem is more evident in vector controlled drives. The required fast dynamic performance as showed in fig. 5 can produce dc-link unbalance because the output frequency is changed so rapidly that PWM pulse patterns are changed even before a fundamental cycle is finished. Then the redundant vectors that are available in one pulse pattern and normally evenly distributed over a complete fundamental cycle of that pattern may be not present in the next used pulse pattern if pattern changes are made in the middle of the fundamental cycle. Offsets in the current measurements which are used as feedback of inner closed current loops may also introduce unbalance on the dc-link voltages.

Figure 6 shows a dc-link unbalance experimentally measured during a fast deceleration of a medium voltage drive that uses a three-level inverter without any balancing function. Around 300ms after motor deceleration the upper and lower capacitor mean voltages values start to differ each other. The drive needed to shutdown, interrupting its operation, to avoid excessive voltage in the upper capacitor voltage.

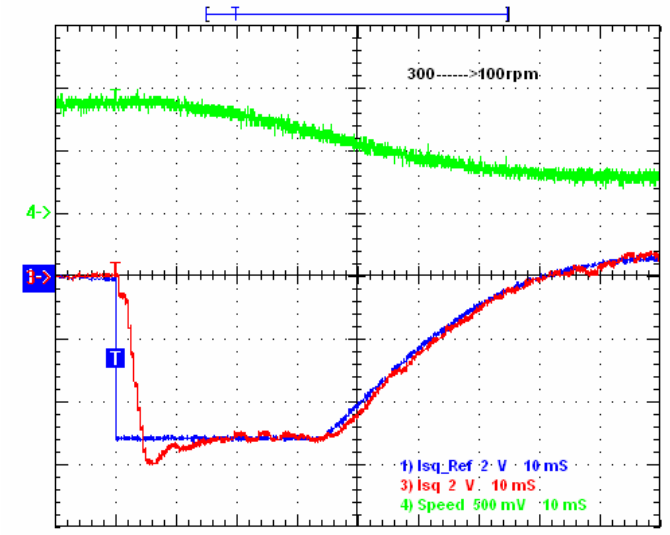

Fig 5. Performance of a medium voltage vector controlled drives during a fast deceleration; trace 1: Current torque reference(120A/div); trace 2: Real torque(120A/div); trace 4: Motor speed(180 rpm/div).

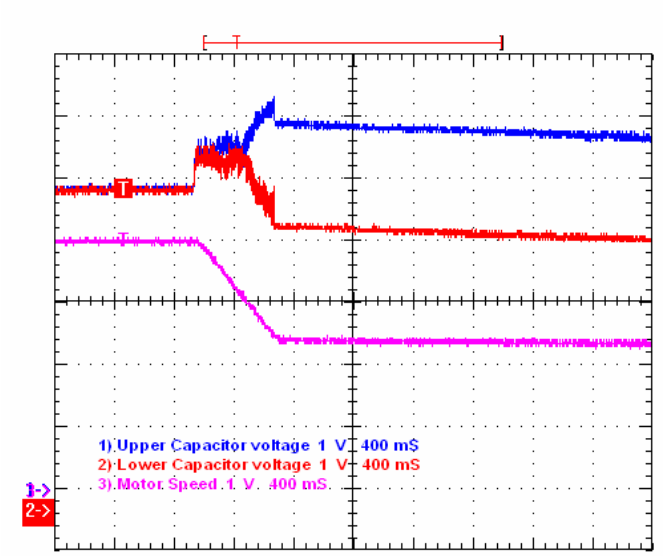

Fig. 6. DC link unbalance during a deceleration without any capacitor balancing control; trace 1: Upper capacitor voltage(586V/div); trace 2: Lower capacitor voltage(586V/div); trace 3: Motor speed(360rpm/div).

V. BALANCING STRATEGY WITH OPP

The basic idea of the algorithm is to identify if the inverter is motoring or regenerating and, when a redundant vector is available, choose if it should be used or not, during the PWM interrupt service routine, to compensate the unbalance of the dc-link.

Both dc-link voltages must be measured (see Fig. 1.) and then we can calculate [7]

$$\Delta u_d = U_{d1} - U_{d2} \quad (1)$$

The algorithm starts to use the redundant vectors if

$$|\Delta u_d| \geq e_d \quad (2)$$

where, for example, we can set the reference value e_d at some percentage value of the total dc-link. Then if equation (2) is satisfied and the motor is motoring and if

$$\Delta u_d \geq 0 \quad (3)$$

then all vectors that commutate like $\mathbf{u}_{21}^-$, $\mathbf{u}_{22}^-$, $\mathbf{u}_{23}^-$, $\mathbf{u}_{24}^-$, $\mathbf{u}_{25}^-$ and $\mathbf{u}_{26}^-$ should be changed by their redundant $\mathbf{u}_{15}^+$, $\mathbf{u}_{16}^+$, $\mathbf{u}_{17}^+$, $\mathbf{u}_{18}^+$, $\mathbf{u}_{19}^+$ and $\mathbf{u}_{20}^+$.

If the motor is regenerating or

$$\Delta u_d < 0 \quad (4)$$

then all vectors that commutate like $\mathbf{u}_{15}^+$, $\mathbf{u}_{16}^+$, $\mathbf{u}_{17}^+$, $\mathbf{u}_{18}^+$, $\mathbf{u}_{19}^+$ and $\mathbf{u}_{20}^+$ should be changed by their redundant $\mathbf{u}_{21}^-$, $\mathbf{u}_{22}^-$, $\mathbf{u}_{23}^-$, $\mathbf{u}_{24}^-$, $\mathbf{u}_{25}^-$ and $\mathbf{u}_{26}^-$.

Fig. 7 shows an example of the phase to neutral point and phase to phase inverter output voltages when using optimal synchronous PWM with four calculated angles. In this example all redundant switching state vectors are used and distributed uniformly over the fundamental period of output frequency.

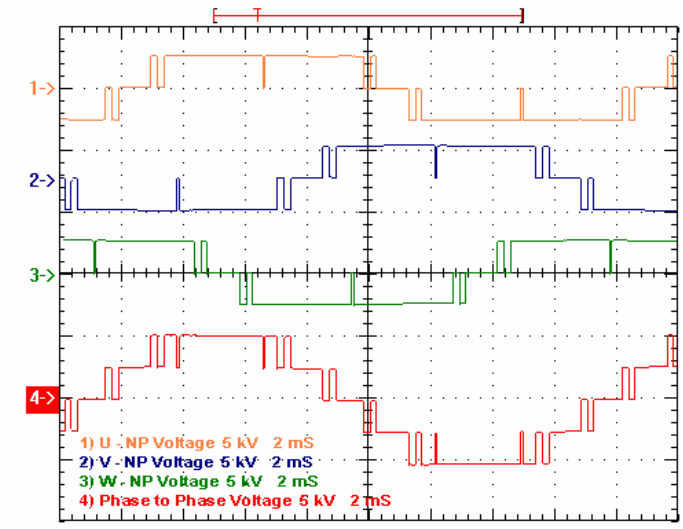

Fig. 7. Phases to inverter neutral point and phase to phase inverter output voltages with redundant vector evenly distributed over one fundamental period.

In Fig. 8 only positive redundant vectors are used. This modified pattern will cause an unbalance on the dc-link capacitor voltages in one sense.

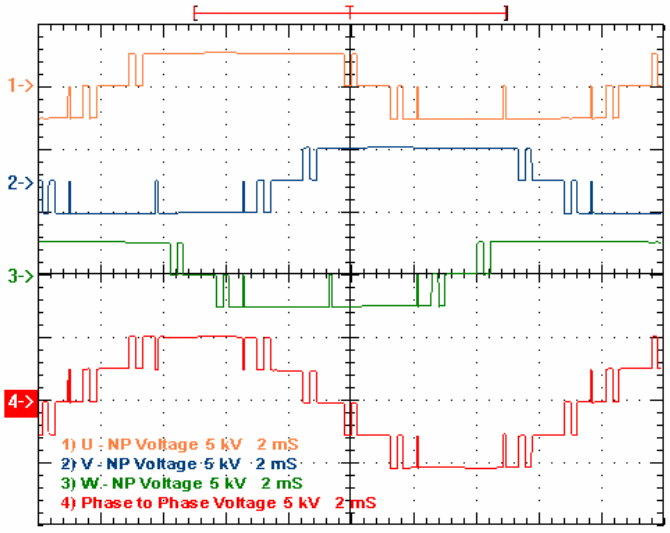

Fig. 8. Phases to inverter neutral point and phase to phase inverter output voltages with only positive redundant vectors applied over one

In Fig. 9 only the negative redundant vectors are used. This causes an unbalance on dc-link capacitor voltage in opposite sense of that one caused when only positive redundant vectors are used.

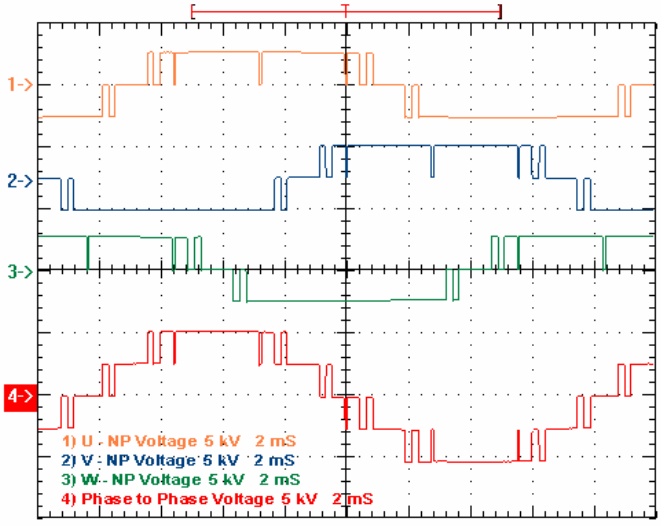

Fig. 9. Phases to inverter neutral point and phase to phase inverter output voltages with only negative redundant vectors applied over one fundamental period.

Comparing Fig.7 to 9 and looking on the phase to phase voltage graph, we can see its waveform does not change although the phases to neutral point voltages have been modified on their pulse patterns.

VI. Experimental Results

The performance of neutral point potential control was tested with a medium voltage motor fed by a 1.8 MW – 4160 V using a three-level inverter and some experimental results obtained are presented here. The dc-link is supplied through a 12-pulse input diode rectifier from AC line supply. The neutral point is obtained by series connection of two capacitor banks (2.34 mF each). Static voltage balance is supported by sharing resistors parallel connected to each capacitor bank. There are not any connection between this inverter medium point and the input rectifier what means the inverter control is the only responsible for the capacitors voltage balancing.

Fig. 10 demonstrates the application instants of positive and negative redundant vectors as explained before in a steady state condition. The dc-link capacitor voltages can be driven to any needed direction depending how the redundant vectors are chosen.

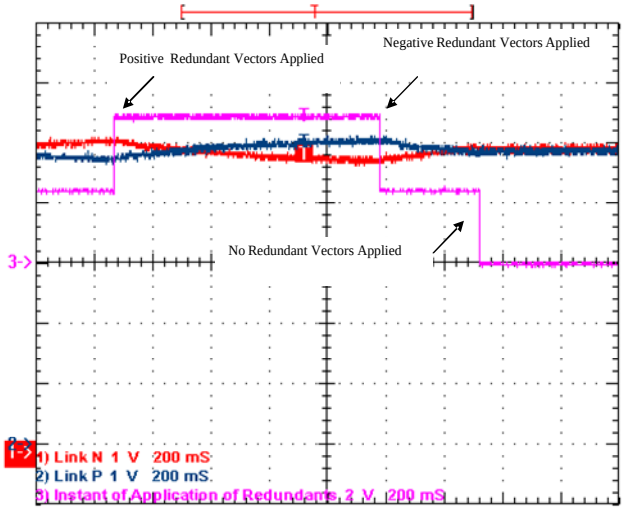

Fig. 10. DC link unbalance using forced different set of redundant vectors; trace 1: Lower capacitor bank voltage(586V/div); trace 2: Upper capacitor bank voltage(586V/div); trace 3: Balancing algorithm control signal.

Another result is showed in Fig. 11. This result was measured with the closed loop balancing control algorithm running and monitoring the unbalance. When the voltage difference between the two dc-link capacitors is higher than a reference value, equation (2), a redundant vector set was applied during 8mS, forcing the dc-link to balance quickly. Important to note the phase motor current that was distorted during the unbalance goes to a a very sinusoidal wave shape without any disturbance transient.

VII. Conclusion

This paper presents a control algorithm to avoid dc-link capacitor voltage unbalance of a three-level Neutral-Point-Clamped (NPC) inverter with optimal synchronous PWM used at high modulation index and driving a motor load.
The dc-link are rapidly returned to the balance state and the motor currents do not shows any disturbance transient.

Experimental measurements done in a medium voltage high power inverter shows good results. The dc-link unbalance problem is more evident in vector controlled drives due to the fast dynamic required. The balancing algorithm presented here can be applied to overcome this problem. It makes use of the redundant vectors available on the NPC topology.

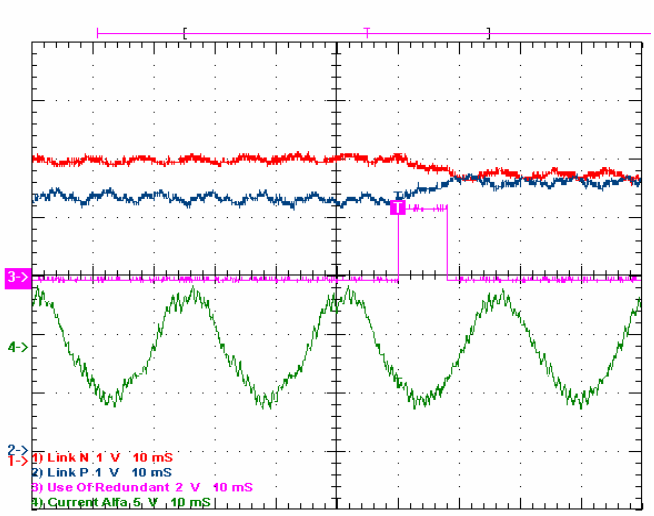

Fig 11. DC Link unbalance eliminated by applied Redundant Vectors during 8mS; trace 1: Lower capacitor bank voltage(586V/div); trace 2: Upper capacitor bank voltage(586V/div); trace 3: Balancing algorithm On/Off; trace 4: Motor fase alfa current (300A/div)

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