DIMMABLE LIGHTING SYSTEM FOR INTEGRAL COMPACT FLUORESCENT LAMPS

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***Abstract* – This paper presents a 200 W high power factor dimming system for integral compact fluorescent lamps (electronic ballast + compact fluorescent lamp) using two cascaded converters. The first stage is a boost converter operating in critical conduction current mode that supplies the second stage. The second stage is a buck converter, which operates in continuous conduction current mode and controls the output voltage for feeding an integral compact fluorescent lamp group. The characteristics of integral compact fluorescent lamps are presented in order to implement the system. Simulation, design equations, and experimental results of the implemented prototype are presented to validate the proposed idea.**

***Keywords* – power factor correction, dimming, compact fluorescent lamps, electronic ballasts.**

I. INTRODUCTION

Artificial illumination is responsible for 30% of the world-wide electrical energy consumption. Recent studies of European Lamps Companies Federation present estimated sales data for all types of lamps for the Western European market place.

The general lighting source (GLS) or incandescent lamps make up only a minor share of the light generated annually; they are the major in terms of annual sales. Most of the light is generated by fluorescent lamps (FL) and High-intensity discharge (HID) lamps. It is justified, since GLS have low efficiency (12 lm/W) compared to compact fluorescent lamps (CFL) and tubular fluorescent lamps (TFL), which present 60 up to 100 lm/W.

That study observes that industrial and residential applications with fluorescent lamps consume $164 \cdot 10^9$ kWh/year, and GLS consume $96 \cdot 10^9$ kWh/year. However, GLS produce only 4% of lumens and fluorescent lamps produce 49 % [1]. Considering a continuous market growing 20% per year, electronic ballasts are widely spread over the world replacing electromagnetic ballast and incandescent lamps [2].

Dimming systems using FL have been studied in several works [3]-[11]. On the other hand, it is well know that integral CFL are not suitable for dimming systems used in GLS. The electronic ballasts that supply CFL are widely employed in residential and commercial application due to considerably high energy saving provided when replacing GLS.

However, usually these kinds of systems do not present power factor correction (PFC) and dimming capability. In this work a high power factor (PF) system is proposed, which allows an integral CFL(iCFL) group to be dimmed through a variable DC voltage provided by two cascaded converters.

This paper is organized as follow: Second section shows the proposed idea. Third, and Fourth section present the simulation, and experimental results. Section V shows the preliminary conclusions of this work.

II. PROPOSED IDEA

Fig. 1 shows the concept of the proposed system. The first stage is an EMI filter to smooth the input current waveform, and the second stage is a boost converter operating in critical conduction mode. The third stage is the PWM buck converter operating in continuous conduction current mode, which controls the output voltage for the integral CFL group.

The fourth stage is the load, i. e., the set of iCFL dimmed through a variable voltage provided from the buck converter.

In order to implement the proposed system a brief study of one integral CFL (iCFL) was made. First, a 20 W iCFL was tested during 5,000 hours using low supply voltage (V_{bus}=80 V). The filaments of the CFL were visually observed without any blackening.

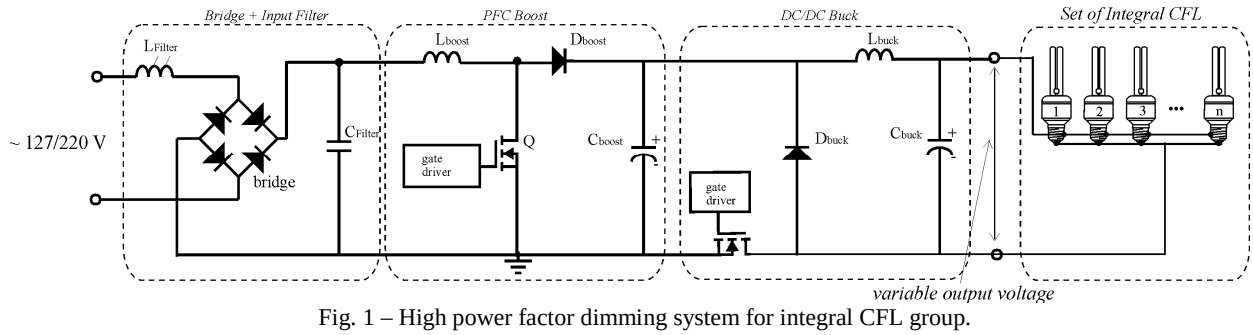


Fig. 1 – High power factor dimming system for integral CFL group.

[1] CNPq scholarship

Integral CFL generally uses self-oscillating command circuitry that presents input voltage, and load dependence [12]. In order to understand the behavior of the iCFL supplied by a controlled voltage source a study of several conditions were carried out. Experimental data were obtained from a 20 W iCFL using the scheme shown in Fig. 2.

Fig. 3 summarizes these results. Fig. 3(a) shows the illuminance in per unit versus bus voltage of one integral CFL (V_{bus}) obtained from a fixed position using a lux meter (0.5 m from CFL for all data in a dark environment, see Fig. 2). These data were obtained in order to evaluate the illuminance changing as V_{bus} is controlled trough an autotransformer (V_{ac}), as shown in Fig. 2. The base value of illuminance is 800 lux.

Fig. 3(b) shows the behavior of the load resistance under V_{bus} variation. It shows that the load equivalent resistance is lower as the number of iCFL increases. Fig. 3(c) shows the voltage V_{bus} versus iCFL current (I_{avg}) as a function of the iCFL number.

Analyzing the presented data, Fig. 3(a) shows significant illuminance changing as V_{bus} is controlled from 80 up to 311 V. This feature allows dimming iCFL through a voltage source. Another important characteristic is that the load changing is not significant, being possible to supply the systems without feedback. Fig. 3(b) shows that the equivalent resistance changing is not significant when the number of iCFL is higher than two.

Since the main load characteristic was determined, next section presents the buck converter behavior operating in open loop in order to implement the complete system.

III. DESIGN EQUATIONS, SIMULATION, AND EXPERIMENTAL RESULTS

This section presents design equations, simulation, and experimental results for the proposed system.

A. Design Equations

The boost PFC converter parameters were determined using the equations obtained from [13]. The inductance for the buck converter is obtained through classical methods, considering the minimal inductance to maintain the continuous current conduction mode base on [14], [15].

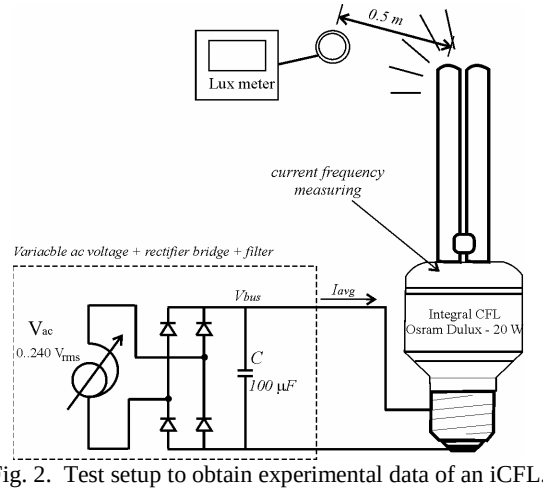
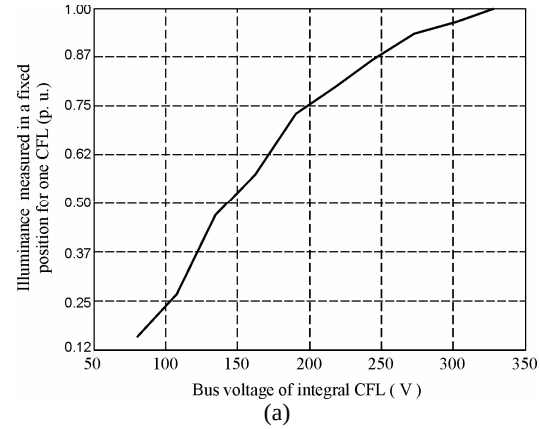
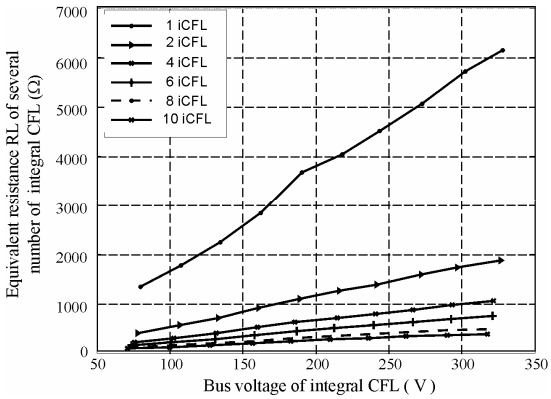


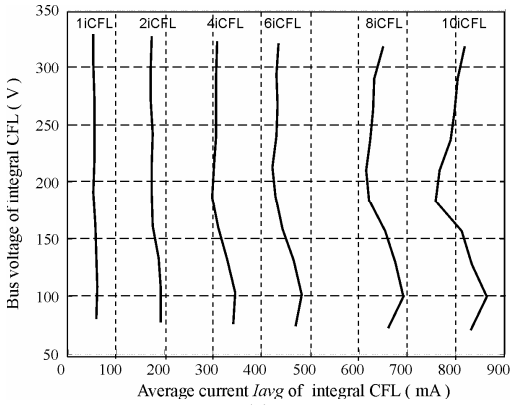
Fig. 2. Test setup to obtain experimental data of an iCFL.



(a)



(b)



(c)

Fig. 3. Experimental data of the integral CFL under voltage control.

The value of the buck inductor is determined using the critical inductance value, L_{crit}, i. e., the inductance of the buck inductor L_{buck} must be higher than L_{crit}, which is obtained for light load condition, and minimum duty cycle.

The limits to obtain these parameters are obtained through (1) and (2).

The maximum output voltage of the buck converter will be considered 311V, since the iCFL present nominal utility line voltage of 220 V_{rms}, 60Hz.

To obtain this equivalent voltage, the buck converter maximum duty-cycle must be D_{max}:

$$D_{max} = \frac{V_{out,max}}{V_{in}} = \frac{311}{400} = 0.78 \qquad (1)$$

Since the minimal output voltage is 80 V, the minimal duty cycle, D_{min} is

$$D_{min} = \frac{V_{out,min}}{V_{in}} = \frac{80}{400} = 0.20 \quad (2)$$

Where:

$V_{out,max}$ - output voltage of the buck converter considering the maximum supply voltage of the iCFL group.

$V_{out,min}$ - output voltage of the buck converter considering the minimum supply voltage of the iCFL group.

V_{in} - regulated voltage obtained from the boost PFC converter.

Therefore the criterion to obtain the L_{Buck} inductor is $L_{buck}>L_{crit}$ through (3).

$$L_{crit} = \frac{(V_{in} - V_{out})D_{min}}{2\Delta I_{Lbuck} f_s} = \frac{(400-80)\cdot 0.2}{2\cdot 0.2\cdot 0.3\cdot 60000} = 8.7mH \quad (3)$$

Where:

f_s - switching frequency.

ΔI_{Lbuck} - buck current variation (20% of I_{avg}, since iCFL presents internal capacitor).

In order to guarantee the continuous conduction mode $L_{buck}>L_{crit}$, thus L_{buck} is obtained from (4):

$$L_{Buck} > 2L_{critical} = 18mH \quad (4)$$

Since *esr* resistance of capacitor C_{buck} is neglected the capacitance value is obtained from (5) considering the ripple of 1,5 %.

$$C_{Buck} = \frac{\Delta_{iL}}{\Delta V_{out} 8 f_s} = \frac{0.2\cdot 0.3}{1.2\cdot 8\cdot 60000} \cong 10\mu F \quad (5)$$

Where:

ΔI_{Lbuck} - L_{buck} current variation;

ΔV_{out} – output voltage maximal ripple.

From the above parameters the simulation was carried out and the complete system was implemented.

B. Simulation results

The boost converter simulation is not presented in this paper since it is regulated, and considered a voltage source for simulation purpose.

Fig. 4 shows the schematic to obtain the simulation results of the buck converter using Psim 7.0.5.

Fig. 5, and Fig. 6 show the simulation results of a buck dc/dc converter feeding two, and eight iCFL operating in continuous conduction mode, considered as light and heavy load, respectively.

These results are obtained for different loads conditions considering the previous results of the equivalent load resistance R_L obtained in section II (see, Fig. 3(b)) for two output voltage conditions defined in (1), and (2), and reported on Fig. 5, and 6 in (a), and (b).

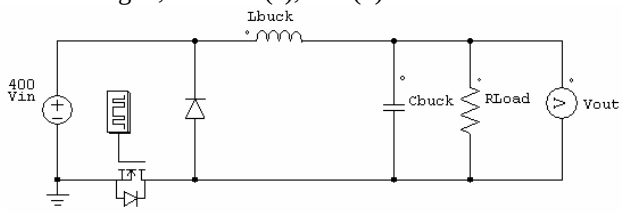
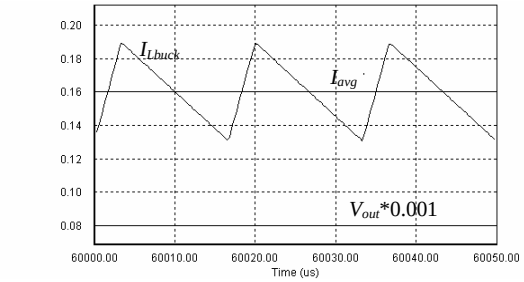


Fig. 4. Schematic implemented to simulate the buck converter.

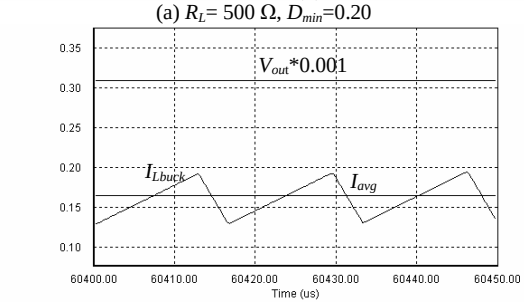
Fig. 5 shows the waveforms of the buck converter obtained from a dc voltage source of 400 V. Fig. 5(a), and Fig. 5(b) comprises results of the buck inductor current I_{Lbuck}, and the load current I_{avg} represented from a resistive load instead the integral CFL group. For both waveforms I_{Lbuck} remained in continuous current conduction mode, and the output voltage presented the desired voltage for conditions of light load.

Fig. 6 also presents similar waveforms. However the results were obtained considering heavy load, i. e., the equivalent resistance represent the maximal load of eight integral CFL (eight integral CFL).

The results obtained allow the boost and buck cascaded converters implementation to supply the iCFL group using a variable voltage source.

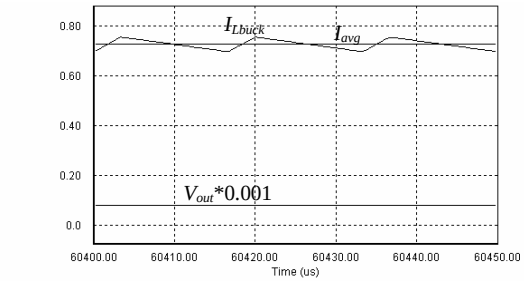


(a) R_L= 500 Ω, D_{min}=0.20

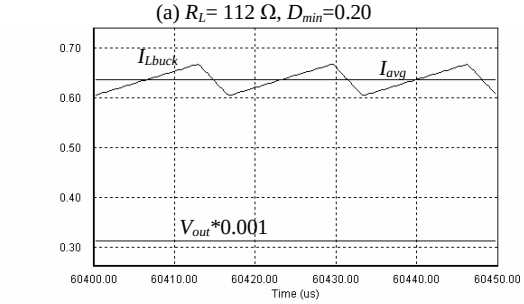


(b)R_L= 1879 Ω, and D_{max}=0.78

Fig. 5. Simulation results of buck inductor current I_{Lbuck}, load current I_{avg}, and output voltage V_{out} for two iCFL.



(a) R_L= 112 Ω, D_{min}=0.20



(b) R_L=489Ω, D_{max}=0.78

Fig. 6. Simulation results of buck inductor current I_{Lbuck}, load current I_{avg}, and output voltage V_{out} for eight iCFL.

C. Experimental Results

Fig. 7 shows the schematics of the implemented prototype comprising the boost and buck cascaded converters. Fig. 8, and Fig. 9 show the boost converter output voltage, and utility line voltage, and current. Fig. 8, and Fig. 9 show the waveforms obtained for conditions of light, and heavy load, respectively.

For both waveforms the system operates with PFC near of unity, and the load variation does not affect the boost output voltage, since it presents feedback. It guarantees constant voltage, and high PF of the converter for all range of loads.

In order to show the critical current conduction mode of the boost converter Fig. 10, and Fig. 11 show the boost inductor currents for light and heavy load, respectively. These figures presents detail of the waveforms for different time scales in Figs. 10, 11, (a), and (b).

Fig. 12 shows waveforms of the buck dc/dc converter supplying integral CFL group from the output of the regulated voltage obtained from the boost converter. For all conditions were observed the continuous conduction current mode of the buck current. The waveforms show also the switch voltage and output voltage. It shows also the output voltage changing to supply the CFL with a wide range of 80 V(duty cycle of 30 %) to 300 V (duty cycle of 70%).

In order to illustrate different conditions these waveforms were obtained for tree conditions: two, six, and eight integral CFL shown in Figs. 12-14. Figs. 12-14 (a), and (b) are shown different conditions of the output voltage: low and high voltage, respectively.

Fig. 15 shows the CFL waveforms for conditions of minimal and maximal output power obtained for minimal and maximal voltage of the buck converter output.

IV. CONCLUSIONS

A dimmable high PF boost converter with a downstream buck converter supplying a group of iCFL was implemented successfully. The advantage of the proposed systems is the capability to obtain PFC for iCFL, and CFL dimming features. Simulations and experimental results confirm the possibility of the proposed idea. The study of the load features allows implementing the buck converter without feedback reducing cost and complexity.

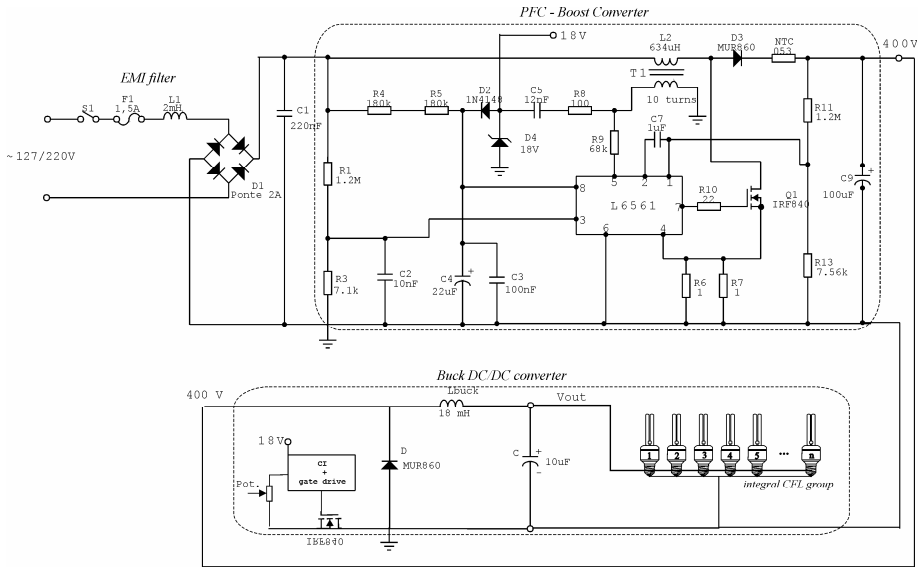


Fig. 7 . Simplified schematic of the implemented prototype of boost and buck cascaded converter.

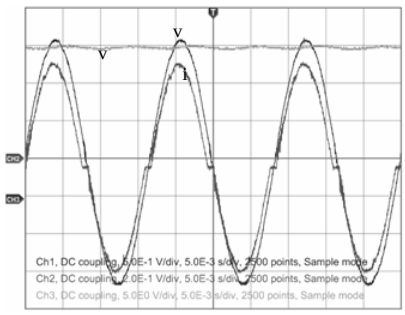


Fig. 8. Input power of the system for two integral CFL: Ch1 – line voltage - 100V/div; Ch2 – line current 0.2A /div, and Ch3 – boost converter output voltage - 100V/div; time scale: 5ms/div.

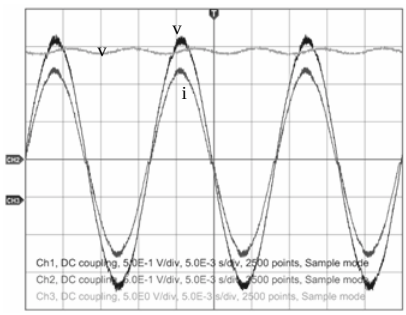
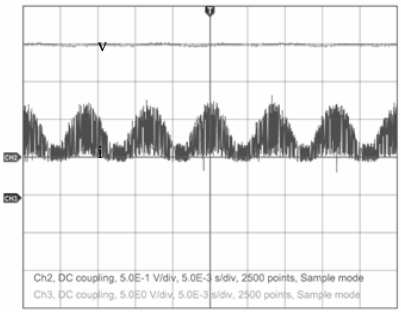
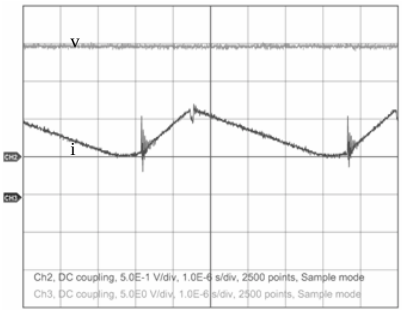


Fig. 9. Input power of the system for load power of eight integral CFL: Ch1 - line voltage - 100V/div; Ch2 - line current 0.5A/div, and Ch3 – boost converter output voltage - 100V/div; time scale: 5ms/div.

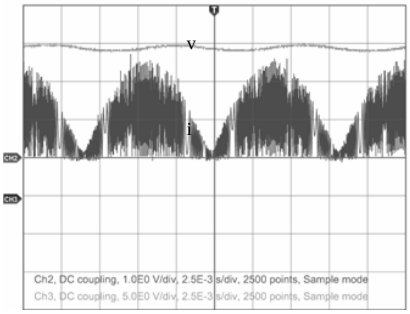


(a)

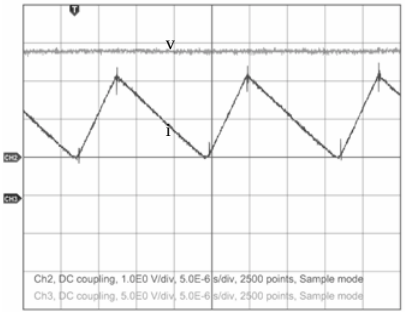


(b)

Fig. 10. Boost inductor currents (Ch2 - 0.5A/div) and boost output voltages (Ch3 – 100V/div) for two integral CFL: (a) time scale: 5ms/div, and (b) time scale: 1µs/div.

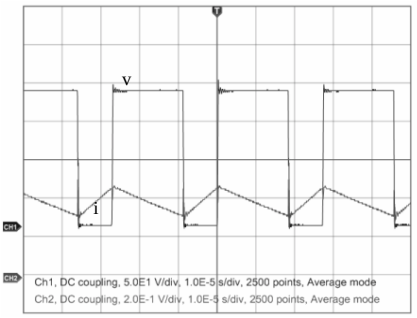


(a)

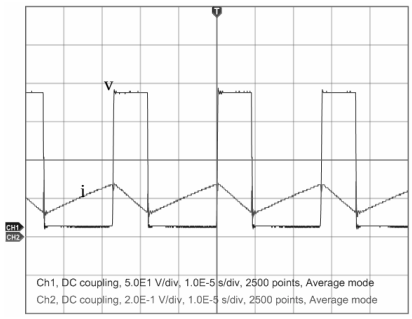


(b)

Fig. 11. Boost inductor currents (Ch2 – 0,5 A/div) and boost output voltages (Ch3 – 100V/div) for eight integral CFL: (a) time scale: 5ms/div, and (b) time scale: 1µs/div.

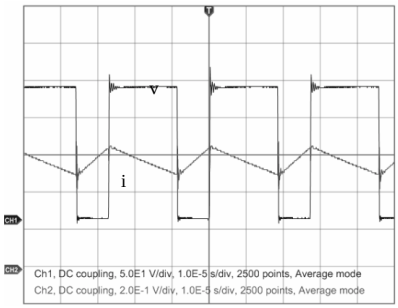


(a) D=30 %

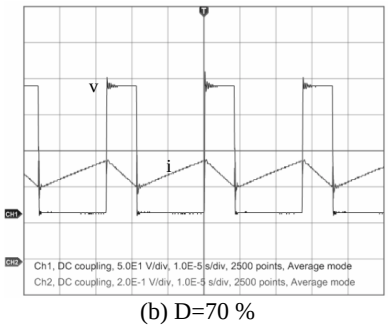


(b)D=70 %

Fig. 12. Buck converter waveforms: Ch1 – switch voltage – 100 V/div; Ch2 – buck inductor current - 200mA/div, and Ch3 –output voltage - 100V/div feeding two integral 20 W CFL.

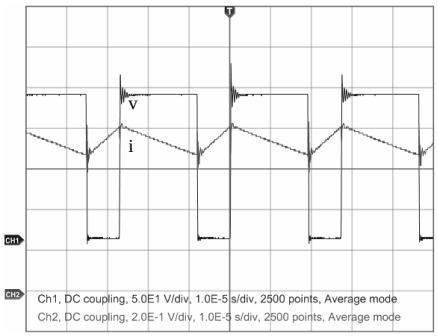


(a) D= 30 %

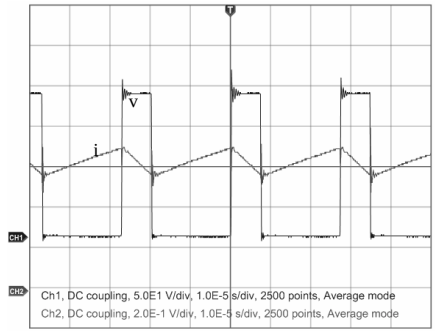


(b) D=70 %

Fig. 13. Buck converter waveforms: Ch1 – Switch voltage – 100 V/div; Ch2 – buck inductor current - 200mA/div, and Ch3 –output voltage - 100V/div feeding six integral 20 W CFL.

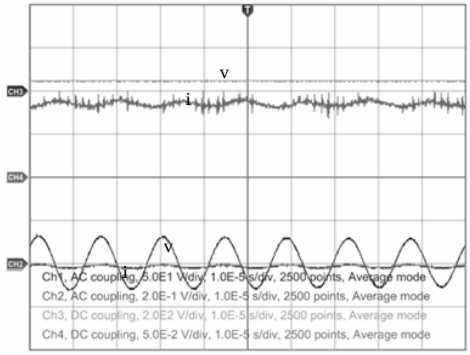


(a) D=30 %

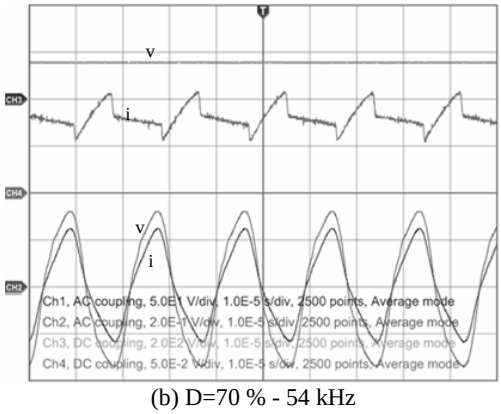


(b) D=70 %

Fig. 14. Buck converter waveforms: – switch voltage Ch1 - 100 V/div; Ch2 – buck inductor current - 200mA/div, and Ch3 –output voltae - 100V/div feeding eight integral CFL.



(a) D=30 % - 69 kHz



(b) D=70 % - 54 kHz

Fig. 15. Behavior of one CFL for minimal (a) D=30%, and maximal (b) D=70 % dimming conditions: Ch1 - lamp voltage - 100 V/div; Ch2 – lamp current - 200 mA/div; integral CFL voltage - Ch3 - 400 V/div; integral CFL current – Ch4 – 50 mA/div; time scale – 10 µs/div.

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