NEW SYMMETRICAL HYBRID MULTILEVEL DC-AC CONVERTERS - SINGLE-PHASE CIRCUITS

Reynaldo Ramos Astudillo and Domingo Ruiz-Caballero

Power Electronic Laboratory - LEP
Electric Engineering School - EIE
PONTIFICIA UNIVERSIDAD CATÓLICA DE VALPARAÍSO
Av. Brasil 2147, Casilla 4059, Valparaíso, Chile. domingo.ruiz@ucv.cl

Abstract **– This paper presents the analysis and simulation of two new symmetrical hybrid multilevel inverters for high-voltage and high power applications. A three-level cell and its respective commutation pattern are proposed. The purpose of the circuits is minimizing the reverse voltage stress that affects the power switches and decreasing the harmonic distortion of the voltage applied to the load. Two symmetrical hybrid multilevel inverters circuits were generated with this cell.**

Keywords: **DC-AC converters, Hybrid Inverters, Symmetrical Multilevel Inverters.**

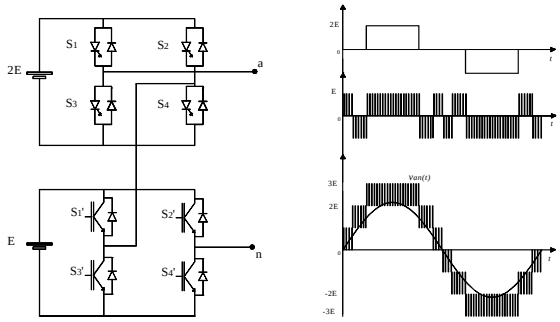
1. INTRODUCTION

In the eighties, Nabae and others [12] catapulted the interest in the high power conversion through multilevel inverters when introducing the topology of NPC (Neutral Point Clamped). In the course of time numerous topologies have been introduced and studied [1]-[11]. These converters are suitable in high-voltage and high power applications due to their synthesizing waveshape capacity with better harmonic spectrum and obtaining high voltages using devices with not much voltage reverse capacity [1].

The NPC topology can be applied to obtain great number of levels in the output. As this number increases, the output waveshape contains more steps and gets closer to a sinusoidal wave. Theoretically it is possible to get an output signal with zero harmonic distortion, a pure sinusoidal wave, by using an infinite number of levels. Unfortunately, the number of the achievable voltage levels is limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout and packaging constraints [9].

The magnetic coupled multipulse converters synthesize the sinusoidal wave by varying transformer turns ratio with complicated zigzag connections. However they present problems of volume, weight and losses [8]. With the previous being said, the method of synthesizing multilevel voltages through condenser is preferred instead of the method through magnetic coupled. There are three reported capacitor voltage synthesis-based multilevel converters: NPC, Flying capacitor and cascaded-inverters with separated DC sources and within this last classification the hybrid multilevel cells.

Figure 1(a) shows the asymmetrical hybrid multilevel inverter of seven-level voltage. This is based on the binary configuration of the voltage sources, it means that this circuit can synthesize $2^{N+1} - 1$ levels on the load voltage, being N the number of DC sources. The upper full-bridge is composed by switches of great voltage blockade capacity and therefore of low operation frequency (GTO for example), while the bottom full-bridge is constituted by switches of high speed of commutation, but with not much voltage reverse capacity (IGBT for example).



(a) (b)

Fig. 1 (a) Asymmetrical Hybrid Multilevel Inverter.
(b) Modulation Strategy of the Hybrid Multilevel Inverter.

Using an appropriate modulation strategy (Figure 1(b)) it is possible to synthesize waveshapes with seven-level voltage, -3E, -2E, -E, 0, E, 2E and 3E. The waveshape output voltage for this circuit is shown in figure 1(b). The modulation strategy includes the hybrid modulation concept, which is based on the unique pulse modulation together with the sinusoidal pulse width modulation. Under this modulation strategy, the slow switches are modulated to commutate to the fundamental frequency, the fast switches could be utilized to commutate a higher frequency, and as a result of that providing an improvement in the output waveshape quality. Then, the spectral response of the output voltage would depend on the fast switches, while the whole capacity of voltage generation would depend on the slow switches [1].

Patent Pending

Although the KVA capacity of the hybrid multilevel inverter devices is the same that in the conventional cascade multilevel inverter, it is possible to obtain a meaningful reduction on the expenses with an appropriate device selection [2].

The main purpose this article is to introduce two new topologies and that these were an alternative to conventional hybrid multilevel circuit.

2. DERIVATION OF THE PROPOSED CELL

The figure 2(a) [7] shows the topology of the three-level Buck converters; and the load voltages, as well as the control strategy of the switches of this converter are illustrated in the figure 2(b). The principal characteristics of this converter are:

The frequency on the output filter is twice the switching frequency of the switches, thus the filter can be significantly reduce.

The voltage stress across the switches is the half of the DC link. Besides with a suitable control strategy, the voltage of capacitors will be balanced.

The converter shown in the figure 2(a) is the starting point to the presented topologies in this paper. Figure 3(a) shows the circuit of the figure 2(a), in which the capacitors have been replaced by DC sources. In order to obtain a multilevel inverter the switches of figure 3(a) must be bidirectional. This is shown in the figure 3(b). The theoretical output voltage waveform of the circuit is shown in figure 3(c) where it is possible to appreciate this signal has three levels.

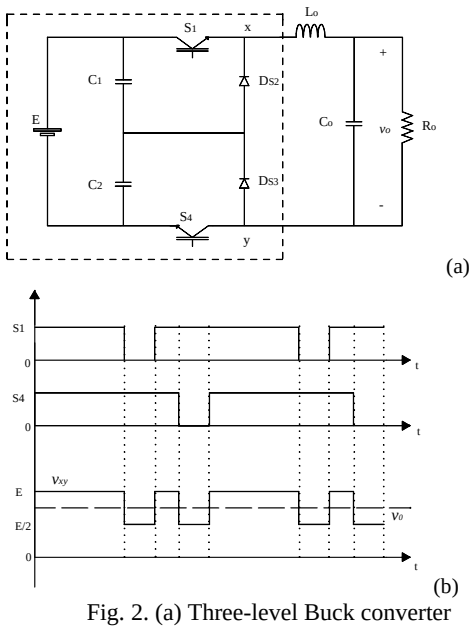


Fig. 2. (a) Three-level Buck converter
(b) Voltage waveforms of the three-level buck converter.

3. SINGLE-PHASE HALF-BRIDGE SYMMETRICAL HYBRID MULTILEVEL INVERTER (IH1ϕ-HB-TC)

From the previous statement we have that in the circuit of figure 3(a) the voltage between the points 'x' and 'y' is always positive or zero. Figure 4(a) shows the arrangement made in the circuit to get a load voltage levels less than zero.

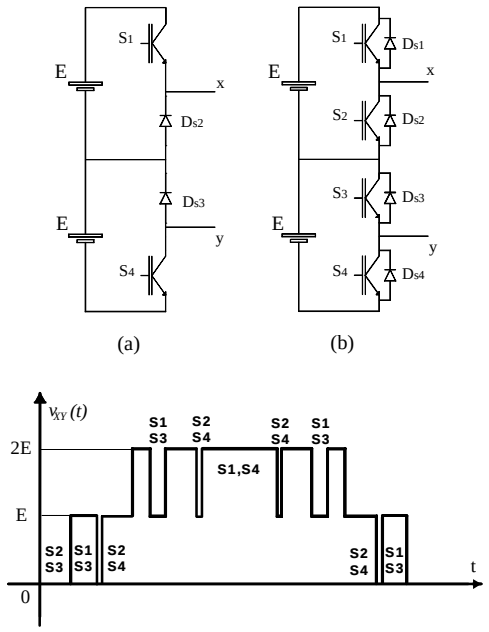
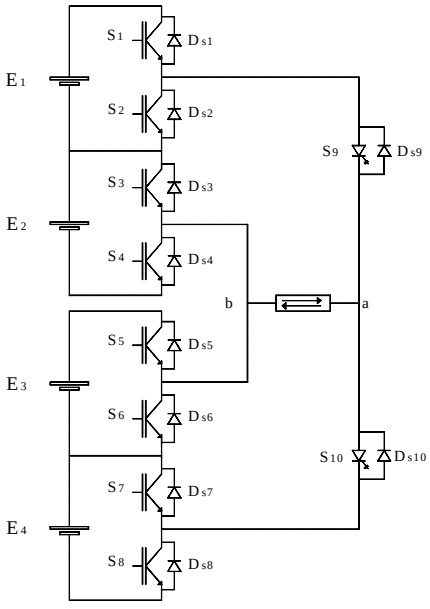
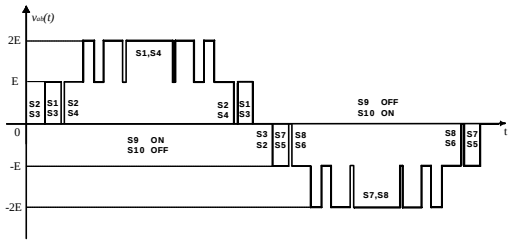


Fig. 3 (a) Redraw of the circuit shown by the Fig.2(a).
(b) Derivation of three-level cell (TC).
(c) Waveform of the voltage between x and y.

As appreciated in figure 4, the topology is an anti parallel connection of two three levels cells, both circuits apply its output voltage to the load through two switches (S_9 for the upper cell, S_{10} for the bottom cell), which work together.

In this case the number of levels in the load voltage is given by: N+1 level, where N represents the number of DC voltage sources, with the same value. From figure 4(a) we have that N is 4, therefore the number of levels in the output voltage is 5 (Fig.4 (b)).





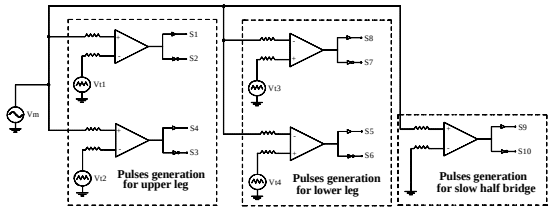
(b)

Fig. 4 (a) Single-phase Half-bridge Symmetrical Hybrid multilevel Inverter, IH1ϕ-HB-TC
(b) Output (Vab) voltage waveform.

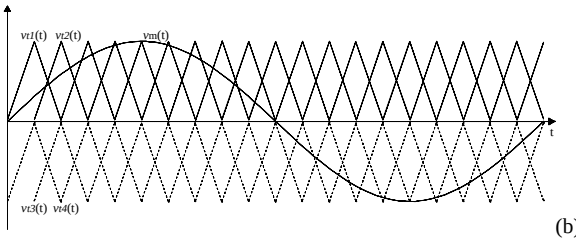
3.1. Modulation strategy

The modulation strategy for the switches drive is based on the technique of sinusoidal pulse wide modulation (PWM). For each cell the signals are generated through the comparison of a modulating signal V_m with two triangular carrier signals (V_{t1} - V_{t2} for the upper cell and $V_{t3} - V_{t4}$ for the bottom cell) to be displaced from another by 180 degree.

To generate the command pulses for the slow switches, the modulating signal is compared with a zero level. The signals generation scheme is shown in figure 5(a). Figure 5(b) presents the waveforms of the reference also called modulating signal and the carrier signal. As illustrated in figure 5(b), the triangular signals for the upper cell are of a positive polarity, while the signals for the bottom cell are of a negative polarity.



(a)



(b)

Fig. 5. (a) Command circuit for the switches of each inverter cell. (b) Modulating signal and carrier.

3.2. Design specifications

To verify the functioning principle IH1ϕ-HB-TC, with the modulation method already presented, a design example is done with the following specifications:

$E = 1.5KV$ $P_o = 120KW$ $f_0 = 50Hz$ $V_{f1} = 2KVrms$
$\cos(f) = 0.8$ $ind.$ $m_i = 0.94$ $R_o = 21.33\Omega$ $L_o = 51mH$
$f_s = 1600Hz$.

Where:

P_o : Output Power
f_0 : Load Fundamental Frequency
V_{f1} : Fundamental effective phase voltage
$\cos(f)$: Load power factor
m_i : Modulation Index
R_o : Load equivalent resistance
L_o : Load equivalent inductance
f_s : Switching frequency

With the previous mentioned, the necessary parameters are defined for the simulation IH1ϕ-HB - TC.

3.3. Single-phase hybrid symmetrical half-bridge multilevel inverter simulations.

In this section we can see the results obtained through digital simulation, with the project data previously pointed out, of the circuit in figure 4. For the circuit simulation is considered all the ideal components. The main waveforms are shown in the following lines. Figure 6 shows the waveform of the output phase voltage IH1ϕ-HB-TC in steady state. In this figure it is possible to appreciate that the level amount in the phase voltage is five levels, -3KV, -1.5KV, 0, 1.5KV and 3KV.

Figure 7 shows the frequency spectrum of this voltage, where it is possible to observe that the high frequency components appear in lateral bands around multiple pairs of the switches commutation frequency.

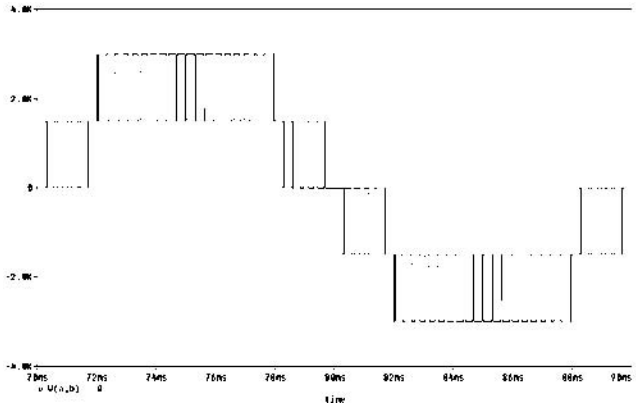


Fig. 6. The generated output phase voltage waveforms $v_{ab}(t)$ in steady state - IH1ϕ-HB-TC.

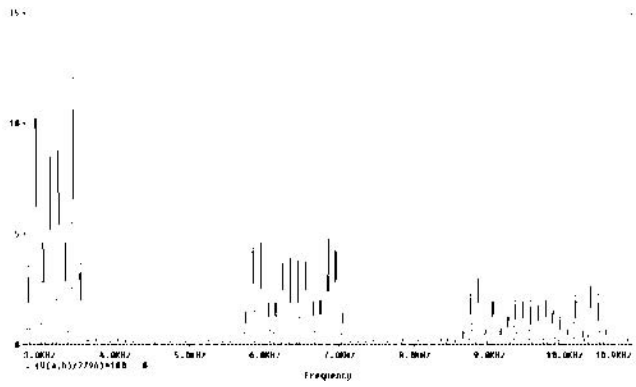


Fig. 7. Frequency spectrum of the load voltage $v_{ab}(t)$ in percentage of the fundamental frequency.

The Fourier analysis for the single-phase inverter voltage indicates 24.30% of THD, a quite acceptable result. The highest phase voltage is 2800V.

The current in the load was practically sinusoidal due to this voltage, with a maximum value of 105A. The outcomes of the Fourier analysis for this current indicate that the highest value of the fundamental component is 105A with a 0.7% THD.

4. SINGLE-PHASE HYBRID SYMMETRICAL FULL-BRIDGE MULTILEVEL INVERTER (IH1ϕ-FB-TC)

It is possible to obtain, starting from the circuit in figure 4(a), a similar waveform to the one shown in figure 4(b), by doing the arrangement shown in figure 8. With a proper actioning pattern of the switches S_1 – S_4, it is possible to obtain a voltage waveform between the points *x-y* as shown in figure 9 The switches S_5 – S_8 and S_6 – S_7 operate every half cycle of the modulating signal, in order that they apply the voltage $v_{xy}(t)$ to the output in an alternated forms. Thus we achieve a voltage format $v_{ab}(t)$, as shown in 12.

Then the circuit of figure 8 behaves as a five-level output voltage single-phase inverter. Of the same way that in the IH1ϕ-HB-TC, the cell switches endure ´E´ voltage value, besides is possible, with a proper modulation technique that they work in high frequency (a few KHz). On the other hand, the full bridge switches (S_5, S_6, S_7 and S_8) must endure a highest voltage level of *'2E'*. However these switches operate only in a semi cycle of the output voltage, therefore its functioning can be in low frequency.

With the previous, it is possible to operate the circuit with fast switches in the cells of the inverter, but that they are able to support low voltage levels and with slow switches in the full bridge, but enduring a higher voltage level. That means that the IH1ϕ-FB-TC can also be classified among the hybrid multilevel inverters group. As shown in [3] and [6], the multilevel inverters based on the full-bridge symmetrical cascade have a number of levels in its output voltage given by 2N+1. For our case, that is for the circuit shown in figure 8 its output voltage levels are also obtained through the same expression. Therefore we have 2N+1 levels in the load, where N is still the number of DC sources.

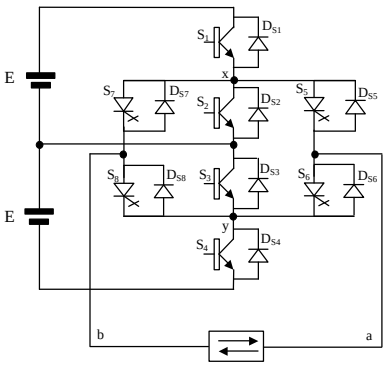


Fig. 8. Single-phase symmetrical hybrid multilevel inverter based on a TC. Full-bridge configuration, IH1ϕ-FB-TC.

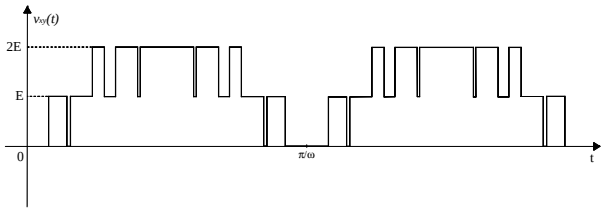
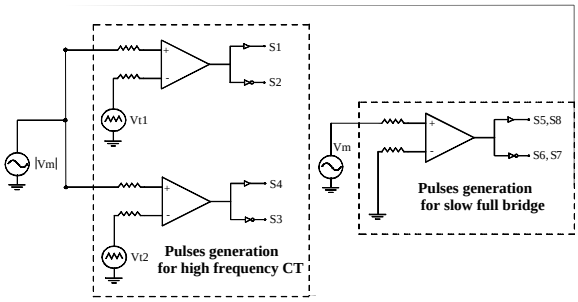


Fig. 9. Voltage waveform between the points x-y.

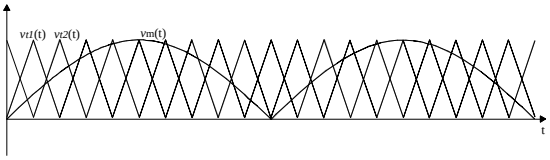
4.1. Modulation strategy

The modulation strategy for the switches actioning is based on the PWM sinusoidal modulation technique.

The signals generation scheme is shown in figure 10(a). Figure 10(b) presents the waveforms of the modulating signal and the carrier signal in a form very similar to the circuit shown in Fig. 4. With this modulation scheme it is possible to generate the command signals for the switches.



(a)



(b)

Fig. 10. (a) Command circuit for the switches of an inverter arm. (b) Modulating signal and carrier signal for an IH1ϕ-FB-TC.

4.2. Design specifications

To verify the functioning principle of the IH1ϕ-FB-CT, with the modulation method already presented, a design example is fulfilled with the same specifications used for the IH1ϕ-HB-TC in the previous section. With this, the parameters are established for the simulation of the IH1ϕ-FB-TC.

4.3. Simulations of the full-bridge single-phase hybrid multilevel inverter.

In this section the outcomes obtained through digital simulation of the circuit are shown in figure 8, with the design data previously pointed out. For the circuit simulation all the ideal components are considered. The main waveforms are shown up next.

Figure 12 shows the output voltage waveform of the IH1ϕ-FB-TC. It is possible to see that the voltage has five levels, -3KV, -1.5KV, 0, 1.5KV and 3KV.

The frequency spectrum of this voltage, in fundamental frequency percentage is shown in figure 13. It is obvious that the frequency spectrum will be identical to the one obtained for the half-bridge multilevel.

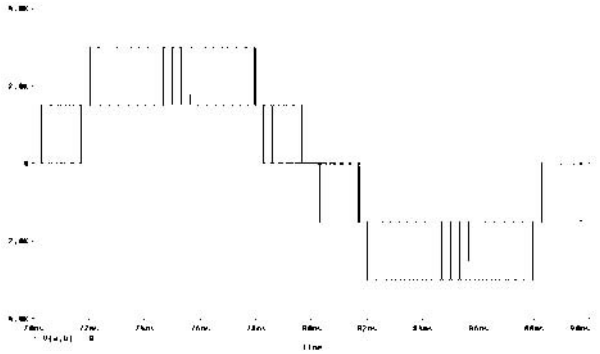


Fig. 12. The generated load voltage waveforms $v_{ab}(t)$ in steady state. - IH1ϕ-FB-TC.

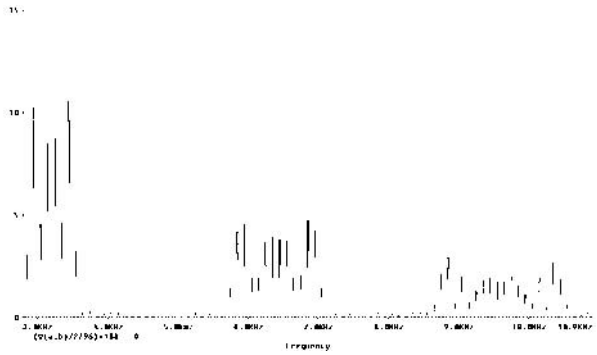


Fig. 13. Frequency spectrum of the output inverter voltage $v_{ab}(t)$ in percentage of the fundamental.

5. THEORETICAL FREQUENCIES SPECTRUM OF THE LOAD VOLTAGE.

This section presents the study of the frequencies spectrum and the total harmonic distortion (THD) for the output voltages of the topologies studied in the previous sections.

The equations that define the output signals are obtained and their main characteristics are studied.
The calculation methodology of these equations is shown in [13].

The expression that defines the load voltage of the single-phase topologies IH1ϕ-HB-TC and IH1ϕ-FB-TC is given by:

$$v_{ab}(t) = 2E\, m_i\, sen(w_1 t) + \sum_{n,par}^{\infty} \sum_{v,impar}^{\infty} \frac{4E}{np} J_v(np\, m_i) \begin{Bmatrix} sen(vw_1 t + nw_s t) \\ + sen(vw_1 t - nw_s t) \end{Bmatrix} \quad (1)$$

Where $J_v(\cdot)$ represents the Bessel function of v order.

When watching the previous expression it is possible to see that the harmonic components exist in lateral bands (vw_1) around multiple pairs of the switching frequency (nw_s), fact already observed in the simulations and ratified by the equation (1). Figure 14 is graphic form of the previous equation normalized with regard to 'E', for a 0.94 modulation index.

The highest amplitude of the harmonic components of the inverter output voltage and its harmonics frequencies are tabulated in table 1 and shown graphically in function of the modulation index m_i in figure 15.

TABLE I
Amplitude of the load voltage harmonic components

Harmonic	Amplitude	Frequency
Fundamental A_1	$A_1 = 2E\, m_i$	w_1
Components $A_{n,v}$ n = 2,4,6... v = 1,3,5...	$A_{n,v} = \frac{4E}{np}\left\|J_v(np\, m_i)\right\|$	$(vw_1 \pm nw_s)$

6. CONCLUSIONS

This article presented the single-phase symmetrical hybrid multilevel inverter circuit based on the three-level cell (IH1ϕ-HB-TC), half-bridge configuration and the associated modulation technique. It was also presented the single-phase symmetrical hybrid multilevel inverter circuit, based on the three-level cell, in full-bridge configuration (IH1ϕ-FB-TC) and its associated modulation technique.

Both circuits are characterized by operating with fast switches in the inverter cell and with slow switches in full-bridge configuration, to transfer the energy to the load. And being these fed through DC sources of the same value (symmetrical hybrid topology), having an alternative to the asymmetrical hybrid multilevel inverter.

The outcomes through digital simulation for both inverters feeding an inductive load were obtained through a simple PWM modulation only needing a sinusoidal reference unlike of that conventional one. From these it was possible to observe that the fast switches that compose every inverter cell endure a maximum voltage equal half the DC link voltage, whereas the maximum voltage endured by the slow switches is equal the entire DC voltage ($2E_i$).

The load waveform obtained, for both circuits, has five levels of voltage and a low harmonic distortion, having also the high frequency components displaced to the double of the carrier frequency, an important matter when projecting the output filter of the inverter.

Unlike the IH1ϕ-HB–TC, the circuit of the IH1ϕ-FB–TC requires fewer switches and less DC voltage sources. However the sources of the IH1ϕ-FB–TC must process double energy, for the same output power than the circuit sources IH1ϕ-HB–TC. Of same way, the effective currents in all switches that compose of the multilevel inverter in full-bridge configuration will be higher than the currents in the all the switches of the IH1ϕ-HB–TC. It is evident that the

most suitable and efficient circuit, which has been presented from former analysis, is that with smaller amount of switches (full bridge configuration).

Through the equations that define the output signals it was possible to confirm the outcomes obtained in simulations, for example, that the frequency spectrum of the signals are known for having harmonic components in lateral bands around multiple pairs of commutation frequency.

The main purpose this article is to introduce two new topologies and that these were an alternative to conventional hybrid multilevel circuit and others.

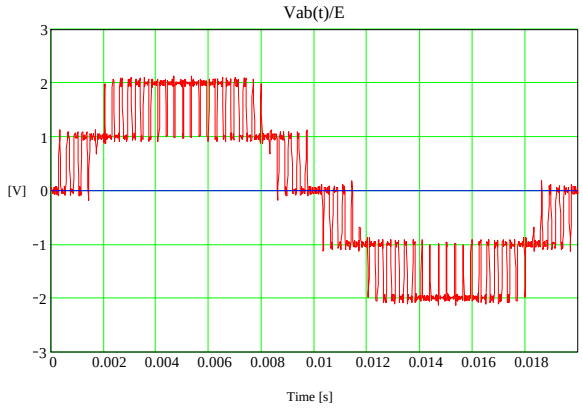


Fig. 14. Equation graph (1), for n=100 and v=25.

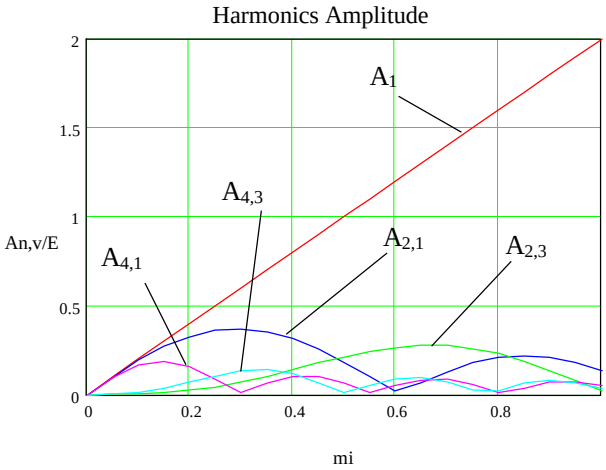


Fig. 15. Harmonic components amplitude of the voltage IH1ϕ-HB-TC e IH1ϕ-FB-TC: A_1 = fundamental component, $A_{n,v}$ = frequency harmonic $(vw_1 \pm nw_s)$; n = 2, 4, 6...; v = 1, 3, 5,...

7. REFERENCES

[1] Madhav D. Manjrekar and Thomas A. Lipo, “A hybrid multilevel inverter topology for drive applications”. Publisher Item identifier S 0-7803-4343-3/98, IEEE-APEC 1998.

[2] Madhav D. Manjrekar, Peter Steimer and Thomas A. Lipo, “Hybrid Multilevel Power Conversion System: a competitive solution for high power applications”. Publisher Item identifier S 0-7803-5589-X/99, IEEE 1999.

[3] Fang Zheng Peng, “A Generalized Multilevel Inverter Topology with Self Voltage Balancing”. IEEE Transactions on Industry Applications, vol. 37, N° 2, march/april 2001.

[4] Leon M. Tolbert, Fang Zheng Peng and Thomas G. Habetler, “Multilevel Converters for Large Electric Drives”. IEEE Transactions on Industry Applications, vol. 35, N° 1, january/february 1999.

[5] Yiqiao Liang and C. O. Nwankpa, “A New Type of STATCOM Based on Casading Voltage-Source Inverters with Phase-Shifted Unipolar SPWM”. IEEE Transactions on Industry Applications, vol. 35, N° 5, september/october 1999.

[6] Fang Zheng Peng, Jih-Sheng Lai, John W. McKeever and James VanCoevering “A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation”. IEEE Transactions on Industry Applications, vol. 32, N° 5, september/october 1996.

[7] Xinbo Ruan, Bin Li and Qianhong Chen. “Three-Level Converters – A New Approach for High Voltage and High Power DC-to-DC Conversion”. PESC Australia 2002.

[8] Jih-Sheng Lai and Fang Zheng Peng. “Multilevel Converters – A New Breed of Power Converters”. IEEE Transactions on Industry Applications, vol. 32, N° 3, may/june 1996.

[9] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng. “Multilevel Inverters: A Survey of Topologies, Controls, and Applications”. IEEE Transactions on Industrial Electronics, vol. 49, N° 4, august 2002.

[10] Thierry A. Meynard, Henri Foch, Francois Forest, Christophe Turpin, Frédéric Richardeau, Laurent Delmas, Guillaume Gateau, and Elie Lefeuvre. “Multicell Converters: Derived Topologies”. IEEE Transactions on Industrial Electronics, vol. 49, N° 5, October 2002.

[11] Gui-Jia Su. “Multilevel DC-Link Inverter”. IEEE Transactions on Industry Applications, vol. 41, N° 3, may/june 2005.

[12] A. Nabae, I. Takahashi and H. Akagi. “A New Neutral-Point-Clamped PWM Inverter”. IEEE Transactions on Industry Applications, vol. IA-17, No. 5, pp 518-523, 1981.

[13] Reynaldo Ramos Astudillo. “Familia de Inversores Multinivel Híbridos para Aplicaciones en Alta Tensión y Alta Potencia”. Tesis para Optar al Grado de Magíster en Ingeniería. Capitulo 2-3-5. PUCV – Chile año 2006.