GENERALIZED MODULATION STRATEGY FOR MATRIX CONVERTERS CONSIDERING UNBALANCED LOADS AND UNBALANCED INPUT VOLTAGES

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***Abstract*— In this paper, the generalized scalar pulse-width modulation technique used in inverters is adapted to the matrix converters. Three different modulation techniques for matrix converters are exposed by a different point of view. The input current control defines which input voltages are employed to synthesize the output voltages of the matrix converter. Simulation results show that the most known control strategies for matrix converters can be implemented through this concept. Situations with unbalanced loads and unbalanced input voltages are also tested.**

***Keywords* - AC-AC Power Conversion, Frequency Converters, Pulse Width Modulation, Simulation.**

I. INTRODUCTION

The first study about direct AC-AC frequency converters was presented in 1976 by *Gyugyi* and *Pelly* [1]. Later, in 1980, *Venturini* and *Alesina* introduced the term "Matrix Converter" (Fig. 1) and presented the first algorithm capable of synthesizing output sinusoidal reference voltages, from a balanced three-phase voltage source connected to the converter input terminals [2][3]. In some Pulse-Width Modulation (PWM) techniques, the input voltage of one phase is not used during many consecutive switching periods for synthesizing the output voltages, making the respective input current zero for a long time and producing low order current harmonics [4]. Other techniques use the three input voltages to produce the output voltages, improving the input current waveforms. Some researchers presented control techniques for controlling simultaneously the desired output voltages and input currents [2][5]. However, there is not a study that generalizes the implementation of all these techniques.

In this paper, the generalized PWM technique for the input currents and output voltages control of matrix converters is tested for different situations with unbalanced loads and unbalanced input voltages. The mentioned generalization of the proposed strategy is related to the capability to obtain any of the previous PWM techniques through modification of its parameters. In "Generalized Modulation Strategy for Matrix Converters - Parts I and II"[6][7], the details about how this technique implements each of the well-known PWM schemes is presented.

II. THE PROPOSED GENERALIZED STRATEGY

A possible "dissociation" between the input currents and the output voltages control in the matrix converters was

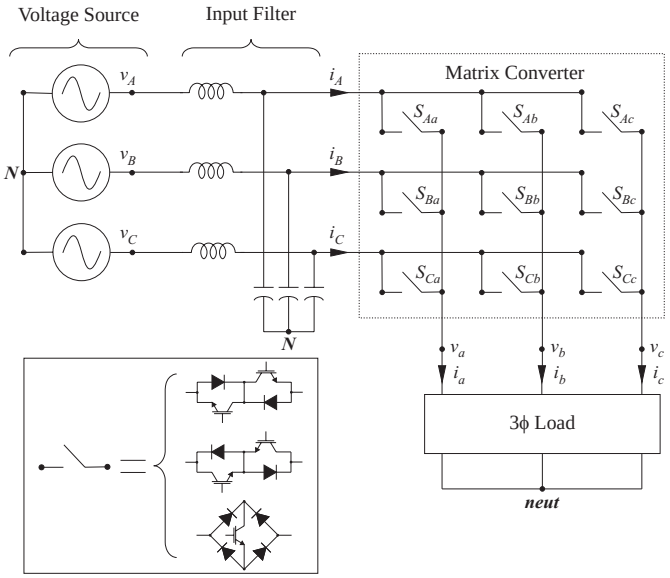


Fig. 1: Structure of a matrix converter.

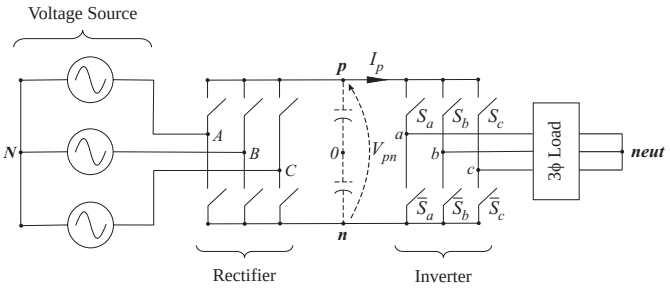


Fig. 2: Topology used to understand the proposed strategy.

proposed by *Huber* and *Borojevic* [8]. They presented a vector PWM technique based on a structure similar to the AC-DC-AC converters, but without the DC link capacitor (Fig. 2). The difference between this topology and the matrix converter is that only one or two of the input voltages may be connected to the output load terminals: the input voltages connected to the points p and n in Fig. 2. These voltages are chosen in the input currents control algorithm and, after that, it is possible to synthesize the desired output voltages of the matrix converter (Fig. 1).

A. Input Currents Control

Let $i_A^*(t)$, $i_B^*(t)$ and $i_C^*(t)$ be the normalized desired input currents, i. e., the input currents divided by the absolute value of the input current vector:

$$\begin{cases} i_A^*(t) = \cos(\omega_i t + \phi_i) \\ i_B^*(t) = \cos(\omega_i t + \frac{2\pi}{3} + \phi_i) \\ i_C^*(t) = \cos(\omega_i t + \frac{4\pi}{3} + \phi_i) \end{cases}, \quad (1)$$

where ω_i is the angular frequency of the grid and ϕ_i is the desired displacement between the input currents and input voltages.

In order to determine which input voltages will be connected to the points p and n of Fig. 2, the following steps are used:

1) organize the normalized desired input currents in (1) in the growing order of their absolute values, where i_{max} is the normalized desired input current that has the highest absolute value, i_{int} is the normalized desired input current that has the intermediate absolute value and i_{min} is the normalized desired input current that has the lowest absolute value;
2) the time intervals Δt_{minc} and Δt_{intc} are:

$$\Delta t_{minc} = |i_{min}|T_s, \ \Delta t_{intc} = |i_{int}|T_s, \quad (2)$$

where Δt_{minc} and Δt_{intc} are the time intervals during which the input voltages related to i_{min} and i_{int}, respectively, will be connected to p or n.
3) determine the signal of i_{max}:
   a) if the signal of i_{max} is positive, the input voltage related to i_{max} will be connected to p during the period $\Delta t_{minc} + \Delta t_{intc}$ and the input voltages related to i_{min} and i_{int} will be connected to n during the time intervals Δt_{minc} and Δt_{intc}, respectively;
   b) if the signal of i_{max} is negative, the input voltage related to i_{max} will be connected to n during the period $\Delta t_{minc} + \Delta t_{intc}$ and the input voltages related to i_{min} and i_{int} will be connected to p during the time intervals Δt_{minc} and Δt_{intc}, respectively.

A third interval Δt_{m0} completes the switching period. During Δt_{m0}, $v_{pn} = 0$, since the same voltage is applied to the points p and n: $v_p = v_n = v_K$ ($K = \{A, B \text{ or } C\}$).

B. Output Voltages Control

To simplify the comprehension of the duty cycles of the switches using the generalized scalar PWM, a general analysis of the inverter stage in Fig. 2 is done.

Assuming that the load currents do not have zero-sequence components, the instantaneous voltages between the output terminals of the inverter and the load neutral point are written as:

$$\begin{bmatrix} v_{aneut}(t) \\ v_{bneut}(t) \\ v_{cneut}(t) \end{bmatrix} = \frac{v_{pn}(t)}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix}, \quad (3)$$

where v_{jneut} is the voltage between phase j ($j = \{a, b \text{ or } c\}$) and the load neutral point ($neut$), v_{pn} is the instantaneous voltage between points p and n and $S_j(t)$ is the switching function of the output terminal j which can be defined as:

$$S_j(t) = \begin{cases} 1 \Rightarrow & \text{switch } S_j \text{ closed} \\ 0 \Rightarrow & \text{switch } S_j \text{ open} \end{cases}. \quad (4)$$

The switching function $\overline{S}_j$ is the complement of S_j.

The average values of the inverter output voltages in the k^{th} switching period are given by:

$$\begin{bmatrix} \overline{v}_{aneut}[k] \\ \overline{v}_{bneut}[k] \\ \overline{v}_{cneut}[k] \end{bmatrix} = \frac{V_{pn}[k]}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \tau_a[k] \\ \tau_b[k] \\ \tau_c[k] \end{bmatrix}, \quad (5)$$

where $\overline{v}_{jneut}$ is the average value of the output voltage in terminal j and τ_j is the duty cycle of S_j, which is defined as:

$$\tau_j = \frac{\Delta t_j}{T_s}, \quad (6)$$

Δt_j being the time interval in which S_j stays closed in T_s.

To solve (5) it is necessary to analyze the matrix $\mathbf{P}$ defined as:

$$\mathbf{P} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}. \quad (7)$$

The rank of the matrix $\mathbf{P}$ is equal to 2, then, only two phase voltages are linearly independent, due to the ungrounded neutral of the load. Therefore, there are infinite combinations of τ_a, τ_b and τ_c that satisfy (5). These infinite combinations are related to infinite values that the "distribution" parameter μ can assume. Nevertheless, if one of the duty cycles (τ_j) is imposed, the others will be uniquely defined as:

$$\begin{cases} \tau_a[k] = \tau_j[k] + \frac{1}{V_{pn}[k]}[\overline{v}_{aneut}[k] - \overline{v}_{jneut}[k]] \\ \tau_b[k] = \tau_j[k] + \frac{1}{V_{pn}[k]}[\overline{v}_{bneut}[k] - \overline{v}_{jneut}[k]] \\ \tau_c[k] = \tau_j[k] + \frac{1}{V_{pn}[k]}[\overline{v}_{cneut}[k] - \overline{v}_{jneut}[k]] \end{cases} \quad (8)$$

Considering the capacitors of the fictitious DC link identical, the following relation can be written:

$$V_{p0} = -V_{n0} = \frac{V_{pn}}{2}, \quad (9)$$

where V_{p0} and V_{n0} are the voltages between points p and n, respectively, and the central point "0" of the fictitious DC link in Fig. 2.

The same situation occurs in the inverters with a DC link (capacitor bank). As the inverter structure, it is possible to achieve the particular solution of (5):

$$\begin{cases} \tau_a[k] = \frac{v_a^*[k]}{V_{pn}[k]} + \frac{1}{2} \\ \tau_b[k] = \frac{v_b^*[k]}{V_{pn}[k]} + \frac{1}{2} \\ \tau_c[k] = \frac{v_c^*[k]}{V_{pn}[k]} + \frac{1}{2} \end{cases}. \quad (10)$$

where v_j^* is the desired output voltage of the terminal j ($j = \{a, b \text{ or } c\}$) referenced to the central point "0" of the fictitious DC link.

This particular solution yields sinusoidal output phase voltages. The maximum output voltage achieved with the particular solution is $\frac{V_{pn}}{2}$, as can be seen in (10). If the voltage V_{pn} is constant, the maximum voltage ratio is given by:

$$q_{max} = \frac{V_{omax}}{V_i} = \frac{3}{4}\cos\phi_i. \quad (11)$$

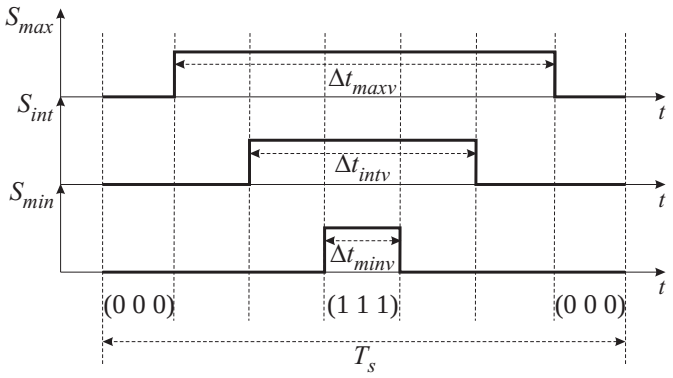


Fig. 3: Possible switching pattern of an inverter.

With the particular solution, it is possible to achieve 75% in the voltage ratio.

In order to generalize the PWM technique, it is necessary to determine the biggest (τ_{max}), the intermediate (τ_{int}) and the smallest (τ_{min}) of the three duty cycles in (10). Suppose that Fig. 3 presents the switching pattern of S_{max}, S_{int} and S_{min} corresponding to solution (10) when the pulses are centralized in T_s.

Observing Fig. 3, it is seen that the time interval in which S_a, S_b and S_c are closed (1 1 1) always coincides with Δt_{minv} and that the time interval in which S_a, S_b and S_c are open (0 0 0) is equal to $T_s - \Delta t_{maxv}$. Further, it can be observed that augmenting or reducing the widths of the three pulses by the same amount of time does not affect the mean values of the three phase voltages. The generalization of the inverter PWM technique [9] regards the way that the states (1 1 1) and (0 0 0) are used in the switching pattern. To generalize the duty cycles, the time intervals for applying the the states (1 1 1) and (0 0 0) are weighted and added to the duty cycles of the particular solution (10). This general solution is given by:

$$\tau_j^G[k] = \tau_j[k] - \mu\frac{\Delta t_{minv}}{T_s} + (1-\mu)\left(1 - \frac{\Delta t_{maxv}}{T_s}\right), \quad (12)$$

where $\tau_j[k]$ is defined using (10) and $0 \leq \mu \leq 1$. The parameter μ is named as the "distribution" parameter.

All this generalization process can be described in the following algorithm:

1) determine the particular solution for the duty cycles in (10);
2) choose μ and calculate the generalized duty cycles using (12).

With the input current control in the rectifier stage (II-A) and the duty cycles of the inverter stage determined in (12), an adaptation of both controls to the matrix converters topology can be made.

C. Input Currents and Output Voltages Simultaneous Control

Since the switching period is divided in three time intervals, two of them with different input voltages connected to the points p and n, it is necessary to weight the duty cycles of the output voltages obtained in (12) with m_1 and m_2 given by:

$$m_1 = \frac{\Delta t_{m1}}{T_s}, \quad (13)$$

$$m_2 = \frac{\Delta t_{m2}}{T_s}, \quad (14)$$

where Δt_{m1} can be equal to Δt_{intc} or Δt_{minc}, depending of the chosen switching sequence. If $\Delta t_{m1} = \Delta t_{intc}$, $\Delta t_{m2} = \Delta t_{minc}$, otherwise $\Delta t_{m1} = \Delta t_{minc}$ and $\Delta t_{m2} = \Delta t_{intc}$.

Therefore, the duty cycles in (12) are distributed to each v_{pn} of m_1 and m_2. The weighted duty cycles of the output voltages are:

$$\tau_{jm_1}[k] = \frac{\Delta t_{jm_1}[k]}{T_s} = m_1[k]\tau_j^G[k], \quad (15)$$

$$\tau_{jm_2}[k] = \frac{\Delta t_{jm_2}[k]}{T_s} = m_2[k]\tau_j^G[k], \quad (16)$$

where Δt_{jm_1} is the time interval during which the output terminal j is connected to the input voltage v_p associated with m_1 and Δt_{jm_2} is the time interval during which the output terminal j is connected to the input voltage v_p associated with m_2.

In each switching period, during $\Delta t_{m_1} + \Delta t_{m_2}$ either the input voltage associated with p or the input voltage associated with n does not change. In the scalar current control, v_p does not change if the signal of i_{max} is positive and v_n does not change if the signal of i_{max} is negative.

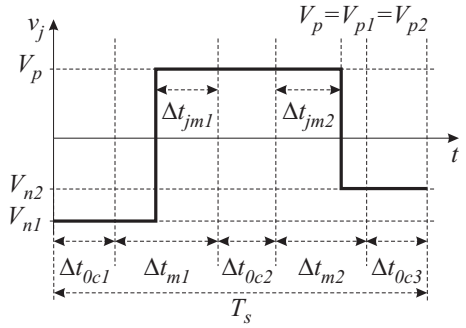
The switching pattern used in the matrix converter for each output terminal j is described as follow:

- divide $\Delta t_{m0} = T_s - (\Delta t_{m1} + \Delta t_{m2})$ in three time intervals: Δt_{m01}, Δt_{m02} and Δt_{m03}.
- if V_p should be connected to the same input during Δt_{m_1} and Δt_{m_2} ($V_{p1} = V_{p2} = V_p$):
  1) apply V_{n1} from the beginning of the switching period until $(\Delta t_{m01} + \Delta t_{m1} - \Delta t_{jm1})$;
  2) apply V_p from $(\Delta t_{m01} + \Delta t_{m1} - \Delta t_{jm1})$ to $(\Delta t_{m01} + \Delta t_{m1} + \Delta t_{m02} + \Delta t_{jm2})$;
  3) apply V_{n2} during the rest of T_s.
- if V_n should be connected to the same input during Δt_{m_1} and Δt_{m_2} ($V_{n1} = V_{n2} = V_n$):
  1) apply V_{p1} from the beginning of the switching period until $(\Delta t_{m01} + \Delta t_{jm1})$;
  2) apply V_n from $(\Delta t_{m01} + \Delta t_{jm1})$ to $(\Delta t_{m01} + \Delta t_{m1} + \Delta t_{m02} + \Delta t_{m2} - \Delta t_{jm2})$;
  3) apply V_{p2} during the rest of T_s.

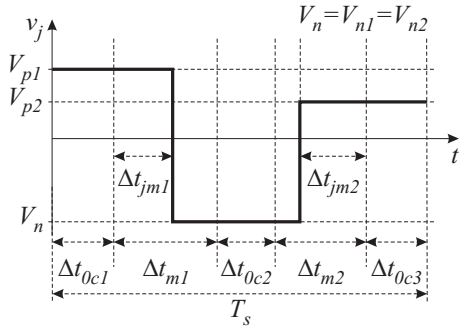
Both cases are illustrated in Fig. 4.

The following algorithm summarizes the proposed general approach for PWM techniques:

1) use the input currents control strategy to determine m_1 and m_2;
2) determine the generalized duty cycles of the command output voltages using the scheme described in section II-B;
3) calculate the weighted duty cycles adapted to the matrix converter from (15) and (16);
4) follow the switching pattern described in this section.



(a) V_p does not change during $\Delta t_{m_1} + \Delta t_{m_2}$



(b) V_n does not change during $\Delta t_{m_1} + \Delta t_{m_2}$

Fig. 4: Switching pattern in the proposed technique.

III. EXAMPLE OF THE GENERALIZATION

The proposed generalization may be used to implement any of the previous PWM techniques and the most popular PWM techniques are used to exemplify the generalization of the new strategy.

A. Alesina and Venturini's (AV) Technique

It is demonstrated that distorting the output phase voltages, the output voltage limit can be increased to 86.6% of the input voltage amplitude [10][11].

In (10), v_j^* is referenced to the central point of the fictitious DC link. It was shown in [7] that the distorted voltage ($v_j^{*'}$) does not depend of the third harmonic component of the input frequency:

$$v_j^{*'} = v_j^* + qV_i \left\{ -\frac{1}{6} \cos\left(3\omega_o t\right) \right\}, \qquad (17)$$

and the general solution for the AV's technique is given by:

$$\tau_j^G[k] = \tau_j[k] + \frac{qV_i}{V_{pn}} \left\{ -\frac{1}{6} \cos\left(3\omega_o t\right) \right\}, \qquad (18)$$

where these times are equivalent to the distorted voltage referenced to the central point of the fictitious DC link. The output voltages referenced to "N" in the AV's technique are shown in Fig. 5 for $q = 86.6\%$.

B. Rodriguez's Technique

To adapt the generalized PWM technique to the *Rodríguez*'s technique [4], the most positive and the most negative input voltages are connected to the points p and n, respectively, during all the switching period. To ensure this condition, the duty cycles used in the input current strategy

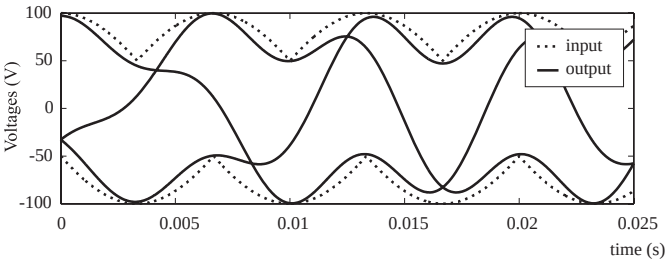


Fig. 5: Output voltages in the AV's technique for $q = 86.6\%$.

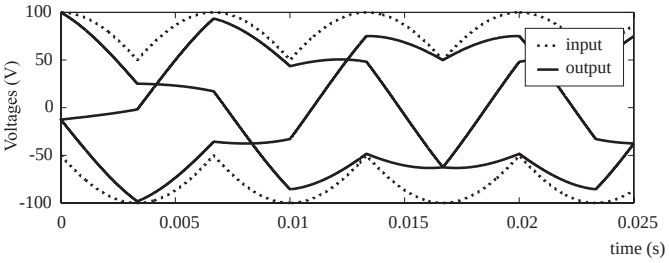


Fig. 6: Output voltages in the *Rodríguez*'s technique for $q = 75\%$.

are: $m_1 = 1$ and $m_2 = m_0 = 0$, and v_{pn} is the biggest input line-to-line voltage. In the output voltage control, the particular solution (10) is used for obtaining the duty cycles of S_j. The output voltages referenced to "N" in the *Rodríguez*'s technique are shown in Fig. 6 for $q = 75\%$. It can be seen that this is the real limit for the technique proposed by *Rodríguez* and $q > 75\%$ results in output voltages that can not be made from "pieces" of the input voltages.

C. Huber and Borojevic's (HB) Technique

To obtain the HB's technique [8] from the generalized PWM technique, m_1, m_2 and m_0 of the input current control are calculated in according to section II-A. The distribution of m_0 in the switching pattern is described as: $m_{01} = m_{03} = 0$ and $m_{02} = m_0$ (Fig. 4). In the output voltage control, the general solution (12) is used for obtaining the duty cycles of S_j. If i_{max} (input current that has the highest absolute value) is positive, $\mu = 0$ is chosen and if i_{max} is negative, $\mu = 1$ is chosen (pulsed μ pattern). The output voltages referenced to "N" in the HB's technique are shown in Fig. 7 for $q = 86.6\%$.

IV. PROPOSED TECHNIQUES

Klumpner and *Blaabjerg* proposed an adaptation of the HB's technique for the two-stage direct power converter topology presented in Fig. 2 [12]. In this case, m_1 and m_2

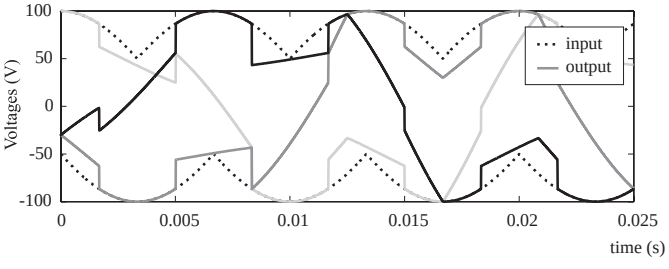


Fig. 7: Output voltages in the HB's technique for $q = 86.6\%$.

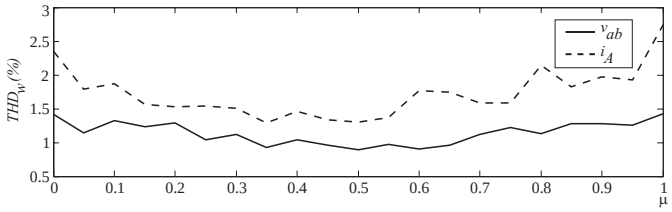


Fig. 8: THD_w for input current and output voltage ($q = 50\%$).

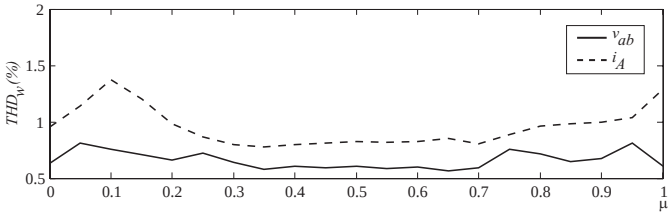


Fig. 9: THD_w for input current and output voltage ($q = 86.6\%$).

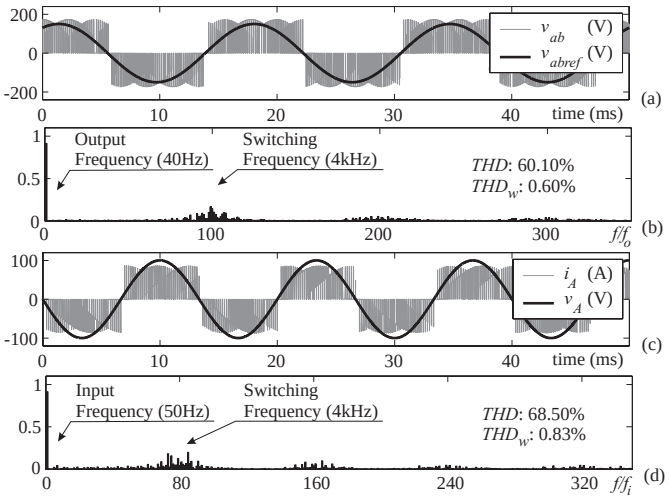


Fig. 11: Simulation results for PT1 with $q = 86.6\%$ and $\mu = 0.5$).

are adjusted and expressed by:

$$m_1' = \frac{m_1}{m_1 + m_2}, \tag{19}$$

$$m_2' = \frac{m_2}{m_1 + m_2}. \tag{20}$$

A. Technique 1

In the Proposed Technique 1 (PT1), m_1 and m_2 are calculated in the same way as in (13) and (14) and their values are adjusted with (19) and (20). Therefore, in this technique, $m_{0c} = 0$.

In PT1, there is only one parameter to adjust (μ). Using the generalized solution in (12), different distributions of the zero voltage vectors (different values of μ) are used to study the harmonic distortion of the input currents and line-to-line output voltages. Figures 8 ($q = 50\%$) and 9 ($q = 86.6\%$) show the weighted total harmonic distortion (THD_w) of phase A input current and line-to-line output voltage v_{ab} for different values of μ. In terms of THD_w, with $q = 50\%$, the best results for both input currents and output voltages occurred with $\mu = 0.5$. With $q = 86.6\%$, the best results for the input currents occurred with $\mu = \frac{1}{3}$ and for the output voltages occurred with $\mu = \frac{2}{3}$. The output voltages referenced to "N" in the PT1 are shown in Fig. 10 for $q = 86.6\%$ and $\mu = 50\%$. Figure 11 shows the simulation results with a load angle of 30° connected to the matrix converter output. It can be seen the frequency spectrum of the unfiltered input current and output voltage for the PT1. The PT1 presents dominant harmonics only in switching frequency multiples.

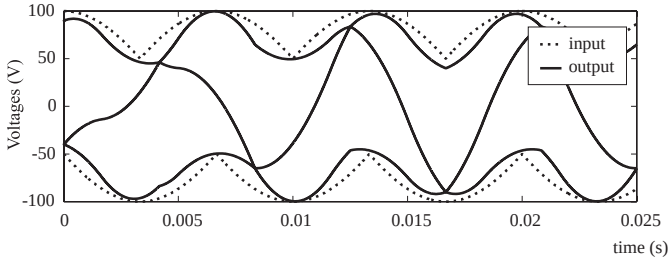


Fig. 10: Output voltages in the PT1 for $q = 86.6\%$ and $\mu = 0.5$.

B. Technique 2

Different from PT1, in the proposed technique 2 (PT2), m_1 and m_2 are calculated in the same way as in (13) and (14) (in this technique, $m_{0c} \neq 0$). The generalized solution in (12) is used and the total time for obtaining zero voltage in the fictitious DC link (zero vector in the matrix converter) is divided in three identical times for the three possibilities (three zero vectors). The main idea of PT2 is divide the total zero vector application time equally to all zero vectors of matrix converter, the same way as inverters. With the proposed generalized strategy, this can be obtained observing a new definition of the total zero vector application time:

$$t_{00} = \Delta t_{0v}(m_1 + m_2) + m_{0c}T_s \tag{21}$$

and the three times of Fig. 4 for PT2 are:

- if $V_{p1} = V_{p2} = V_p$:
  $\Delta t_{0c1} = t_{00}/3 - \mu\Delta t_{0v}m_1$
  $\Delta t_{0c2} = t_{00}/3 - (1-\mu)\Delta t_{0v}(m_1 + m_2)$
  $\Delta t_{0c3} = t_{00}/3 - \mu\Delta t_{0v}m_2$
- if $V_{n1} = V_{n2} = V_n$:
  $\Delta t_{0c1} = t_{00}/3 - (1-\mu)\Delta t_{0v}m_1$
  $\Delta t_{0c2} = t_{00}/3 - \mu\Delta t_{0v}(m_1 + m_2)$
  $\Delta t_{0c3} = t_{00}/3 - (1-\mu)\Delta t_{0v}m_2$

The output voltages referenced to "N" in the PT2 are shown in Fig. 12 for $q = 86.6\%$. Figure 13 shows the simulation results with a load angle of 30° connected to the matrix converter output. It can be seen the frequency spectrum of the unfiltered input current and output voltage for the PT2. The PT2 presents dominant harmonics only in switching frequency multiples.

V. MODULATION TECHNIQUES COMPARISON

$MATLAB^{®}$ was the software used for all simulations presented in this paper. The converter was considered to be fed by an balanced ideal voltage source with the following characteristics: voltage amplitude (V_i) of $100V$ and frequency (f_i) of $50Hz$. For the output terminals of the matrix converter, it is desired a frequency (f_o) of $40Hz$. The balanced inductive load, with displacement factor of $\cos 30° = 0.866$ and unity

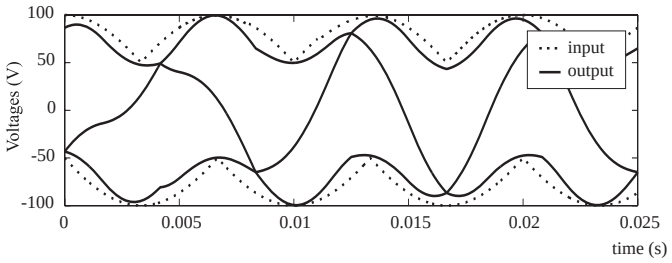


Fig. 12: Output voltages in the PT2 for $q = 86.6\%$.

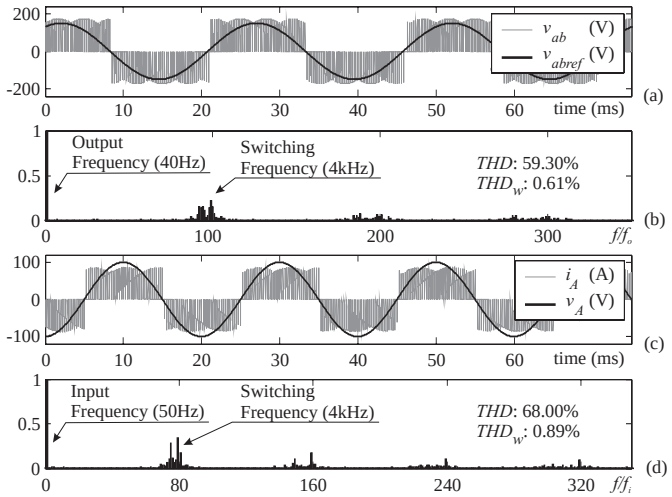


Fig. 13: Simulation results for PT2 with $q = 86.6\%$.

impedance, has the following characteristics: inductance of $2mH$ and resistance of 0.87Ω. The bidirectional switches are considered ideal and the switching frequency (f_s) is $4kHz$.

The Total Harmonic Distortion (THD) and the weighted THD (THD_w) are defined as:

$$THD = \left\{ \frac{\sum_{h=2}^{\infty} F_{rms}(h)^2}{F_{rms}(1)^2} \right\}^{1/2} 100\% \qquad (22)$$

$$THD_w = \left\{ \frac{\sum_{h=2}^{\infty} (\frac{F_{rms}(h)}{h})^2}{F_{rms}(1)^2} \right\}^{1/2} 100\% \qquad (23)$$

In practice, the higher harmonic component of the THD and THD_w that can be calculated is equal to half of the sample frequency of the input and output signals (in all simulations the sample frequency was $100kHz$). Then, all THD and THD_w have harmonic components up to $50kHz$.

The original AV's, *Rodriguez*'s and HB's techniques are simulated. Besides the original techniques, PT2 and three PT1 are simulated: PT1a with $\mu = \frac{1}{3}$, PT1b with $\mu = 0.5$ and PT1c with $\mu = \frac{2}{3}$. The following comparisons between techniques are made.

Figures 14 and 15 present a comparison of the output line-to-line voltages and the input currents, respectively, for all techniques with $q = 50\%$, $q = 75\%$ and $q = 86.6\%$. It can be seen that the PT1 present the best results in terms of THD_w for the output voltages for low values of q (50%). When q increases, the PT1 performance is similar to the HB's technique, with PT1b and PT1c having the best results. Rodriguez's and AV's techniques do not present good results.

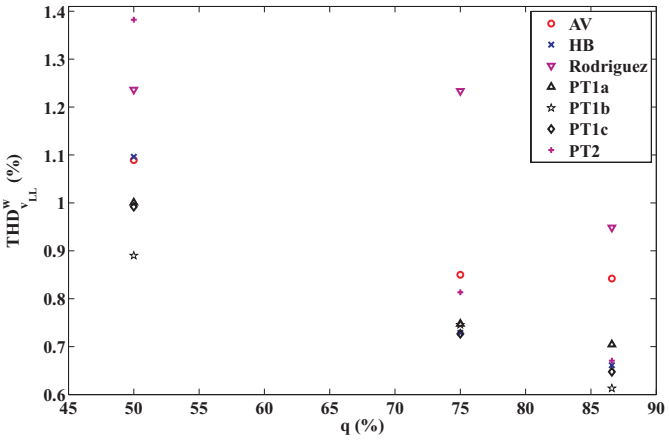


Fig. 14: THD_w for the output line-to-line voltage without input filter.

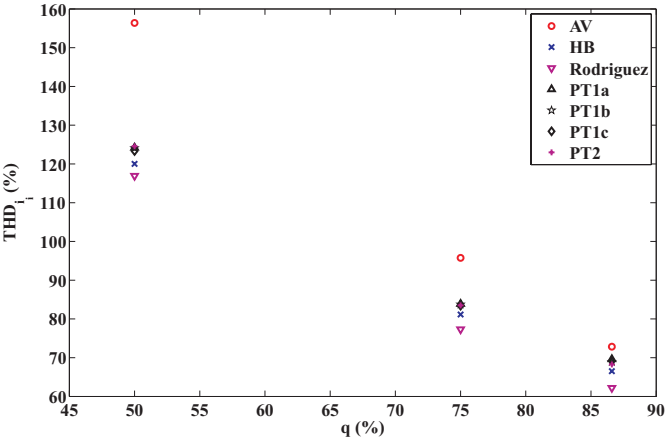


Fig. 15: THD for the input current without input filter.

For the THD of the input currents, the Rodriguez's and HB's techniques present the best results for all range of q. The worst results are for the AV's technique. The proposed techniques (PT1 and PT2) have intermediates values.

Due to the direct frequency conversion, the matrix converter does not need bulky storage devices used in the traditional converters. Thus, reactive elements are only necessary to compose the input and the output filters. Due to its inductive nature, the load can be used as an output filter for the high frequency components of the output voltages. Therefore, the output line currents are sinusoidal (with low ripple due to low order harmonics).

It is also important to test the techniques considering the effect of the input filter in the matrix converter (Fig. 2). Two different filter topologies was simulated: the star-connected LC filter (Fig. 2) and the delta-connected LC filter. The results of the delta and star-connected filters are very similar and therefore the star-connected filter is used in all following simulations. The components of the filter have the following characteristics: inductance of $5mH$, inductance stray resistance of 0.01Ω and capacitance of $330\mu F$. The cut-off frequency of the filter is approximately $124Hz$. Without any output filter, it is reasonable to use the THD_w for the input currents because it represents the distortion taking into account a higher contribution of the low order harmonics. Using the input filter, the high frequency components are

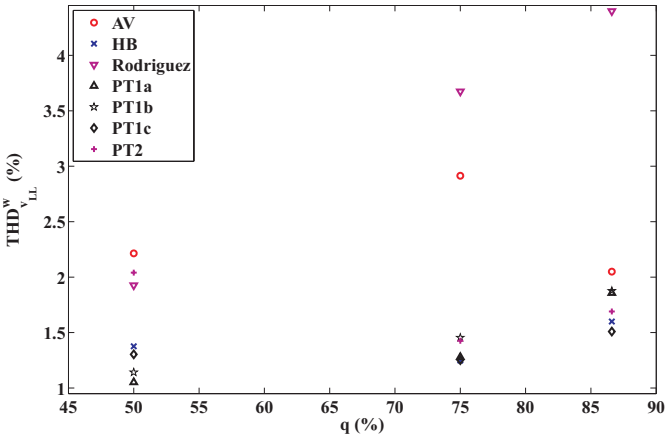


Fig. 16: THD_w for the output line-to-line voltage with input filter.

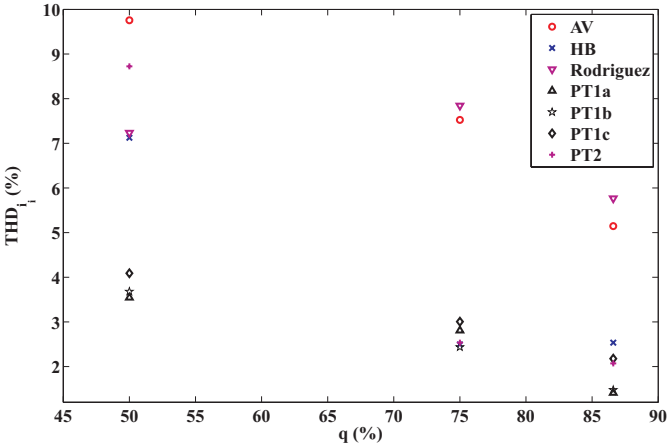


Fig. 17: THD for the input current with input filter.

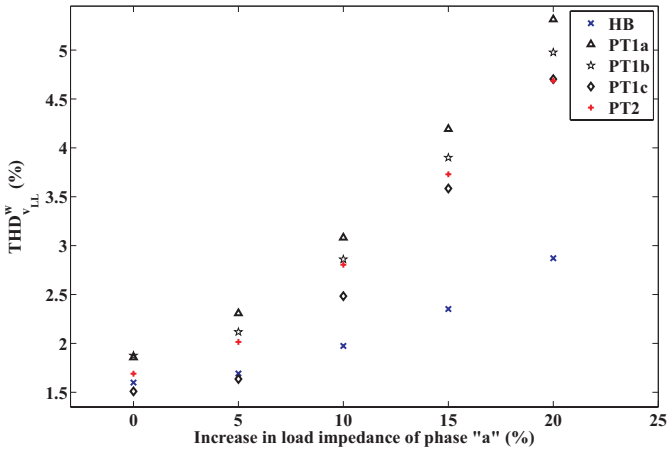


Fig. 18: THD_w for the output line-to-line voltage with unbalanced loads.

filtered and only the THD will be discussed for the input currents.

Figures 16 and 17 present comparisons of the output line-to-line voltages and the input currents considering the input filter of the matrix converter. It can be seen that the PT1c and HB's techniques present the best result in terms of THD_w for the output voltages. The PT1c is the best for $q = 50\%$ and $q = 86.6\%$. The performance of PT1a, PT1b and PT1c are very similar. The PT2, Rodriguez's and AV's techniques have similar performances with no good results. The results without input filter (Fig. 14) and with input filter (Fig. 16) are equivalent in terms of comparison among the techniques, showing that the input filter does not change considerably the output voltages. AV's and Rodriguez's techniques present bad results for the input currents. The PT2 and the HB's techniques have good performance for high values of q, but the PT1a and PT1b present the best results.

Considering the combined results for output voltages and input currents (with and without input filter), the AV's and Rodriguez's techniques present the worst general performance and they will not be used for the simulations considering unbalanced loads and unbalanced input voltages. Due to the unbalanced conditions, phases *a*, *b* and *c* present different values of THD_w and THD for the output line-to-line voltages and the input currents, respectively. Therefore, in this paper, the critical values (the maximum values among the three phases) of THD_w and THD were used to compare the techniques.

Figures 18 and 19 present a comparison among the techniques for $q = 86.6\%$ considering unbalanced loads with the input filter in the matrix converter. Progressive increases by 5% in the impedance of the load of phase *a* are considered up to a maximum of 20%. It is important to note that the displacement factor of the load does not change in all simulations. For example: for unbalance of 20%, the inductance of phase *a* increases by 20% and its final value is $2.4mH$; the resistance increases to 1.04Ω.

The HB's technique only presents best results with highly unbalanced loads considering the THD_w for the output voltages and the THD for the input currents. Among the proposed techniques, the PT1c and PT2 present the best performance for the output voltages and the input currents, respectively, with acceptable unbalanced loads.

Unbalanced input voltages are also tested increasing the amplitude of the phase *A* voltage by 5%, 10%, 15% and 20% ($105V$ to $120V$) and keeping the amplitude in phase *B* in $100V$ (Figures 20 and 21). Phase *C* is obtained by the relation $v_A + v_B + v_C = 0$. In these unbalanced conditions, the input filter of the matrix converter was considered and the amplitude of the output voltages are fixed in $85V$ ($q = 85\%$), because this is the maximum value that can be used in the critical abnormal condition (20%).

It can be seen that the PT1c presents the best results for the output voltages with acceptable values of unbalance (Fig. 20). The PT2 and HB's technique are good in almost all range, but PT2 presents the worst result for 20%. For the input currents (Fig. 21), the HB's technique has the worst results for low values of unbalance (up to 10%) and the best results for high values of unbalance (15% and 20%). The PT1 and PT2 present good results for low values of unbalance, with PT2 having the best performance for 20%.

VI. CONCLUSION

This paper presents a new strategy to control the switches of the matrix converter based in the indirect frequency converter. The proposed strategy can be modified for being equivalent to the previously proposed modulation techniques for matrix converters. The simulation results show that all

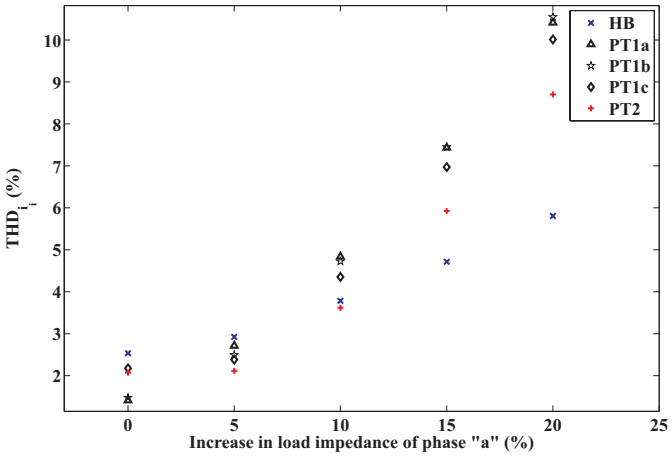


Fig. 19: THD for the input current with unbalanced loads.

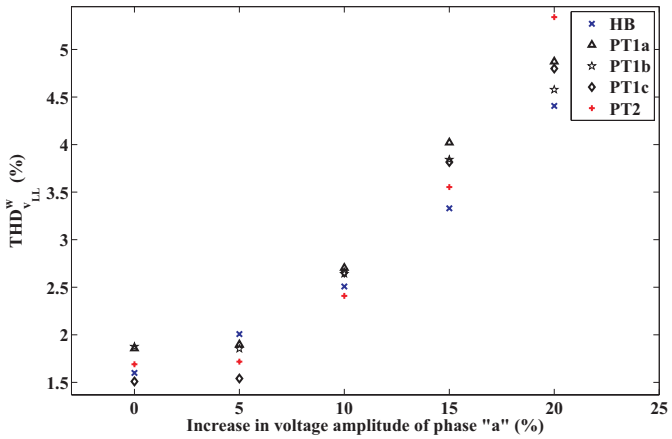


Fig. 20: THD_w for the output line-to-line voltage with unbalanced voltages.

techniques reach the objective of synthesizing the output reference voltage. The input currents of the techniques are easily filtered because they present relevant harmonic values only near to the switching frequency and its multiples. Considering the results for output voltages and input currents, the Alesina and Venturini's and Rodriguez's techniques present the worst general performance. It is possible to observe that the output voltage and input current present a better waveform quality for the proposed technique 1, since the lowest harmonic content was achieved, making this strategy better than the others techniques in $q = 50\%$, $q = 75\%$ and $q = 86.6\%$.

For unbalanced loads and unbalanced input voltages, the proposed technique 1 is the best technique for low values of unbalance. The HB's technique presents better results than the proposed techniques for high values of unbalance. Considering that the highly unbalanced loads and unbalanced input voltages only happen in critical situations (small probability of occurrence), the matrix converter should be operated with techniques that present good results for the normal conditions or with low values of unbalance. Therefore, the proposed technique 1 is chosen to be used in the matrix converter.

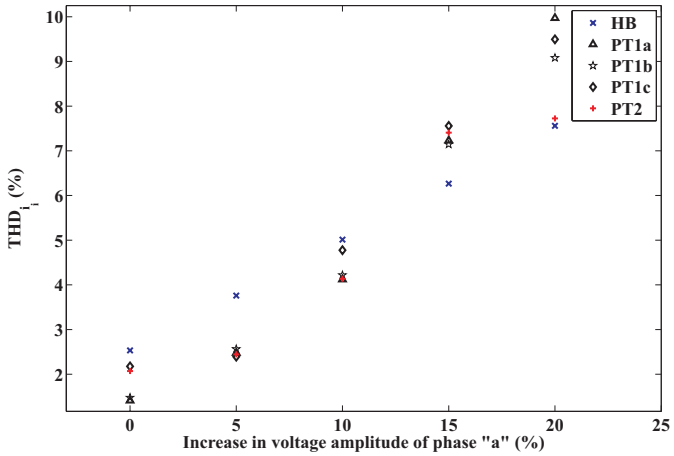


Fig. 21: THD for the input current with unbalanced input voltages.

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