ANALYSIS, DESIGN, AND IMPLEMENTATION OF A GENERAL HIGH STEP-UP DC-DC CONVERTER

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***Abstract* – A new general high step-up DC-DC converter based on three-state switching cell is proposed, as a viable solution for photovoltaic systems, fuel cells power systems, low power UPS, small wind generators, etc. In this converter, the output to input voltage ratio, for a given duty cycle, can be raised adding transformer turns ratio and additional secondary windings. Another important feature of this converter is the lower blocking voltage across the controlled switches compared to the similar circuits, which allows the utilization of switches with low on-resistance R_{DS}(on) MOSFETs. In order to show the circuit performance, experimental tests have been carried out for a 1kW laboratory prototype. Principle of operation, theoretical analysis and a design example are also shown to verify the feasibility of this topology.**

***Keywords* - high step-up dc-dc converter, high efficiency converter, photovoltaic applications, three-state switching cell.**

I. INTRODUCTION

In photovoltaic and fuel cell applications, is commonly necessary to raise the lower input voltage (12Vdc – 48Vdc), to high output DC bus voltage (300Vdc – 400Vdc), in order to feed voltage source inverters-VSI utilized within UPS systems, motor drives, etc. For this application, the classical boost converter is not a good choice, because for a very high duty cycle, the output diode conducts a very short time during each commutation cycle, thus resulting in serious reverse recovery problems and an increase of the output diode rating. An alternative might be the use of boost converters in cascade, but this solution deals with lower efficiency, due to the amount of power processing stages. To overcome this disadvantage some solutions using step-up converters capable of operating with high voltage gain ratio were proposed in the literature and some of them are here analyzed [1-8].

In Fig.1 is shown a topology [1,2] that consists in a clamp-mode coupled-inductor boost converters operating with the advantages of high voltage gain ratio and half output voltage stress across the switches. As disadvantage, it can be pointed out the pulsating input current and the high current stress through the clamping capacitor Cc.

Two-inductor boost converters with an auxiliary transformer were presented in [3,4] whose circuit is shown in Fig. 2. They operate as an interleaved boost converter. To maximize the voltage gain of the converter, the output side of each circuit was configured as a voltage doubler rectifier using two diodes and two capacitors. As advantages of the converter, the input current drawn from the voltage source is non-pulsating with low ripple, and the maximum voltage stress across the switches is half of the output voltage. The indicated circuit was connected without common input-output ground, making the use of an isolated sample output voltage or isolated gate drives necessary.

Also, as shown in Fig. 3, a non-isolated converter based on the interleaved boost converter, integrated with multiplier capacitors connected in series was proposed in [5]. These capacitors present similar behavior when compared to the series capacitor of the Sepic converter. These capacitors, however, allow obtaining high static gain. It presents the following advantages: the input current drain of the voltage source is non-pulsating with low ripple, and the maximum voltage stress across the switches is half of the output voltage. The series capacitors on the converter limit the high power processing due to their lifetime.

Fig. 4 shows, a converter with high static gain based on boost-flyback was proposed in [6,7]. It is similar to the topologies proposed in [1,2]. As advantage, it presents the voltage stress across the switches lower than half output voltage and naturally clamped by the output filter capacitor C_1, and as disadvantage, it has a pulsating input current.

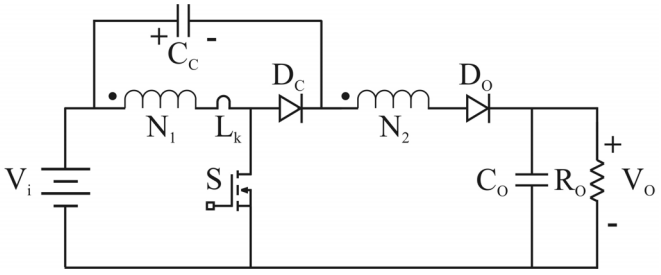


Fig. 1. High voltage gain, clamp-mode coupled-inductor boost DC-DC converter proposed in [1, 2].

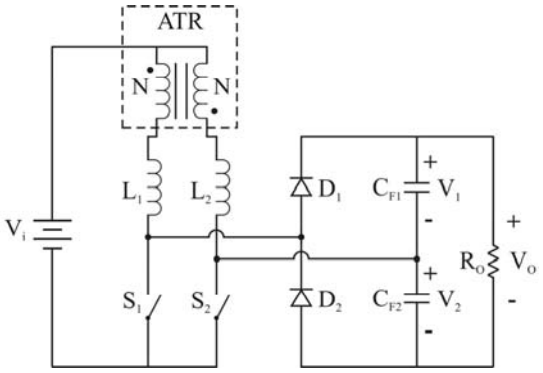


Fig. 2. A two inductor boost converter with auxiliary transformer proposed in [3, 4].

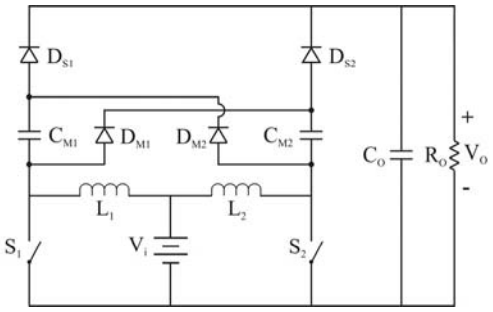


Fig. 3. An interleaved boost converter integrated with multiplier capacitors in series proposed in [5].

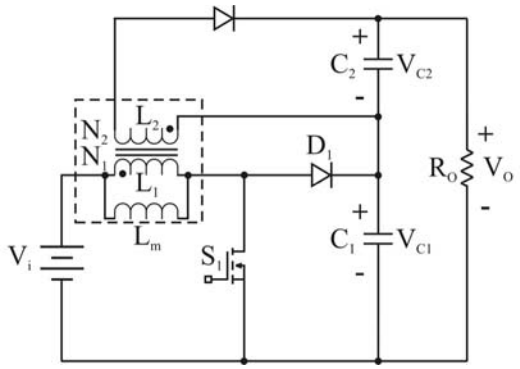


Fig. 4. Integrated boost-flyback step-up converter proposed in [6, 7].

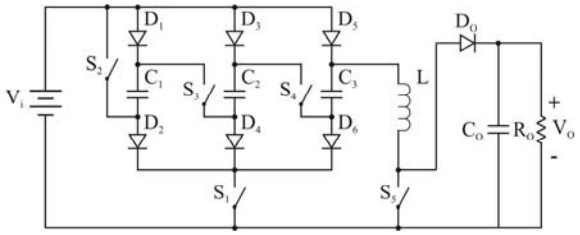


Fig. 5. Step-up switching converter with a high voltage ratio based on switched capacitor circuit proposed in [8].

Finally, as shows in Fig. 5, the switching capacitor technique was used in [8], in order to elevate the input voltage up-to a required output voltage. This idea is adequate only to the development of low power converters, since many switches with several voltage stress and many capacitors are necessary.

A general version of the proposed converter is shown in Fig. 6, which is based on the three-state switching cell [9]. The proposed converter has as advantages: the input current is non-pulsating with low ripple; the input inductor operates with the double of the switching frequency, allowing weight and volume reduction; the voltage stress across the switches is lower than a half output voltage and naturally clamped by one output filter capacitor, so, a small snubber is necessary on each switch. It is also important to notice that for a given duty cycle, the output voltage can be elevated incrementing the transformer turns ratio without compromising the voltage stress across the switches. The lower voltage across the switches allows the use of low on-resistance MOSFETs, improving therefore, the efficiency. As disadvantage, the converter does not operate appropriately for a duty cycle lower than 0.5 due to magnetic induction problems of the transformer.

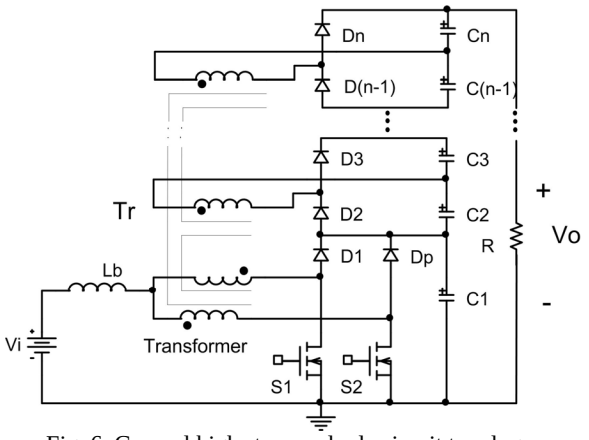


Fig. 6. General high step-up dc-dc circuit topology.

II. CIRCUIT DESCRIPTION

The particular application of the generalized converter is shown in Fig. 7. It is composed by the following devices: a voltage source V_i, storage inductor L_b, transformer T_r, controlled switches S_1 and S_2, rectifier diodes D_1, D_2, D_3 and D_p, filter capacitors C_1, C_2, C_3, and load resistor R.

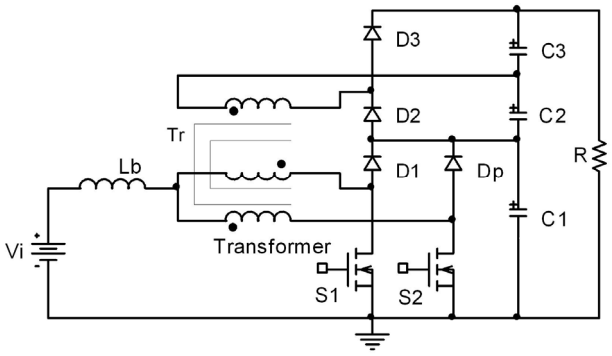


Fig. 7. Particular proposed topology.

III. OPERATION ANALYSIS

In order to explain the principle of operation of this converter, it is analyzed in steady-state and continuous conduction mode (CCM), with switches duty cycle higher than 0.5. For this purpose, the semiconductors and magnetic elements are considered ideals.

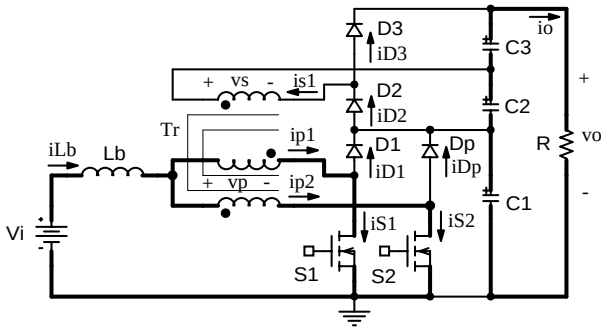
During one commutation period of the converter operation, it is possible to observe four operating stages, as shown in Fig. 8, as the relevant waveforms are depicted in Fig. 9.

➢ ***First Stage (t_0, t_1):*** The switches S_1 and S_2 are turned-on. The energy is only stored in the inductor L_b and is not transferred to the load. The interval is finished when switch S_1 is turned-off. This stage is represented on the circuit shown in Fig. 8.a and its waveforms characteristics shown in Fig. 9. The differential equation during this interval is given by,

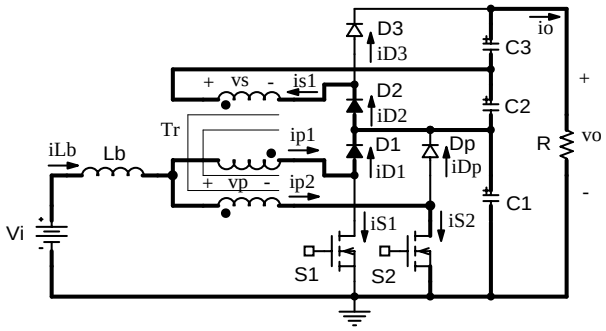
$$L_b \frac{di_{Lb}}{dt} - V_i = 0 \qquad (1)$$

Where:

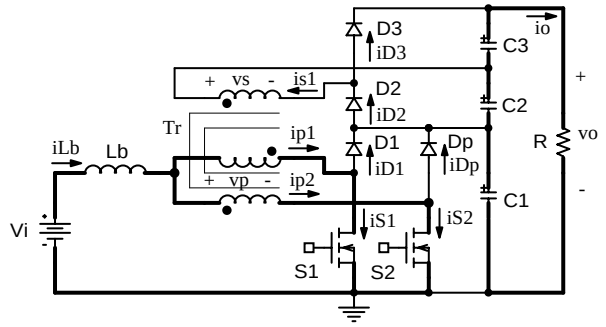
L_b - Inductance value of inductor L_b.



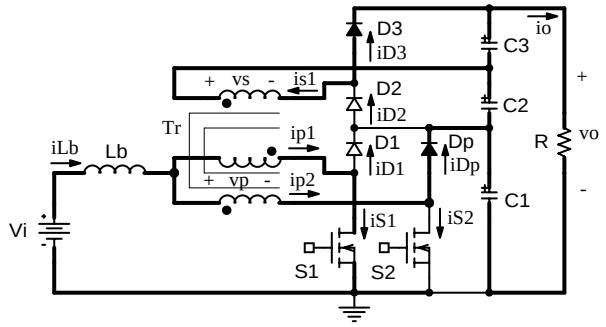
(a) First stage.



(b) Second stage.



(c) Third stage.



(d) Fourth stage.

Fig. 8. Operation stages shown topologically.

i_{Lb} - Instantaneous current through inductor L_b.
V_i - Input voltage.

➢ ***Second Stage (t_1, t_2):*** Switch S_2 remains on. The voltage across switch S_1 is equal to the voltage across capacitor C_1. The diodes D_1 and D_2 are forward biased. The energy stored in the inductor in the first interval, as well as the energy from the voltage source are transferred to the filter capacitors C_1 and C_2. This stage is represented in Fig. 8.b according to the theoretical waveforms shown in Fig. 9. The differential equation during this interval is equal to,

$$L_b \frac{di_{Lb}}{dt} + \frac{V_i}{2(1-D)} - V_i = 0 \qquad (2)$$

Where:

D - Duty cycle.

➢ ***Third Stage (t_2, t_3):*** This stage is similar to the first one, where switches S_1 and S_2 are turned-on, and the energy is only stored in the inductor L_b. It is finished when switch S_2 is turned-off. This stage is represented in Fig. 8.c and main waveforms shown in Fig. 9.

➢ ***Fourth Stage (t_3, t_4):*** Switch S_1 remains on. The voltage across switch S_2 is equal to the voltage across capacitor C_1. The diodes D_p and D_3 are forward biased. The energy stored in the inductor during the third interval, as well as the energy from the voltage source are transferred to the filter capacitors C_1 and C_3. This stage is represented in Fig. 8.d. and its waveforms characteristics shown in Fig. 9

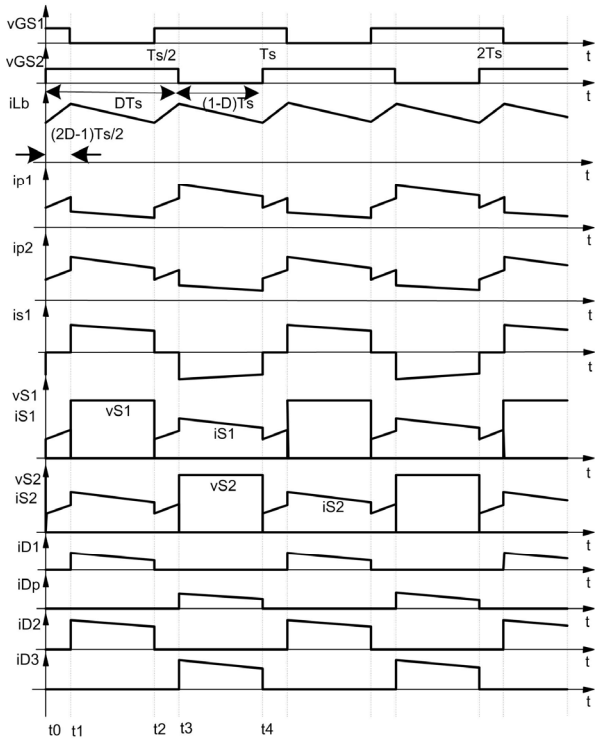


Fig. 9. Theoretical waveforms of the converter.

IV. THEORETICAL ANALYSIS

A. Static Voltage Gain

The output-input voltage ratio, as a function of the duty cycle, named as static voltage gain of the generalized

converter, considering *k* equal secondary windings, is given by

$$G_V = \frac{V_o}{V_i} = \frac{(k \cdot a + 1)}{(1 - D)} \quad (3)$$

Where:

V_o - Output voltage.
k - Number of equal secondary winding.
a - Transformer turn ratio.

B. Inductor Design

Using the expressions (1), (3) and the time interval during the first stage, the current ripple on the inductor is equal to

$$\Delta I_{Lb} = \frac{(2D-1)(1-D)V_o}{2 f_s (k \cdot a + 1) L_b}. \quad (4)$$

In (4), ΔI_{Lb} is the current ripple on the inductor L_b, and f_s is the switching frequency of the converter.

Rearranging the terms in (4), the normalized current ripple on the inductor is given by

$$\overline{\Delta I_{Lb}} = \frac{2\Delta I_{Lb} L_b f_s (k \cdot a + 1)}{V_o} = (2D-1)(1-D). \quad (5)$$

Fig. 10, obtained using (5), shows the normalized current ripple on the inductor as a function of the duty cycle.

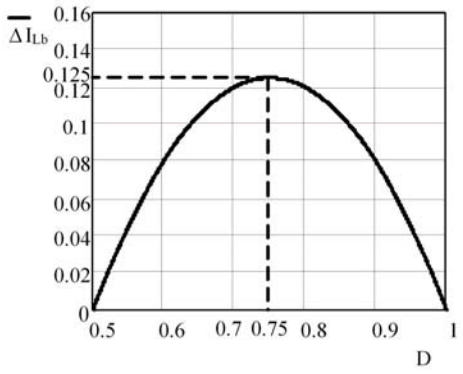


Fig. 10. Normalized ripple current on the inductor L_b.

It is possible to conclude that the maximum current ripple on the inductor occurs when the duty cycle is 0.75 and the normalized current ripple is 0.125. Given a certain value to the current ripple, it is possible to calculate the inductor value using

$$L_b = \frac{V_o}{16 f_s (k \cdot a + 1) \Delta I_{Lb}}. \quad (6)$$

C. Transformer Design

The high frequency transformer must be designed for the following power processing level given by

$$P_p = \frac{(2 \cdot k \cdot a + 1)}{(1 + k \cdot a)} \frac{P_o}{2}. \quad (7)$$

In (7), P_p is the power processing level of the transformer, and, P_o is the output power of the converter.

D. Output Capacitors Design

Considering the voltage ripple small, the average voltage across the capacitors C_1, C_2 e C_3 are described by (8) and (9).

$$VC_1 = \frac{V_i}{(1-D)}, \quad (8)$$

$$VC_2 = VC_3 = \frac{a}{2} \cdot \frac{V_i}{(1-D)}, \quad (9)$$

The capacitance of each capacitor can be calculated using the expressions (10) and (11),

$$C_1 \geq \frac{(1-D) P_o}{2 f_s \Delta V_o V_i (1 + k \cdot a)}, \quad (10)$$

$$C_2 = C_3 \geq \frac{(1-D) P_o}{f_s \Delta V_o V_i (1 + k \cdot a)}. \quad (11)$$

In (10) and (11), ΔV_o is the total output voltage ripple.

E. Maximum Voltage across the Switches S_1 and S_2

The maximum normalized voltage across switches S_1 and S_2, without considering overshoots due to layout inductances, is given by

$$VS_1 = VS_2 = \frac{V_i}{(1-D)}. \quad (12)$$

F. Maximum Reverse Voltage across the Diodes D_1, D_2, D_3, and D_p

The maximum reverse voltage across the diodes D_1, D_2, D_3, and D_p are given by (13) and (14), respectively.

$$VD_{1(PIV)} = VD_{p(PIV)} = \frac{Vi}{(1-D)}, \quad (13)$$

$$VD_{2(PIV)} = VD_{3(PIV)} = \frac{a \cdot V_i}{(1-D)}. \quad (14)$$

V. SIMPLIFIED DESIGN EXAMPLE

A. Converter Specifications

The design specifications of the proposed high gain boost converter are shown in Table I.

TABLE I
Converter Specifications

Input voltage range	V_i = 42V_{DC} - 54V_{DC}
Output power	P_o = 1kW
Output voltage	V_o = 400V
Switching frequency	f_s = 25kHz
Secondary winding number	k = 1

The assumed parameters are: the maximum boost inductor current ripple is $\Delta I_{Lb} = 0.20 I_{i\max}$, the transformer turns ratio is $a = N_s / N_p = 2$, the maximum fixed duty cycle of the switches is $D_{\max} = 0.70$ to minimum input voltage, and the output voltage ripple is ΔV_o=0.01V_o.

B. Design Procedure

The boost inductor is obtained according to (6), substituting values in it is equal to

$$L_b = \frac{400}{16 \cdot 25000 \cdot (1 \cdot 2 + 1) \cdot 4.76} = 70.0 \mu H.$$

The transformer of the converter was built using the push-pull DC-DC converter guidelines, for power obtained by (7). Thus,

$$P_p = \frac{(2\cdot 1\cdot 2+1)}{(1+1\cdot 2)}\cdot\frac{1000}{2} = 833.34W\ .$$

The capacitances of the output filter capacitors were calculated using expressions (10) and (11). Substituting values they are obtained as

$$C_1 \geq \frac{(1-0.7)\cdot 1000}{2\cdot 25000\cdot 4\cdot 42\cdot(1+1\cdot 2)} = 11.9\mu F\ ,$$

$$C_2 = C_3 \geq \frac{(1-0.7)\cdot 1000}{25000\cdot 4\cdot 42\cdot(1+1\cdot 2)} = 23.81\mu F\ .$$

The voltage across such capacitors must be higher than the values calculated using (8) and (9). So,

$$VC_1 = \frac{42}{(1-0.7)} = 140V\ ,$$

$$VC_2 = VC_3 = \frac{2}{2}\cdot\frac{42}{(1-0.7)} = 140V\ .$$

The breakdown voltage of the controlled switches must be higher than the value obtained using (12). Thus,

$$VS_1 = VS_2 = \frac{42}{(1-0.7)} = 140V\ .$$

The maximum reverse voltage of the rectifier diodes must be higher than the values calculated from (13) and (14). So,

$$VD_{1(PIV)} = VD_{p(PIV)} = \frac{42}{(1-0.7)} = 140V\ ,$$

$$VD_{2(PIV)} = VD_{3(PIV)} = \frac{2\cdot 42}{(1-0.7)} = 280V\ .$$

VI. EXPERIMENTAL RESULTS

A prototype has been realized with the characteristics reported in the section V. (shown in Table II)

TABLE II
Prototype Parameters

Diodes D_1, D_2, D_3, D_p	HFA15PB60
Inductor L_b	L_b = 70µH NEE-55/28/21 (Thornton Ipec) NL_b= 15 turns (62x26AWG) δ=1mm (gap)
Output Filter Capacitors C_1, C_2, C_3	470µF / 250V
Switches S_1, S_2	SPW47N60C2
High Frequency Transformer	NEE-65/26 (Thornton Ipec) Np1=Np2=13 turns (30x26AWG) Ns1=26 turns (14x26AWG)

The implemented capacitance values of the output capacitors are different to the calculated, due to non-linear load connection (inverter).

Fig. 11 shows the measured gate-to-source voltages of switches S_1 and S_2, the currents through the primary side of the transformer T_r and boost inductor L_b. It can be seen in Fig. 11 that the current drawn by the proposed converter presents a low current ripple, increasing the reliability of the battery bank for example. Fig. 12 shows the same control signals of switches S_1 and S_2, the voltage and current in the switch S_1. According to the Fig. 12, the drain-to-source voltage in S_1 is lower than half output voltage, as expected in the theoretical analysis. Fig. 13 shows the same gating signals as showed before in Figs. 11 and 12, and the current through the diodes D_3 and D_1. The resulting current through the diodes D_3 and D_1 are a bit different compared to the theoretical waveforms. Compared to the theoretical waveforms shown in Fig. 9, all experimental results presented a little difference due to the leakage inductance obtained during the construction of the magnetic components.

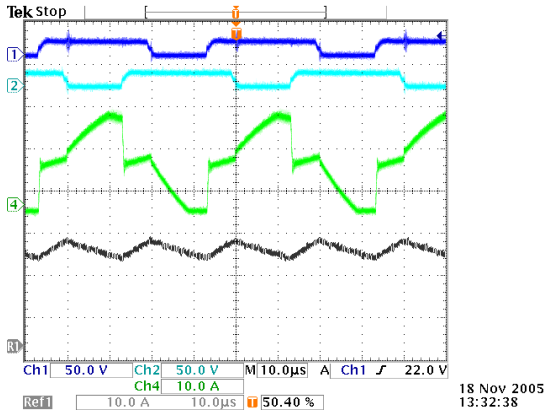


Fig. 11. Measured gate-to-source voltages V_{GS1} and V_{GS2}, primary current through the transformer I_{p1} and current through the inductor L_b (50V/div.; 10A/div.; 10A/div.; 10us/div.)

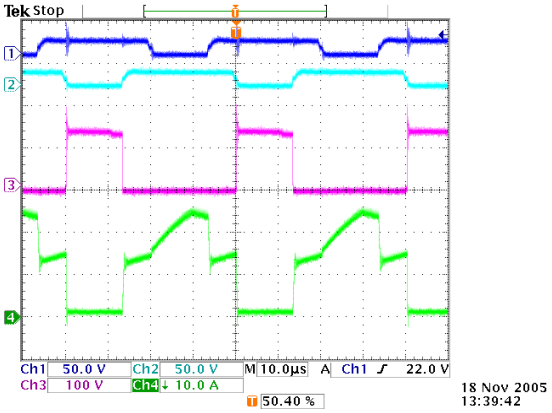


Fig. 12. Measured gate-to-source voltages V_{GS1} and V_{GS2}, drain-to-source voltage V_{S1} and drain current I_{S1} (50V/div.; 100V/div.; 10A/div.; 10us/div.)

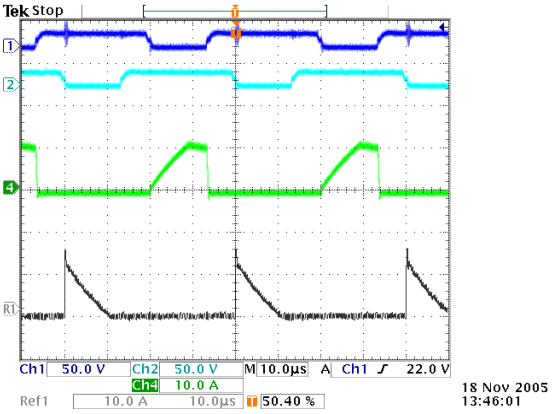


Fig. 13. Measured gate-to-source voltages V_{GS1} and V_{GS2}, current through diodes D_3 and D_1 (50V/div.; 10A/div.; 10us/div.)

Fig. 14 shows the secondary voltage and current in the transformer T_r, where a symmetry of each semi-cycle is observed. Fig. 15 shows the input and output voltage and current. Due to the utilization of a tiristor controlled power supply, the input voltage presents a voltage ripple. As seen in Fig. 15, the output voltage is regulated in the desired value and the current drawn by the input source presents a low ripple. Finally, Fig. 16 presents the efficiency of the converter as a function of the output power. Compared to other related in [1-9], this converter presented a good efficiency.

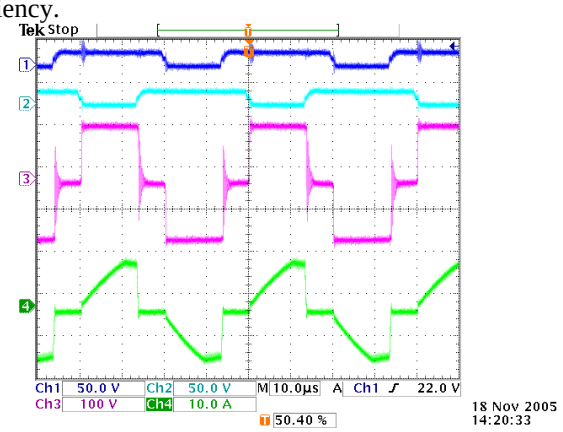


Fig. 14. Measured gate-to-source voltages V_{GS1} and V_{GS2}, secondary voltage and current in the transformer (50V/div.; 100V/div.; 10A/div.; 10us/div.)

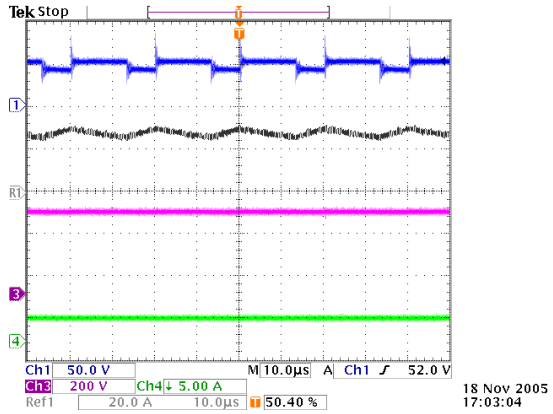


Fig. 15. Input voltage V_i and current I_{Lb}, and the output voltage V_o and current I_o (50V/div.; 20A/div.; 200V/div.; 5A/div.; 10us/div.)

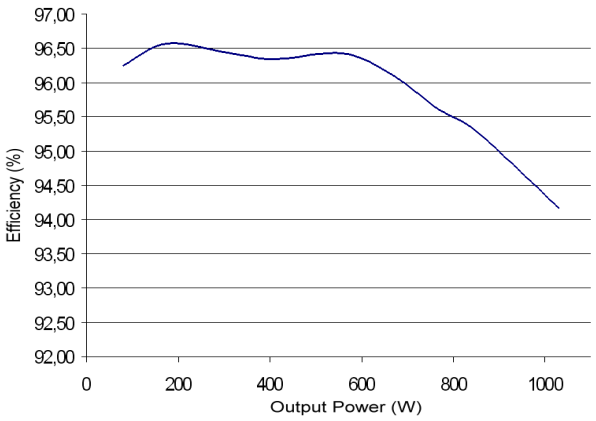


Fig. 16. Efficiency of the converter, as a function of the output power.

VII. CONCLUSION

The performance of a non-isolated boost converter with a high voltage gain has been analyzed and verified by experimental tests. There are several applications where this circuit is recommended such as photovoltaic, fuel cells, small wind generators and UPS systems that require a high voltage gain between the input and output voltages.

Furthermore, the results obtained have show the lower blocking voltages across the controlled switches compared to similar circuits, which allow the utilization of MOSFETs switches with lower conduction losses.

The qualitative analysis, theoretical analysis, simplified design example and the experimental results were carried out for a 1kW laboratory prototype under steady state conditions. The experimental results are quite satisfactory, showing the effectiveness of the proposed topology compared to previous proposed configurations for the same purpose. The efficiency of the converter can be improved using lower on-resistance drain-source MOSFETs and lower reverse voltage diodes.

ACKNOWLEDGEMENT

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